

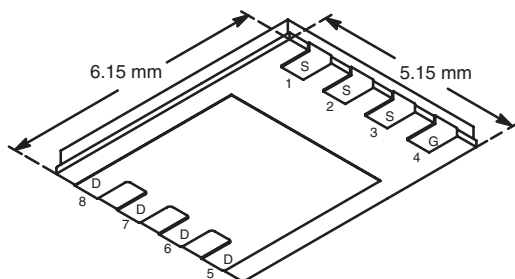


N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, e}	Q_g (Typ.)
40	0.019 at $V_{GS} = 10$ V	21	5.8 nC
	0.0225 at $V_{GS} = 4.5$ V	19.6	

PowerPAK SO-8



Bottom View

Ordering Information: SiR836DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

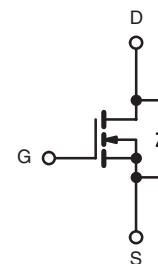
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- POL
- Synchronous Rectification



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	50	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
Single Pulse Avalanche Current	I_{AS}	10	
Avalanche Energy	E_{AS}	5	mJ
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{f, g}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	27	32	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	6.4	8.0	

Notes:

a. Based on $T_C = 25^\circ\text{C}$.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.d. Maximum under Steady State conditions is 70°C/W .

e. Package limited.

f. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

g. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SiR836DP

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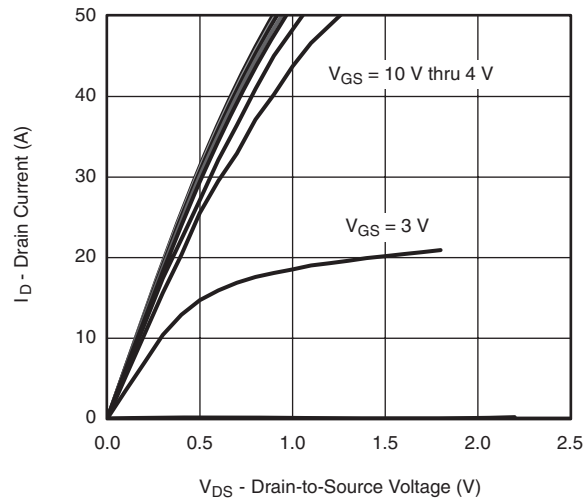
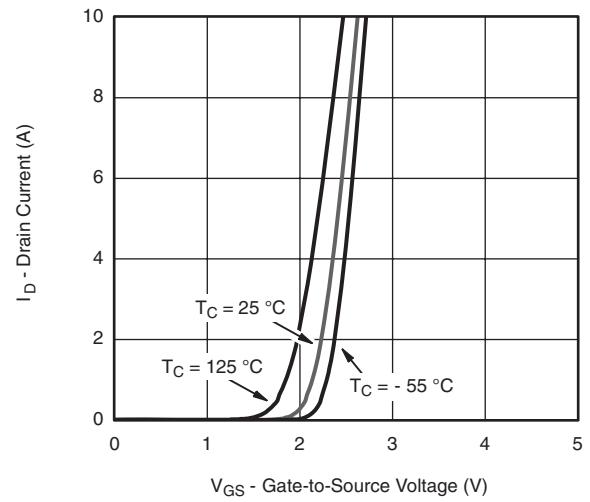
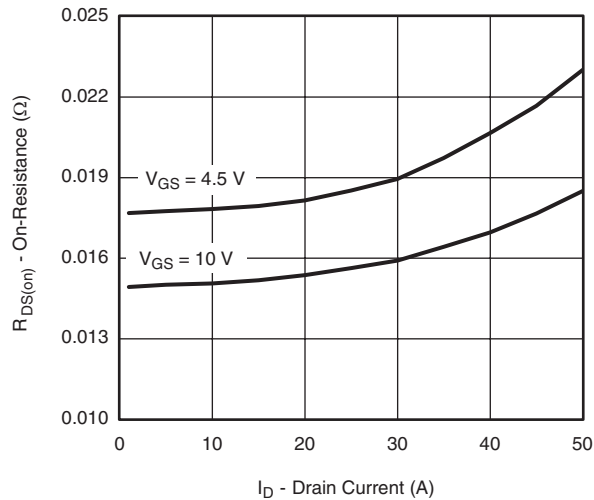
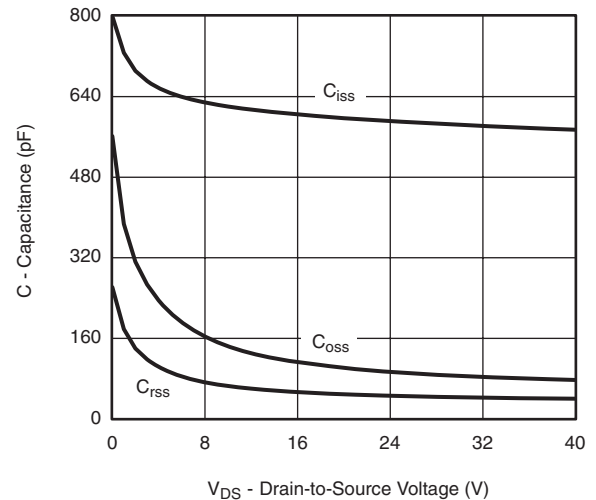
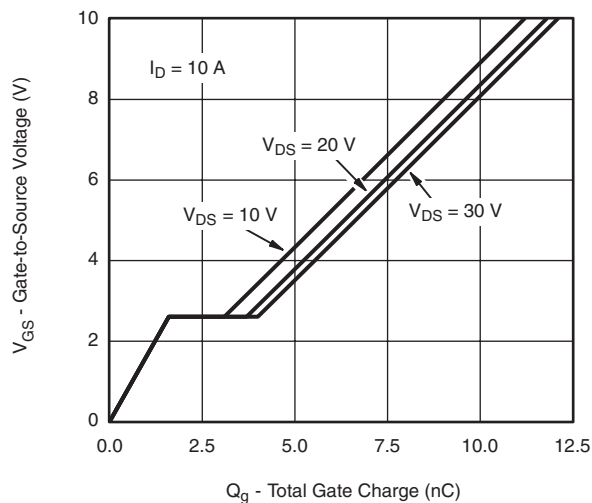
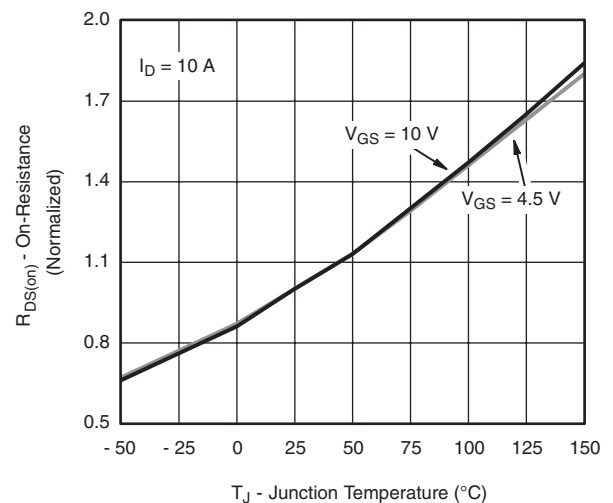
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	40			V		
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		50		mV/ $^{\circ}\text{C}$		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4.8				
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.5	V		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA		
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^{\circ}\text{C}$			10			
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A		
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.015	0.019	Ω		
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$		0.018	0.0225			
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		35		S		
Dynamic ^b								
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		600		pF		
Output Capacitance	C_{oss}			100				
Reverse Transfer Capacitance	C_{rss}			50				
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		11.8	18	nC		
Gate-Source Charge	Q_{gs}	$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		5.8	9			
Gate-Drain Charge	Q_{gd}			1.6				
Gate Resistance	R_g			2.1				
Turn-On Delay Time	$t_{d(on)}$	$f = 1\text{ MHz}$	0.5	2.4	4.8	Ω		
Rise Time	t_r		$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		14		28	ns
Turn-Off Delay Time	$t_{d(off)}$				19		38	
Fall Time	t_f				17		34	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$			11	22		
Rise Time	t_r			8	16			
Turn-Off Delay Time	$t_{d(off)}$			13	26			
Fall Time	t_f			15	30			
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			14	A		
Pulse Diode Forward Current ^a	I_{SM}				50			
Body Diode Voltage	V_{SD}	$I_S = 3\text{ A}$		0.77	1.1	V		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^{\circ}\text{C}$		15	30	ns		
Body Diode Reverse Recovery Charge	Q_{rr}			7.5	15	nC		
Reverse Recovery Fall Time	t_a			8		ns		
Reverse Recovery Rise Time	t_b			7				

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

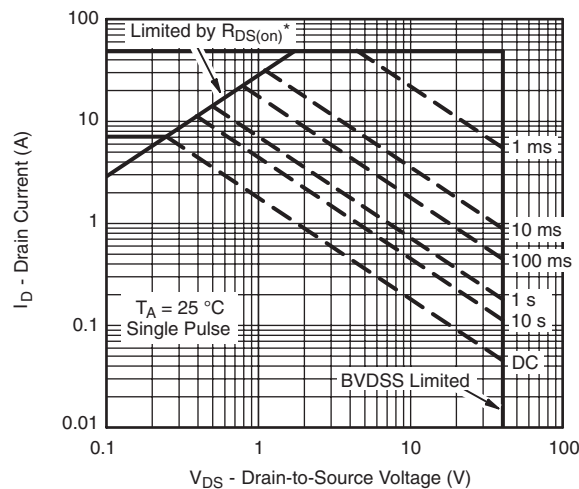
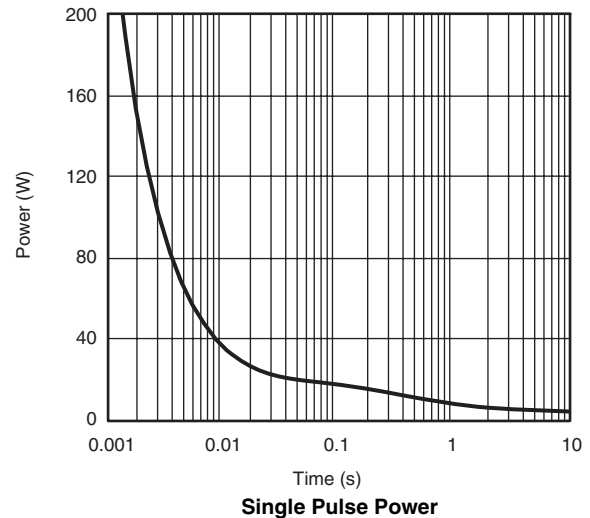
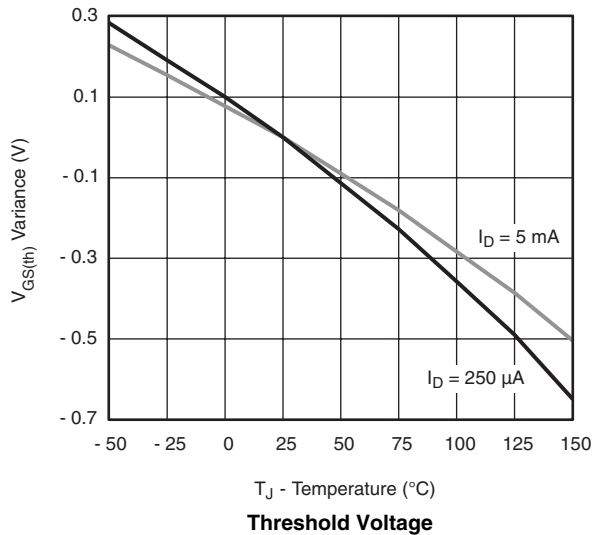
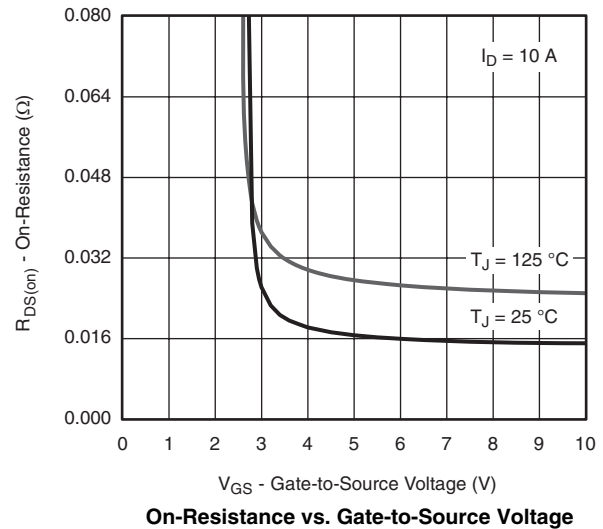
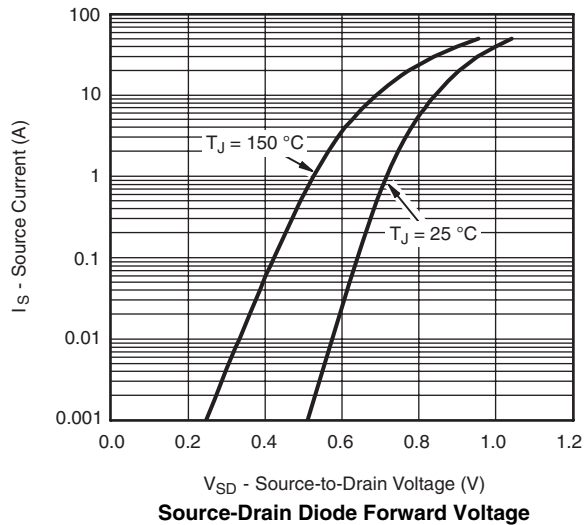
b. Guaranteed by design, not subject to production testing.

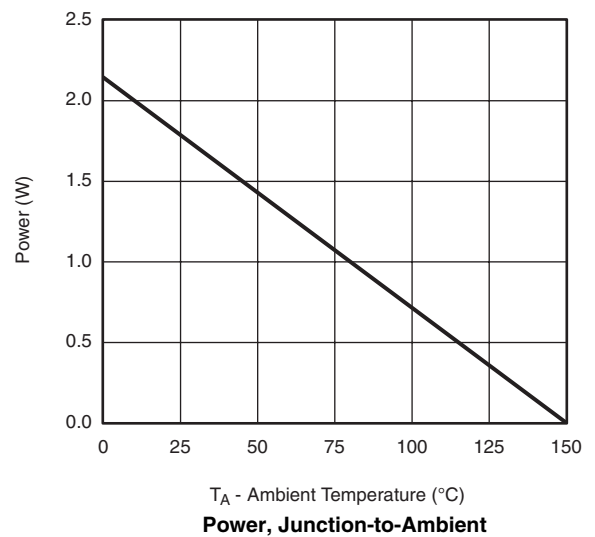
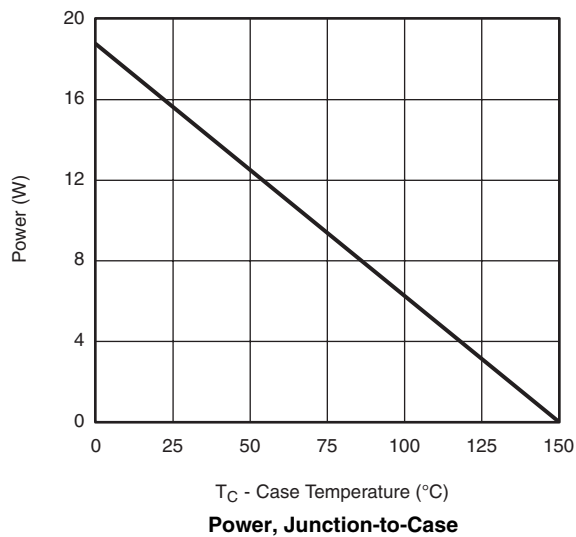
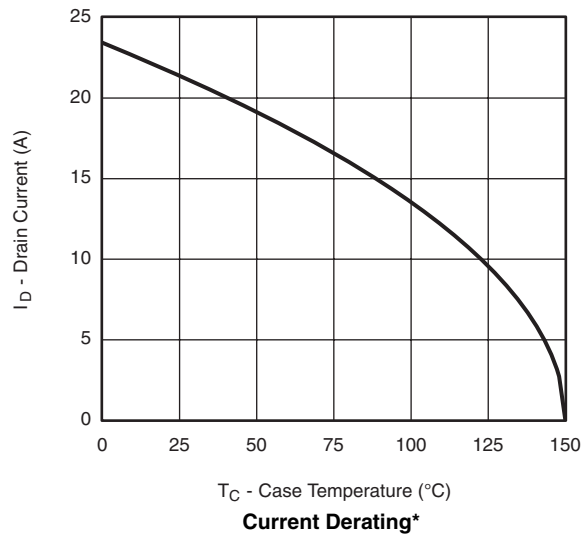
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

SiR836DP

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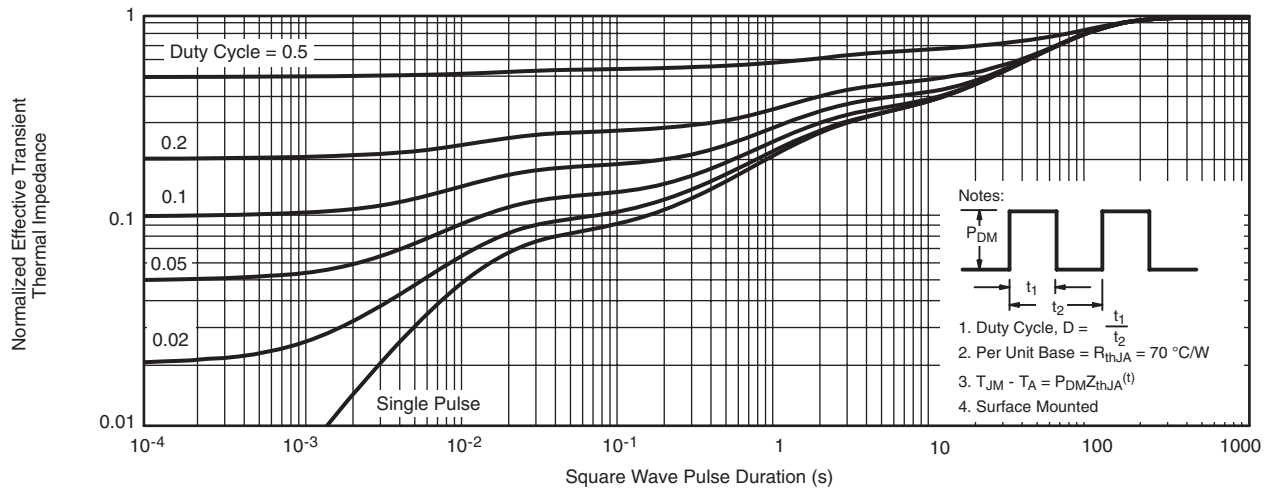
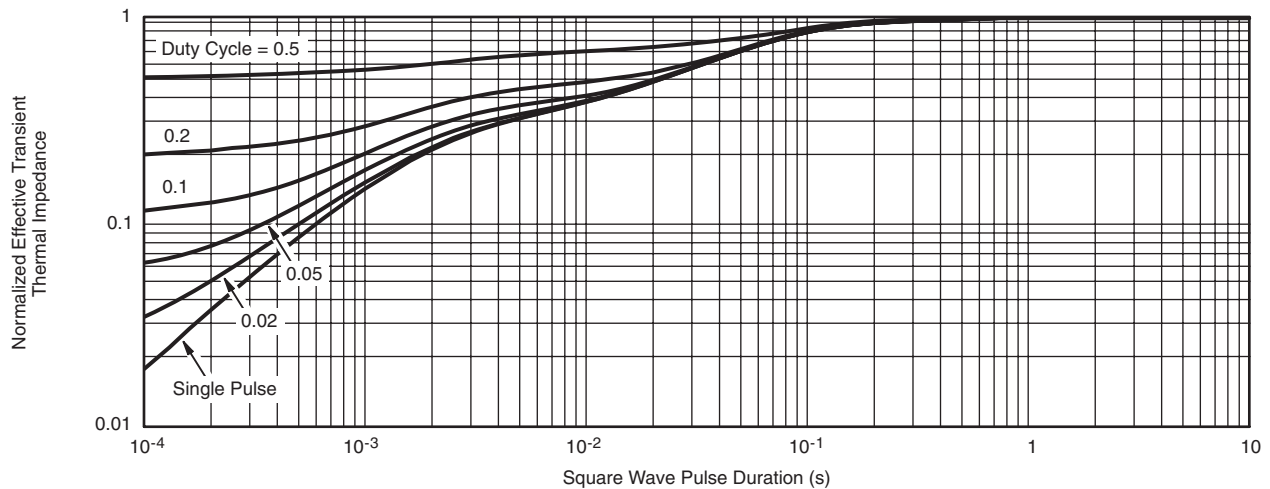
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiR836DP

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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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