700MHZ, CYRSTAL-TO-3.3V DIFFERENTIAL LVPECL FREQUENCY SYNTHESIZER

ICS8432-51

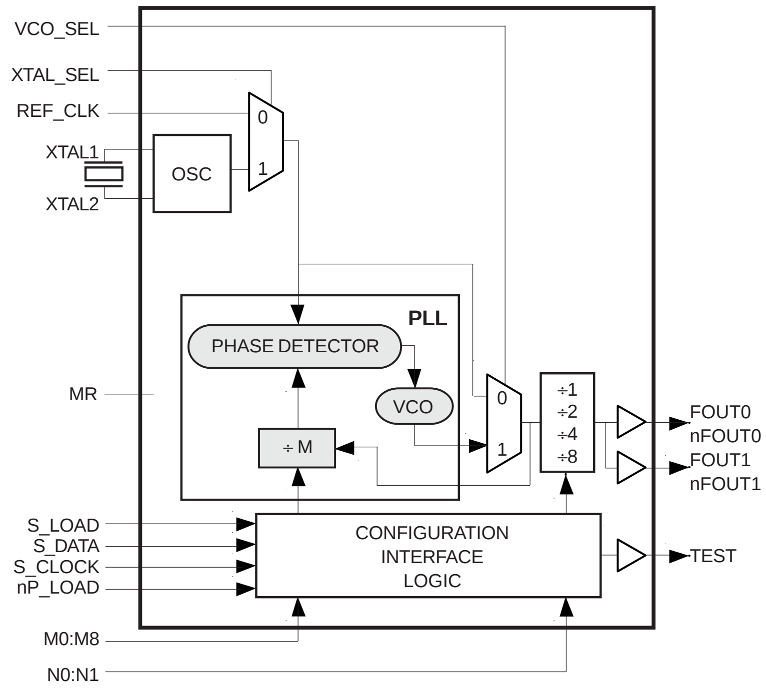
GENERAL DESCRIPTION

The ICS8432-51 is a general purpose, dual output Crystal-to-3.3V Differential LVPECL High Frequency Synthesizer. The ICS8432-51 has a selectable REF_CLK or crystal input. The VCO operates at a frequency range of 250MHz to 700MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interface to the configuration logic. The low phase noise characteristics of the ICS8432-51 make it an ideal clock source for Gigabit Ethernet, Fibre Channel 1 and 2, and Infiniband applications.

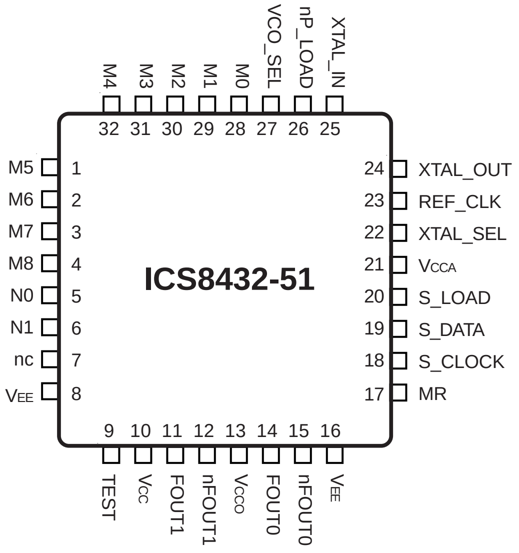
FEATURES

- Dual differential 3.3V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL REF_CLK
- Output frequency range: 31.25MHz to 700MHz
- Crystal input frequency range: 12MHz to 25MHz
- VCO range: 250MHz to 700MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 3.5ps (maximum)
- Cycle-to-cycle jitter: 25ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages
- Replaces the ICS8432-01

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

FUNCTIONAL DESCRIPTION

NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The ICS8432-51 features a fully integrated PLL and therefore, requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8432-51 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows: $f_{VCO} = f_{xtal} \times M$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as $10 \le M \le 28$. The frequency out is defined as follows: $FOUT = \frac{fVCO}{N} = fxtal \times \frac{M}{N}$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data, Shift Register Input
1	0	Output of M divider
1	1	CMOS Fout

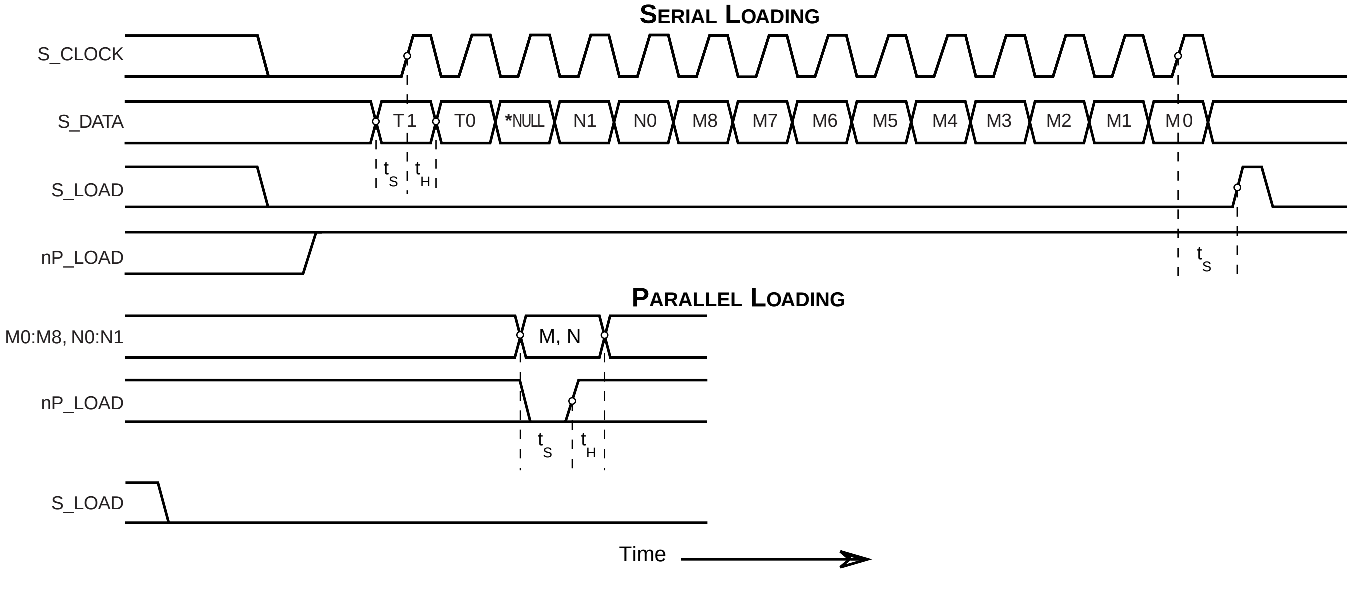


FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS

***NOTE:** The NULL timing slot must be observed.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	M5	Input	Pullup	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTL interface levels.
2, 3, 4, 28, 29, 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines output divider value as defined in Table 3C, Function Table. LVCMOS / LVTTL interface levels.
7	nc	Unused		No connect.
8, 16	V_{EE}	Power		Negative supply pins.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS / LVTTL interface levels.
10	V_{CC}	Power		Core supply pin.
11, 12	FOUT1, nFOUT1	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
13	V_{CCO}	Power		Output supply pin.
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
17	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not effect loaded M, N, and T values. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels.
21	V_{CCA}	Power		Analog supply pin.
22	XTAL_SEL	Input	Pullup	Selects between crystal or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS / LVTTL interface levels.
23	REF_CLK	Input	Pulldown	Referenc clock input. LVCMOS / LVTTL interface levels.
24, 25	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. PARALLEL AND SERIAL MODE FUNCTION TABLE

Inputs							Conditions
MR	**nP_LOAD**	**M**	**N**	**S_LOAD**	**S_CLOCK**	**S_DATA**	
H	X	X	X	X	X	X	Reset. Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓= Falling edge transition

TABLE 3B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE

VCO Frequency (MHz)	M Divide	256	128	64	32	16	8	4	2	1
		M8	**M7**	**M6**	**M5**	**M4**	**M3**	**M2**	**M1**	**M0**
250	10	0	0	0	0	0	1	0	1	0
275	11	0	0	0	0	0	1	0	1	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
700	28	0	0	0	0	1	1	1	0	0

NOTE 1: These M divide values and the resulting frequencies correspond to crystal or TEST_CLK input frequency of 25MHz.

TABLE 3C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

Inputs		N Divider Value	Output Frequency (MHz)	
N1	**N0**		**Minimum**	**Maximum**
0	0	1	250	700
0	1	2	125	350
1	0	4	62.5	175
1	1	8	31.25	87.5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5 V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	
32 Lead LQFP	47.9°C/W (0 lfpm)
32 Lead VFQFN	41.07°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = V_{CCO} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.15	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				135	mA
I_{CCA}	Analog Supply Current				15	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = V_{CCO} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	VCO_SEL, XTAL_SEL, MR, S_LOAD, nP_LOAD, N0:N1, S_DATA, S_CLOCK, M0:M8		2		V_{CC} + 0.3	V
		REF_CLK		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	VCO_SEL, XTAL_SEL, MR, S_LOAD, nP_LOAD, N0:N1, S_DATA, S_CLOCK, M0:M8		-0.3		0.8	V
		REF_CLK		-0.3		1.3	V
I_{IH}	Input High Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, REF_CLK, S_DATA, S_LOAD, nP_LOAD	$V_{CC} = V_{IN}$ = 3.465V			150	µA
		M5, XTAL_SEL, VCO_SEL	$V_{CC} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, REF_CLK, S_DATA, S_LOAD, nP_LOAD	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		M5, XTAL_SEL, VCO_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage	TEST; NOTE 1		2.6			V
V_{OL}	Output Low Voltage	TEST; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO}/2.

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50 Ω to V_{CCO} - 2V. See "Parameter Measurement Information" section, figure "3.3V Output Load Test Circuit".

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	REF_CLK; NOTE 1		12		25	MHz
		XTAL_IN, XTAL_OUT; NOTE 1		12		25	MHz
		S_CLOCK				50	MHz

NOTE 1: For the input crystal and REF_CLK frequency range, the M value must be set for the VCO to operate within the 250MHz to 700MHz range. Using the minimum input frequency of 12MHz, valid values of M are 21 ≤ M ≤ 58. Using the maximum frequency of 25MHz, valid values of M are 10 ≤ M ≤ 28.

TABLE 6. CRYSTAL CHARACTERISTICS

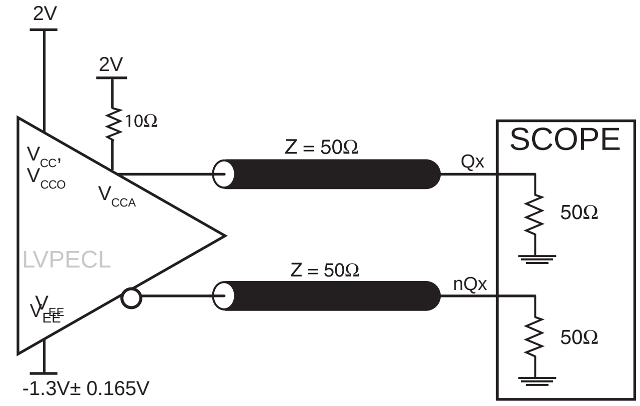
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		25	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 7. AC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

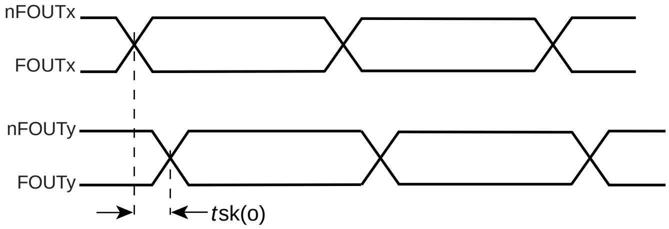
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency			31.25		700	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 3		fVCO > 350MHz			25	ps
*t*jit(per)	Period Jitter, RMS; NOTE 1					3.5	ps
*t*sk(o)	Output Skew; NOTE 2, 3					15	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		700	ps
t_S	Setup Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
t_H	Hold Time	M, N to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			ns
		S_CLOCK to S_LOAD		5			ns
odc	Output Duty Cycle		N > 1	48		52	%
t_{PW}	Output Pulse Width		N = 1	t_{PERIOD}/2 - 150		t_{PERIOD}/2 + 150	ps
t_{LOCK}	PLL Lock Time					1	ms

See Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

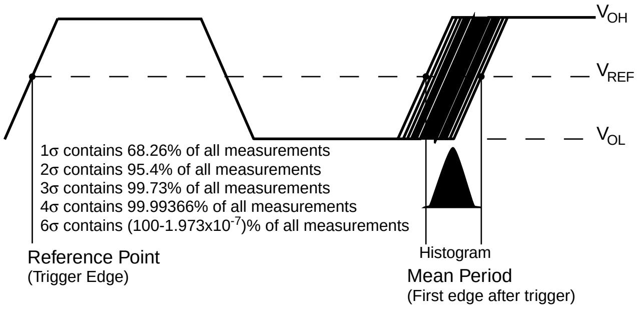
PARAMETER MEASUREMENT INFORMATION



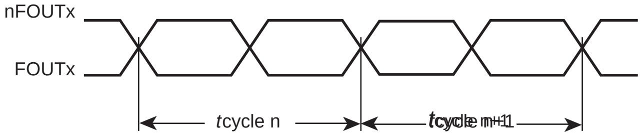
3.3V Output Load AC Test Circuit



Output Skew



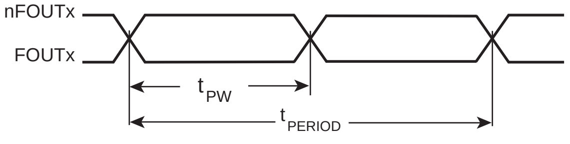
Period Jitter



$$t\text{jit(cc)} = t\text{cycle } n - t\text{cycle } n{+}1$$

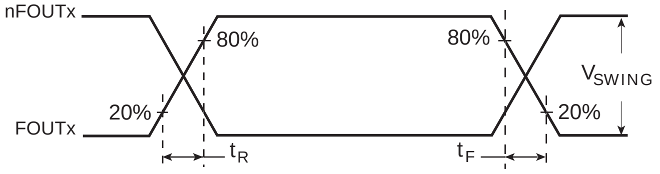
1000 Cycles

Cycle-to-Cycle Jitter



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

APPLICATION INFORMATION

STORAGE AREA NETWORKS

A variety of technologies are used for interconnection of the elements within a SAN. The tables below lists the common frequencies used as well as the settings for the ICS8432-51 to generate the appropriate frequency.

Table 8. Common SANs Application Frequencies

Interconnect Technology	Clock Rate	Reference Frequency to SERDES (MHz)	Crystal Frequency (MHz)
Gigabit Ethernet	1.25 GHz	125, 250, 156.25	25, 19.53125
Fibre Channel	FC1 1.0625 GHz FC2 2.1250 GHz	106.25, 53.125, 132.8125	16.6015625, 25
Infiniband	2.5 GHz	125, 250	25

Table 9. Configuration Details for SANs Applications

Interconnect Technology	Crystal Frequency (MHz)	ICS8432-51 Output Frequency to SERDES (MHz)	ICS8432-51 M & N Settings										
			M8	M7	M6	M5	M4	M3	M2	M1	M0	N1	N0
Gigabit Ethernet	25	125	0	0	0	0	1	0	1	0	0	1	0
	25	250	0	0	0	0	1	0	1	0	0	0	1
	25	156.25	0	0	0	0	1	1	0	0	1	1	0
	19.53125	156.25	0	0	0	1	0	0	0	0	0	1	0
Fiber Channel 1	25	53.125	0	0	0	0	1	0	0	0	1	1	1
	25	106.25	0	0	0	0	1	0	0	0	1	1	0
Fiber Channel 2	16.6015625	132.8125	0	0	0	1	0	0	0	0	0	1	0
Infiniband	25	125	0	0	0	0	1	0	1	0	0	1	0
	25	250	0	0	0	0	1	0	1	0	0	0	1

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8432-51 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

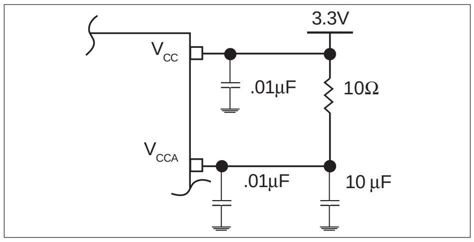


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS8432-51 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

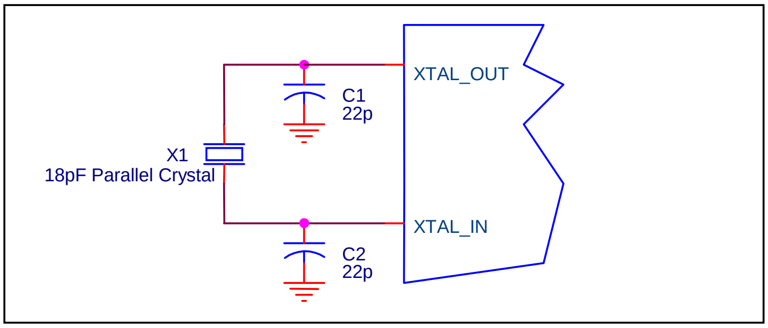


FIGURE 3. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

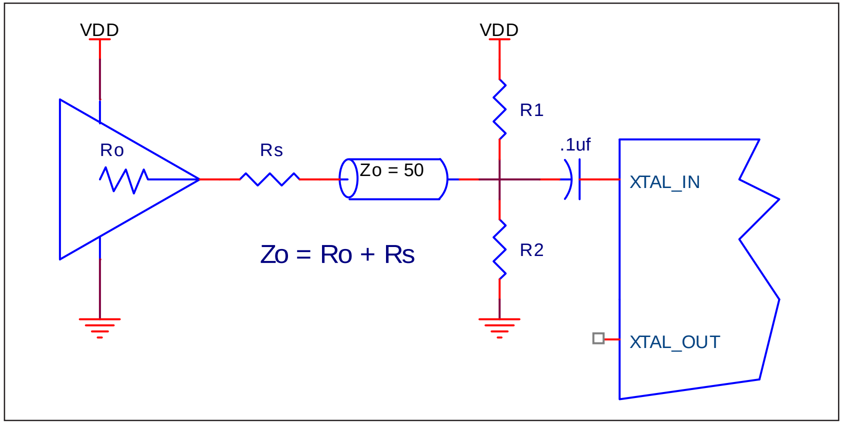


FIGURE 4. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

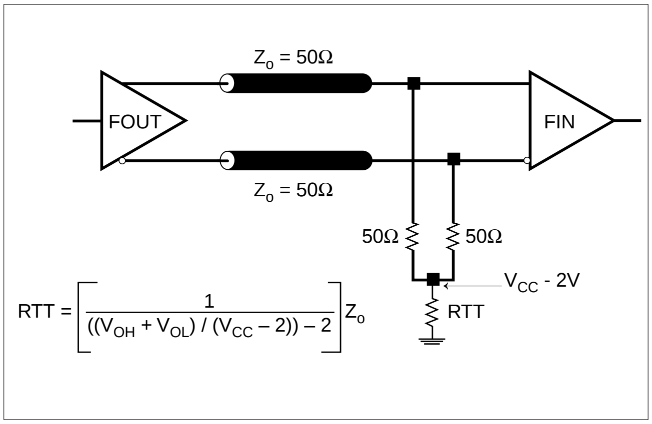
LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUTx and nFOUTx are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



$$RTT = \left[\frac{1}{((V_{OH} + V_{OL}) / (V_{CC} - 2)) - 2}\right] Z_o$$

FIGURE 5A. LVPECL OUTPUT TERMINATION

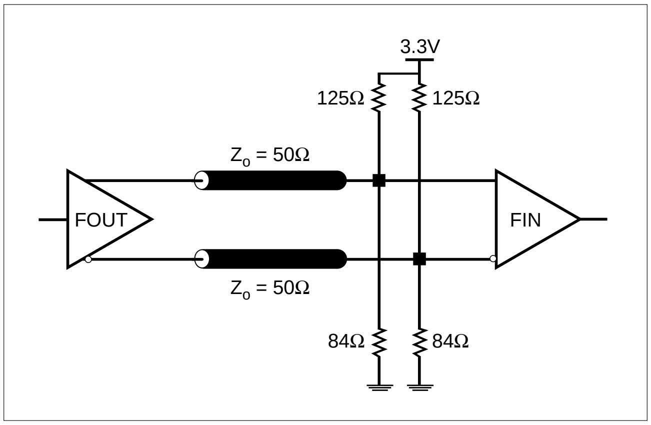


FIGURE 5B. LVPECL OUTPUT TERMINATION

VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/ Electrically Enhance Leadfame Base Package, Amkor Technology.

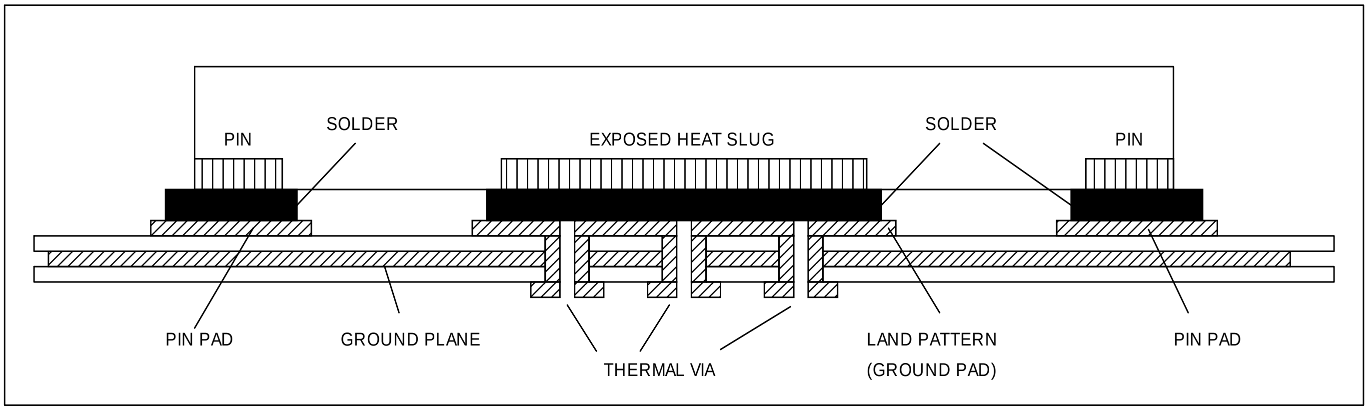


FIGURE 6. P.C.ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

LAYOUT GUIDELINE

The schematic of the ICS8432-51 layout example used in this layout guideline is shown in *Figure 7A.* The ICS8432-51 recommended PCB board layout for this example is shown in *Figure 7B.* This layout example is used as a general guideline.

The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

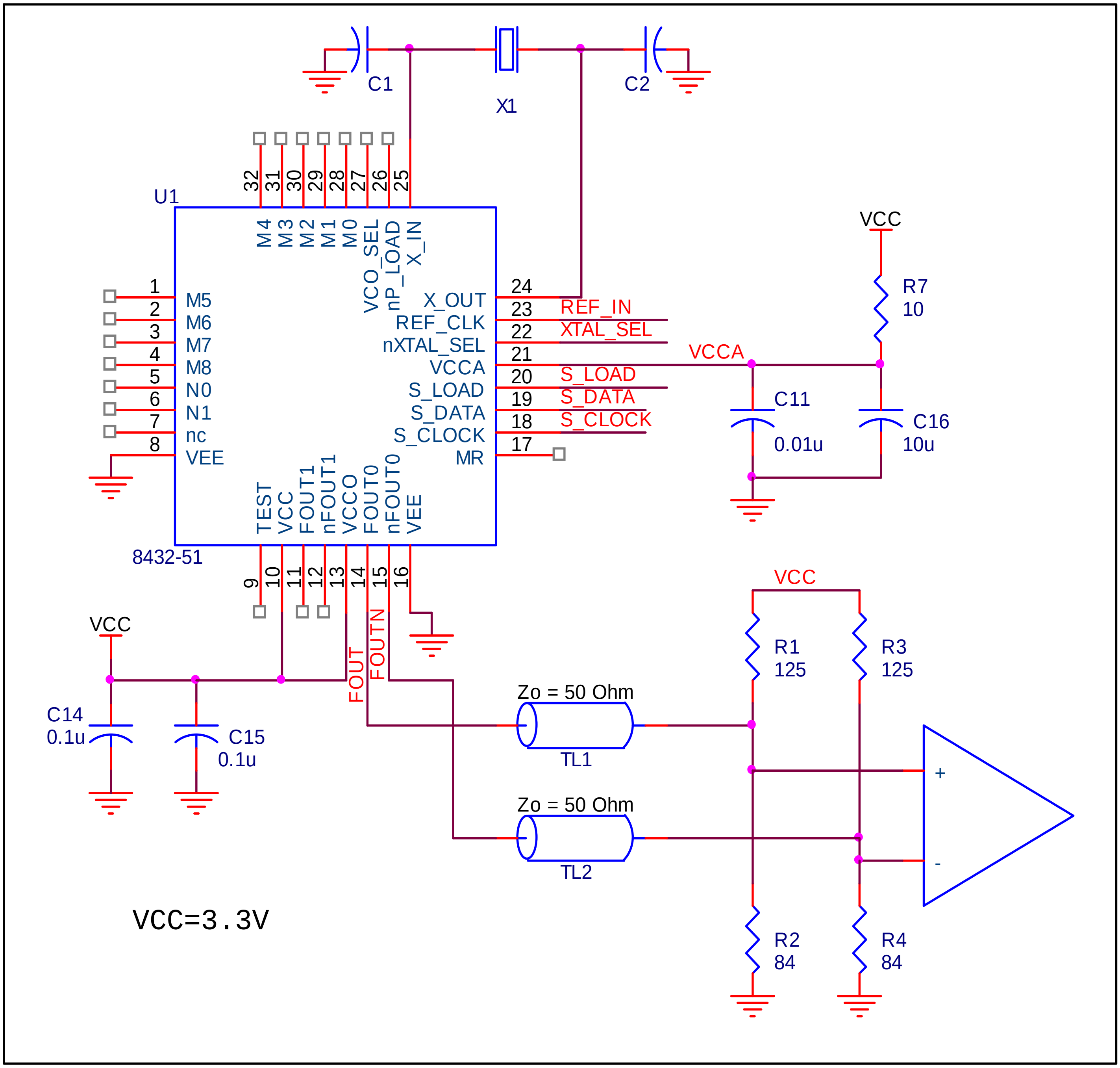


FIGURE 7A. SCHEMATIC OF RECOMMENDED LAYOUT

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors C14 and C15, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.
Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.
The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{CCA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

CRYSTAL

The crystal X1 should be located as close as possible to the pins 24 (XTAL_OUT) and 25 (XTAL_IN). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

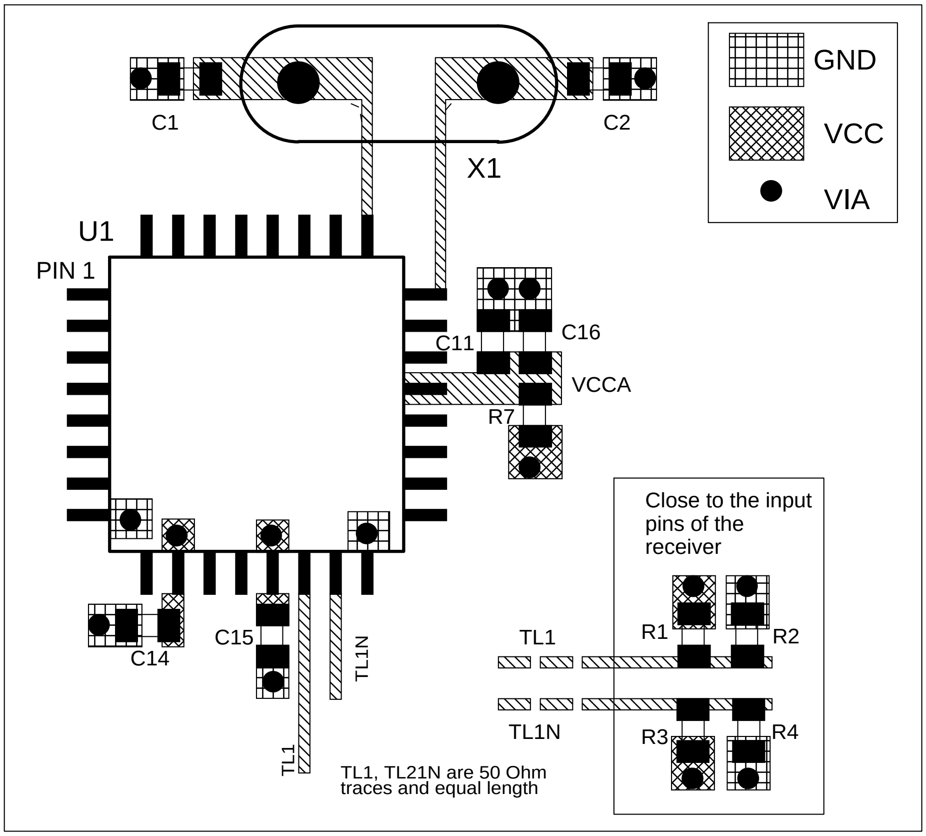


FIGURE 7B. PCB BOARD LAYOUT FOR ICS8432-51

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8432-51. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8432-51 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 135mA = **467.8mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

Total Power $_{\_MAX}$ (3.465V, with all outputs switching) = 467.8mW + 60mW = **527.8mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 10A below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.528W * 42.1°C/W = 92.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 10A. THERMAL RESISTANCE θ_{JA} FOR 32-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 10B. THERMAL RESISTANCE θ_{JA} FOR 32-PIN VFQFN, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	34.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 8.*

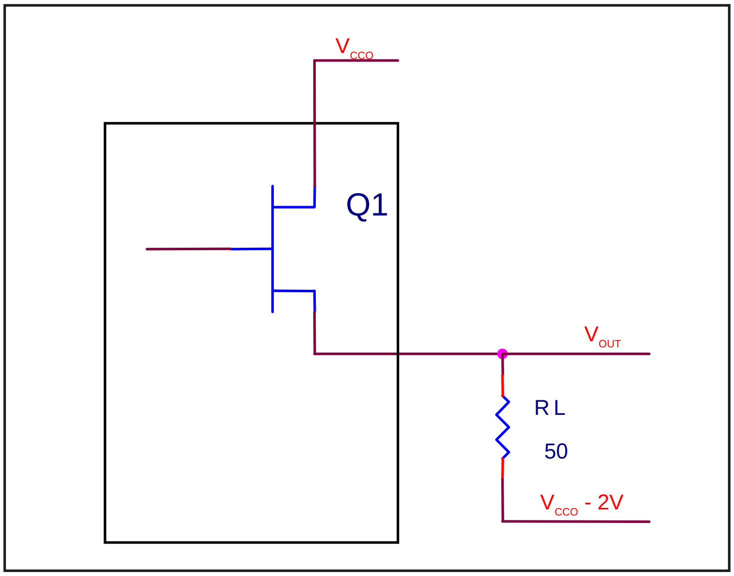


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega) * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega) * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 11A. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 11B. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD VFQFN PACKAGE

θ_{JA} by Velocity (Linear Feet per Minute)	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	34.8°C/W

TRANSISTOR COUNT

The transistor count for ICS8432-51 is: 3743

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

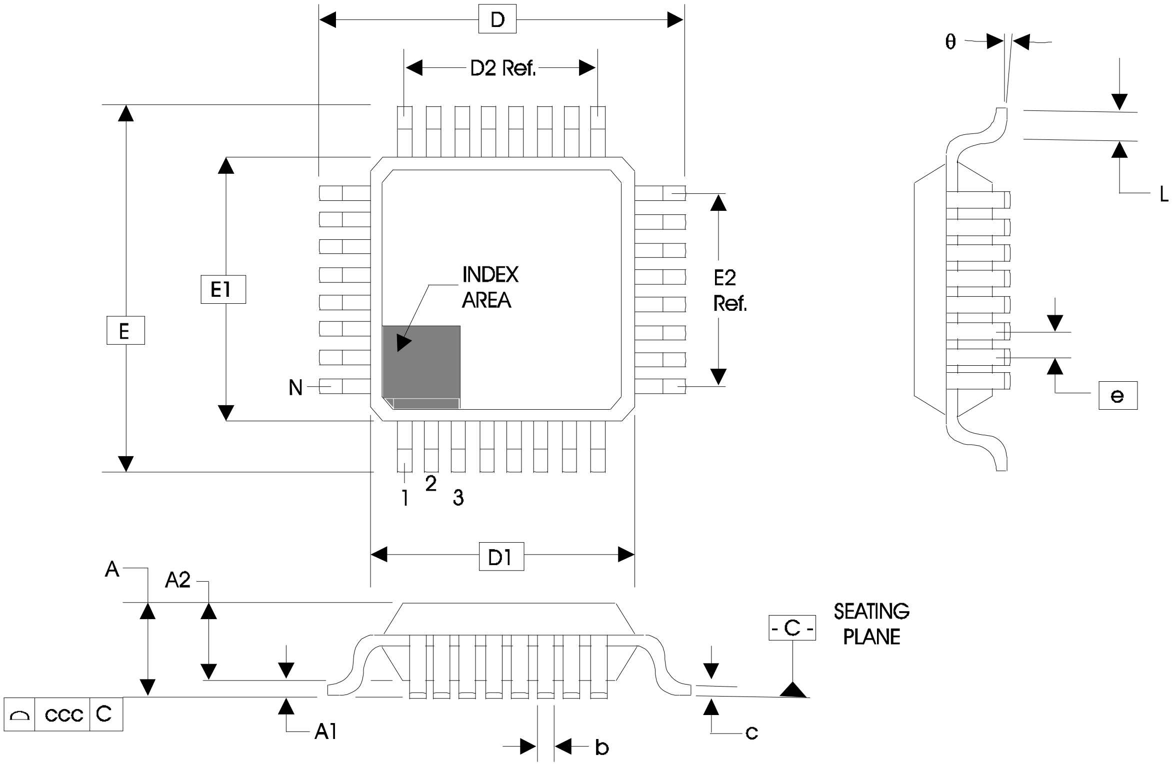
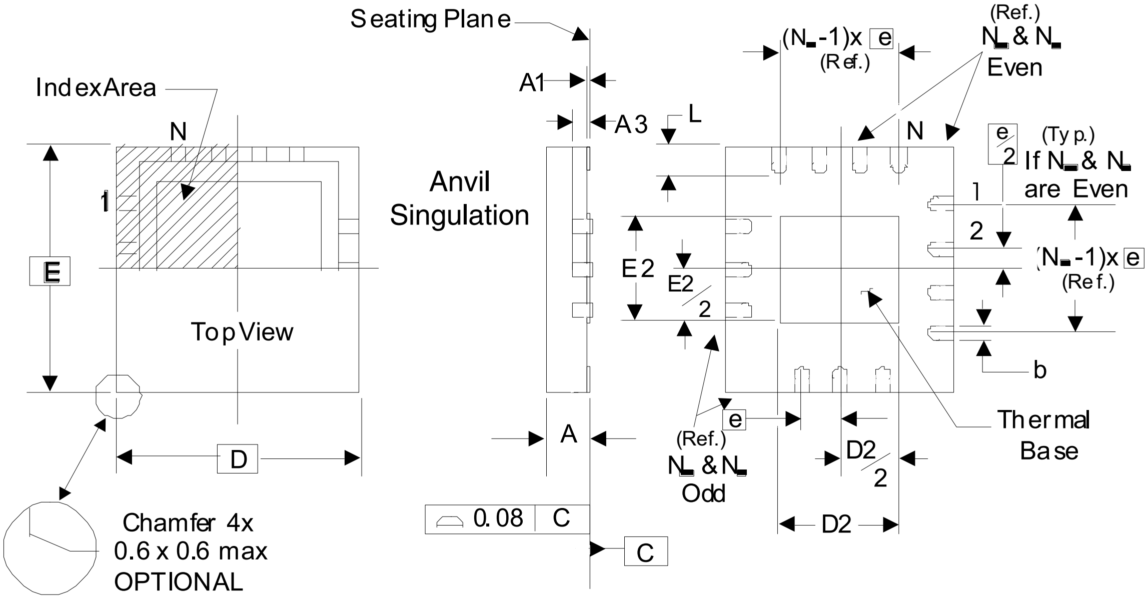


TABLE 12A. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**BBA**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
●	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

PACKAGE OUTLINE - K SUFFIX 32 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

TABLE 12B. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**Minimum**	**Maximum**
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D	5.0	
D2	3.0	3.30
E	5.0	
E2	3.0	3.30
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 13. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8432CY-51LF	ICS8432CY51L	32 lead "Lead Free" LQFP	Tube	0°C to +70°C
8432CY-51LFT	ICS8432CY51L	32 lead "Lead Free" LQFP	Tape and Reel	0°C to +70°C
8432CK-51LF	ICS8432C51L	32 lead "Lead Free" VFQFN	Tube	0°C to +70°C
8432CK-51LFT	ICS8432C51L	32 lead "Lead Free" VFQFN	Tape and Reel	0°C to +70°C

NOTE: "LF" suffix to the part number are the PB-free configuration, RoHS compliant

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A		2	Corrected labels on the Parallel & Serial Load Operations diagram.	12/18/02
B	T1	3	Revised MR pin description.	2/13/03
	T4A	5	Power Supply table - changed I_{DD} to 155mA max. from 130mA max., changed I_{DDA} to 20mA max. from 15mA max., and changed I_{DDO} to 55mA max. from 45mA max.	
B		9	Added LVDS Driver Termination Section.	3/12/03
C		1	General Description & Features - changed VCO min. from 200MHz to 250MHz and replaced throughout the datasheet in: (Functional Description pg2, T3C Program. Output Divider Func. Table pg4, and T5 Input Freq Charac. Table pg6). - Features - changed min. Output Frequency Range from 25MHz to 31.25MHz.	5/9/03
	T1	3	Pin Descriptions Table - revised XTAL1, XTAL2 pin description.	
	T2	3	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical.	
	T3B	4	Prog. VCO Freq. Func. Table - deleted 200 and 225 rows, does not apply.	
	T4A	5	Power Supply DC Characteristics Table - deleted V_{DDO} & I_{DDO} rows, does not apply.	
	T7	6	AC Characteristics Table - change F_{OUT} 25MHz min. to 31.25MHz min.	
C		1	Pin Assignment - corrected XTAL pins. Pin 24 is labeled XTAL2 and pin 25 is labeled XTAL1.	5/28/03
		2	Revised Parallel & Serial Load Operations diagram.	
	T1	3	Pin Descriptions Table - corrected XTAL pins to correspond with the pin number. Changed XTAL1 to read input and XTAL2 to read output.	
		10	Updated Figure 5A schematic to correspond the XTAL pins with the Pin Assignment.	
		11	Crystal section, corrected pin 24 to read XTAL2 and pin 25 to read XTAL1.	
C		1	Features Section - added Lead-Free bullet.	4/8/05
	T13	16	Ordering Information - added Lead-Free part number.	
D		1	Added 32 Lead VFQFN Package for Pin Assignment.	4/13/06
	T4A	5	Power Supply DC Characteristics Table - changed V_{CCA} min. from 3.135V to V_{CC} - 0.15V.	
	T6	6	Crystal Characteristics Table - added Drive Level.	
		9	Added *LVCMOS to XTAL Interface.*	
		10	Added *Recommendations for Unused Input and Output Pins.*	
			Added VFQFN package throughout the datasheet.	
E		1	Changed naming convention of TEST_CLK to REF_CLK, (pin 24) XTAL2 to XTAL_OUT, and (pin 25) XTAL1 to XTAL_IN. Changed throughout the datasheet.	4/10/07
	T4C	6	LVPECL DC Characteristics Table - corrected V_{OH} max. from V_{CCO} - 1.0V to V_{CCO} - 0.9V.	
		13 - 14	Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 4C.	
	T13	18	Ordering Information Table - corrected ICS8432BK-51 marking to ICS8432BK51. Added VFQFN marking.	
F		1	Pin Assignment - corrected typo on pin 25 from XTAL_OUT to XTAL_IN.	5/13/08
		11	Added *VFQFN EPAD Thermal Release Path section.*	
F		1	General Description - deleted the HiperClocks logo.	11/13/12
	T12B	18	VFQFN Package Dimensions - corrected D2/E2 dimensions	
	T13	19	Ordering Information Table - per PCN# N1209-02 updated die revision ordering and marking from "B" to "C".	
			Updated footer part number from revision "B" to "C".	

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