Precision Digital Power Monitor

ISL28022

The ISL28022 is a bi-directional high-side and low-side digital current sense and voltage monitor with serial interface. The device monitors current and voltage and provides the results digitally along with calculated power. The ISL28022 provides tight accuracy of less than 0.3% for both voltage and current monitoring over the entire input range. The digital power monitor has configurable fault thresholds and measurable ADC gain ranges.

The ISL28022 handles common-mode input voltage ranging from 0V to 60V. The wide range permits the device to handle telecom, automotive and industrial applications with minimal external circuitry. Both high and low-side ground sensing applications are easily handled with the flexible architecture.

The ISL28022 consumes an average current of just 700µA and is available in the space saving 10 Ld MSOP package. The ISL28022 is also offered in a 16 Ld QFN package. The part operates over the extended temperature range from -40°C to +125°C.

Features

- Bus voltage sense range . . . . . 0V to 60V
- 16-bit ∑ΔADC monitors current and voltage
- Voltage measuring error . . . . . <0.3%
- Current measuring error . . . . . <0.3%
- Handles negative system voltage
- Over/undervoltage and current fault monitoring
- I^2C/SMBus interface
- Wide V_{CC} range . . . . . 3V to 5.5V
- ESD (HBM). 8kV
- Supports high speed I^2C 3.4MHz

Applications

- Routers and servers
- DC/DC, AC/DC converters
- Battery management/charging
- Automotive power
- Power distribution
- Medical and test equipment

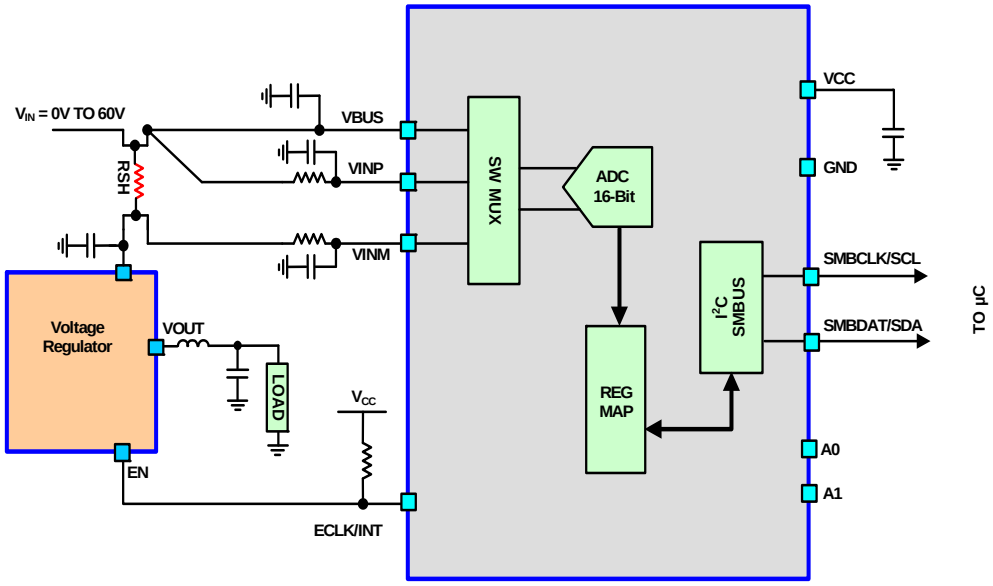

FIGURE 1. TYPICAL APPLICATION

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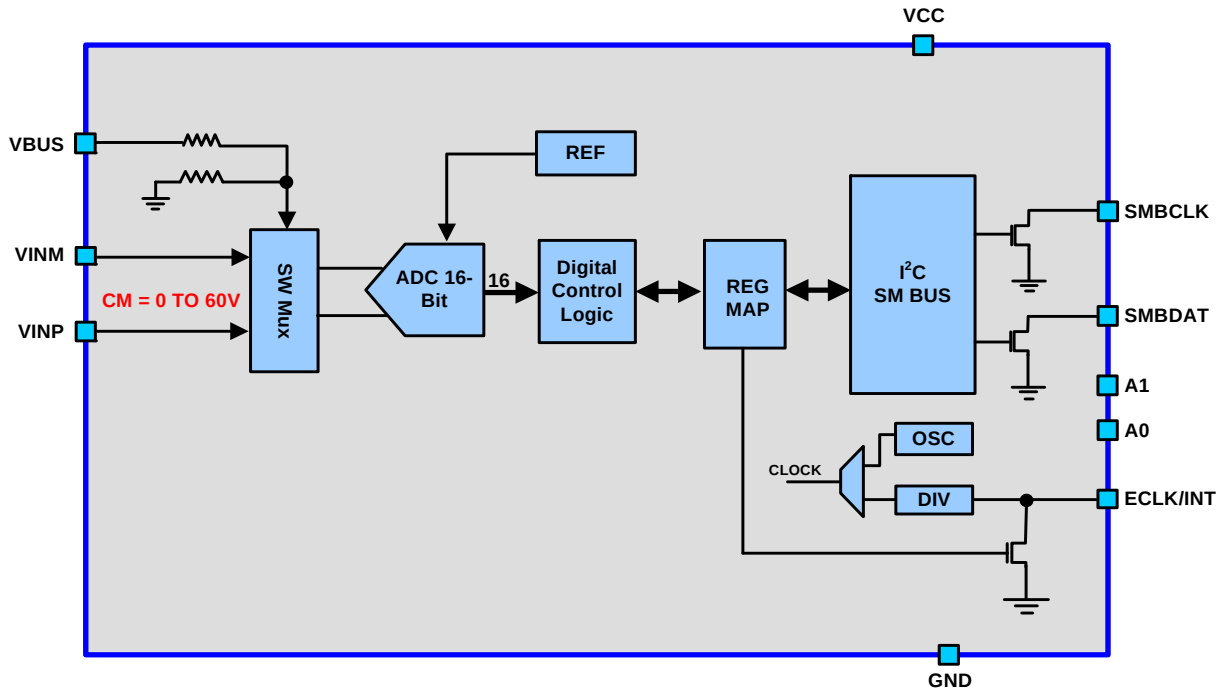
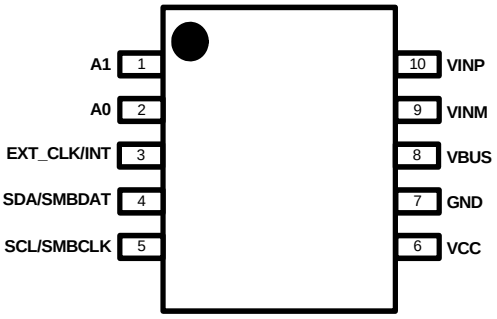
Block Diagram

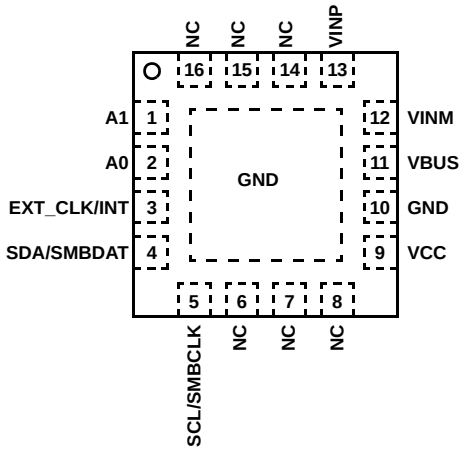


Pin Configurations

ISL28022
(10 LD MSOP)
TOP VIEW



ISL28022
(16 LD QFN)
TOP VIEW



Pin Descriptions

MSOP PIN NUMBER	QFN PIN NUMBER	PIN NAME	DESCRIPTION
1	1	A1	I^2C address, bit 1
2	2	A0	I^2C address, bit 0
3	3	EXT_CLK/INT	External ADC clock input or CPU interrupt output signal. When the pin is configured as an interrupt, the output is an open drain.
4	4	SMBDAT/SDA	I^2C serial data input/output
5	5	SMBCLK/SCL	I^2C clock input
6	9	VCC	Positive power pin. The positive power supply to the part.
7	10	GND	Negative power pin. Can be connected to ground or a negative voltage.
8	11	VBUS	VBUS power voltage sense.
9	12	VINM	Current sense minus input.
10	13	VINP	Current sense plus input.
	6	NC	No connect. No internal connection.
	7	NC	No connect. No internal connection.
	8	NC	No connect. No internal connection.
	14	NC	No connect. No internal connection.
	15	NC	No connect. No internal connection.
	16	NC	No connect. No internal connection.
	Epad	GND	Negative power pin. Can be connected to ground or a negative voltage

Ordering Information

PART NUMBER (Note 4)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
Coming Soon ISL28022FUZ (Note 1)	8022F	10 Ld MSOP	M10.118
Coming Soon ISL28022FRZ (Note 1)	022F	16 Ld QFN	L16.3x3B
ISL28022FRZR5453	022F	16 Ld QFN	L16.3x3B
ISL28022FRZ-TR5453 (Note 2)	022F	16 Ld QFN	L16.3x3B
ISL28022FRZ-T7AR5453 (Note 2)	022F	16 Ld QFN	L16.3x3B
ISL28022FUZR5453	8022F	10 Ld MSOP	M10.118
ISL28022FUZ-TR5453 (Note 2)	8022F	10 Ld MSOP	M10.118
ISL28022FUZ-T7AR5453 (Note 2)	8022F	10 Ld MSOP	M10.118

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL28022. For more information on MSL please see tech brief TB363.

Absolute Maximum Ratings

VCC 6.0V
VBUS Voltage. 63V
Common Mode Input Voltage (V_{INP}, V_{INM}) 63V
Differential Input Voltage (V_{INP}, V_{INM}) . . . . . ±63V
Input Voltage (Digital Pins) . . . . . GND-0.3V to 5.5V
Output Voltage (Digital Pins) . . . . . GND-0.3 to VCC+0.3V
Open Drain Output Current 10mA
Open Drain Voltage (Interrupt) 24V
ESD Rating
- Human Body Model 8kV
- Machine Model 300V
- Charged Device Model 2.0kV

Latch up . . . . . 60V @ + 125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN (Notes 5, 6)	52	6.5
10 Ld MSOP (Notes 7, 8)	150	55

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature (T_{JMAX}) . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. For θJC, the "case temp" location is taken at the package top center.

Electrical Specifications

T_A = +25°C, V_{CC} = 3.3, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP}-V_{INM} = 32mV, unless otherwise specified. All voltages with respect to GND pin.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
INPUTS						
$V_{SENSEDIFF}$	Useful Full Scale Current Sense Differential Voltage Range (V_{INP}-V_{INM})	PGA Gain = /1	0		±40	mV
		PGA Gain = /2	0		±80	mV
		PGA Gain = /4	0		±160	mV
		PGA Gain = /8	0		±300	mV
V_{SHUNT_step}	LSB Step Size, Shunt Voltage			10		µV
$V_{CMSENSE}$	Current Sense Common Mode (VINP, VINM)		0		V_{BUS}	V
V_{OS}	V_{SENSE} Offset Voltage	PGA Gain = /1, /2, /4, /8; ADC Setting = 1111		±10	±75	µV
V_{OSTC}	V_{SENSE} Offset Voltage Temperature Coefficient			0.15		µV/°C
CMRR	V_{SENSE} V_{OS} vs Common Mode	V_{BUS} = 0 to 60V; BRNG = 2, 3	110	130		dB
PSRR	V_{SENSE} V_{OS} vs Power Supply	V_{CC} = 3V to 5V		105		dB
A_{CS}	Current Sense Gain Error			±40		m%
A_{CSTC}	Current Sense Gain Error Temperature Coefficient			±1		m%/°C
I_{VINACT}	Input Leakage, VIN Pins	Active Mode (for both V_{INP} and V_{INM} pins)		±20		µA
I_{VINACT}	Input Leakage, VIN Pins	Power Down Mode (for both V_{INP} and V_{INM} pins)		±0.1	±0.5	µA

Electrical Specifications T_A = +25°C, V_{CC} = 3.3, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP}-V_{INM} = 32mV, unless otherwise specified. All voltages with respect to GND pin. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
V_{BUS}	Useful Bus Voltage Range	BRNG = 0	0		16	V
		BRNG = 1	0		32	V
		BRNG = 2, 3	0		60	V
V_{BUS}_Step	LSB Step Size, Bus Voltage	BRNG = 0		4		mV
V_{BUS}_VCO	V_{BUS} Voltage Coefficient			50		ppm/V
R_{VBACT}	Input Impedance, VBUS Pin	Active Mode		600		kΩ
DC ACCURACY						
	ADC Resolution (Native)	PGA gain = /1, V_{SENSE} = ±300mV		16		Bits
	Current Measurement Error	T_A = +25°C		±0.2	±0.3	%
	Current Measurement Error Over Temperature	T_A = -40°C to +85°C			±0.5%	%
		T_A = -40°C to +125°C			±1%	%
	Bus Voltage Measurement Error	T_A = +25°C		±0.2	±0.3	%
	Bus Voltage Measurement Error Over Temperature	T_A = -40°C to +85°C			±0.5%	%
		T_A = -40°C to +125°C			±1%	%
ADC TIMING SPECS						
t_s	ADC Conversion Time	ADC setting = 0000		72	79.2	µs
		ADC setting = 0001		132	145.2	µs
		ADC setting = 0010		258	283.8	µs
		ADC setting = 0011		508	558.8	µs
		ADC setting = 1001		1.01	1.11	ms
		ADC setting = 1010		2.01	2.21	ms
		ADC setting = 1011		4.01	4.41	ms
		ADC setting = 1100		8.01	8.81	ms
		ADC setting = 1101		16.01	17.61	ms
		ADC setting = 1110		32.01	35.21	ms
		ADC setting = 1111		64.01	70.41	ms
I^2C INTERFACE SPECIFICATIONS						
V_{IL}	SDA and SCL Input Buffer LOW Voltage		-0.3		0.3 x VCC	V
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		0.7 x V_{CC}		V_{CC} + 0.3	V
Hysteresis	SDA and SCL Input Buffer Hysteresis			0.05 x V_{CC}		V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{CC} = 5V, I_{OL} = 3mA	0	0.02	0.4	V
C_{PIN}	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{CC} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF
f_{SCL}	SCL Frequency				400	kHz

Electrical Specifications T_A = +25°C, V_{CC} = 3.3, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP}-V_{INM} = 32mV, unless otherwise specified. All voltages with respect to GND pin. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing.	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing.	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}.	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	20		900	ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 x Cb		300	ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 x Cb		300	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip		75		pF
R_{PU}	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ~2.5kΩ. For Cb = 40pF, max is about 15kΩ~20kΩ	1			kΩ

Electrical Specifications T_A = +25°C, V_{CC} = 3.3, V_{INP} = V_{BUS} = 12V, V_{SENSE} = V_{INP}-V_{INM} = 32mV, unless otherwise specified. All voltages with respect to GND pin. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
POWER SUPPLY						
	Operating Supply Voltage Range		3		5.5	V
I_{CCEXT}	Power Supply Current On V_{CC} Pin, Active Mode	External power supply mode, V_{CC} = 5V		0.7	1.0	mA
I_{CCPD}	Power Supply Current On V_{CC} Pin, Power-Down Mode	External power supply mode, V_{CC} = 5V		5	15	µA

NOTE:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, S(B)ADC =15; unless otherwise specified.

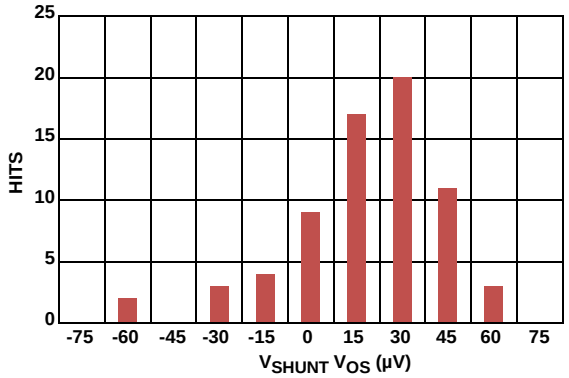


FIGURE 2. V_{SHUNT} V_{OS}

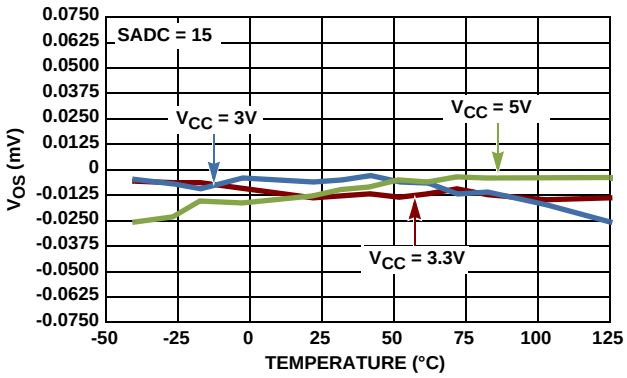


FIGURE 3. V_{SHUNT} V_{OS} vs TEMPERATURE

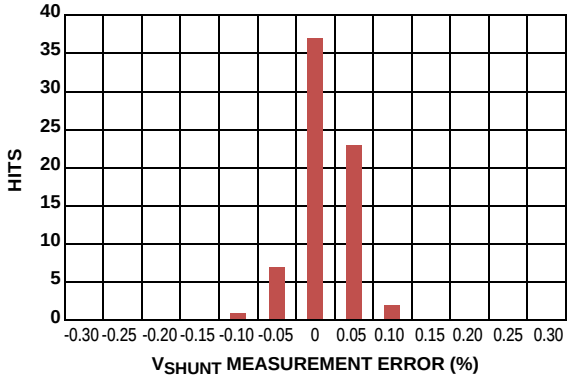


FIGURE 4. V_{SHUNT} MEASUREMENT ERROR

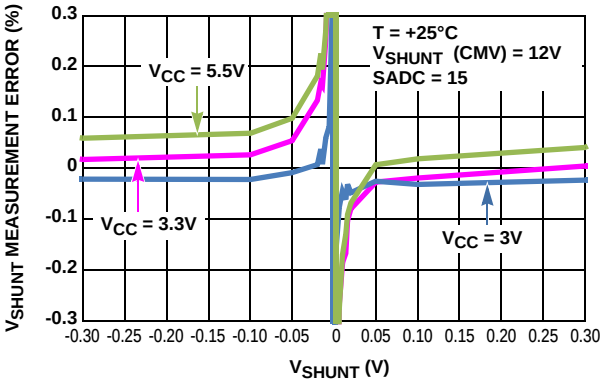


FIGURE 5. V_{SHUNT} MEASUREMENT ERROR vs V_{SHUNT} INPUT

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, S(B)ADC =15; unless otherwise specified. **(Continued)**

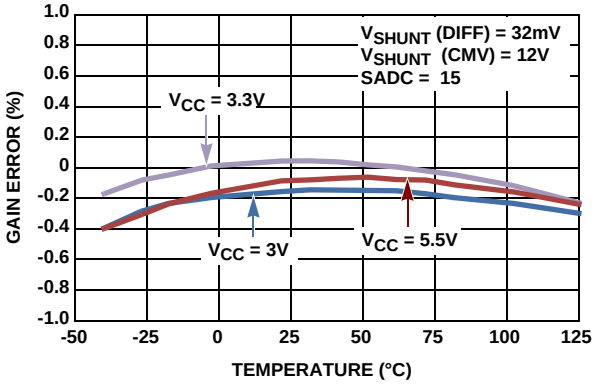


FIGURE 6. V_{SHUNT} GAIN vs TEMPERATURE

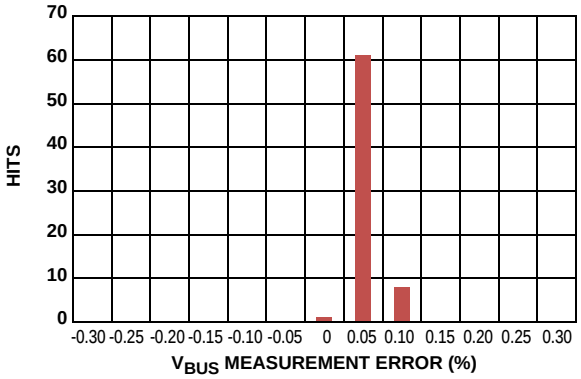


FIGURE 7. V_{BUS} MEASUREMENT ERROR DISTRIBUTION

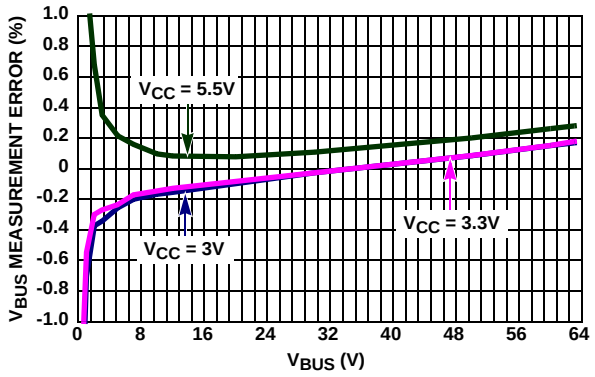


FIGURE 8. V_{BUS} MEASUREMENT ERROR vs V_{BUS} (T_A = +25°C)

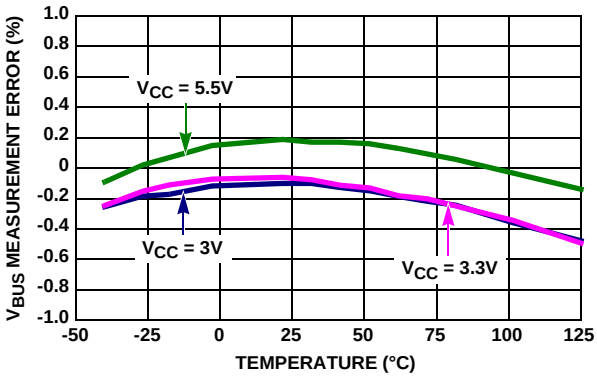


FIGURE 9. V_{BUS} MEASUREMENT ERROR vs TEMPERATURE

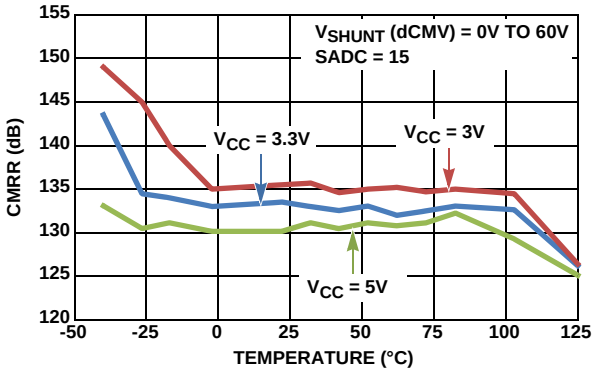


FIGURE 10. CMRR vs TEMPERATURE

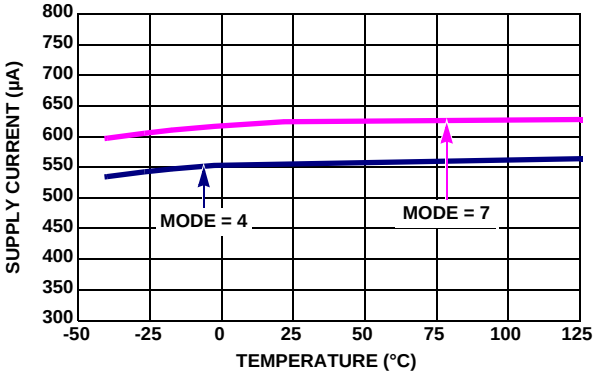


FIGURE 11. SUPPLY CURRENT vs MODE vs TEMPERATURE

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, S(B)ADC =15; unless otherwise specified. **(Continued)**

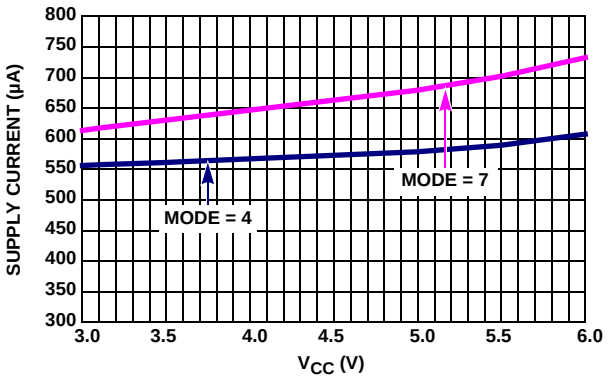


FIGURE 12. SUPPLY CURRENT vs MODE vs VCC

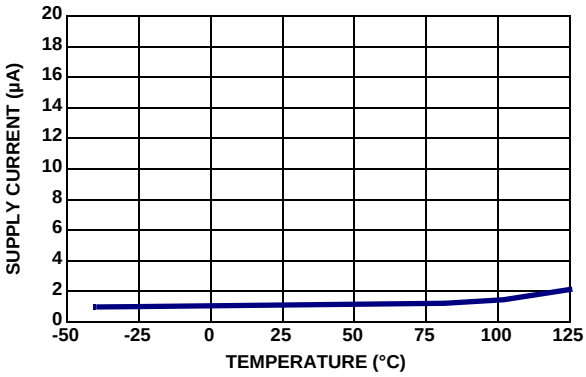


FIGURE 13. SUPPLY CURRENT vs MODE 0 vs TEMPERATURE

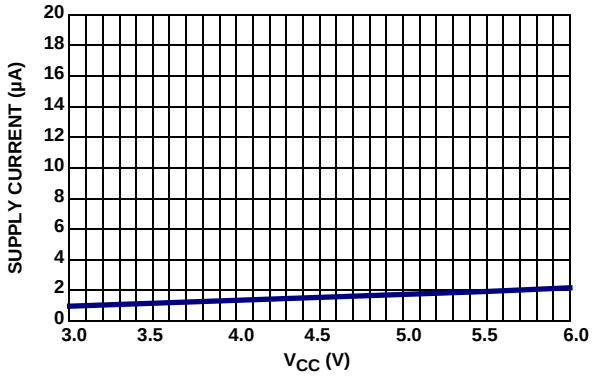


FIGURE 14. SUPPLY CURRENT vs MODE 0 vs V_{CC}

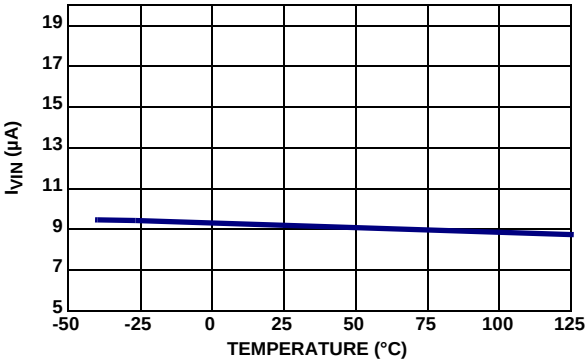


FIGURE 15. SHUNT I_{VIN} vs TEMPERATURE (MODE 5)

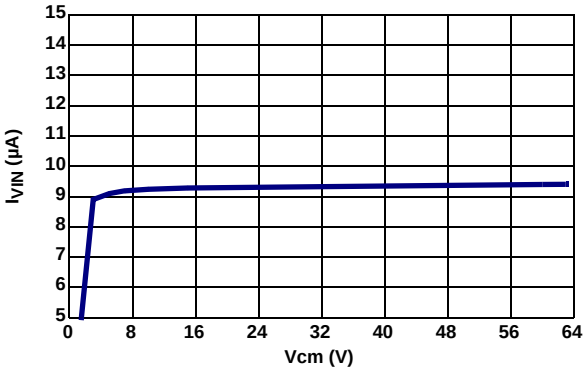


FIGURE 16. SHUNT I_{VIN} vs COMMON MODE VOLTAGE (MODE 5)

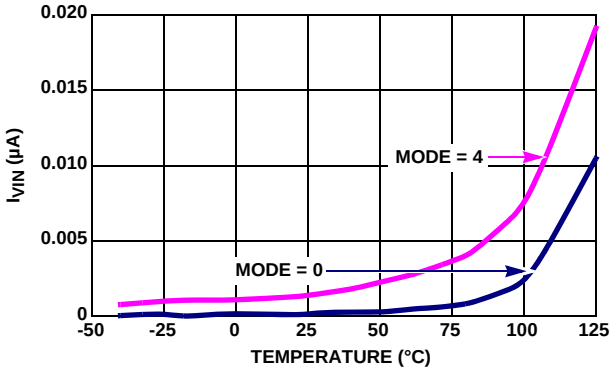


FIGURE 17. SHUNT I_{VIN} vs TEMPERATURE (MODE 0, 4)

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, S(B)ADC =15; unless otherwise specified. **(Continued)**

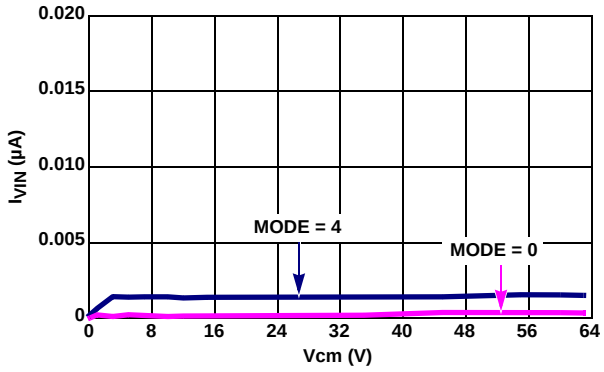


FIGURE 18. SHUNT I_{VIN} vs COMMON MODE VOLTAGE (MODE 0, 4)

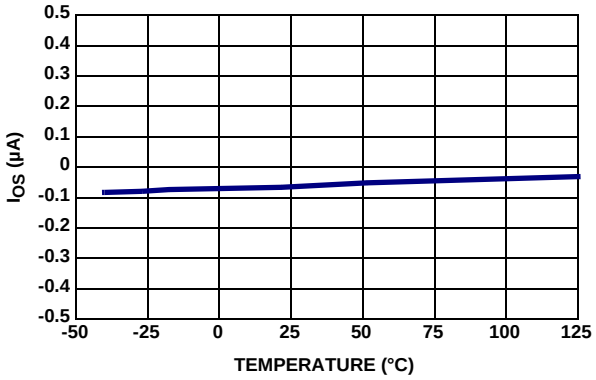


FIGURE 19. SHUNT I_{OS} vs TEMPERATURE (MODE 5)

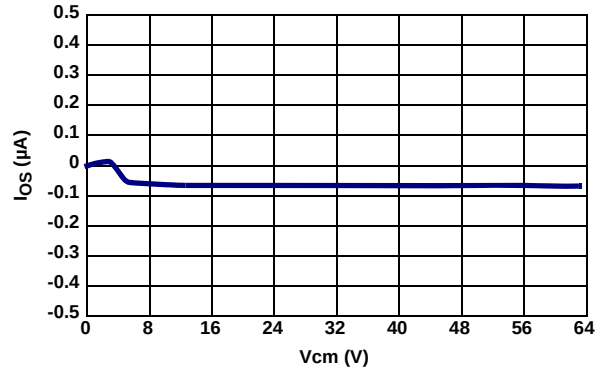


FIGURE 20. SHUNT I_{OS} vs COMMON MODE VOLTAGE (MODE 5)

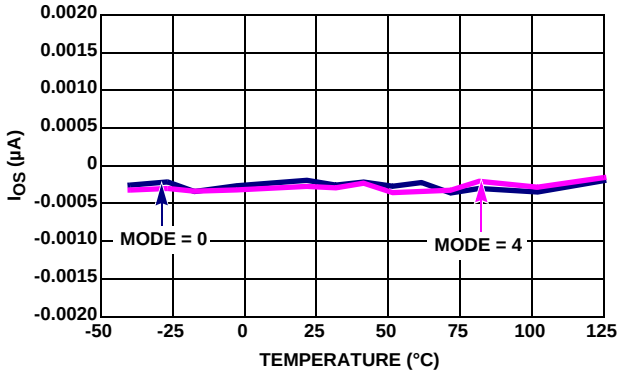


FIGURE 21. SHUNT I_{OS} vs TEMPERATURE (MODE 0, 4)

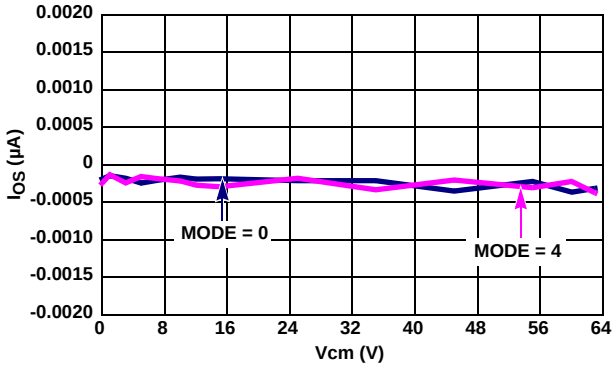


FIGURE 22. SHUNT I_{OS} vs COMMON MODE VOLTAGE (MODE 0, 4)

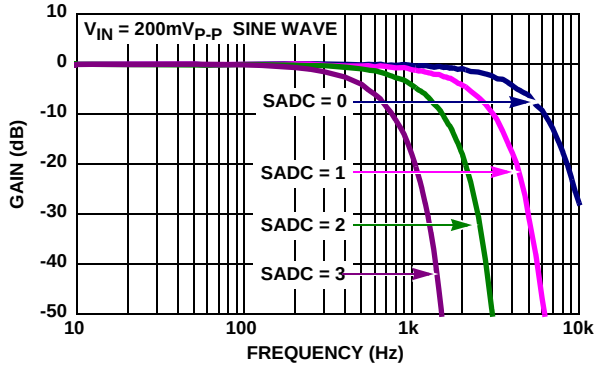


FIGURE 23. V_{SHUNT} BANDWIDTH vs SADC MODE

Typical Performance Curves

T_A = +25°C, V_{CC} = 3.3V, V_{INP} = V_{BUS} = 12V, S(B)ADC =15; unless otherwise specified. **(Continued)**

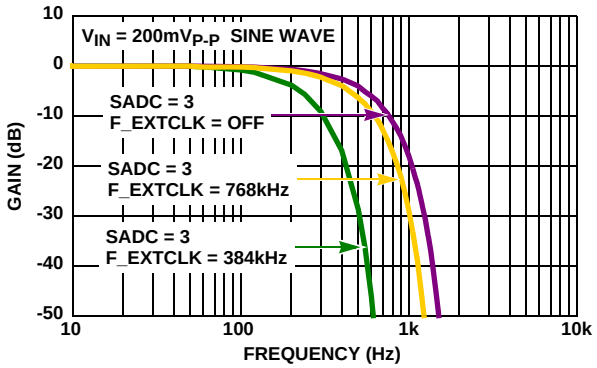


FIGURE 24. V_{SHUNT} BANDWIDTH vs EXTERNAL CLOCK FREQUENCY

Functional Description

Overview

The ISL28022 is a digital power monitor (DPM) device that is capable of measuring bi-directional currents while monitoring the bus voltage.

The DPM requires an external shunt resistor to enable current measurements. The shunt resistor translates the bus current to a voltage. The DPM measures the voltage across the shunt resistors and reports the measured value out digitally via an I^2C interface. A register within the DPM is reserved to store the value of the shunt resistor. The stored current sense resistor value allows the DPM to output the current value to an external digital device.

The ISL28022 measures bus voltage and current sequentially. The device has a power measurement functionality that multiplies current and voltage measured values. The power calculation is stored in a unique register. The power measurement allows the user to monitor power to or from the load in addition to current and voltage.

The ISL28022 can monitor supplies from 0 to 60V while operating on a chip supply ranging from 3V to 5.5V.

The ISL28022 ADC sample rate can be configured to an internal oscillator (500kHz) or a user can provide a synchronized clock.

Detailed Description

The ISL28022 consists of a two channel analog front end multiplexer, a 16-bit sigma delta ADC and digital signal processing/serial communication circuitry.

The main block within the device is a 3rd order Sigma Delta ADC. The input signal bandwidth is 1kHz, wide enough for power monitoring applications. The main block includes an internal 1.2V band gap voltage reference that is used to drive the ADC.

The analog front end multiplexer selects the input to the ADC. The selection to the input of the ADC is either a single ended V_{BUS} measurement or a fully differential measurement across a shunt resistor.

The digital block contains controllable registers, I^2C serial communication circuitry and a state machine. The state machine controls the behavior of the ADC acquisition, whether the acquisition is triggered or continuous. A more detailed description of the state machine states can be found in “MODE: Operating Mode” on page 14.

Pin Descriptions

A1

A1 is the address select pin. A1 is one of two I^2C/SMBus slave address select pins that are multi-logic programmable for a total of 16 different address combinations.

There are four selectable levels for A1, VCC, GND, SCL/SMBCLK, and SDA/SMBDAT. See Table 21 for more details in setting the slave address of the device.

A0

A0 is the address select pin. A0 is one of two I^2C/SMBus slave address select pins that are multi-logic programmable for a total of 16 different address combinations.

There are four selectable levels for A0, VCC, GND, SCL/SMBCLK, and SDA/SMBDAT. See Table 21 for more details in setting the slave address of the device.

EXT_CLK/INT

EXT_CLK/INT is the External/Interrupt clock pin. EXT_CLK/INT is a bi-directional pin. The pin provides a connection to the system clock. The system clock is connected to the ADC. The acquisitions rate of the ADC can be varied through the EXT_CLK/INT pin. The pin functionality is set through a control register bit.

When the EXT_CLK/INT pin is configured as an output, the pin functionality becomes an interrupt flag to connecting devices. EXT_CLK/INT pin as an output requires a pull up resistor to a power supply, up to 20V, for proper operation.The internal threshold detectors (OV_{sh}/UV_{sh}/OV_b/UV_b) signal level relative to the measured value determines the state of the INT pin.

SDA/SMBDAT

SDA/SMBDAT is the serial data input/output pin. SDA/SMBDAT is a bi-directional pin used to transfer data to and from the device. The pin is an open drain output and may be wired with other open drain/collector outputs. The open drain output requires a pull-up resistor for proper functionality. The pull-up resistor should be connected to VCC of the device.

SCL/SMBCLK

SCL/SMBCLK is the serial clock input pin. The SCL/SMBCLK input is responsible for clocking in all data to and from the device.

VCC

VCC is the positive supply voltage pin. VCC is an analog power pin. VCC supplies power to the device.

GND

GND is the ground pin. All voltages internal to the chip are referenced to ground. GND should be tied to 0V for single supply applications. For dual supply applications, the pin should be connected to the most negative voltage in the application.

VBUS

VBUS is the power bus voltage input pin. The pin should be connected to the desired power supply bus to be monitored.

VINP

VINP is the shunt voltage monitor positive input pin. The pin connects to the most positive voltage of the current shunt resistor.

VINM

VINM is the shunt voltage monitor negative input pin. The pin connects to the most negative voltage of the current shunt resistor.

TABLE 1. ISL28022 REGISTER DESCRIPTIONS

REGISTER ADDRESS (HEX)	REGISTER NAME	FUNCTION	POWER-ON RESET VALUE (HEX)	ACCESS
00	Configuration	Power On Reset, Bus and Shunt ranges, ADC acquisition times, Mode configuration	799F	R/W
01	Shunt Voltage	Shunt voltage measurement value	0000	R
02	Bus Voltage	Bus voltage measurement value	0000	R
03	Power	Power measurement value	0000	R
04	Current	Current measurement value	0000	R
05	Calibration Register	Register used to enable current and power measurements.	0000	R/W
06	Shunt Voltage Threshold	Min/Max Shunt thresholds	7F81	R/W
07	Bus Voltage Threshold	Min/Max VBUS thresholds	FF00	R/W
08	DCS Interrupt Status	Threshold interrupts	0000	R/W
09	Aux Control Register	Register to control the interrupts and external clock functionality	0000	R/W

TABLE 2. CONFIGURATION REGISTER

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	RST	BRNG1	BRNG0	PG1	PG0	BADC3	BADC2	BADC1	BADC0	SADC3	SADC2	SADC1	SADC0	MODE2	MODE1	MODE0

Register Descriptions

Table 1 is the register map for the device. The table describes the function of each register and its respective value. The addresses are sequential and the register size is 16 bits (2 bytes) per address.

CONFIGURATION REGISTER

The configuration register (Table 2) controls the functionality of the chip. ADC measurable range, converter acquisition times, converter resolution and state machine modes are configurable bits within this register.

RST: Reset Bit

Configuring the reset bit (bit15) to a 1 generates a system reset that initializes all registers to their default values and performs a system calibration.

BRNG: Bus Voltage Range

Bits 13 and 14 of the configuration register sets the bus measurable voltage range. Table 3 shows the BRNG bit configurations versus the allowable full scale measurement range. The shaded row is the power-up default.

TABLE 3. BRNG BIT SETTINGS

BRNG1	BRNG0	USABLE FULL SCALE RANGE (V)
0	0	16
0	1	32
1	0	60
1	1	60

PG: PGA (Shunt Voltage Only)

Bits 11 and 12 of the configuration register determines the shunt voltage measurement range. Table 4 shows the PGA bit configurations versus the allowable full scale measurement range. The shaded row is the power up default.

TABLE 4. PGA BIT SETTINGS

PG1	PG0	GAIN	RANGE (mV)
0	0	1	±40
0	1	÷2	±80
1	0	÷4	±160
1	1	÷8	±300

BADC: Bus ADC Resolution/Averaging

Bits [10:7] of the configuration register sets the ADC resolution/averaging when the ADC is configured in the V_{BUS} mode. The ADC can be configured versus bit accuracy. The bit accuracy selections range from 12 to 15-bits. The ADC is configurable versus the number of averages. The selection ranges from 2 to 128 samples. Table 5 shows the breakdown of each BADC setting. The shaded row is the default setting upon power up.

SADC: Shunt ADC Resolution/Averaging

Bits [10:7] of the configuration register sets the ADC resolution/Averaging when the ADC is configured in the V_{SHUNT} mode. The ADC can be configured versus bit accuracy. The bit accuracy selections range from 12 to 15-bits. The ADC is configurable versus number of averages. The selection ranges from 2 to 128 samples. Table 5 shows the break down of each SADC setting. The shaded row is the default setting upon power-up.

MODE: Operating Mode

Bits [2:0] of the configuration register controls the state machine within the chip. The state machine globally controls the overall functionality of the chip. Table 6 shows the various states the chip can be configured to, as well as the mode bit definitions to achieve a desired state. The shaded row is the default setting upon power-up.

TABLE 5. ADC SETTINGS, APPLIES TO BOTH SADC AND BADC CONTROL

ADC3	ADC2	ADC1	ADC0	MODE/SAMPLES	CONVERSION TIME
0	X	0	0	12-Bit	72µs
0	X	0	1	13-Bit	132µs
0	X	1	0	14-Bit	258µs
0	X	1	1	15-Bit	508µs
1	0	0	0	15-Bit	508µs
1	0	0	1	2	1.01ms
1	0	1	0	4	2.01ms
1	0	1	1	8	4.01ms
1	1	0	0	16	8.01ms
1	1	0	1	32	16.01ms
1	1	1	0	64	32.01ms
1	1	1	1	128	64.01ms

TABLE 6. OPERATING MODE SETTINGS

MODE2	MODE1	MODE0	MODE
0	0	0	Power-Down
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	ADC Off (disabled)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

SHUNT VOLTAGE REGISTER 01H (READ-ONLY)

The Shunt Voltage Register reports the measured value across the shunt pins (Vinp and Vinm) into the register. The shunt register LSB is independent of PGA range settings. The PGA setting for the shunt register masks the unused most significant bit with a sign bit. For lower range of PGA settings, multiple sign bits are returned by the DPM. Only one sign bit should be used to calculate the measured value.

Tables 7 through 10 show the weights of each bit for various PGA ranges. The tables should be used to calculate the measured value across the shunt pins from the binary to decimal domains.

To calculate the measured decimal value across the shunt, first read the shunt voltage register. Assume the PGA setting is set to the 80mV range. For this example, the reading output by the chip is 1111 1010 0000 0101. The 80mV range has three sign bits. Only one sign bit needs to be used to calculate the measured decimal value. Bits 14 and 15 are omitted from the calculation. This leaves a binary reading of 11 1010 0000 0101.

Next, multiply each bit by its respective weight. Bit0 value would be multiplied by bit0 weight (1), Bit1 value * Bit1 weight (2), etc....

Add all the multiplied values to equate to a single number. For the binary reading 11 1010 0000 0101 this equates to -1531.

The LSB for a shunt register is 10µV. Multiplying the decimal value by the LSB weight yields the measured voltage across the shunt. A 1111 1010 0000 0101 reading equals -15.31mV measured across the shunt pins.

TABLE 7. SHUNT VOLTAGE REGISTER, PG GAIN = /8 (RANGE = 11), FULL SCALE = ±300MV, 15 BITS WIDE

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT	-32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 8. SHUNT VOLTAGE REGISTER, PG GAIN = /4 (RANGE = 10), FULL SCALE = ±160MV, 14 BITS WIDE

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT		-16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 9. SHUNT VOLTAGE REGISTER, PG GAIN = /2 (RANGE = 01), FULL SCALE = ±80MV, 13 BITS WIDE

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Sign	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT			-8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 10. SHUNT VOLTAGE REGISTER, PG GAIN = /1 (RANGE = 00), FULL SCALE = ± 40MV, 12 BITS WIDE

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	Sign	Sign	Sign	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT				-4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 11. BUS VOLTAGE REGISTER, BRNG = 10 OR 11, FULL SCALE = 60V, 14 BITS WIDE

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CNVR	OVF
WEIGHT	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1		

TABLE 12. BUS VOLTAGE REGISTER, BRNG = 01, FULL SCALE = 32V, 13 BITS WIDE

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		CNVR	OVF
WEIGHT	4096	2048	1024	512	256	128	64	32	16	8	4	2	1			

TABLE 13. BUS VOLTAGE REGISTER, BRNG = 00, FULL SCALE = 16V, 12 BITS WIDE

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME		Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		CNVR	OVF
WEIGHT		2048	1024	512	256	128	64	32	16	8	4	2	1			

TABLE 14. CALIBRATION REGISTER, 05h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

BUS VOLTAGE REGISTER 02H (READ-ONLY)

The Bus Voltage Register is where the DPM reports the measured value of the V_{bus}. There are three scale ranges possible depending on the BRNG setting controlled from the configuration register(00H).

Tables 11 through 13 are the weight bits for each BRNG setting. The binary value recorded in the Bus Voltage Register is translated to a decimal value in the same way as the shunt voltage register is converted to a decimal value.

$$V_{bus} = \left[\sum_{n=0}^{15}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot Vbus_{LSB} \quad \text{(EQ. 1)}$$

Equation 1 is the mathematical equation for converting the binary V_{bus} value to a decimal value. N is the bit number. The LSB value for the V_{bus} measurement equals 4mV across all bus range (BRNG) settings.

CNVR: Conversion Ready (Bit 1)

The Conversion Ready Bit indicates when the ADC has finished a conversion and transferred the reading(s) to the appropriate register(s). The CNVR is only operable when the DPM is set to one of three trigger modes. The CNVR is at a high state when the conversion is in progress. The CNVR transitions and remains at a low state when the conversion is complete.

The CNVR bit is initialized or re-initialized in the following ways;

1. Writing to the configuration register.
2. Reading from Power Register

OVF: Math Overflow Flag (Bit 0)

The Math Overflow Flag (OVF) is a bit that is set to indicate the current or power data being read from the DPM is over ranged and meaningless.

CALIBRATION REGISTER 05H (READ/WRITE)

To accurately read the current and power measurements from the chip, the calibration register needs to be programmed.

The calibration register value is calculated as follows:

1. Calculate the full scale current range that is desired. This is calculated using Equation 2. R_{shunt} is the value of the shunt resistor. Vshunt is the full scale setting that is desired. In most cases, it is the PGA full scale range (300mV, 160mV, 80mV and 40mV) that the DPM is programmed to.

$$Current_{FS} = \frac{Vshunt_{FS}}{R_{shunt}} \quad \text{(EQ. 2)}$$

2. From the current full scale range, the current LSB is calculated using Equation 3. Current full scale is the outcome from Equation 2. ADC_{res} is the resolution of shunt voltage reading. The value is determined by the SADC setting in configuration register. SADC setting equal to 3 and greater will have a 15-bit resolution. The ADC_{res} value equals 2^{15} or 32768.

$$Current_{LSB} = \frac{Current_{FS}}{ADC_{res}} \quad \text{(EQ. 3)}$$

3. From Equation 3, the calibration resister value is calculated using Equation 4. The resolution of the math that is processed internally in the DPM is 4096 or 12 bits of resolution. The Vshunt LSB is set to 10µV. Equation 4 yields a 16-bit binary number that can be written to the calibration register. The calibration register format is represented in Table 14.

$$CalReg_{val} = integer\left[\frac{Math_{res} \cdot Vshunt_{LSB}}{\left(Current_{LSB} \cdot R_{shunt}\right)}\right]$$

$$CalReg_{val} = integer\left[\frac{0.04096}{\left(Current_{LSB} \cdot R_{shunt}\right)}\right] \quad \text{(EQ. 4)}$$

CURRENT REGISTER 04H (READ-ONLY)

Once the calibration register (05H) is programmed, the output current is calculated using Equation 5.

$$Current = \left[\sum_{n=0}^{15}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot Current_{LSB} \quad \text{(EQ. 5)}$$

Bit is the returned value of each bit from the current register either 1 or a 0. The weight of each bit is represented in Table 15. N is the bit number. The current LSB is the value calculated from Equation 3.

POWER REGISTER 03H (READ-ONLY)

The Power register only has meaning if the calibration register (05H) is programmed. The units for the power register are in watts. The power is calculated using Equation 6.

$$Power = \left[\sum_{n=0}^{15}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot Power_{LSB} \cdot 5000 \quad \text{(EQ. 6)}$$

Bit is the returned value of each bit from the power register either 1 or a 0. The weight of each bit is represented in Table 16. N is the bit number. The power LSB is calculated from Equation 7.

$$Power_{LSB} = Current_{LSB} \cdot Vbus_{LSB} \quad \text{(EQ. 7)}$$

If V_{bus} range, BRNG, is set to 60V, the power equation in Equation 6 is multiplied by 2.

TABLE 15. CURRENT REGISTER, 04h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Bit 15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WEIGHT	-32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

TABLE 16. POWER REGISTER, 03h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
WEIGHT	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

THRESHOLD REGISTERS

The shunt voltage or V_{bus} threshold registers are used to set the Min/Max threshold limits that will be tested versus V_{SHUNT} or V_{bus} readings. Measurement readings exceeding the respective Vshunt or V_{bus} limits, either above or below, will set a register flag and perhaps an external interrupt depending on the configuration of the interrupt enable bit (INTREN) in register 09H. The testing of the ADC reading versus the respective threshold limits occurs once per ADC conversion.

TABLE 17. SHUNT VOLTAGE THRESHOLD REGISTER, 06h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	Sign	SMX6	SMX5	SMX4	SMX3	SMX2	SMX1	SMX0	Sign	SMN6	SMN5	SMN4	SMN3	SMN2	SMN1	SMN0
WEIGHT	-128	64	32	16	8	4	2	1	-128	64	32	16	8	4	2	1

SHUNT VOLTAGE THRESHOLD REGISTER 06H (READ/WRITE)

The V_{SHUNT} minimum and maximum threshold limits are set using one register. The shunt value readings are either positive or negative. D15 and D7 bits of Table 17 are given to represent the sign of the limit. SMX bits represent the upper limit threshold. SMN represents the lower threshold limit. Equation 8 is the calculation used to convert the V_{SHUNT} threshold binary value to decimal. Bit is the value of each bit set in the shunt threshold register. The value is either 1 or a 0. The weight of each bit is represented in Table 17. N is the bit number. The shunt voltage threshold LSB is 2.56mV.

$$Vs_{thresh} = \left[\sum_{n=0}^{7}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot VsThresh_{LSB} \quad \text{(EQ. 8)}$$

TABLE 18. BUS VOLTAGE THRESHOLD REGISTER, 07h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	BMX7	BMX6	BMX5	BMX4	BMX3	BMX2	BMX1	BMX0	BMN7	BMN6	BMN5	BMN4	BMN3	BMN2	BMN1	BMN0
WEIGHT	128	64	32	16	8	4	2	1	128	64	32	16	8	4	2	1

BUS VOLTAGE THRESHOLD REGISTER 07H (READ/WRITE)

The V_{bus} minimum and maximum threshold limits are set using one register. The V_{bus} value readings range from 0 to 60V. Table 18 shows the register configuration and bit weights for the V_{bus} threshold register. BMX bits represent the upper limit threshold. BMN represents the lower threshold limit. Equation 9 is the calculation used to convert the V_{bus} threshold binary value to decimal. Bit is the value of each bit set in the V_{bus} threshold register. The value is either 1 or a 0. The weight of each bit is represented in table 18. N is the bit number. The V_{bus} voltage threshold LSB is 256mV.

$$Vb_{thresh} = \left[\sum_{n=0}^{7}\left(Bit_n \cdot Bit\_Weight_n\right)\right] \cdot VbThresh_{LSB} \quad \text{(EQ. 9)}$$

INTERRUPT STATUS REGISTER 08H (READ/WRITE)

The interrupt status register consists of a series of bit flags that indicate if an ADC reading has exceeded the readings respective limit. A 1 or high reading from a warning bit indicates the reading has exceeded the limit. To clear a warning, write a 1 or high to the set warning bit. Table 19 shows the definition of the interrupt status register.

TABLE 19. INTERRUPT STATUS REGISTER, 08h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	SMXW	SMNW	BMXW	BMNW
WEIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BMNW is bus voltage minimum warning. A 1 reading for this bit indicates the bus reading is below the bus voltage minimum threshold limit.

BMXW is bus voltage maximum warning. A 1 reading for this bit indicates the bus reading is above the bus voltage maximum threshold limit.

SMNW is shunt voltage minimum warning. A 1 reading for this bit indicates the shunt reading is below the shunt voltage minimum threshold limit.

SMXW is shunt voltage maximum warning. A 1 reading for this bit indicates the shunt reading is above the shunt voltage maximum threshold limit.

AUX CONTROL REGISTER 09H (READ/WRITE)

The aux control register controls the functionality of the EXTCLK/INT pin of the ISL28022. Table 20 shows the definition of the register.

TABLE 20. AUX CONTROL REGISTER, 09h

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NAME	NA	NA	NA	NA	NA	NA	NA	FORCEINTR	INTREN	ExtClkEn	ExtCLKDiv[5:0]					
WEIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FORCEINTR is the force interrupt bit. Programming a 1 to the bit will force a 0 or a low at the EXTCLK/INT pin.

INTREN is the interrupt enable bit. Programming a 1 to the bit will allow for a threshold measurement violation to set the state of the EXTCLK/INT pin. With the INTREN set, any flag set from the interrupt status register will change the state of the EXTCLK/INT pin from 1 to a 0.

EXCLKEN is the external clock enable bit. Setting the bit enables the external clock. This also changes the EXTCLK/INT pin from an output to an input. The internal oscillator will shut down when the bit is enabled.

EXTCLKDIV are the external clock divider bits. The bits control an internal clock divider that are useful for fast system clocks. The internal clock frequency from pin to chip is represented in Equation 10.

$$freq_{internal} = \frac{f_{EXTCLK}}{(EXTCLKDIV + 1)\cdot 2} \quad \text{(EQ. 10)}$$

f_{EXTCLK} is the frequency of the signal driven to the EXTCLK/INT pin. EXTCLKDIV is the decimal value of the clock divide bits.

I²C Serial Interface

The ISL28022 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL28022 operates as a slave device in all applications.

The ISL28022 uses two bytes to transfer all reads and writes. All communication over the I²C interface is conducted by sending the MSByte of each byte of data first, followed by the LSByte.

Protocol Conventions

For normal operation, data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 25). On power-up of the ISL28022, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL28022 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 25). A START condition is ignored during the power-up sequence.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 25). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

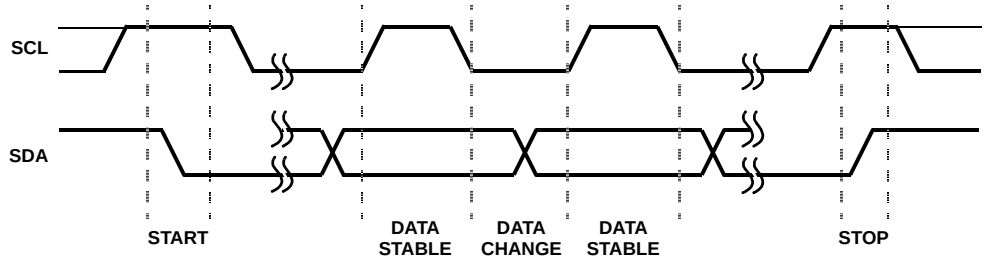


FIGURE 25. VALID DATA CHANGES, START AND STOP CONDITIONS

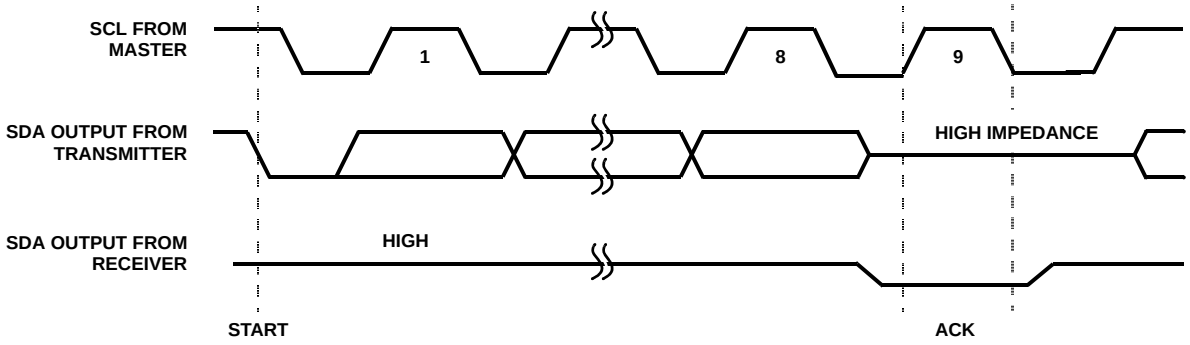


FIGURE 26. ACKNOWLEDGE RESPONSE FROM RECEIVER

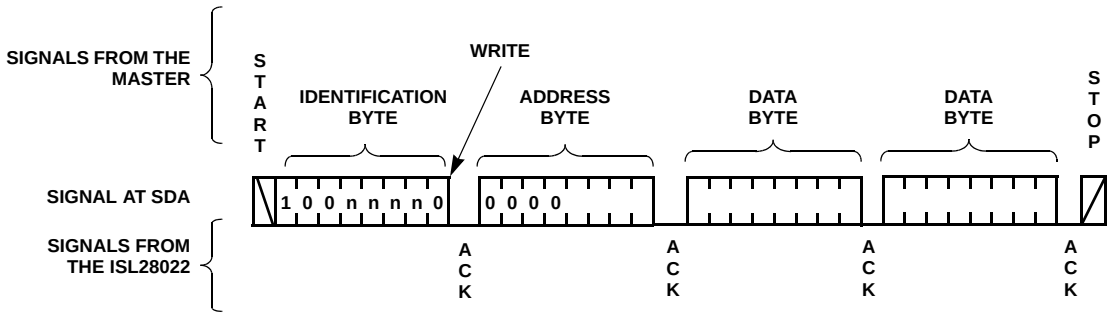


FIGURE 27. BYTE WRITE SEQUENCE (SLAVE ADDRESS INDICATED BY nnnn)

SMBus Support

The ISL28022 supports SMBus protocol, which is a subset of the global I^2C protocol. SMBCLK and SMBDAT have the same pin functionality as the SCL and SDA pins, respectively. The SMBus operates at 100kHz.

Device Addressing

Following a start condition, the master must output a slave address byte. The 7 MSB's are the device identifiers. The A0 and A1 pins control the bus address. These bits are shown in Table 21, there are 16 possible combinations depending on the A0/A1 connections.

TABLE 21. I^2C SLAVE ADDRESSES

A1	A0	SLAVE ADDRESS
GND	GND	1000 000
GND	VCC	1000 001
GND	SDA	1000 010
GND	SCL	1000 011
VCC	GND	1000 100
VCC	VCC	1000 101
VCC	SDA	1000 110
VCC	SCL	1000 111
SDA	GND	1001 000
SDA	VCC	1001 001
SDA	SDA	1001 010
SDA	SCL	1001 011
SCL	GND	1001 100
SCL	VCC	1001 101
SCL	SDA	1001 110
SCL	SCL	1001 111
Broadcast Address		0111 111

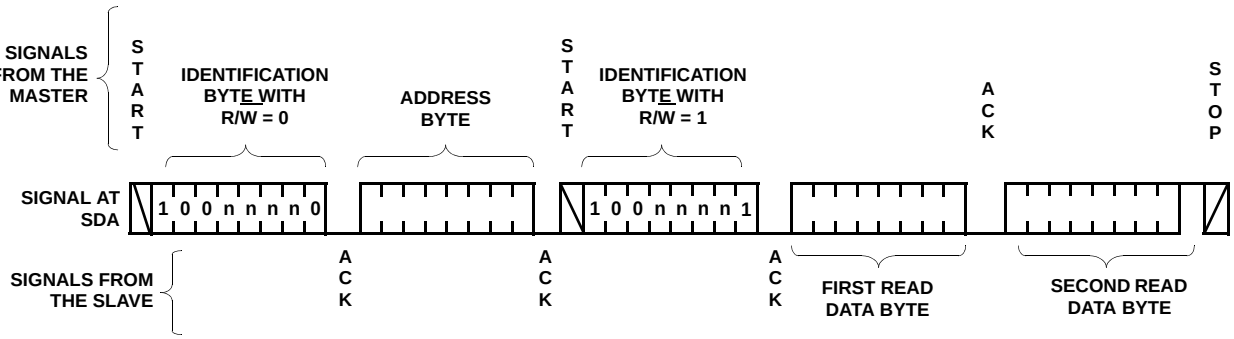


FIGURE 28. READ SEQUENCE (SLAVE ADDRESS SHOWN AS nnnn)

The last bit of the slave address byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a "1", a read operation is selected. A "0" selects a write operation (refer to Figure 27).

After loading the entire slave address byte from the SDA bus, the ISL28022 compares the loaded value to the internal slave address. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the slave byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up, the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the one word address byte, as shown in Figure 28.

In a random read operation, the slave byte in the "dummy write" portion must match the slave byte in the "read" section. For a random read of the registers, the slave byte must be "100nnnnx" in both places.

Write Operation

A write operation requires a START condition, followed by a valid identification byte, a valid address byte, two data bytes, and a STOP condition. The first data byte contains the LSB of the data, the second contains the MSB. After each of the four bytes, the ISL28022 responds with an ACK. At this time, the I^2C interface enters a standby state.

Read Operation

A read operation consists of a three byte instruction, followed by two data bytes (see Figure 28). The master initiates the operation issuing the following sequence: A START, the identification byte with the R/$\overline{W}$ bit set to "0", an address byte, a second START, and a second identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the ISL28022 responds with an ACK. Then the ISL28022 transmits two data bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of the first byte. The master terminates the read operation (issuing no ACK then a STOP condition) following the last bit of the second data byte (see Figure 28).

The data bytes are from the memory location indicated by an internal pointer. This pointer's initial value is determined by the address byte in the read operation instruction, and increments by one during transmission of each pair of data bytes. The highest valid memory location is 09h, reads of addresses higher than that will not return useful data.

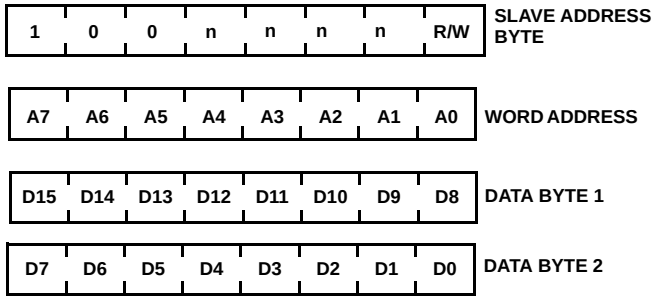


FIGURE 29. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES

Broadcast Addressing

The DPM has a feature that allows the user to configure the settings of all DPM chips at once. For example, a system has 16 DPM chips connected to an I^2C bus. A user can set the range or initiate a data acquisition in one I^2C data transaction by using a slave address of 0111 111. The broadcast feature saves time in configuring the DPM as well as measuring signal parameters in time synchronization. The broadcast should not be used for DPM read backs. This will cause all devices connected to the I^2C bus to talk to the master simultaneously.

I^2C Clock Speed

The ISL28022 supports high-speed digital transactions up to 3.4Mbs. To access the high speed I^2C feature, a master byte code of 0000 1nnn is attached to the beginning of a standard frequency read/ write I^2C protocol. The n in the master byte code can either equal a 0 or a 1. The master byte code should be clocked into the chip at frequencies equal or less than 400kHz. The master code command configures the internal filters of the ISL28022 to permit data bit frequencies greater than 400kHz. Once the master code has been clocked into the device, the protocol for a standard read/ write transaction is followed. The frequency at which the standard protocol is clocked in at can be as great as 3.4MHz. A stop bit at the end of a standard protocol will terminate the high speed transaction mode. Appending another standard protocol serial transaction to the data string without a stop bit, will resume the high speed digital transaction mode. Figure 30 illustrates the data sequence for the high speed mode.

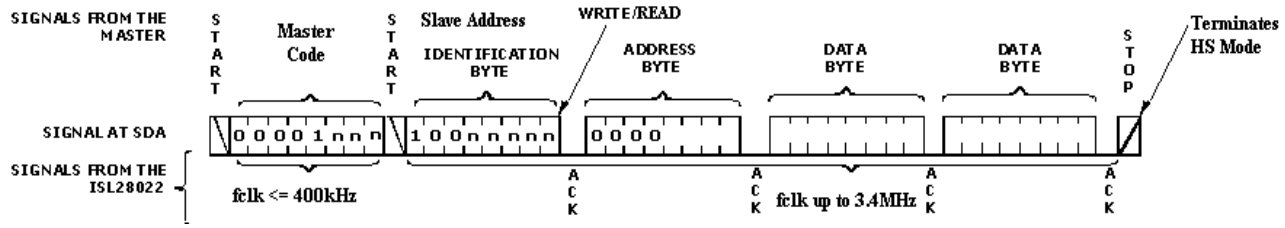


FIGURE 30. BYTE TRANSACTION SEQUENCE FOR INITIATING DATA RATES ABOVE 400Kbs

Signal Integrity

The purity of the signal being measured by the ISL28022 is not always ideal. Environmental noise or noise generated from a regulator can degrade the measurement accuracy. The ISL28022 maintains a high CMRR ratio from DC to approximately 10kHz, as shown in Figure 31.

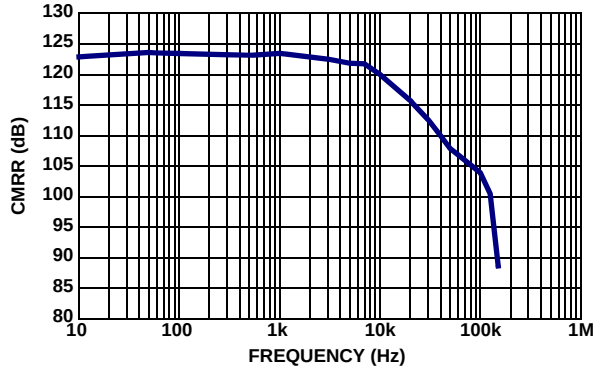


FIGURE 31. CMRR vs FREQUENCY

The CMRR vs Frequency graph best represents the response of the ISL28022 when an aberrant signal is applied to the circuit. The normal state of the measured signal is DC and is the state at which the ISL28022 internal calibration is performed.

The graph was generated by shorting the ISL28022 input without any filtering and applying a 0 to 10V triangle wave to the shunt inputs, Vinp and Vinm. The voltage shunt measurement was recorded for each frequency applied to shunt input.

The CMRR of can be improved by designing an filter stage for the of the ISL28022. The purpose of the filter stage is to attenuate the amplitude of the unwanted signal to the noise level of the ISL28022. Figure 32 is a simple filter example to attenuate unwanted signals.

The filter circuit in Figure 32 attenuates unwanted signals. CSH and RSH is single pole RC filter that differentially attenuates unwanted signals to the ISL28022. Most power monitoring applications require a shunt resistor to be low in value to measure large currents. For small shunt resistors, a large value capacitor is required to attenuate low frequency signals. Most large value capacitors are not offered in space saving packages. The corner frequency of the differential filter, CSH and RSH, should be designed for higher value frequency filtering.

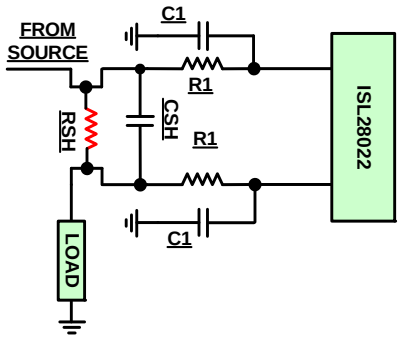


FIGURE 32. SIMPLIFIED FILTER DESIGN TO IMPROVE NOISE PERFORMANCE TO THE ISL28022

R1 and C1 for both inputs are the single ended filter to the ISL28022. The value of the series resistor to the ISL28022 can be a larger value than the shunt resistor, RSH. A larger series resistor to the input allows for a lower cutoff frequency filter design to the ISL28022. The ISL28022 can source up to 20µA of transient current in the measurement mode. The transient or switching offset current can be a large as 10µA. The switching offset current combined with the series resistance, R1, creates an error offset voltage. A balance of the value of R1 and the shunt measurement error should be achieved for this filter design.

The common mode voltage of the shunt input stage ranges from 0V to 60V. The capacitor voltage rating for C1 and CSH should comply with the nominal voltage being applied to the input.

Measurement Stability vs Acquisition Time

The BADC and SADC bits within the Configuration register configures the conversion time and accuracy for the bus and shunt inputs respectively. The faster the conversion time the less accuracy and more noise introduced into the measurement. Figure 33 is a graph that illustrates the shunt measurement variability versus a set SADC mode. The standard deviation of 2048 shunt Vos measurements is used to quantify the measurement variability of each mode.

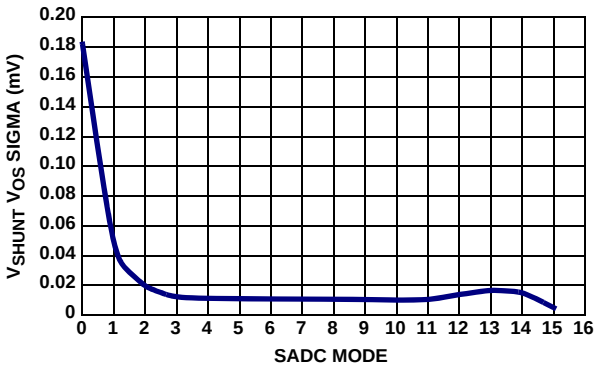


FIGURE 33. MEASUREMENT STABILITY vs SADC MODE

Fast Transients

An small isolation resistor placed between ISL28022 inputs and the source is recommended. In hot swap or other fast transient events, the amplitude of a signal can exceed the recommended operating voltage of the part due to the line inductance. The isolation resistor creates a low pass filter between the device and the source. The value of the isolation resistor should not be too large. A large value isolation resistor can effect the measurement accuracy. The offset current for shunt input can be as large as 10µA. The value of the isolation resistor combined with the offset current creates an error offset voltage at the shunt input. The input of the Bus channel is connected to the top of a precision resistor divider. The accuracy of the resistor divider determines the gain error of the Bus channel. The input resistance of the Bus channel is 600kΩ. Placing an isolation resistor of the 10Ω will change the gain error of the Bus channel by 0.0016%.

External Clock

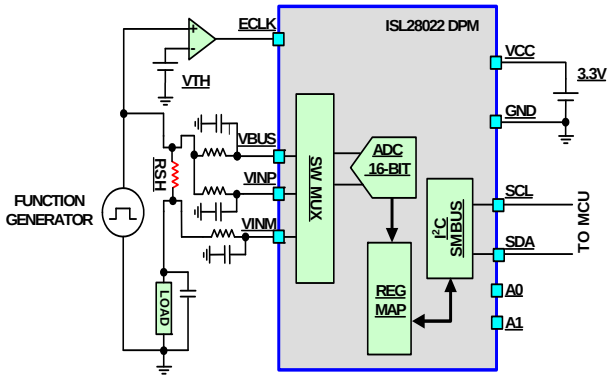


FIGURE 34. SIMPLIFIED SCHEMATIC OF THE ISL28022 SYNCHRONIZED TO A PWM SOURCE

An externally controlled clock allows measurements to be synchronized to an event that is time dependent. The event could be application generated, such as timing a current measurement to a charging capacitor in a switch regulator application or the event could be environmental. A voltage or current measurement may be suspectable to crosstalk from a controlled source. Instead of filtering the environmental noise from the measurement, another approach would be to synchronize the measurement to the source. The variability and accuracy of the measurement will improve.

The ISL28022 has the functionality to allow for synchronization to an external clock. The speed of the external clock combined with the choice of the internal chip frequency division value determines the acquisition times of the ADC. The internal system clock frequency is 500kHz. The internal system clock is also the ADC sampling clock. The acquisition times scale linearly from 500kHz. For example, an external clock frequency of 1.0MHz with a frequency divide setting of 2 results in acquisition times that equals the internal oscillator frequency when enabled. The internal clock frequency of the ISL28022 should not exceed 500kHz. The ADC modulator is optimized for frequencies of 500kHz and below. Operating internal clock frequencies above 500kHz result in measurement accuracy errors due to the modulator not having enough time to settle.

Suppose an external clock frequency of 1.0MHz is applied with a divide by 8 internal frequency setting, the system clock speed is 125kHz or 4x slower than internal system clock. The acquisition times for this example will increase by 4. For a S(B)ADC setting of 3, the ISL28022 will have an acquisition time of 2.032ms instead of 508µs.

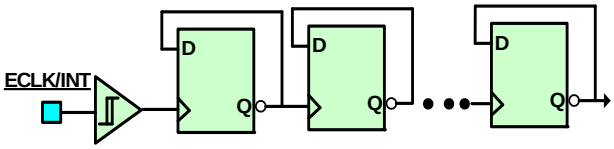


FIGURE 35. SIMPLIFIED INTERNAL BLOCK CONNECTION OF THE ECLK/INT PIN

The ECLK/INT pin connects to a buffer that drives a D-flip flop. Figure 35 illustrates a simple schematic of the ECLK/INT pin internal connection. The series of divide by 2 configured D-flip flops are control by the CLKDIV bits from the Aux Control Register. The buffer is a Schmitt triggered buffer. The bandwidth of the buffer is 4MHz. Figure 36 shows the bandwidth of the ECLK/INT pin.

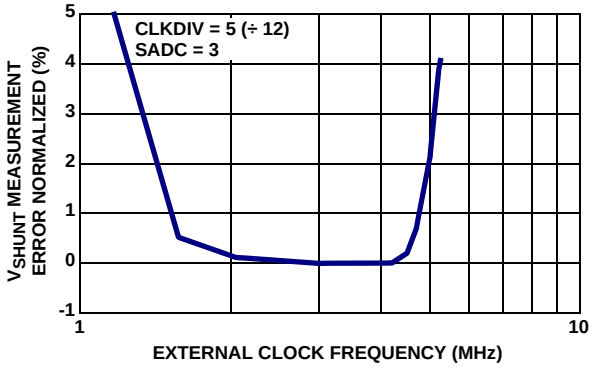


FIGURE 36. EXTERNAL CLOCK BANDWIDTH vs MEASUREMENT ACCURANCY

The V_{SHUNT} measurement error degrades at ECLK frequencies above 4MHz. It is recommended that the ECLK does not exceed 4MHz. At ECLK frequencies below 2.5MHz or internal clock frequencies of 208kHz, the clock frequency to modulator is too slow allowing the charged capacitors to discharge due to parasitic leakages. The capacitor discharge results in a measurement error.

Over-ranging

It is not recommended to operate the ISL28022 outside the set voltage range. In the event of measuring a shunt voltage beyond the maximum set range (300mV) and lower than the clamp voltage of the protection diode (1V), the measured output reading may be within the accepted range but will be incorrect.

Typical Applications

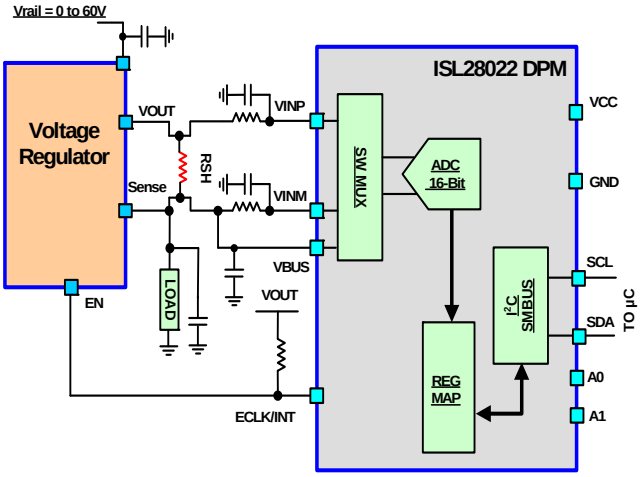


FIGURE 37. POINT OF LOAD MONITORING DESIGN IDEA

Point Of Load Power Monitor

Complex systems are subdivided into smaller simplified specific tasks. The circuit illustrated in Figure 37 is a solution that can be used to monitor a load's performance. The Vreg is a voltage regulator that regulates to a point of load (POL) voltage. 5V, 3.3V, 2.5V and 1.8V are examples of POL voltages.

The main bus voltage applied to the voltage regulator regulates the voltage to the load at the VINM, VBUS and Sense node for the configuration shown above. The placement of the shunt resistor in the circuit allows current to be monitored while regulating the voltage to the load. The maximum shunt voltage the ISL28022 is able to measure is ± 300mV. The shunt resistor value is determined by the Equation 11.

$$R_{shunt} = RSH = \frac{0.30}{Current_{FS}} \quad \text{(EQ. 11)}$$

$Current_{FS}$ is the maximum current to be measured through the load. This is chosen by the user.

The ISL28022 has over/undervoltage (OV/UV) sensing circuitry for the Bus and Shunt inputs. The levels of the error detection circuitry are controlled digitally via a I^2C/SMBus communication protocol. The status of each inputs' error detection can be read digitally via a register. The ISL28022 allows for the summation of error detection bits to be routed to an interrupt pin. For the Point Of Load Monitoring circuit shown in Figure 37, the interrupt pin is connected to the enable pin of the regulator. In a fault condition, the ISL28022 will trigger an interrupt causing the voltage regulator to shutdown. In the case of when a fault always exist, the ISL28022 interrupt pin output state can be digitally programmed.

The ISL28022 calculates the power and current through hardware and stores the results in an internal register. The V_{bus} connected directly to the load enables a measurement system that monitors power to the load.

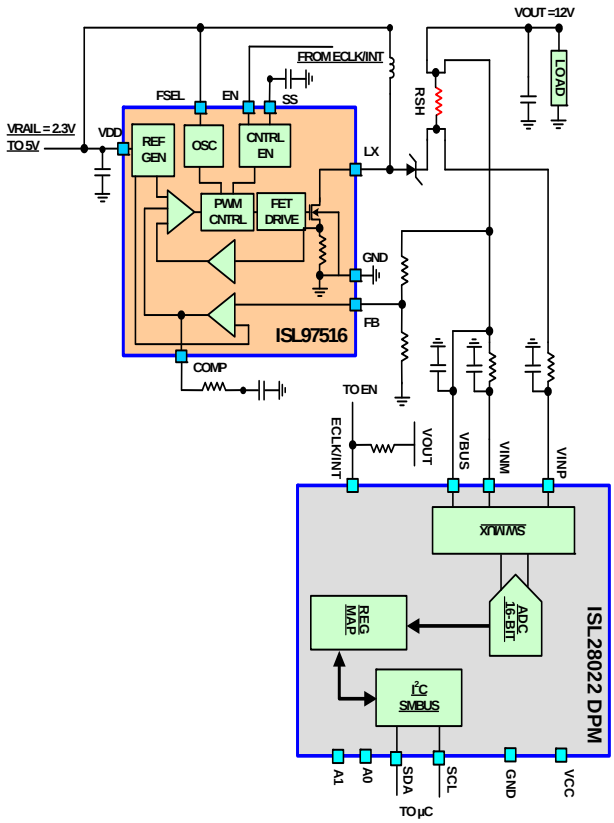


FIGURE 38. POWER MONITOR BOOST REGULATOR DESIGN IDEA

Power Monitor Boost Regulation

The Power Monitor Boost Regular application is an example of the ISL28022 used as a digital helper, Figure 38. With minimal circuitry, the ISL28022 enables smart designs that digitally monitor the electrical parameters to a load. Alternative designs require a current amplifier paired with an ADC. The ADC chosen is often not compliant to common communication standards, such as I^2C. The ISL28022 solves this problem and allows for 16 devices on a single I^2C bus.

The ISL97516 chip is a high efficiency step-up voltage regulator. The max current the regulator can deliver is 2.0A. For this particular application, the ISL97516 is configured to step up the voltage at the VDD pin to 12V. The voltage at VDD can range from 2.3V to 5V for normal 12V regulated operation. A USB power pin could be used to drive the ISL97516.

The regulation node of the circuit, shown in Figure 38 is at V_{OUT}. The ISL97516 has feedback circuitry that removes the current sense resistor, RSH, from impacting the regulation voltage. The current sense resistor is calculated using Equation 11. Equation 11 shows the formula used to calculate R_{shunt}.

The ISL28022 interrupt pin is connected to the Enable pin of the regulator. The ISL28022 has OV/UV alerts for both the Bus and Shunt channels. A fault condition from either channel powers down the voltage regulator.

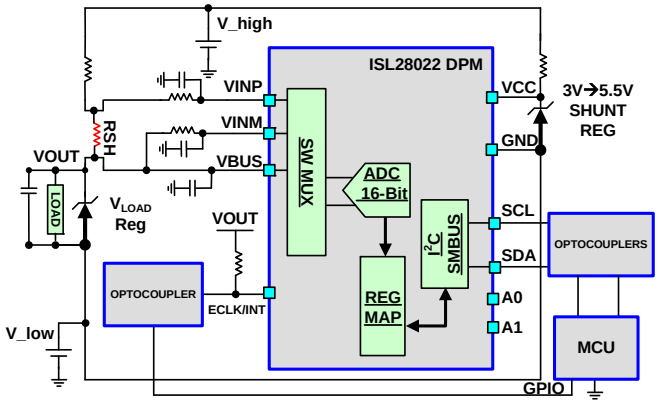


FIGURE 39. FLOATING SUPPLY DESIGN IDEA

Floating Supply DPM (> 60V or < 0V Operation)

The ISL28022 is operational when the potential of the measured circuitry is greater than the potential at the ground pin. In most application the ground pin potential equals 0V. A zero potential ground reference limits the operating range of the ISL28022 to 0V to 60V. This application illustrates the connectivity of the DPM to measure and operate at potentials greater than 60V or less than 0V.

Assume an application that measures a -48V supply. The ground reference voltage of the system, V_low, equals -48V. V_high equals 0V for the example. The power supply voltage to the system is -48V. The load supply voltage is set by the voltage regulator, Vload Reg. The regulator can be either a shunt or a linear regulator.

The voltage levels for I^2C communication lines are determined by V_low and the ISL28022 shunt regulator. A low voltage equals the V_low potential. A high level equals the summation of V_low and the Shunt Regulator voltage. For a -48V system with a 3.3V shunt regulator, a low voltage equals -48V and a high voltage level equals -44.7V. The voltage from the I^2C communication pins can not be directly connected to a ground referenced micro-controller. The optocouplers are used to translate the voltage level from the -48V referenced system to the ground referenced micro-controller system.

The ISL28022 measures voltage between two nodes. For the shunt input, the ISL28022 measures the voltage between VINP and VINM nodes. For the Bus input, the ISL28022 measures the difference between V_{bus} and GND nodes. The V_{bus} voltage for a floating system is calculate using Equation 12.

$$V_{bus} = V_{low} + \left(Vbus_{LSB} \cdot Vbus_{Reg}\right) \quad \text{(EQ. 12)}$$

V_{LOW} is the ground reference voltage of the system. In this instance, the value is -48V. $Vbus_{LSB}$ is the step size of the V_{bus} measurement. This equals 4mV. $Vbus_{Reg}$ is the integer value of the V_{bus} measurement reported by the ISL28022.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
April 26, 2013	FN8386.1	Added R-spec parts to ordering information and updated verbiage in About Intersil.
April 16, 2013	FN8386.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

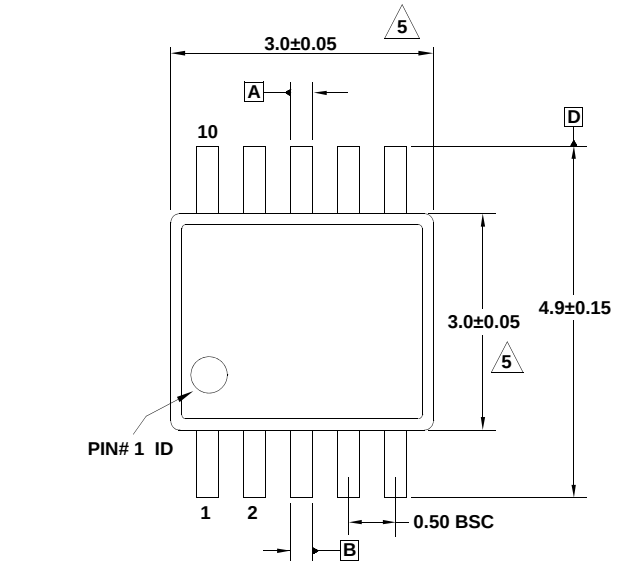
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

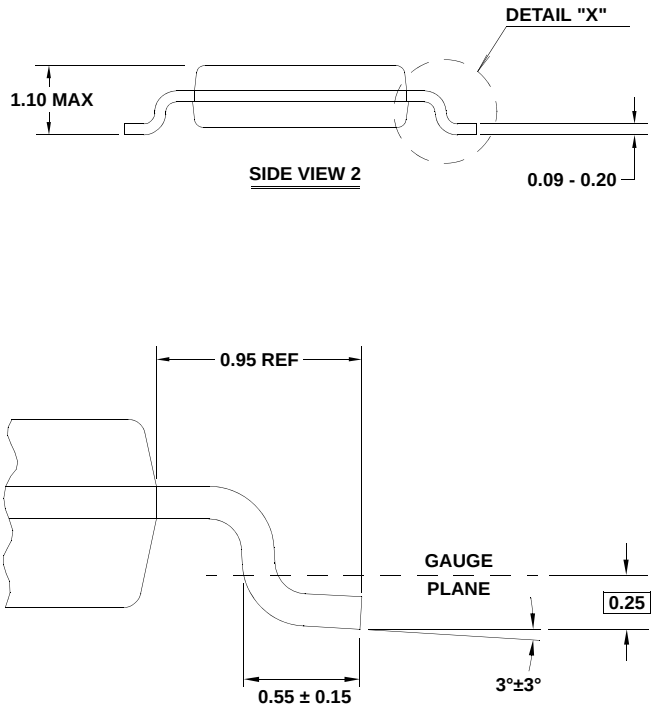
M10.118

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

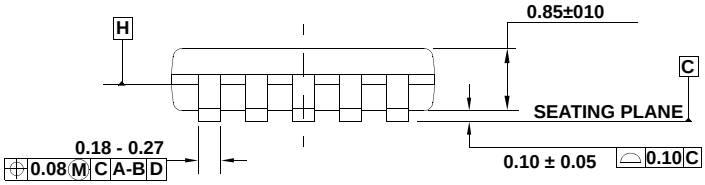
Rev 1, 4/12



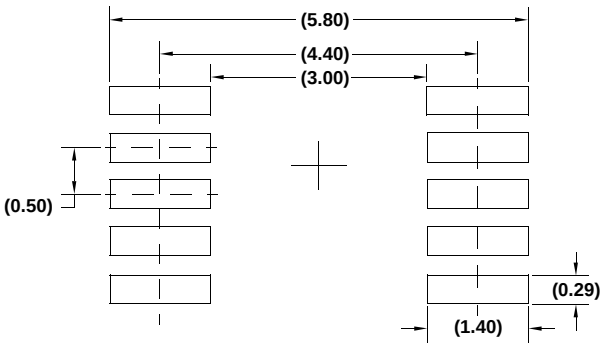
TOP VIEW



DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

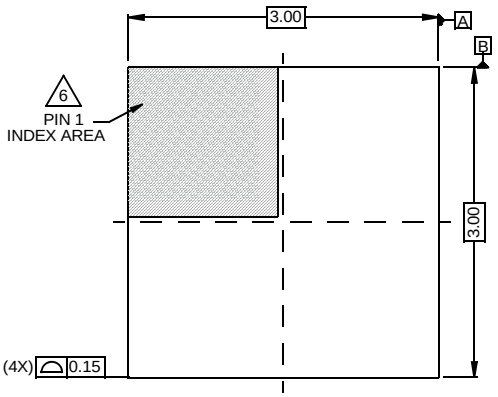
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

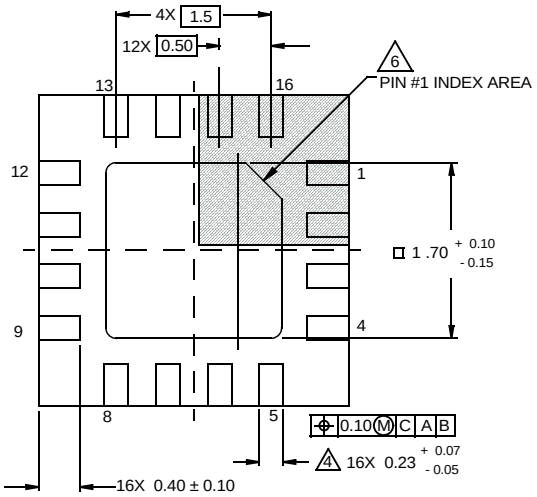
Package Outline Drawing

L16.3x3B

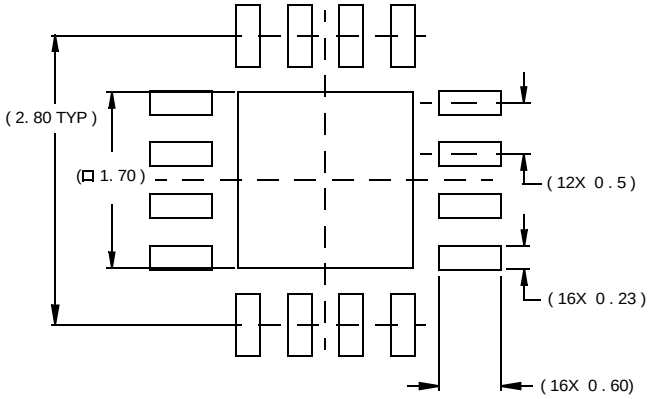
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 4/07



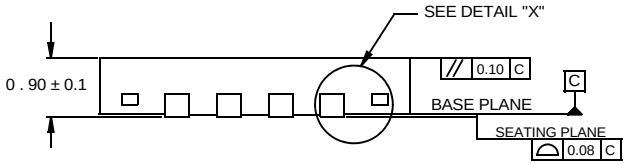
TOP VIEW



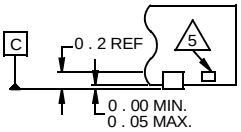
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Стандарт Электрон Связь

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