Features

- **Fastest Propagation Speeds in the Industry $T_{PD\ (F\ grade)}$ = 2.5 ns, $T_{PD\ (G\ grade)}$ = 2.0 ns**
- **Maximum derating for capacitive loads 1.5ns/100 pF (F grade) and 1.1ns/100 pF (G grade)**
- **Very low ground bounce < 0.6V @ V_{CC}=5.00V, T_a=25°C**
- **Excellent noise rejection**
- **Typical output skew ≤0.25ns**
- **Bus Hold circuitry to retain last active state during Tri-state™**
- **Available in SSOP and TSSOP packages**

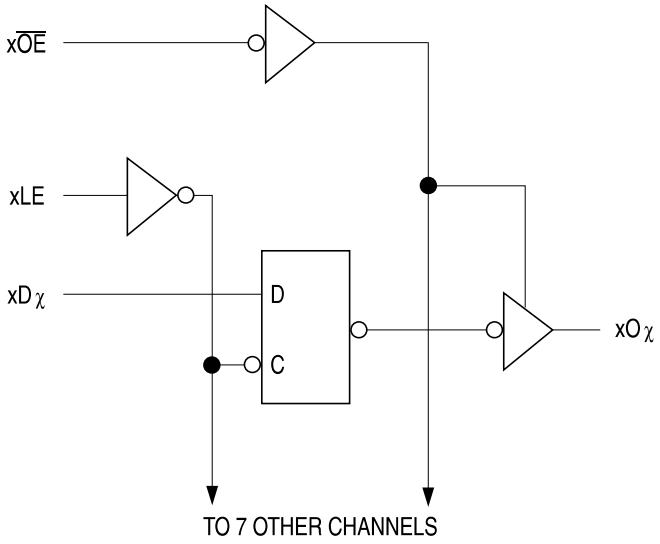
AT16373 Fast Logic™ 16-Bit Transparent Latch

AT16373F AT16373G

Description

Atmel's AT16373 devices provide maximum speed in temporary data storage. They can be operated as either two separate 8 bit latches or as a single 16-bit latch by use of the output enable and the latch enable. The AT16373 has very low ground bounce and excellent input noise rejection, giving the user stable signals in a high speed environment. These devices can drive very large loads while operating in a high speed transparent mode.

Functional Block Diagram (1)

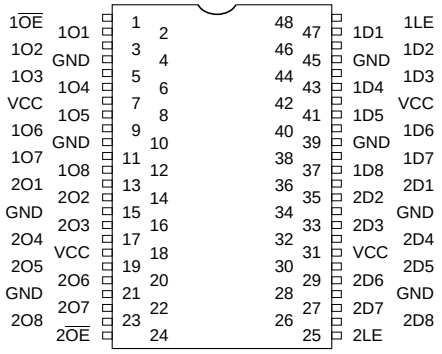


Note: 1. This 8-bit latch function is repeated a second time on each device.

Pin Configurations

Pin Names	Descriptions
$x\overline{OE}$	Output Enable Input (Active Low)
xLE	Latch Enable Inputs (Active High)
xDχ	Data Inputs
xOχ	Tri-State Outputs

SSOP/TSSOP



Top View

0756B

Function Table[1]

Inputs			Outputs
xDχ	xLE	$x\overline{OE}$	xOχ
H	H	L	H
L	H	L	L
X	X	H	Z

Note: 1. X = Don't Care, Z = High Impedance

Absolute Maximum Ratings*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground	-2.0V to +7.0V[1]
Maximum Operating Voltage	6.0V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

5.0 Volt DC Characteristics

Applicable over recommended operating range from T_a = 0°C to +70°C, V_{CC} = +5.0V +/- 5% (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max, V_{IN} = 3.4V		0.8	1.2	mA
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{CC}$			±15	µA
I_{IL}	Input Low Current	V_{IN} = GND			±15	µA
I_{OZ}	Output Leakage Current				±10	µA
$V_{OH}(1)$	Output High Voltage F Grade only	V_{CC} = 4.75V I_{OH} = -10 mA	2.7			V
$V_{OH}(2)$	Output High Voltage G Grade only	V_{CC} = 4.75V I_{OH} = -12 mA	2.7			V
V_{OL}	Output Low Voltage (F Grade)	I_{OL} = 10 mA			0.55	V
V_{OL}	Output Low Voltage (G Grade)	I_{OL} = 12 mA			0.55	V

Note: 1. F grade: At $V_{CC\ (max)}$, the value of $V_{OH(max)}$ = 3.75V and at $V_{CC(min)}$, $V_{OH(max)}$ = 3.25V
2. G grade: At $V_{CC\ (max)}$, the value of $V_{OH(max)}$ = 3.75V and at $V_{CC(min)}$, $V_{OH(max)}$ = 3.35V

AC Characteristics
AT16373F

Applicable over recommended operating range from T_a = 0°C to +70°C, V_{CC} = 5.0V +/- 5% (unless otherwise noted)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Units
t_{PHL} t_{PLH}	Propagation Delay xDχ to xOχ	C_L = 50 pF			2.5	ns
t_{PHL} t_{PLH}	Propagation Delay xLE to xOχ	C_L = 50 pF			5.5	ns
t_{PZH} t_{PZL}	Output Enable	C_L = 50 pF			8.8	ns
t_{PHZ} t_{PLZ}	Output Disable	C_L = 50 pF			6.5	ns
t_{SK}(2)	Output Skew	CL = 50 pF			0.5	ns
Δt_{PHL}(2) Δt_{PLH}	Propagation Delay vs Output Loading			1.3	1.5	ns/100 pF
t_{su}	Set-up Time	C_L = 50 pF	2.0			ns
t_H	Hold Time	C_L = 50 pF	2.0			ns

Note: 1. See test circuit and waveforms.
2. This parameter is guaranteed but not 100% tested.

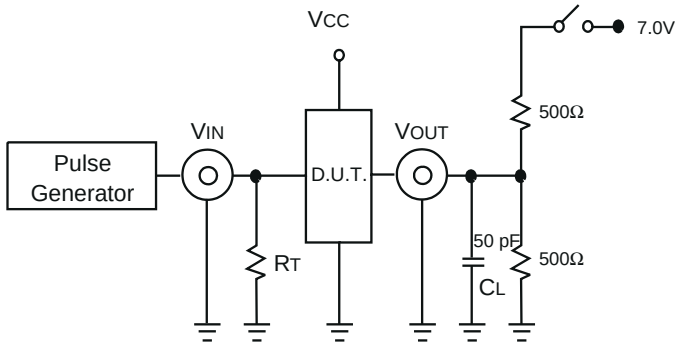
AT16373G

Applicable over recommended operating range from T_a = 0°C to +70°C, V_{CC} = 5.0V +/- 5% (unless otherwise noted)

Symbol	Parameter	Test Conditions[1]	Min	Typ	Max	Units
t_{PHL} t_{PLH}	Propagation Delay xDχ to xOχ	C_L = 50 pF			2.0	ns
t_{PHL} t_{PLH}	Propagation Delay xLE to xOχ	C_L = 50 pF			5.0	ns
t_{PZH} t_{PZL}	Output Enable	C_L = 50 pF			8.8	ns
t_{PHZ} t_{PLZ}	Output Disable	C_L = 50 pF			6.0	ns
t_{SK}(2)	Output Skew	C_L = 50 pF			0.5	ns
Δt_{PHL}(2) Δt_{PLH}	Propagation Delay vs Output Loading			0.9	1.1	ns/100 pF
t_{su}	Set-up Time	C_L = 50 pF	2.0			ns
t_H	Hold Time	C_L = 50 pF	2.0			ns

Note: 1. See test circuit and waveforms.
2. This parameter is guaranteed but not 100% tested.

Test Circuits[1,2]



Note: 1. Pulse Generator: Rate ≤ 1.0 MHz, t_F ≤ 2.5 ns, t_R ≤ 2.5 ns.
2. AC tests are done with a single bit switching, and timings need to be derated when multiple outputs are switching in the same direction simultaneously. This derating should not exceed 0.5 ns for 16 inputs switching simultaneously.

Switch Position

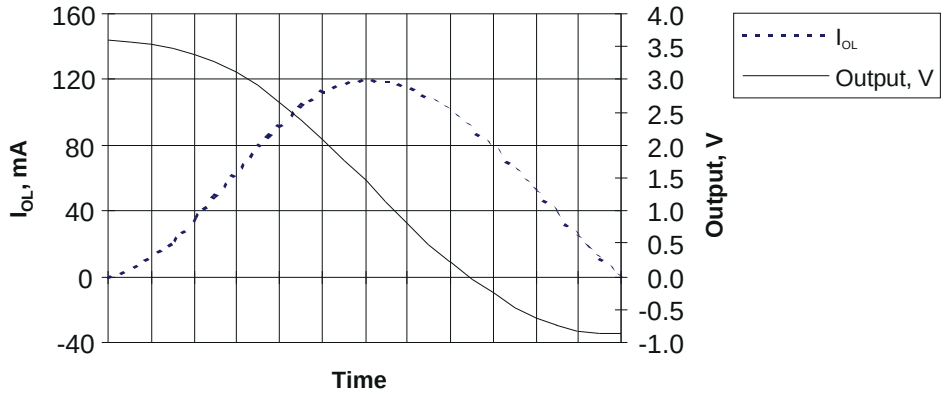
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

Definitions:

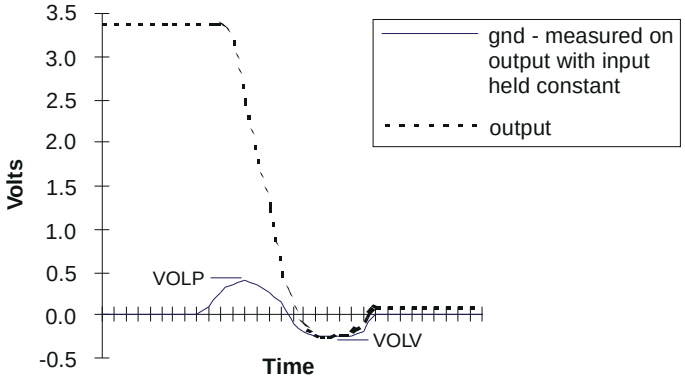
C_L = Load capacitance; Includes jig and probe capacitance.

R_T = Termination resistance; Should be equal to Z_{OUT} of the Pulse Generator.

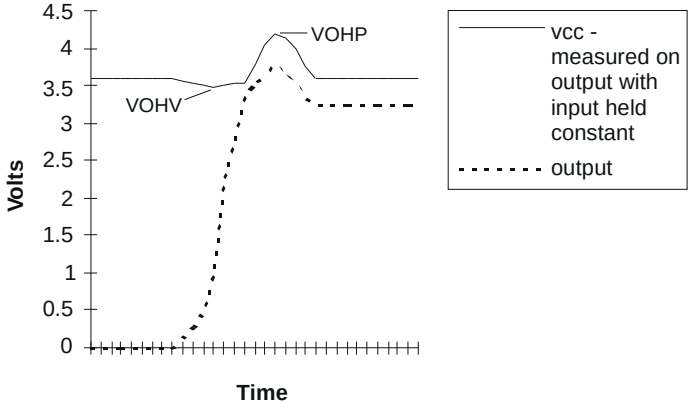
IOL Pull Down Current



Ground Bounce for High to Low Transitions[1]



Supply Bounce for Low to High Transitions[2]



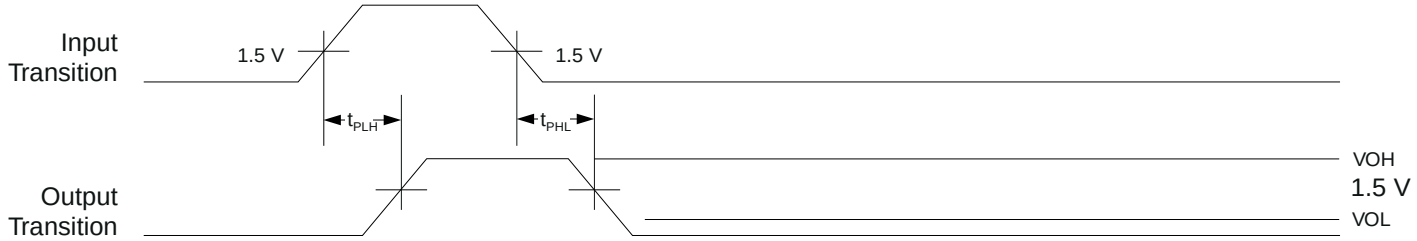
Typical Values

Parameter	Value	Units
V_{OLP}	0.4	V
V_{OLV}	-0.26	V
V_{OHV}	V_{CC} - 0.13	V
V_{OHP}	V_{CC} + 0.6	V

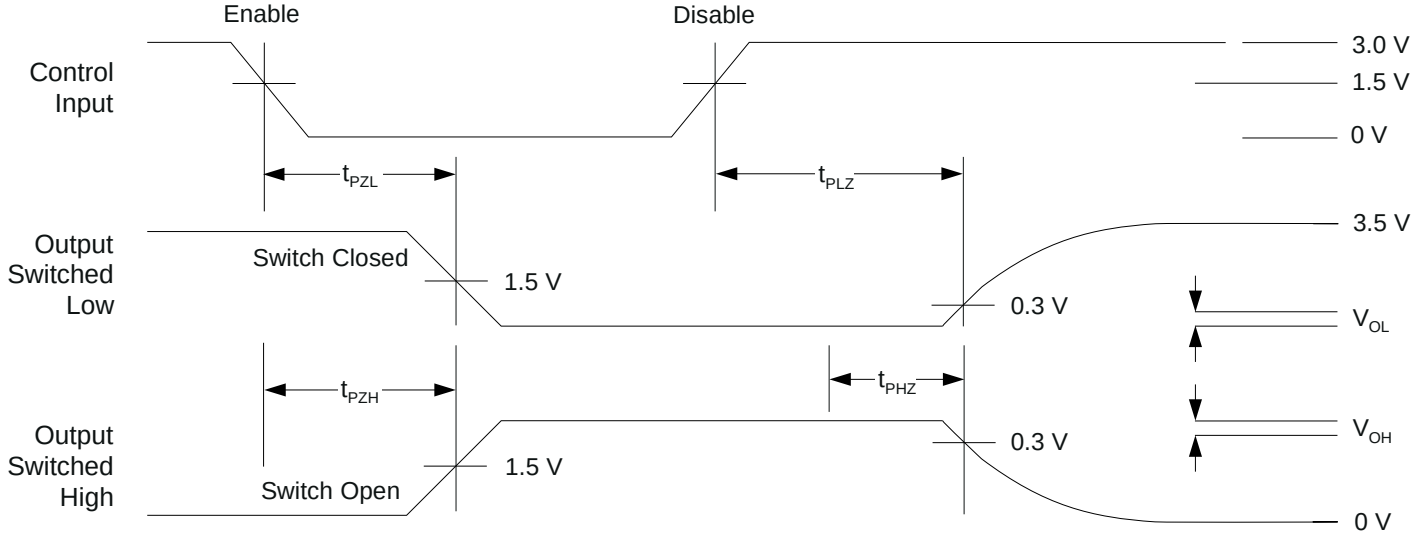
Note: 1. When multiple outputs are switched at the same time, rapidly changing current on the ground and VCC paths causes a voltage to develop across the parasitic inductance of the wire bond and package pins. This occurrence is called simultaneous switching noise. Atmel's AT16373 products have minimized this phenomenon as shown on the graph. Output data is for 15 outputs switching simultaneously at a frequency of 1 MHz. The ground data is measured on the one remaining output, which is set to logic low and will reflect any device ground movement.

2. As on the graph for Ground Bounce, a similar condition occurs for low to high transitions. Output data is for 15 outputs switching simultaneously at a frequency of 1 MHz. V_{CC} droop is measured on the one remaining output pin, which is set to a logic high. This output will reflect any movement on the device V_{CC}.

Propagation Delay Waveforms



Enable and Disable Waveforms(1)



Note: 1. Enable and disable waveforms are the same for both $x\overline{OE}$ and xLE inputs.

Ordering Information

T_{PD}	Ordering Code	Package	Operation Range
2.5 ns	AT16373F - 25YC AT16373F - 25XC	48Y 48X	Commercial
2.0 ns	AT16373G - 20YC AT16373G - 20XC	48Y 48X	Commercial

Package Type	
48X	48 Pin, Plastic Thin Shrink Small Outline Package (TSSOP)
48Y	48 Pin, Plastic Shrink Small Outline Package (SSOP)

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