Rail to Rail I/O 375 nA/Amp Dual/Quad CMOS Op Amps with Power Down

General Description

The SLG88103/4 is a wide voltage range, 375 nA Dual/Quad Channel CMOS Input Operational Amplifier capable of rail-to-rail input and output operation. Each Amplifier can be individually powered down.

Features

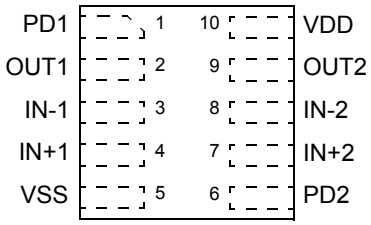
- Low Quiescent Current: 375 nA per Amplifier (typ)
- Low Offset Voltage: ±200 µV (typ)
- Zero-Crossover
- Low Offset Drift: 1 µV/˚C (typ)
- DC Precision:
  - PSRR: 115 dB
  - CMRR: 100 dB
  - A_{OL}: 120 dB
- Gain-Bandwidth Product: 10 kHz (typ)
- Rail to Rail Input/Output
- Supply Voltage: 1.71 V to 5.5 V
- Tiny Package:
  - 10-pin 2 x 2 mm STDFN
  - 20-pin 2 x 3.5 mm STQFN
- Industrial Temperature Range: -40 ˚C to 85 ˚C

Typical Applications

- Battery-Powered Devices
- Portable Devices
- Wearable Products
- Gas Sensors
- Pressure Sensors
- Medical Monitors
- Smoke Detectors
- Active RFID Reader
- Energy Harvester

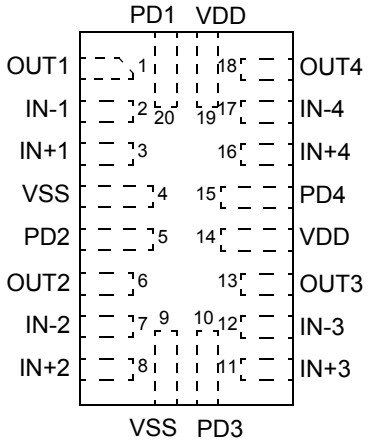
Pin Configurations

SLG88103



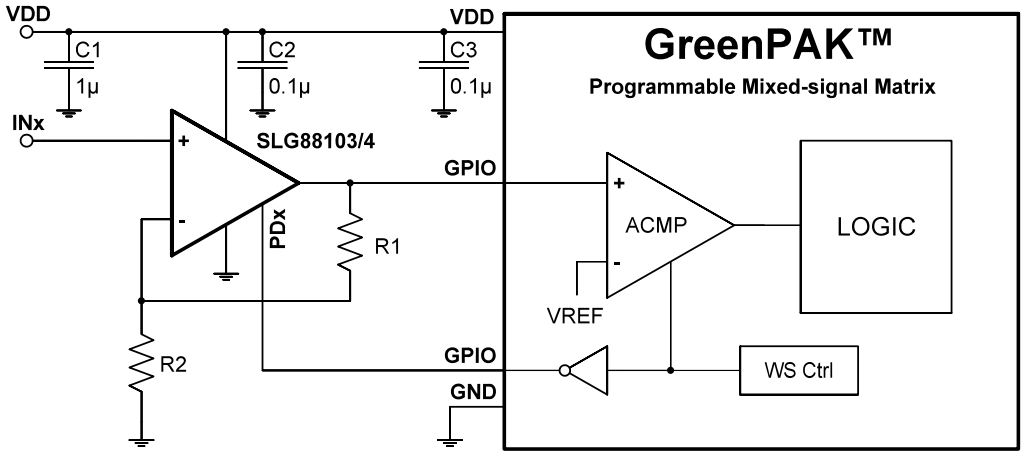
10-pin STDFN
(Top View)

SLG88104



20-pin STQFN
(Top View)

Example Application Circuit: Non-Inverting Amplifier + GreenPAK with Wake-Sleep Controller



Pin Description

Pin #		Pin Name	Type	Pin Description
20L STQFN	10L STDFN			
1	2	OUT1	O	Analog Output (Op Amp 1)
2	3	IN-1	I	Inverting Input (Op Amp 1)
3	4	IN+1	I	Non-inverting Input (Op Amp 1)
4	5	VSS	GND	Negative Power Supply
5	6	PD2	I	Power Down Input (Op Amp 2) When PD pin is high, the respective amplifier is powered down.
6	9	OUT2	O	Analog Output (Op Amp 2)
7	8	IN-2	I	Inverting Input (Op Amp 2)
8	7	IN+2	I	Non-inverting Input (Op Amp 2)
9	--	VSS	GND	Negative Power Supply
10	--	PD3	I	Power Down Input (Op Amp 3) When PD pin is high, the respective amplifier is powered down.
11	--	IN+3	I	Non-inverting Input (Op Amp 3)
12	--	IN-3	I	Inverting Input (Op Amp 3)
13	--	OUT3	O	Analog Output (Op Amp 3)
14	10	VDD	PWR	Power Supply
15	--	PD4	I	Power Down Input (Op Amp 4) When PD pin is high, the respective amplifier is powered down.
16	--	IN+4	I	Non-inverting Input (Op Amp 4)
17	--	IN-4	I	Inverting Input (Op Amp 4)
18	--	OUT4	O	Analog Output (Op Amp 4)
19	--	VDD	PWR	Power Supply
20	1	PD1	I	Power Down Input (Op Amp 1) When PD pin is high, the respective amplifier is powered down.

Ordering Information

Part Number	Type	Production Flow
SLG88103V	10-pin STDFN	Industrial, -40 °C to 85 °C
SLG88103VTR	10-pin STDFN (Tape and Reel)	Industrial, -40 °C to 85 °C
SLG88104V	20-pin STQFN	Industrial, -40 °C to 85 °C
SLG88104VTR	20-pin STQFN (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Voltage on VDD pin relative to GND	-0.3	--	6.0	V
T_A	Operating Range	-40	--	85	˚C
θ_{JA}	Thermal Resistance	--	80	--	˚C/W
T_S	Storage Temperature	-65	--	150	˚C
T_J	Junction Temperature	--	--	150	˚C
ESD_{HBM}	ESD Protection (Human Body Model)	2000	--	--	V
ESD_{CDM}	ESD Protection (Charged Device Model)	500	--	--	V
MSL	Moisture Sensitivity Level		1		

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = 25 °C, V_{DD} = 1.71 V to 5.5 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, unless otherwise stated.

Symbol	Description	Conditions	Min	Typ	Max	Unit
Input Offset						
V_{OS}	Input Offset Voltage	V_{CM} = V_{DD}/2	-1000	±200	1000	µV
		V_{CM} = V_{DD}/2; T_A = -40 ˚C to 85 ˚C	-1100	±250	1100	µV
		V_{CM} = V_{SS}; T_A = -40 ˚C to 85 ˚C	-2400	±350	2400	µV
dV_{OS}/dT	Offset Drift with Temperature	V_{CM} = V_{DD}/2; T_A = -40 ˚C to 85 ˚C	-4	±1	4	µV/˚C
		V_{CM} = V_{SS}; T_A = -40 ˚C to 85 ˚C	-10	±2	10	µV/˚C
dV_{OS}/Time	10 Year Offset Drift	T_A = 85˚C; V_{DD} = 3.3 V	-30	--	+30	µV
		T_A = 85˚C; V_{DD} = 5.0 V	-40	--	+40	µV
PSRR	Power Supply Rejection Ratio	V_{CM} = V_{DD}/2 T_A = -40 ˚C to 85 ˚C	95	115	--	dB
		V_{CM} = V_{SS} T_A = -40 ˚C to 85 ˚C	85	100	--	dB
CS	Channel Separation	V_{DD} = 5 V, f = 10 Hz	--	120	--	dB
		V_{DD} = 5 V, f = 1 kHz	--	95	--	dB
Input Voltage Range						
V_{CMR}	Input Common-Mode Voltage Range	T_A = -40 ˚C to 85 ˚C	V_{SS}	--	V_{DD}	V
CMRR	Common-Mode Rejection Ratio	V_{SS} + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T_A = -40 ˚C to 85 ˚C	65	100	--	dB
		V_{SS} < V_{CM} < V_{SS} + 0.8 V, V_{DD} - 0.8 V < V_{CM} < V_{DD}, T_A = -40 ˚C to 85 ˚C	50	75	--	dB
Input Bias Current and Impedance						
I_B	Input Bias Current[1]		--	2	--	pA
		T_A = 85 ˚C	--	320	500	pA

Electrical Characteristics (continued)

T_A = 25 °C, V_{DD} = 1.71 V to 5.5 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, unless otherwise stated.

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_{OS}	Input Offset Current[2]		--	±0.3	--	pA
		T_A = 85 ˚C	--	±20	--	pA
R_{CM}	Common Mode Input Resistance		--	10^{13}	--	Ω
R_{DIFF}	Differential Input Resistance		--	10^{13}	--	Ω
C_{CM}	Input Capacitance Common-Mode		--	4.3	--	pF
C_{DIFF}	Input Capacitance Differential		--	6	--	pF
Open-Loop Gain						
A_{OL}	DC Open Loop Voltage Gain	R_L = 1 MΩ; V_{SS} + 0.1 V ≤ V_{OUT} ≤ V_{DD} - 0.1 V	100	120	--	dB
		R_L = 50 kΩ; V_{SS} + 0.5 V ≤ V_{OUT} ≤ V_{DD} - 0.5 V	100	120	--	dB
		R_L = 50 kΩ; T_A = 85 ˚C; V_{SS} + 0.1 V ≤ V_{OUT} ≤ V_{DD} - 0.1 V	80	100	--	dB
Output						
V_{OH}, V_{OL}	Maximum Voltage Swing	R_L= 50 kΩ	V_{SS} + 5	--	V_{DD} - 5	mV
V_{OSR}	Linear Output Swing Range	V_{OVR} from Rail	V_{SS} + 100	--	V_{DD} - 100	mV
I_{SC}	Short-circuit Current	V_{DD} = 1.71 V	3.8	4.5	--	mA
		V_{DD} = 3.0 V to 5.5 V	8.5	10	--	mA
C_{LOAD}	Capacitive Load Drive		See Typical Performance Charts			
Power Supply						
V_{DD}	Supply Voltage	Guaranteed by PSRR Test	1.71	--	5.5	V
I_Q	Quiescent Current (Per Amplifier)		--	0.38	0.55	µA
		T_A = -40 ˚C to 85 ˚C	--	0.4	0.8	µA
		PDx = V_{DD}	--	1	--	nA
Frequency Response						
GBW	Gain Bandwidth Product	G = +1 V/V	--	10	--	kHz
PM	Phase Margin	G = +1 V/V	--	54	--	˚
SR	Slew Rate	R_L= 50 kΩ	2.4	5.0	--	V/ms
t_{OR}	Overload Recovery Time	T_A = -40 ˚C to 85 ˚C; R_L= 50 kΩ	--	350	--	µs
Noise						
e_n	Input Voltage Noise	f = 0.1 to 10 Hz	--	6.5	--	μV_{P-P}
V_n	Input Voltage Noise Density	f =1 kHz	--	195	--	nV/√Hz
I_n	Input Current Noise Density	f =1 kHz	--	< 10	--	fA/√Hz

Note:
1. Part is measured to be less than 1 µA during production test.
2. Guaranteed by design, not tested in production.

Typical Performance Charts

T_A = 25 °C, V_{DD} = 5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L , C_L = 80 pF, unless otherwise stated.

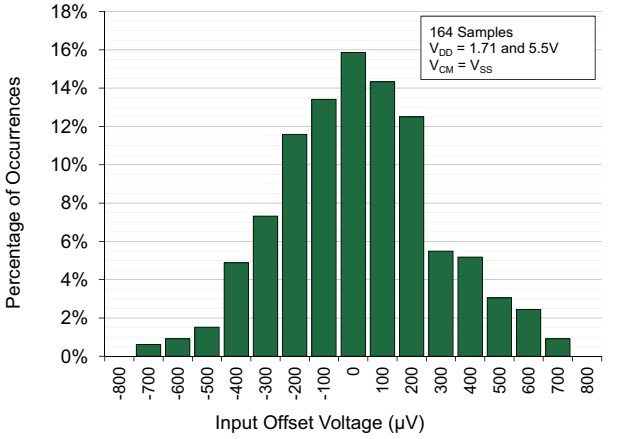


Fig 1. Input Offset Voltage Drift Distribution V_{CM} = V_{SS}; V_{DD} = 1.71 V and 5.5 V; T_A = 25˚C.

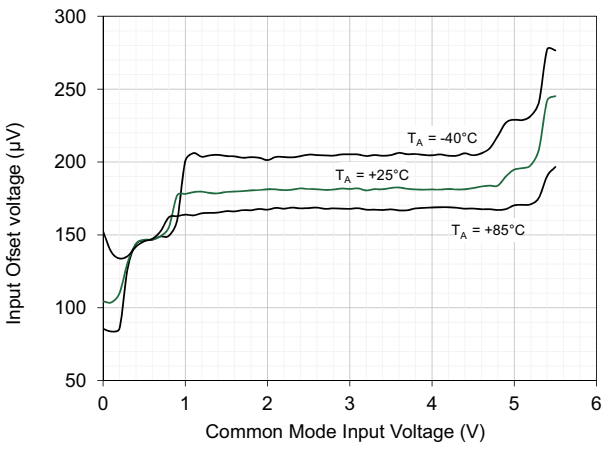


Fig 2. Input Offset Voltage vs. Common Mode Input Voltage V_{DD} = 5.5 V.

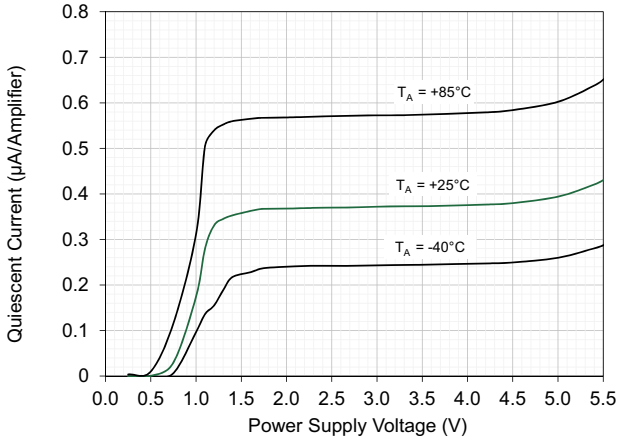


Fig 3. Quiescent Current vs. Power Supply Voltage

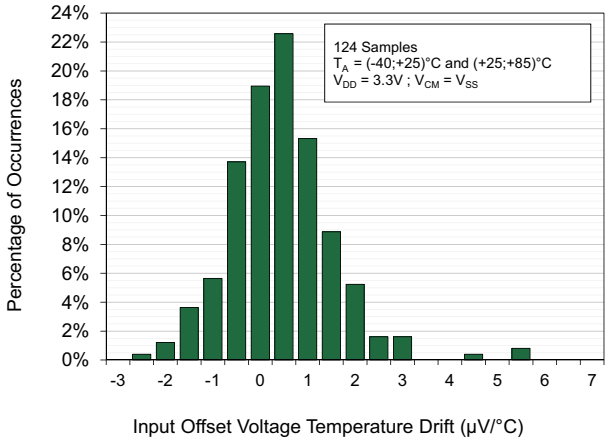


Fig 4. Input Offset Voltage Temperature Drift Distribution V_{CM} = V_{SS}; V_{DD} = 3.3 V; T_A = -40˚C to 85˚C.

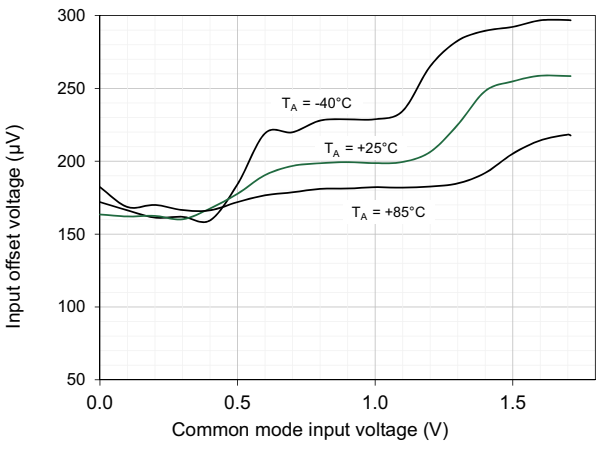


Fig 5. Input Offset Voltage vs. Common Mode Input Voltage V_{DD} = 1.71 V.

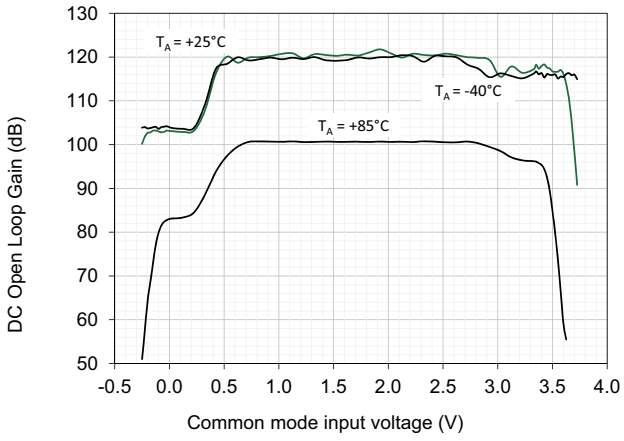


Fig 6. DC Open Loop Gain vs. Common Mode Input Voltage V_{DD} = 3.3 V.

T_A = 25 °C, V_{DD} = 5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L , C_L = 80 pF, unless otherwise stated.

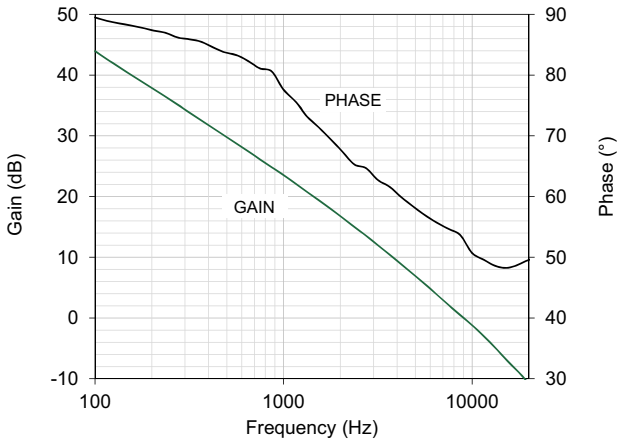


Fig 7. Open Loop Gain and Phase vs. Frequency V_{DD} = 3.3 V.

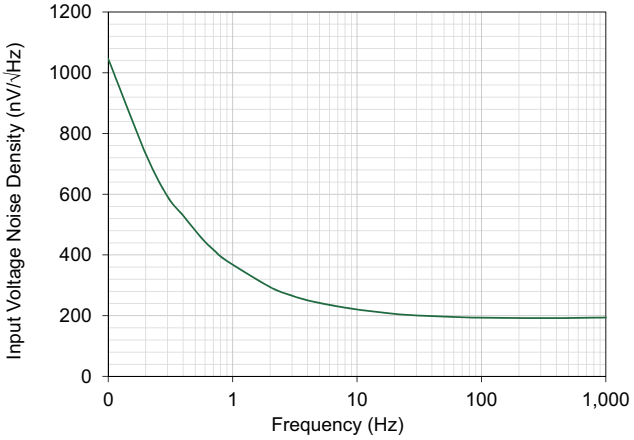


Fig 10. Input Noise Voltage Density vs. Frequency

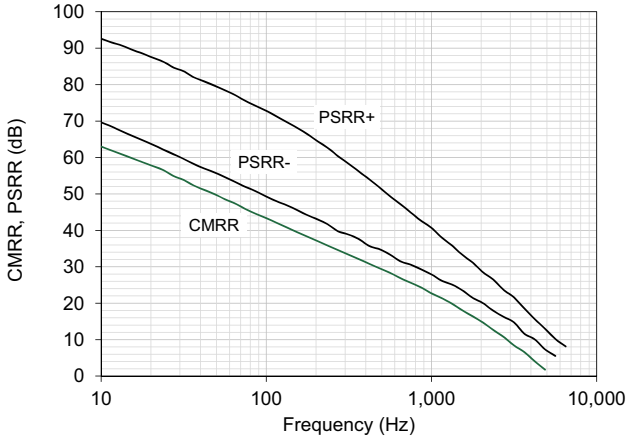


Fig 8. CMRR, PSRR vs. Frequency V_{DD} = 3.3 V.

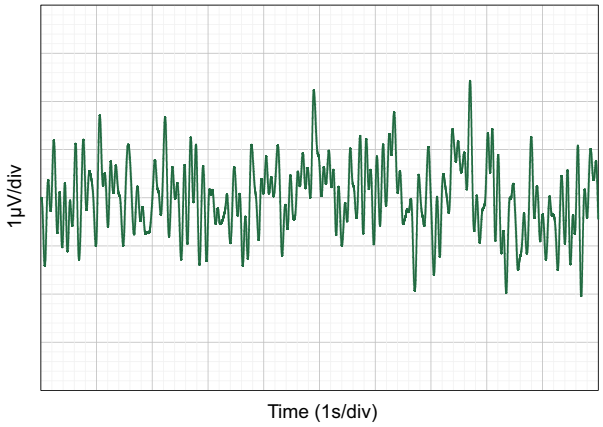


Fig 11. 0.1 Hz to 10 Hz Noise

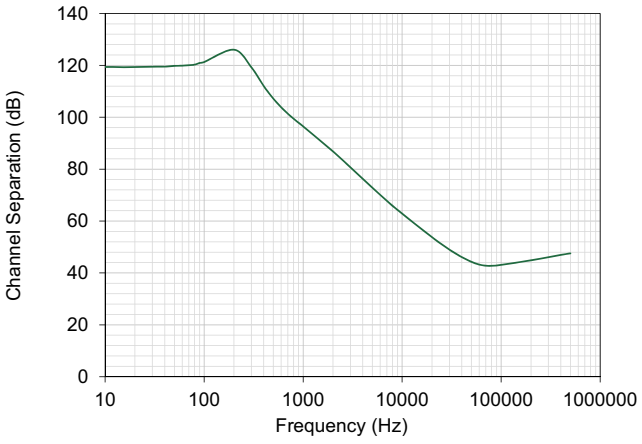


Fig 9. Channel Separation vs. Frequency

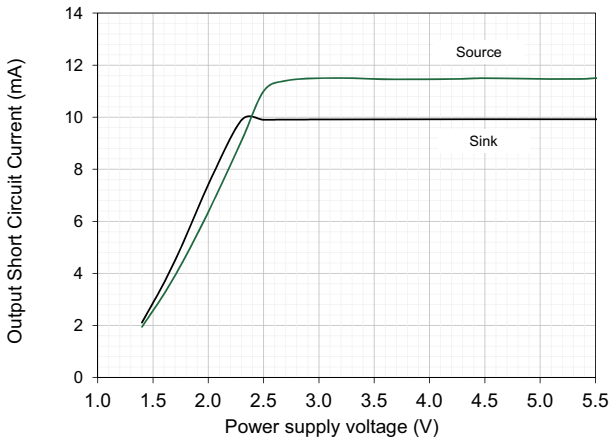


Fig 12. Output Short Circuit Current vs. V_{DD}

T_A = 25 °C, V_{DD} = 5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L , C_L = 80 pF, unless otherwise stated.

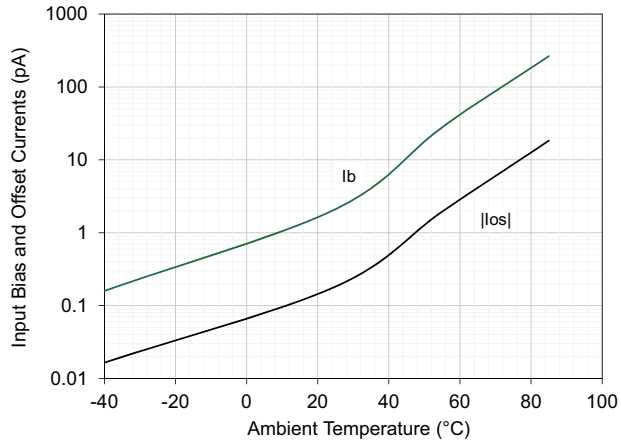


Fig 13. Input Bias, Offset Currents vs. T_A V_{DD} = 3.3 V.

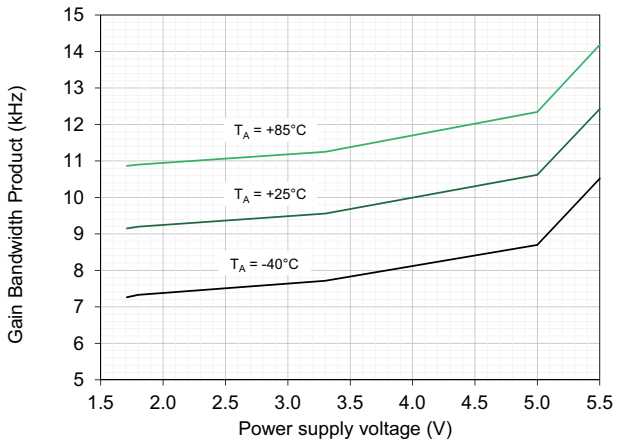


Fig 16. Gain Bandwidth Product vs. Power Supply Voltage

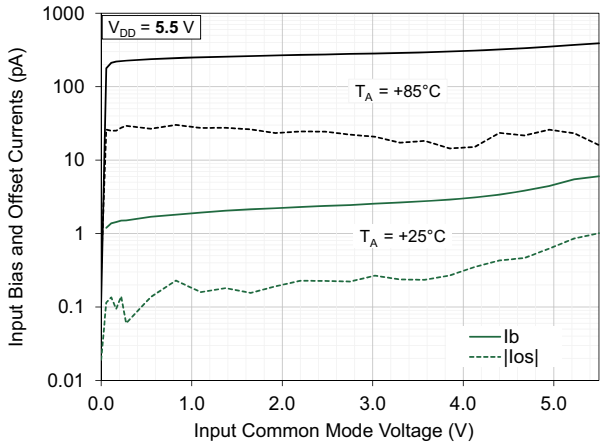


Fig 14. Input Bias, Offset Currents vs. V_{CM} V_{DD} = 5.5 V.

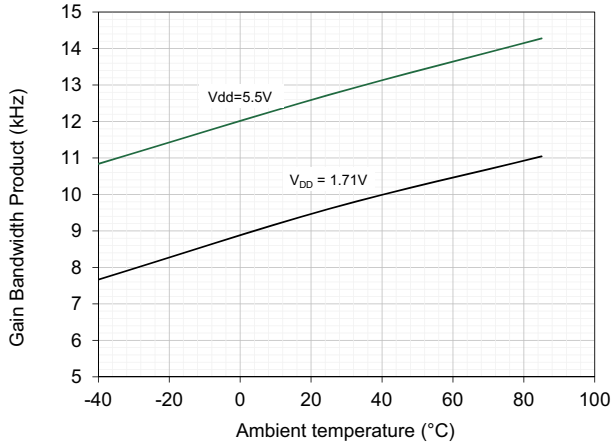


Fig 17. Gain Bandwidth Product vs. Ambient Temperature

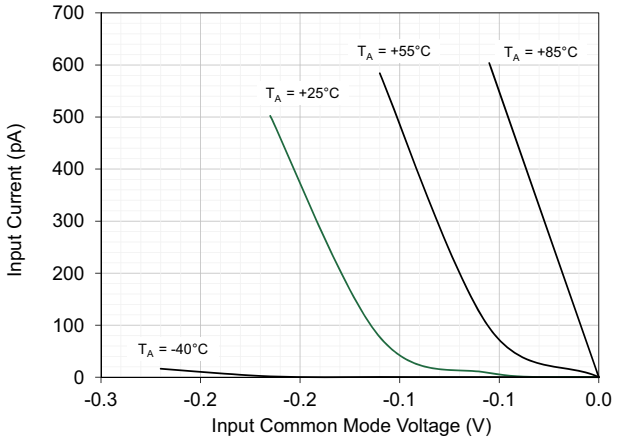


Fig 15. Input Current vs. V_{CM} (below V_{SS}) V_{DD} = 5.5 V.

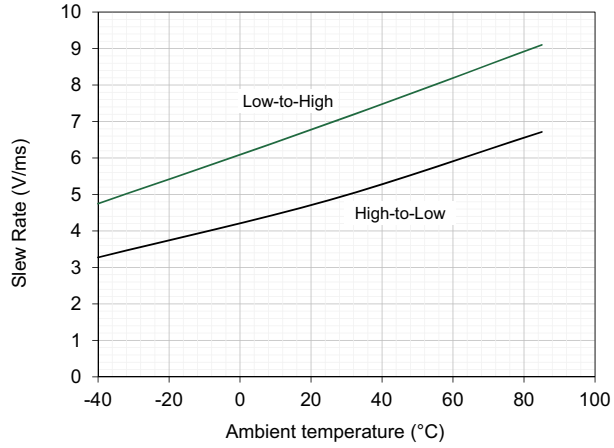


Fig 18. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ

T_A = 25 °C, V_{DD} = 5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L , C_L = 80 pF, unless otherwise stated.

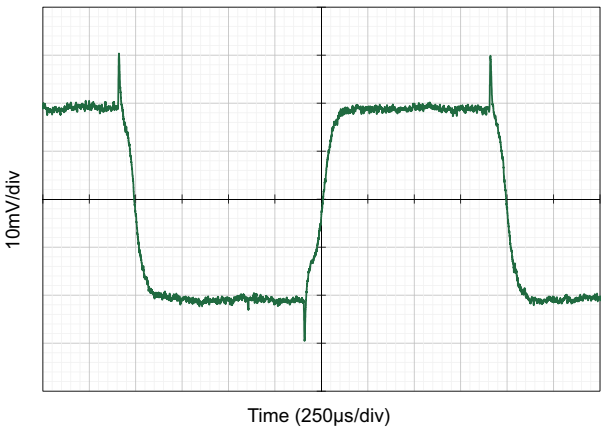


Fig 19. Small Signal Inverting Step Response
G = -1 V/V; R_L = 50 kΩ; C_L = 60 pF.

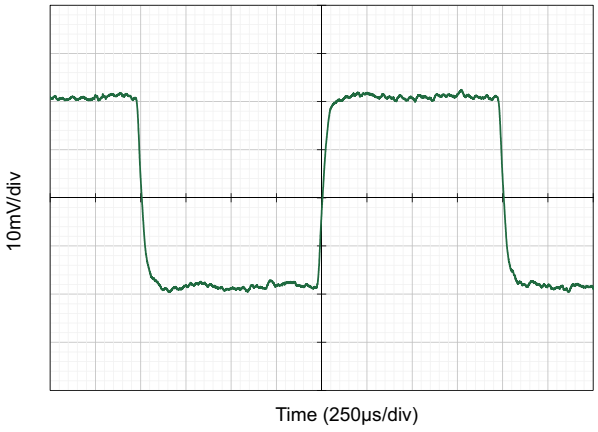


Fig 22. Small Signal Non-inverting Step Response
G = 1 V/V; R_L = 50 kΩ; C_L = 60 pF.

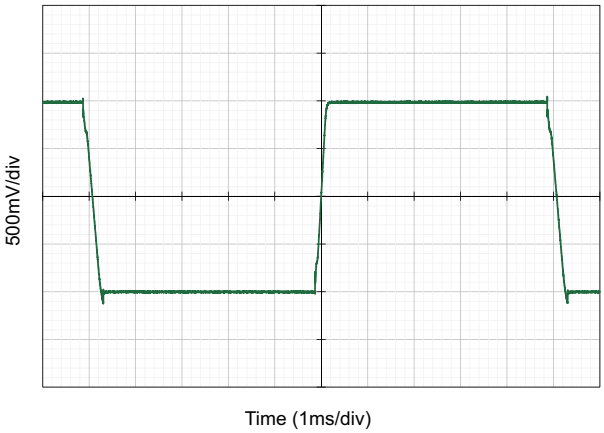


Fig 20. Large Signal Inverting Step Response
G = -1 V/V; R_L = 50 kΩ; C_L = 80 pF.

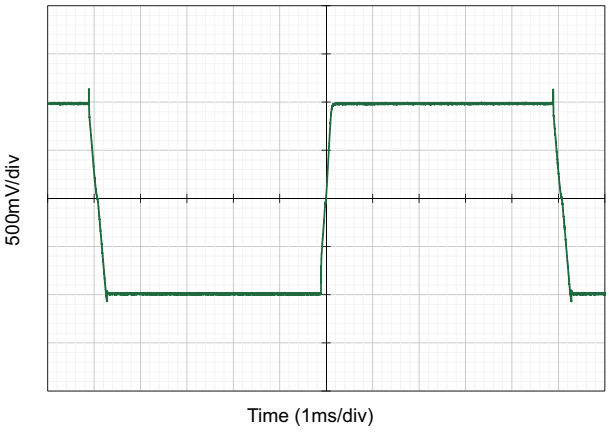


Fig 23. Large Signal Non-inverting Step Response
G = 1 V/V; R_L = 50 kΩ; C_L = 60 pF.

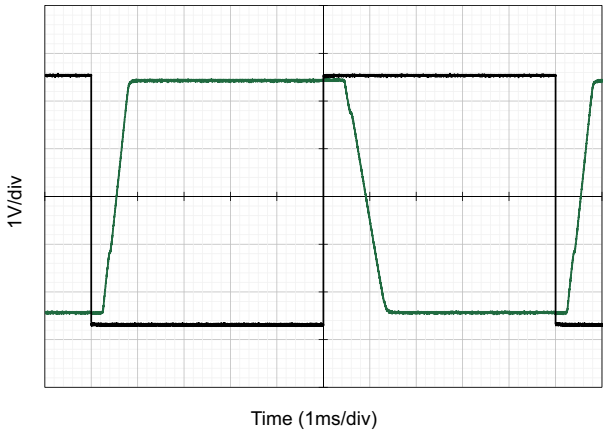


Fig 21. Inverting Overload Recovery
G = -1 V/V; R_L = 50 kΩ; C_L = 60 pF.

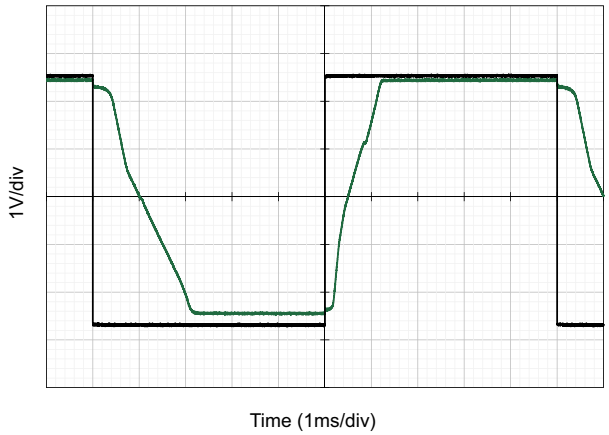


Fig 24. Non-Inverting Overload Recovery
G = 1 V/V; R_L = 50 kΩ; C_L = 60 pF.

T_A = 25 °C, V_{DD} = 5.0 V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L , C_L = 80 pF, unless otherwise stated.

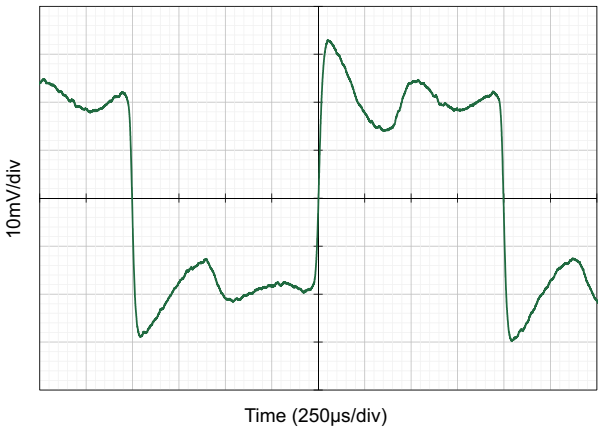


Fig 25. Small Signal Non-inverting Step Response
G = 1 V/V; R_L = 50 kΩ; C_L = 10 nF.

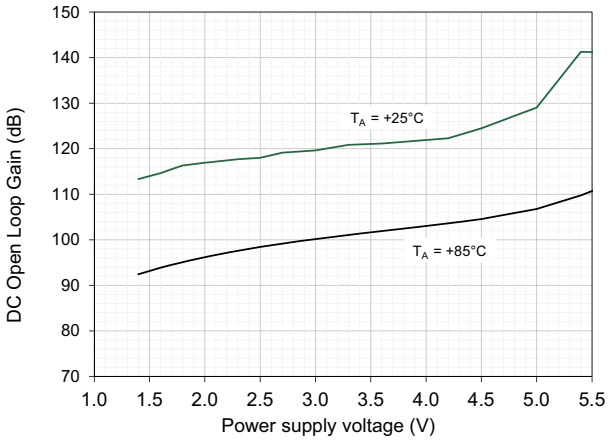


Fig 28. DC Open Loop Gain vs. Power Supply Voltage
R_L = 50 kΩ

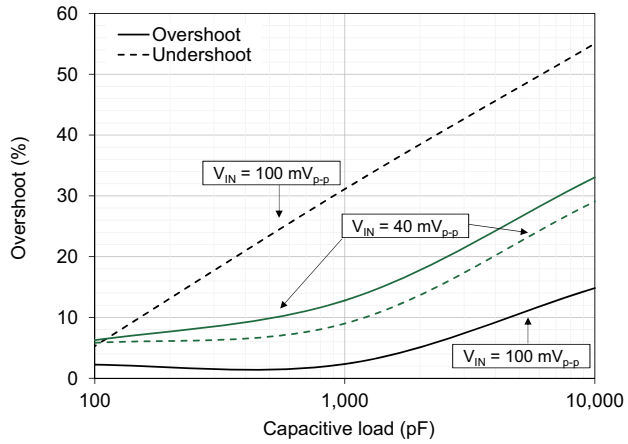


Fig 26. Small Signal Overshoot vs. Capacitive Load
V_{DD} = 3.3 V; V_{IN} = 40 and 100 mV p-p; G = 1 V/V.

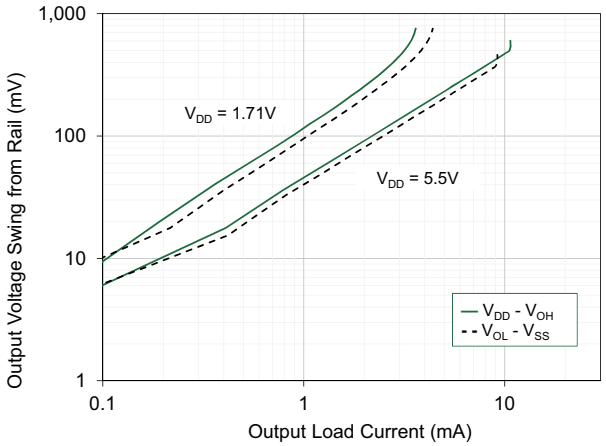


Fig 29. Output Voltage Swing from Rail vs. I_{OUT}
V_{DD} = 1.71 V and 5.5 V.

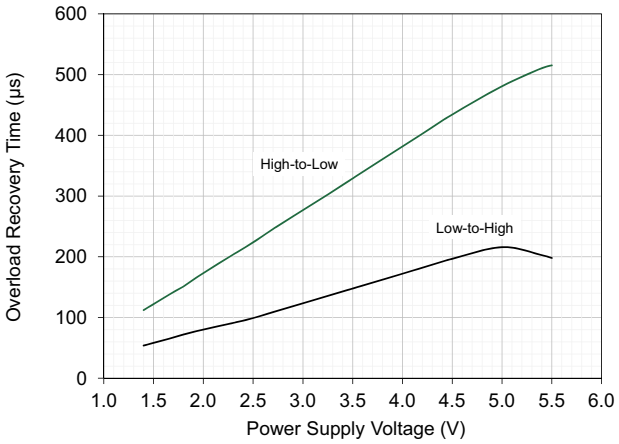


Fig 27. Overload Recovery Time vs. Power Supply Voltage
R_L= 50 kΩ; G = 1 V/V.

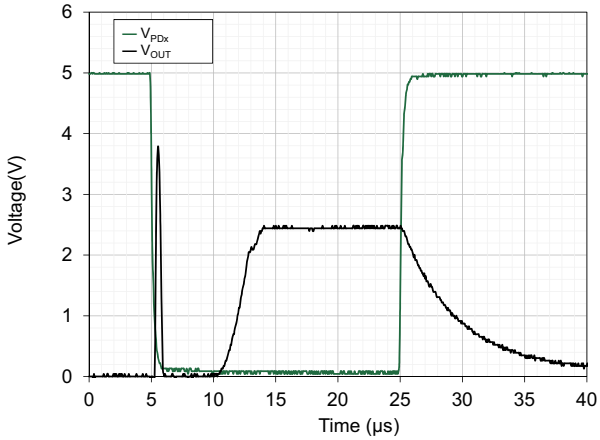


Fig 30. Output Response to Power Down Signal
G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2.

Applications Information

The SLG88103/4 operates on a 1.71 V to 5.5 V power supply over a wide industrial temperature range from -40 °C to 85 °C. This dual/quad op amp chip has two/four active low enable pins used to individually power-up / power-down each op amp. Its common-mode range extends from 0 to V_{DD} and its output swings from rail-to-rail.

Input Protection

Voltage spikes need to be controlled at the inputs of each operational amplifier in order to avoid damaging the device. Electrical events like electrostatic discharge can produce large voltages at these nodes. The SLG88103/4 has internal circuitry to protect the device from these events. If V_{IN} exceeds V_{DD} or drops below V_{SS}, additional currents will flow through the internal ESD diodes and can damage the device even if the supplies are turned off.

In this case we recommend placing a resistor in series to the input to limit current through the internal ESD diodes to 5 mA (or preferably less).

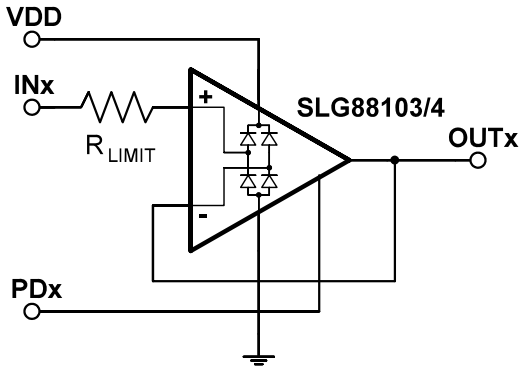


Fig 31. ESD Protection .

Driving Capacitive Loads

Capacitive loads degrade circuit stability by decreasing the phase margin and bandwidth of the operational amplifier circuit. The SLG88103/4 can drive capacitive loads up to 10 nF at low loads. The amplifier's output impedance and the capacitive load add phase lag to the system. This phase lag creates gain peaking in the frequency response and peaking/ringing in the output's transient response. When large capacitive loads need to be driven, isolation resistors need to be used to increase the phase margin. This is done by increasing the output load impedance at higher frequencies. After selecting an isolation resistor value, verify that the frequency peaking and transient overshoot and ringing have been reduced.

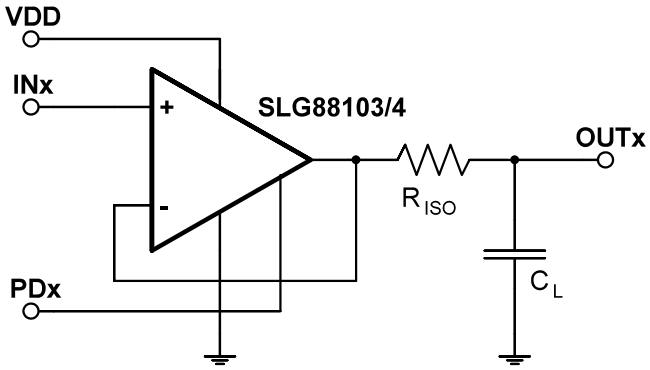


Fig 32. Capacitive Load Test Circuit.

Low Power Considerations

The SLG88103/4 features low quiescent current at 375 nA per amplifier, as well as extremely high-impedance CMOS inputs. To take most advantage of such low power features, high impedance external components should be used. We recommend using low-leakage capacitors (such as ceramic). Other types of capacitors (such as aluminum dielectric) can leak at uA levels and consume more quiescent power than the op-amp itself! High value resistors are needed to keep power consumption low, as well as to avoid gain loss and non-linearities due to loading effects on the ultra-low power-stage of the op amp. On the other hand, higher resistances increase thermal noise and sensitivity to external interference. We recommend impedances between 100 kΩ and 500 kΩ in gain/feedback networks to achieve balanced performance given the ultra-low power characteristics of SLG88103/4.

PCB Layout

For proper PCB layout, place a 100 nF decoupling capacitor close to the VDD pin of the SLG88103/4. To improve sensitive system performance, keep trace lengths similar on the positive and negative inputs of the op amp. Keep feedback resistors as close to the op amp and as short as possible. In addition, remove the PCB ground plane from under the inputs and outputs of the op amp.

For low current applications, board leakage currents on sensitive, high impedance inputs can degrade signal integrity. To maximize system performance, use guard rings / shields around these high impedance op amp inputs. For non-inverting op amps, IN+ should have a guard ring driven to the voltage of IN- by a low impedance source. Similarly, the guard ring around IN- should be driven to IN+ for an inverting amplifier. The IN- and IN+ nodes for non-inverting and inverting amplifiers respectively can be used as low impedance voltage sources. This is because these nodes are effectively low impedance nodes due to op amp feedback properties. For a non-inverting amplifier, leakage current on IN+ will produce a voltage on the input that will be amplified to the op amp's output. On the other hand, the op amp will fight changes in voltage on IN- to match the voltage potential at IN+. These guard rings should be used on both sides of the PCB to help sink stray currents on the PCB before the currents can reach the input pins of the op amp and to minimize stray capacitance.

Proper Setup for Unused Op Amps

For an unused op amp on the SLG88103/4, connect the op amp as a voltage follower with the input tied to ground and it's enable pin tied to VDD. An example circuit using one of the op amps is shown below.

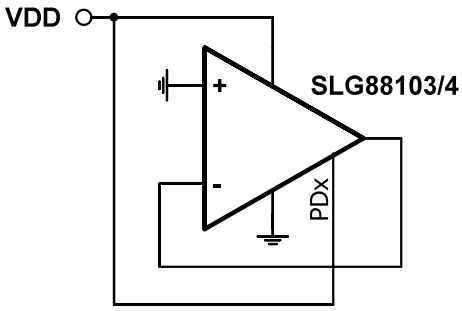


Fig 33. Unused Op Amp Setup.

Application Examples

The SLG88103/4 excels in low-power applications that operate at low frequencies. Please see the "Application Notes" section of this datasheet for application examples which use the SLG88103/4.

Design Resources

1. Spice Macro Model

The most recent SPICE model is available on Silego's website at www.silego.com. This model is intended for simulation purposes only and shouldn't be used in place of hardware testing to verify proper functionality in a full system.

2. Application Notes

For more information on the topics discussed in this datasheet and applications of this device, please see the following applications notes available online at our Application Notes Page. New Application Notes are added regularly.

AN-1106 Custom Instrumentation Amplifier Design

3. Design Support

Please contact a Silego Representative at our Contact Page for more information on the SLG88103/4. They will be happy to assist you by answering additional questions and by offering design support for projects relating to the SLG88103/4 and Silego's GreenPAK devices.

4. Op Amp + GreenPAK EVB

The OP AMP+GreenPAK EVB provides convenient breakout access for various IC's in Silego's Op Amp and GreenPAK product families. Please see the OP AMP+EVB Layout Guide for more information on which GreenPAK devices and op amps can be placed on this PCB.

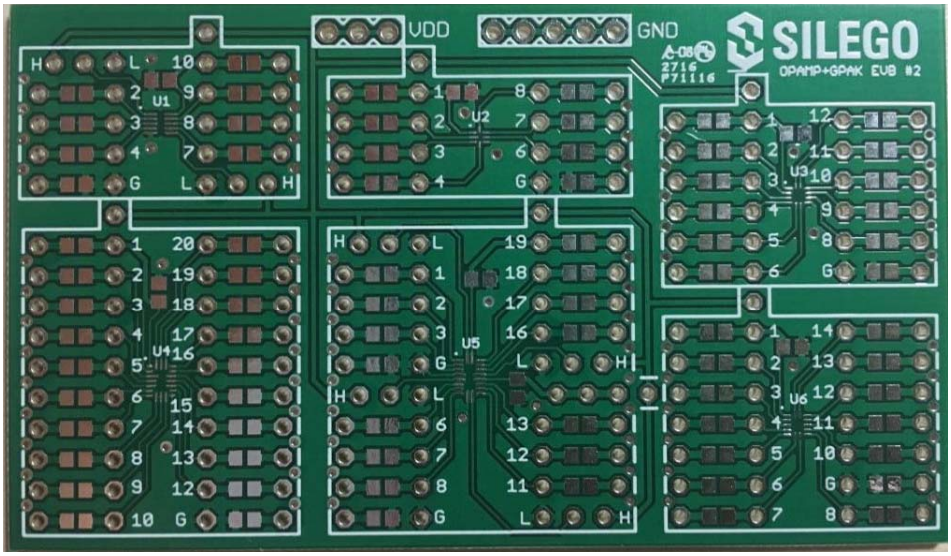
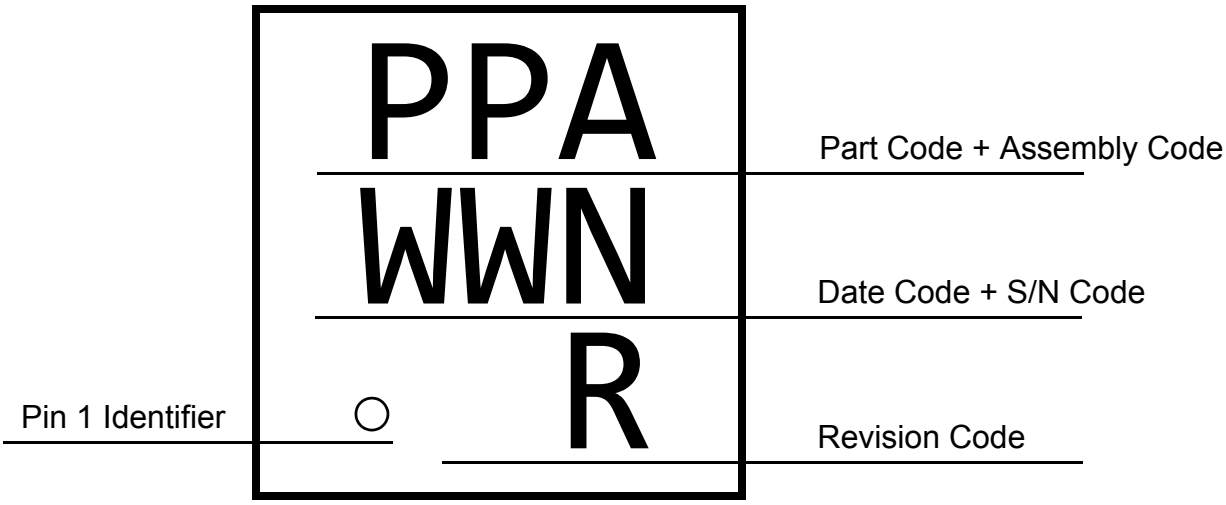


Fig 34. Op Amp + GreenPAK EVB.

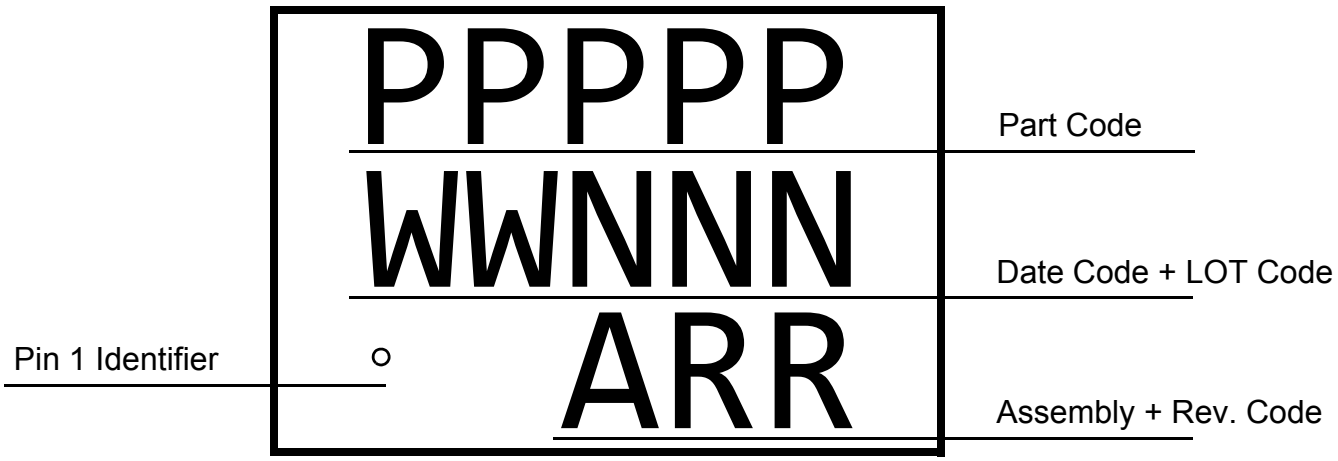
Package Top Marking System Definition - SLG88103



PP - Part ID Field
WW - Date Code Field[1]
N - Lot Traceability Code Field[1]
A - Assembly Site Code Field [2]
R - Part Revision Code Field[2]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Top Marking System Definition - SLG88104

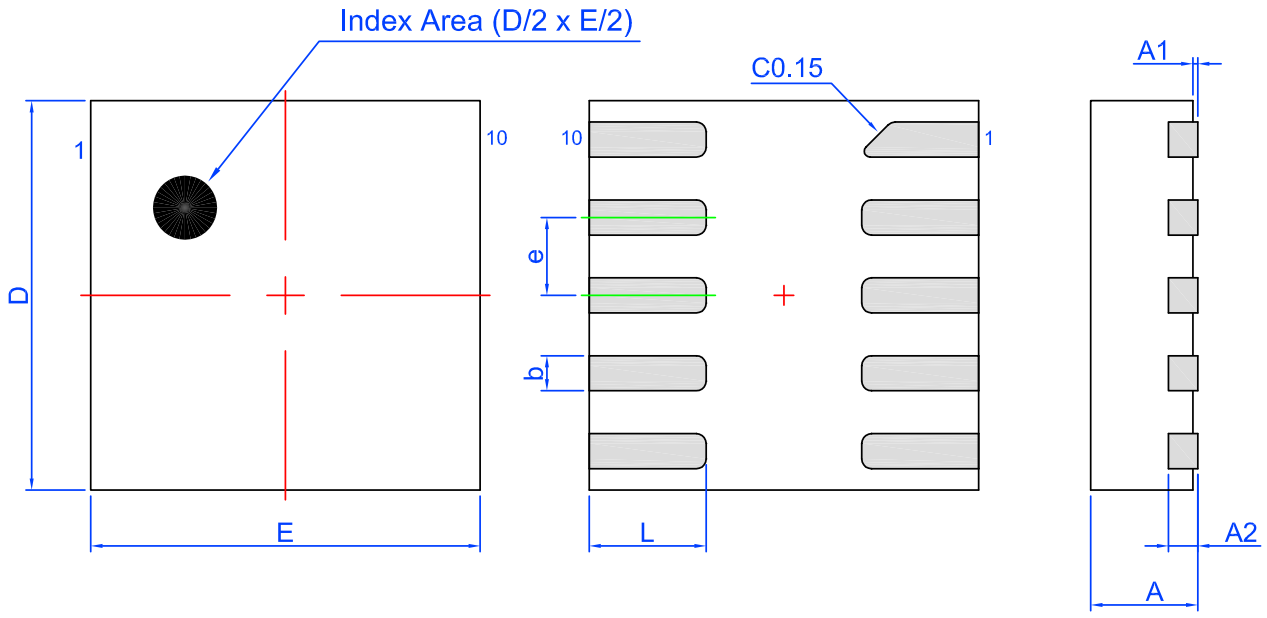


PPPPP - Part ID Field
WW - Date Code Field[1]
NNN - Lot Traceability Code Field[1]
A - Assembly Site Code Field[2]
RR - Part Revision Code Field[2]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions - SLG88103

10 Lead STDFN Package
JEDEC MO-252

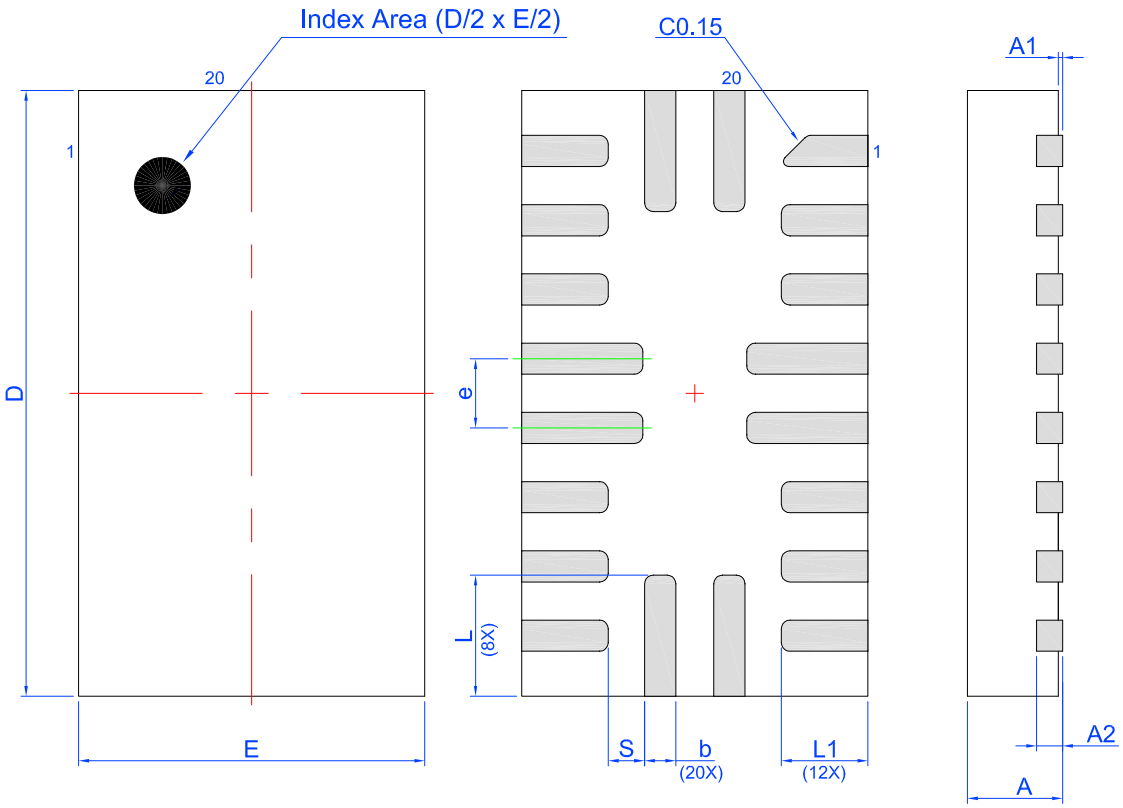


Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.55	0.60	0.65
b	0.13	0.18	0.23	C	0.15 REF		
e	0.40 BSC						

Package Drawing and Dimensions - SLG88104

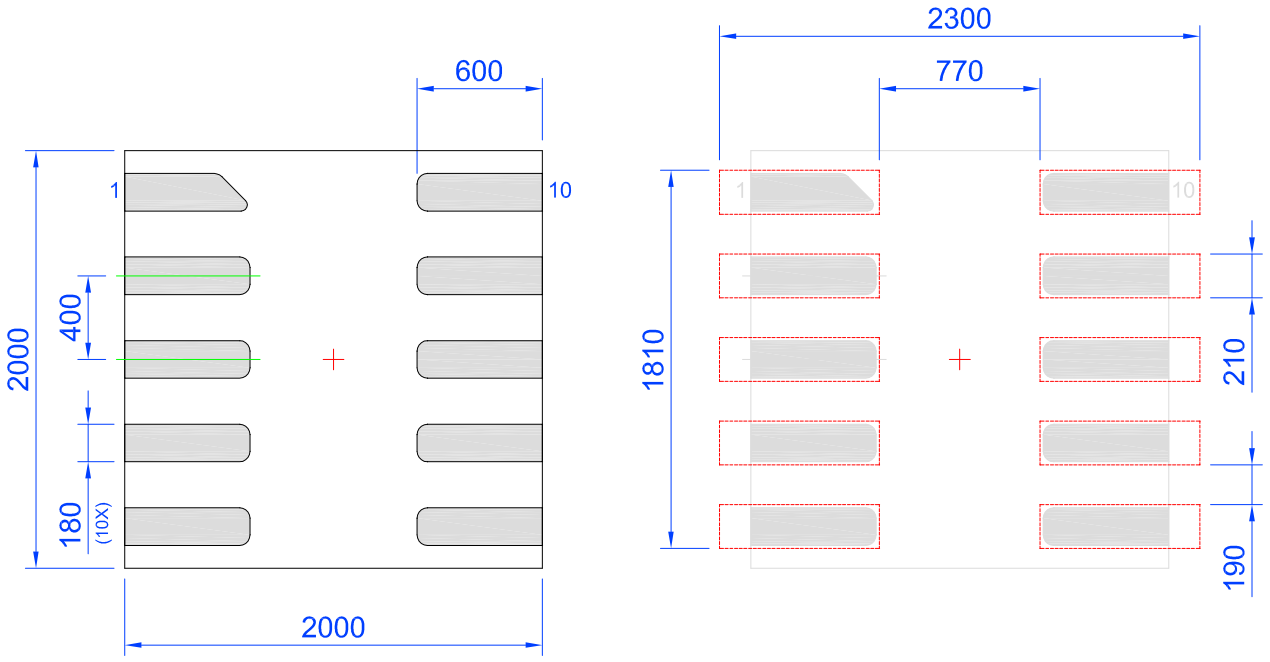
20 Lead STQFN Package



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	3.45	3.50	3.55
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.65	0.70	0.75
b	0.13	0.18	0.23	L1	0.45	0.50	0.55
e	0.40 BSC			C	0.15 REF		
S	0.21 REF						

Recommended Land Pattern - SLG88103

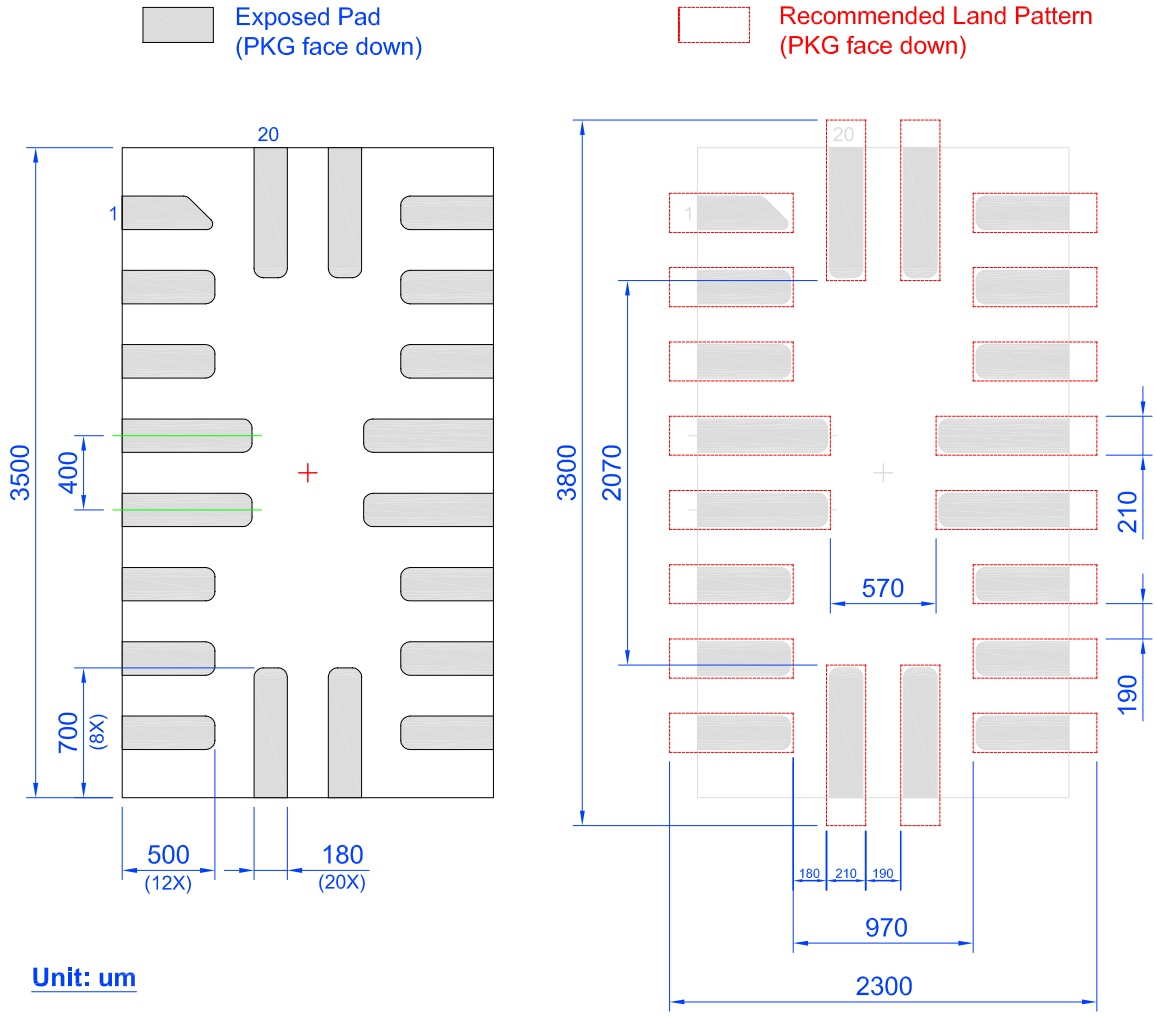


Unit: um

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern - SLG88104



Recommended Reflow Soldering Profile

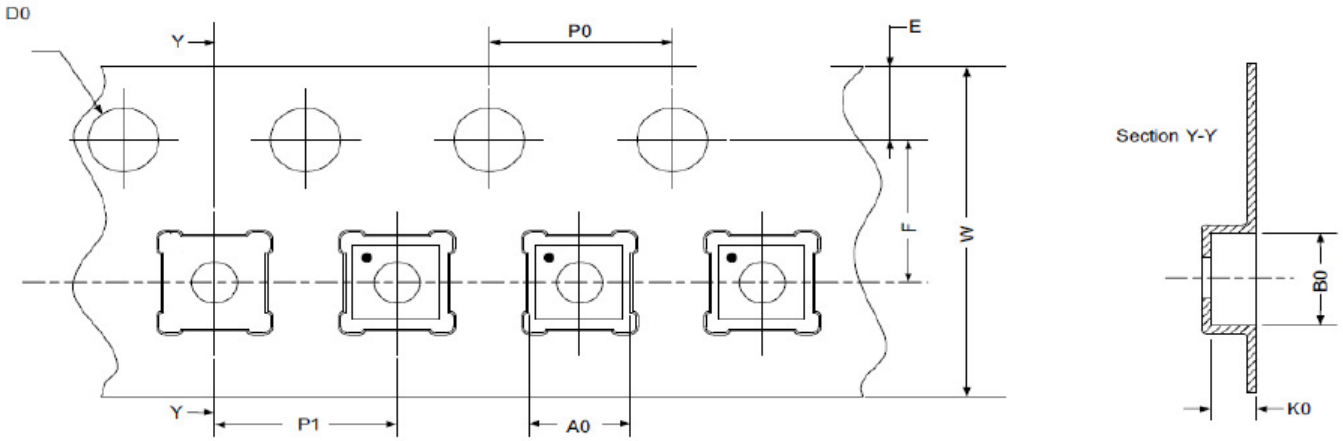
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm^3 (nominal). More information can be found at www.jedec.org.

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 10L 2x2mm 0.4P COL Green	10	2 x 2 x 0.55	3000	3000	178 / 60	100	400	100	400	8	4
STQFN 20L 2x3.5mm 0.4P Green	20	2 x 3.5 x 0.55	5000	10000	330 /100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions - SLG88103

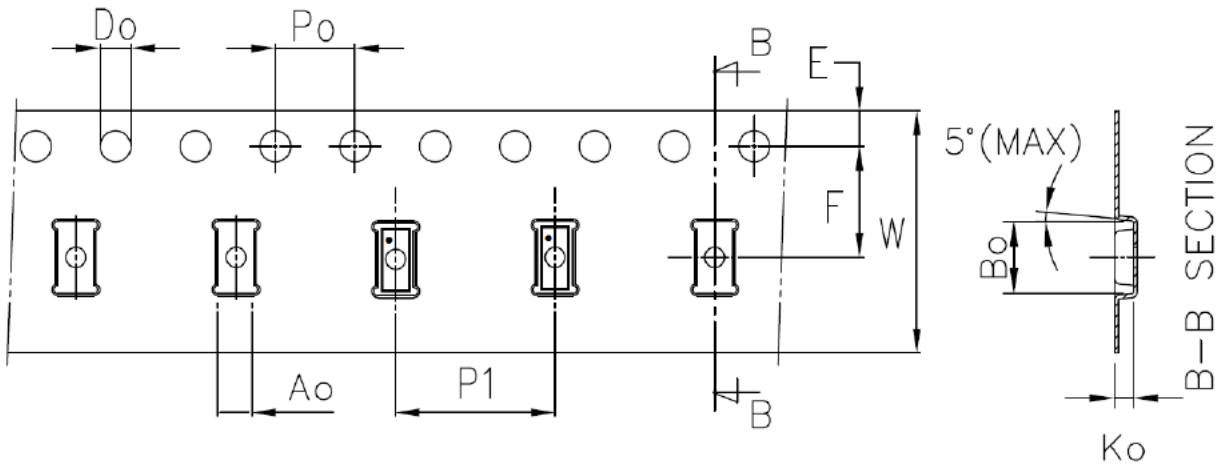
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 10L 2x2mm 0.4P COL Green	2.2	2.2	0.83	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Carrier Tape Drawing and Dimensions Dimensions - SLG88104

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3.5mm 0.4P Green	2.2	3.8	0.8	4	8	1.5	1.75	5.5	12



Refer to EIA-481 specification

Revision History

Date	Version	Change
3/13/2017	1.01	Replaced Slew Rate vs. Ambient Temperature Chart Fixed Chart formatting for some charts. Fixed typos
3/1/2017	1.00	Production Release

Silego Website & Support

Silego Technology Website

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http://greenpak2.silego.com/	http://greenfet2.silego.com/	http://greenclk2.silego.com/
http://greenpak3.silego.com/	http://greenfet3.silego.com/	http://greenclk3.silego.com/

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