# HIP4080A

80V/2.5A Peak, High Frequency Full Bridge FET Driver

FN3658
Rev.8.00
Dec 11, 2019

The HIP4080A is a high frequency, medium voltage Full Bridge N-Channel FET driver IC, available in 20 lead plastic SOIC and DIP packages. The HIP4080A includes an input comparator, used to facilitate the “hysteresis” and PWM modes of operation. Its HEN (high enable) lead can force current to freewheel in the bottom two external power MOSFETs, maintaining the upper power MOSFETs off. Since it can switch at frequencies up to 1MHz, the HIP4080A is well suited for driving Voice Coil Motors, switching power amplifiers and power supplies.

HIP4080A can also drive medium voltage brush motors, and two HIP4080As can be used to drive high performance stepper motors, since the short minimum “on-time” can provide fine micro-stepping capability.

Short propagation delays of approximately 55ns maximize control loop crossover frequencies and dead-times which can be adjusted to near zero to minimize distortion, resulting in precise control of the driven load.

The similar HIP4081A IC allows independent control of all 4 FETs in a Full Bridge configuration.

The Application Note for the HIP4080A is AN9404.

## Ordering Information

| PART NUMBER | TEMPERATURE RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|
| HIP4080AIPZ (Note 1) | -40 to +85 | 20 Ld PDIP | E20.3 |
| HIP4080AIBZ (Note 1) | -40 to +85 | 20 Ld SOIC | M20.3 |

NOTES:

1. Intersil Pb-Free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-Free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.
2. Add “T” suffix for Tape and Reel packing option. HIP4080AIP not available in Tape and Reel.

## Features

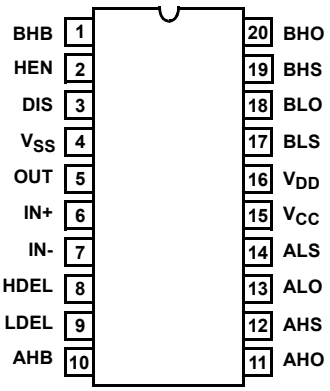
- Drives N-Channel FET Full Bridge Including High Side Chop Capability
- Bootstrap Supply Max Voltage to 95VDC
- Drives 1000pF Load at 1MHz in Free Air at +50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- Charge-Pump and Bootstrap Maintain Upper Bias Supplies
- DIS (Disable) Pin Pulls Gates Low
- Input Logic Thresholds Compatible with 5V to 15V Logic Levels
- Very Low Power Consumption
- Undervoltage Protection
- Pb-Free (RoHS Compliant)

## Applications

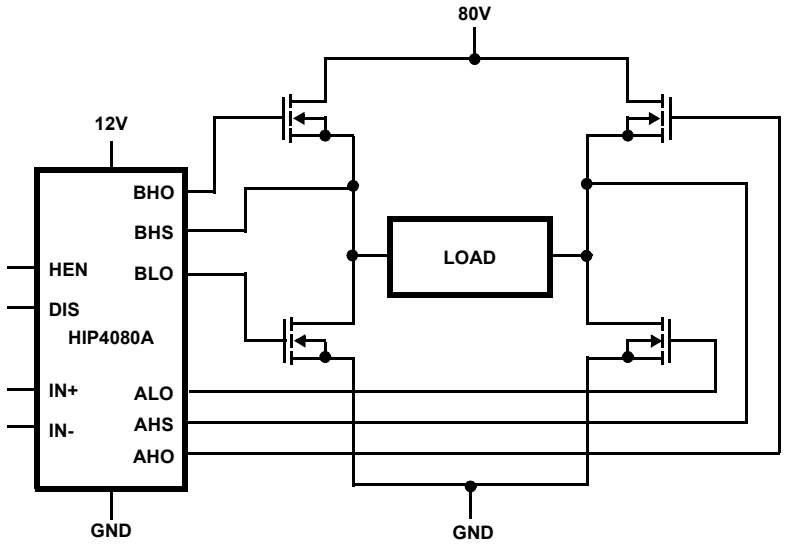
- Medium/Large Voice Coil Motors
- Full Bridge Power Supplies
- Switching Power Amplifiers
- High Performance Motor Controls
- Noise Cancellation Systems
- Battery Powered Vehicles
- Peripherals
- U.P.S.

## Pinout

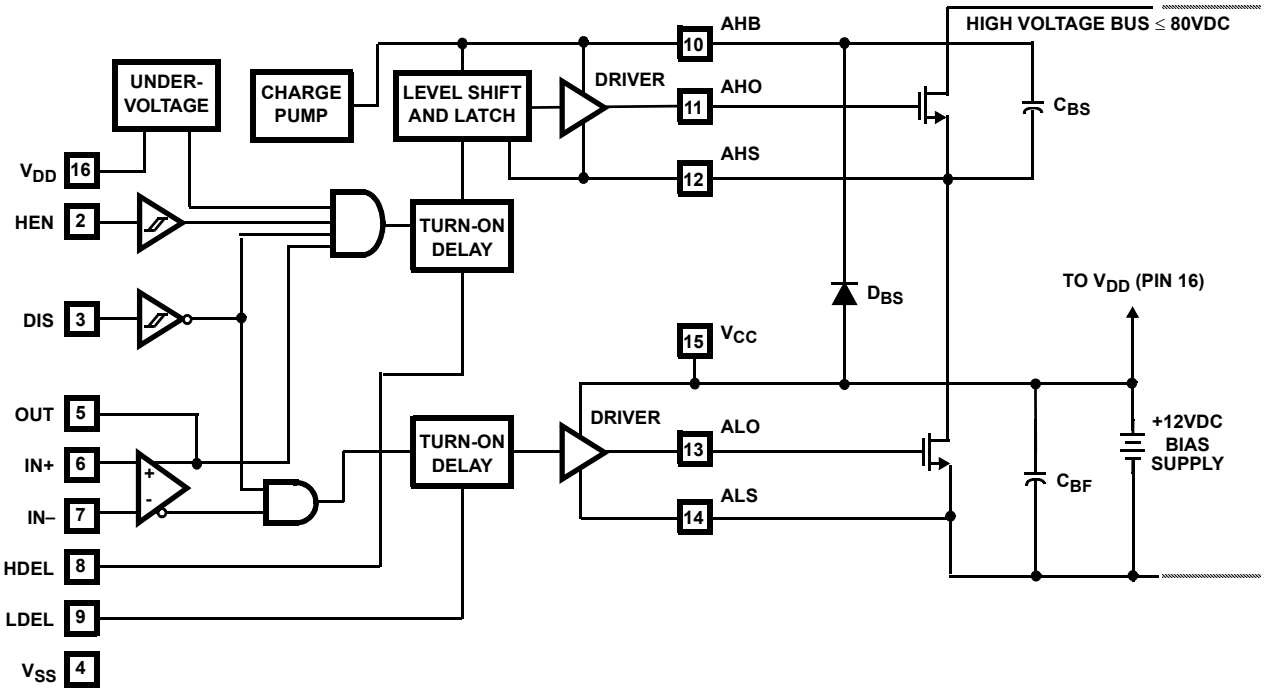
**HIP4080A**
**(PDIP, SOIC)**
TOP VIEW



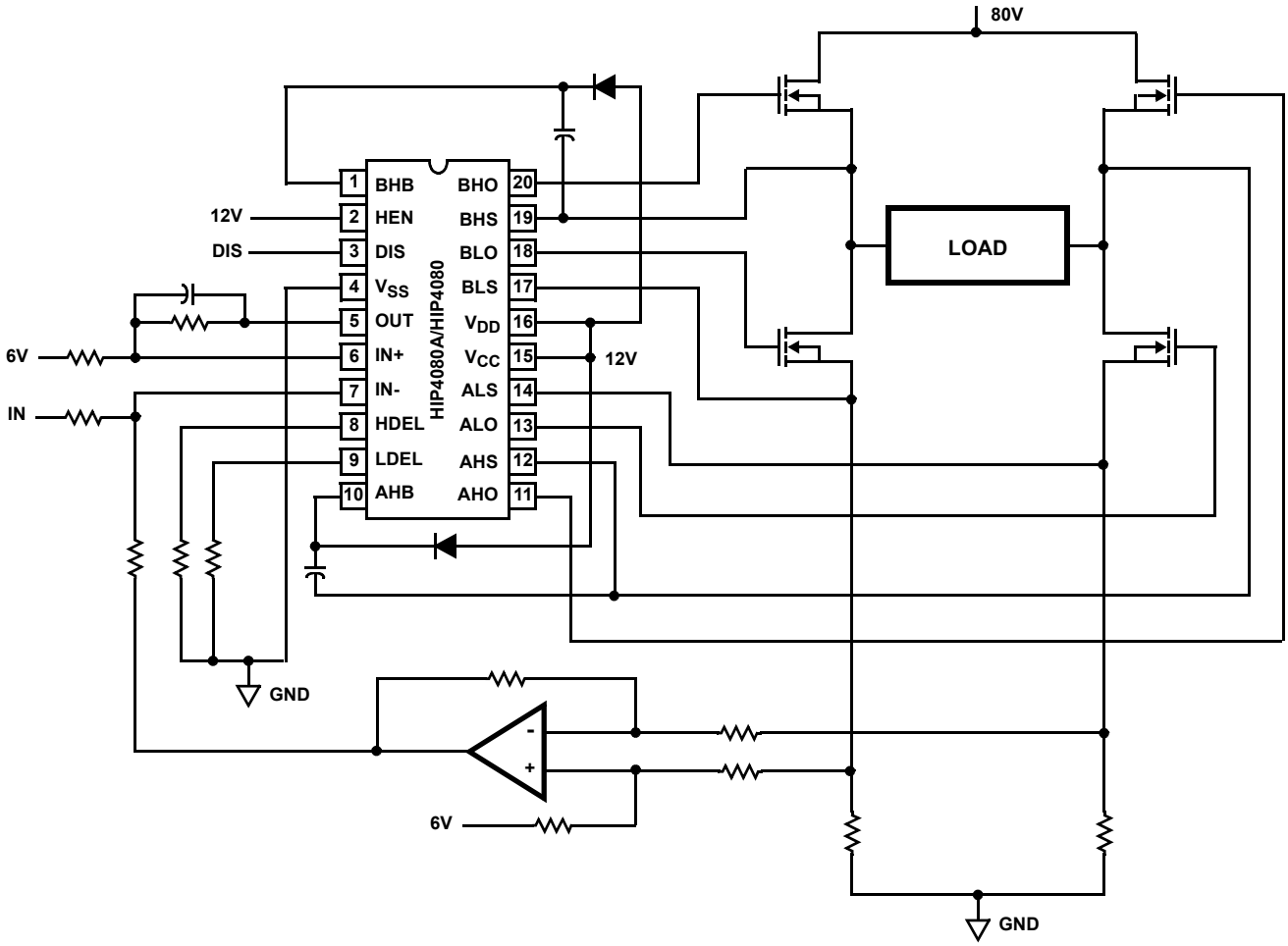
## *Application Block Diagram*




## *Functional Block Diagram* (1/2 HIP4080A)



## *Typical Application (Hysteresis Mode Switching)*



## Absolute Maximum Ratings

Supply Voltage, $V_{DD}$ and $V_{CC}$ . . . . . -0.3V to 16V
Logic I/O Voltages . . . . . -0.3V to $V_{DD}$ +0.3V
Voltage on AHS, BHS . . . -6.0V (Transient) to 80V (25°C to 125°C)
Voltage on AHS, BHS . . . -6.0V (Transient) to 70V (-55°C to 125°C)
Voltage on ALS, BLS . . . . . -2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB . . . . . $V_{AHS, BHS}$ -0.3V to $V_{AHS, BHS}$ +$V_{DD}$
Voltage on ALO, BLO. . . . . $V_{ALS, BLS}$ -0.3V to $V_{CC}$ +0.3V
Voltage on AHO, BHO . . . . . $V_{AHS, BHS}$ -0.3V to $V_{AHB, BHB}$ +0.3V
Input Current, HDEL and LDEL . . . . . -5mA to 0mA
Phase Slew Rate . . . . . 20V/ns
All Voltages relative to $V_{SS}$, unless otherwise specified.

## Operating Conditions

Supply Voltage, $V_{DD}$ and $V_{CC}$. . . . . +9.5V to +15V
Voltage on ALS, BLS . . . . . -1.0V to +1.0V
Voltage on AHB, BHB . . . . . $V_{AHS, BHS}$ +5V to $V_{AHS, BHS}$ +15V
Input Current, HDEL and LDEL . . . . . -500µA to -50µA
Operating Ambient Temperature Range . . . . . -40°C to +85°C

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{JA}$ (°C/W) |
|---|---|
| SOIC Package | 85 |
| PDIP Package | 75 |

Maximum Power Dissipation at +85°C
SOIC Package . . . . . 470mW
PDIP Package . . . . . 530mW
Storage Temperature Range . . . . . -65°C to +150°C
Operating Max. Junction Temperature. . . . . +125°C
Lead Temperature (Soldering 10s) . . . . . +300°C
(For SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

3. $\theta_{JA}$ is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications

$V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J$ = +25°C | | | $T_J$ = - 40°C TO +125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| **SUPPLY CURRENTS AND CHARGE PUMPS** | | | | | | | | |
| $V_{DD}$ Quiescent Current | $I_{DD}$ | IN- = 2.5V, Other Inputs = 0V | 8 | 11 | 14 | 7 | 14 | mA |
| $V_{DD}$ Operating Current | $I_{DDO}$ | Outputs switching f = 500kHz, No Load | 9 | 12 | 15 | 8 | 15 | mA |
| $V_{CC}$ Quiescent Current | $I_{CC}$ | IN- = 2.5V, Other Inputs = 0V, $I_{ALO} = I_{BLO} = 0$ | - | 25 | 80 | - | 100 | µA |
| $V_{CC}$ Operating Current | $I_{CCO}$ | f = 500kHz, No Load | 1 | 1.25 | 2.0 | 0.8 | 3 | mA |
| AHB, BHB Quiescent Current - Qpump Output Current | $I_{AHB}$, $I_{BHB}$ | IN- = 2.5V, Other Inputs = 0V, $I_{AHO} = I_{BHO} = 0$, $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 10V$ | -50 | -25 | -11 | -60 | -10 | µA |
| AHB, BHB Operating Current | $I_{AHBO}$, $I_{BHBO}$ | f = 500kHz, No Load | 0.62 | 1.2 | 1.5 | 0.5 | 1.9 | mA |
| AHS, BHS, AHB, BHB Leakage Current | $I_{HLK}$ | $V_{BHS} = V_{AHS} = 80V$, $V_{AHB} = V_{BHB} = 93V$ | - | 0.02 | 1.0 | - | 10 | µA |
| AHB-AHS, BHB-BHS Qpump Output Voltage | $V_{AHB}$ - $V_{AHS}$ $V_{BHB}$ - $V_{BHS}$ | $I_{AHB} = I_{AHB} = 0$, No Load | 11.5 | 12.6 | 14.0 | 10.5 | 14.5 | V |
| **INPUT COMPARATOR PINS: IN+, IN-, OUT** | | | | | | | | |
| Offset Voltage | $V_{OS}$ | Over Common Mode Voltage Range | -10 | 0 | +10 | -15 | +15 | mV |
| Input Bias Current | $I_{IB}$ | | 0 | 0.5 | 2 | 0 | 4 | µA |
| Input Offset Current | $I_{OS}$ | | -1 | 0 | +1 | -2 | +2 | µA |
| Input Common Mode Voltage Range | CMVR | | 1 | - | $V_{DD}$ -1.5 | 1 | $V_{DD}$ -1.5 | V |

**Electrical Specifications** $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J = +25°C$ | | | $T_J = -40°C$ TO $+125°C$ | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| Voltage Gain | AVOL | | 10 | 25 | - | 10 | - | V/mV |
| OUT High Level Output Voltage | $V_{OH}$ | IN+ > IN-, $I_{OH} = -250\mu A$ | $V_{DD}$ -0.4 | - | - | $V_{DD}$ - 0.5 | - | V |
| OUT Low Level Output Voltage | $V_{OL}$ | IN+ < IN-, $I_{OL} = +250\mu A$ | - | - | 0.4 | - | 0.5 | V |
| Low Level Output Current | $I_{OL}$ | $V_{OUT} = 6V$ | 6.5 | 14 | 19 | 6 | 20 | mA |
| High Level Output Current | $I_{OH}$ | $V_{OUT} = 6V$ | -17 | -10 | -3 | -20 | -2.5 | mA |
| **INPUT PINS: DIS** | | | | | | | | |
| Low Level Input Voltage | $V_{IL}$ | Full Operating Conditions | - | - | 1.0 | - | 0.8 | V |
| High Level Input Voltage | $V_{IH}$ | Full Operating Conditions | 2.5 | - | - | 2.7 | - | V |
| Input Voltage Hysteresis | | | - | 35 | - | - | - | mV |
| Low Level Input Current | $I_{IL}$ | $V_{IN} = 0V$, Full Operating Conditions | -130 | -100 | -75 | -135 | -65 | µA |
| High Level Input Current | $I_{IH}$ | $V_{IN} = 5V$, Full Operating Conditions | -1 | - | +1 | -10 | +10 | µA |
| **INPUT PINS: HEN** | | | | | | | | |
| Low Level Input Voltage | $V_{IL}$ | Full Operating Conditions | - | - | 1.0 | - | 0.8 | V |
| High Level Input Voltage | $V_{IH}$ | Full Operating Conditions | 2.5 | - | - | 2.7 | - | V |
| Input Voltage Hysteresis | | | - | 35 | - | - | - | mV |
| Low Level Input Current | $I_{IL}$ | $V_{IN} = 0V$, Full Operating Conditions | -260 | -200 | -150 | -270 | -130 | µA |
| High Level Input Current | $I_{IH}$ | $V_{IN} = 5V$, Full Operating Conditions | -1 | - | +1 | -10 | +10 | µA |
| **TURN-ON DELAY PINS: LDEL AND HDEL** | | | | | | | | |
| LDEL, HDEL Voltage | $V_{HDEL,}V$ | $I_{HDEL} = I_{LDEL} = -100\mu A$ | 4.9 | 5.1 | 5.3 | 4.8 | 5.4 | V |
| **GATE DRIVER OUTPUT PINS: ALO, BLO, AHO, AND BHO** | | | | | | | | |
| Low Level Output Voltage | $V_{OL}$ | $I_{OUT} = 100mA$ | 0.7 | 0.85 | 1.0 | 0.5 | 1.1 | V |
| High Level Output Voltage | $V_{CC} - V_{OH}$ | $I_{OUT} = -100mA$ | 0.8 | 0.95 | 1.1 | 0.5 | 1.2 | V |
| Peak Pullup Current | $I_O+$ | $V_{OUT} = 0V$ | 1.7 | 2.6 | 3.8 | 1.4 | 4.1 | A |
| Peak Pulldown Current | $I_O-$ | $V_{OUT} = 12V$ | 1.7 | 2.4 | 3.3 | 1.3 | 3.6 | A |
| Under Voltage, Rising Threshold | UV+ | | 8.1 | 8.8 | 9.4 | 8.0 | 9.5 | V |
| Under Voltage, Falling Threshold | UV- | | 7.6 | 8.3 | 8.9 | 7.5 | 9.0 | V |
| Under Voltage, Hysteresis | HYS | | 0.25 | 0.4 | 0.65 | 0.2 | 0.7 | V |

**Switching Specifications** $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 10K$, $C_L = 1000pF$, and $T_A = +25°C$, Unless Otherwise Specified

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J = +25°C$ | | | $T_J = -40°C$ TO $+125°C$ | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| Lower Turn-off Propagation Delay (IN+/IN- to ALO/BLO) | $T_{LPHL}$ | | - | 40 | 70 | - | 90 | ns |
| Upper Turn-off Propagation Delay (IN+/IN- to AHO/BHO) | $T_{HPHL}$ | | - | 50 | 80 | - | 110 | ns |
| Lower Turn-on Propagation Delay (IN+/IN- to ALO/BLO) | $T_{LPLH}$ | | - | 40 | 70 | - | 90 | ns |
| Upper Turn-on Propagation Delay (IN+/IN- to AHO/BHO) | $T_{HPLH}$ | | - | 70 | 110 | - | 140 | ns |
| Rise Time | $T_R$ | | - | 10 | 25 | - | 35 | ns |
| Fall Time | $T_F$ | | - | 10 | 25 | - | 35 | ns |
| Turn-on Input Pulse Width | $T_{PWIN-ON}$ | | 50 | - | - | 50 | - | ns |
| Turn-off Input Pulse Width | $T_{PWIN-OFF}$ | | 40 | - | - | 40 | - | ns |
| Disable Turn-off Propagation Delay (DIS - Lower Outputs) | $T_{DISLOW}$ | | - | 45 | 75 | - | 95 | ns |
| Disable Turn-off Propagation Delay (DIS - Upper Outputs) | $T_{DISHIGH}$ | | - | 55 | 85 | - | 105 | ns |
| Disable to Lower Turn-on Propagation Delay (DIS - ALO and BLO) | $T_{DLPLH}$ | | - | 45 | 70 | - | 90 | ns |
| Refresh Pulse Width (ALO and BLO) | $T_{REF-PW}$ | | 240 | 380 | 500 | 200 | 600 | ns |
| Disable to Upper Enable (DIS - AHO and BHO) | $T_{UEN}$ | | - | 480 | 630 | - | 750 | ns |
| HEN-AHO, BHO Turn-off, Propagation Delay | $T_{HEN-PHL}$ | $R_{HDEL} = R_{LDEL} = 10K$ | - | 40 | 70 | - | 90 | ns |
| HEN-AHO, BHO Turn-on, Propagation Delay | $T_{HEN-PLH}$ | $R_{HDEL} = R_{LDEL} = 10K$ | - | 60 | 90 | - | 110 | ns |

**TRUTH TABLE**

| INPUT | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| IN+ > IN- | HEN | U/V | DIS | ALO | AHO | BLO | BHO |
| X | X | X | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| X | X | 1 | X | 0 | 0 | 0 | 0 |

## Pin Descriptions

| PIN NUMBER | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | BHB | B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V. |
| 2 | HEN | High-side Enable input. Logic level input that when low overrides IN+/IN- (Pins 6 and 7) to put AHO and BHO drivers (Pins 11 and 20) in low output state. When HEN is high AHO and BHO are controlled by IN+/IN- inputs. The pin can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$). |
| 3 | DIS | DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 15V (no greater than $V_{DD}$). |
| 4 | $V_{SS}$ | Chip negative supply, generally will be ground. |
| 5 | OUT | OUTput of the input control comparator. This output can be used for feedback and hysteresis. |
| 6 | IN+ | Noninverting input of control comparator. If IN+ is greater than IN- (Pin 7) then ALO and BHO are low level outputs and BLO and AHO are high level outputs. If IN+ is less than IN- then ALO and BHO are high level outputs and BLO and AHO are low level outputs. DIS (Pin 3) high level will override IN+/IN- control for all outputs. HEN (Pin 2) low level will override IN+/IN- control of AHO and BHO. When switching in four quadrant mode, dead time in a half bridge leg is controlled by HDEL and LDEL (Pins 8 and 9). |
| 7 | IN- | Inverting input of control comparator. See IN+ (Pin 6) description. |
| 8 | HDEL | High-side turn-on DELay. Connect resistor from this pin to $V_{SS}$ to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V. |
| 9 | LDEL | Low-side turn-on DELay. Connect resistor from this pin to $V_{SS}$ to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V. |
| 10 | AHB | A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V. |
| 11 | AHO | A High-side Output. Connect to gate of A High-side power MOSFET. |
| 12 | AHS | A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin. |
| 13 | ALO | A Low-side Output. Connect to gate of A Low-side power MOSFET. |
| 14 | ALS | A Low-side Source connection. Connect to source of A Low-side power MOSFET. |
| 15 | $V_{CC}$ | Positive supply to gate drivers. Must be same potential as $V_{DD}$ (Pin 16). Connect to anodes of two bootstrap diodes. |
| 16 | $V_{DD}$ | Positive supply to lower gate drivers. Must be same potential as $V_{CC}$ (Pin 15). De-couple this pin to $V_{SS}$ (Pin 4). |
| 17 | BLS | B Low-side Source connection. Connect to source of B Low-side power MOSFET. |
| 18 | BLO | B Low-side Output. Connect to gate of B Low-side power MOSFET. |
| 19 | BHS | B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin. |
| 20 | BHO | B High-side Output. Connect to gate of B High-side power MOSFET. |

## *Timing Diagrams*

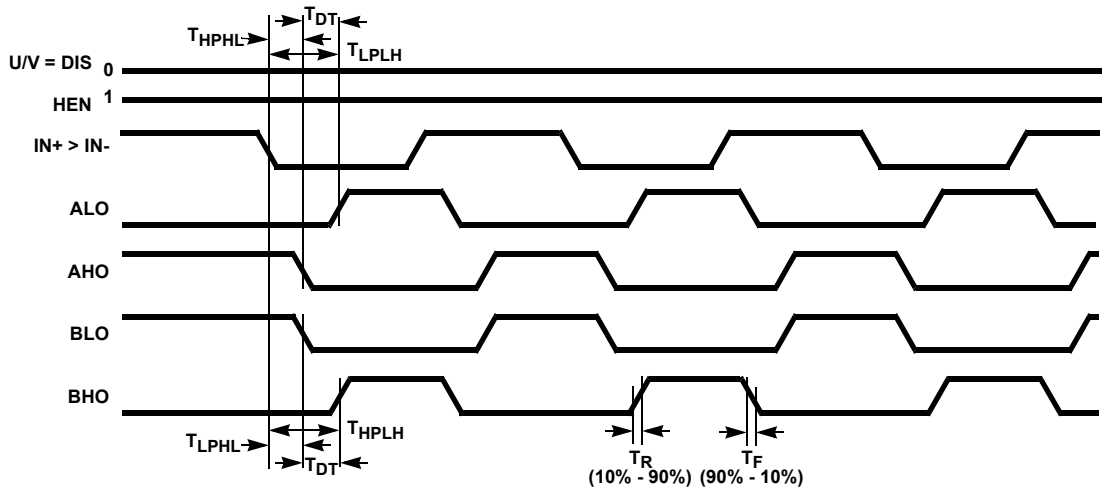



FIGURE 1. BISTATE MODE

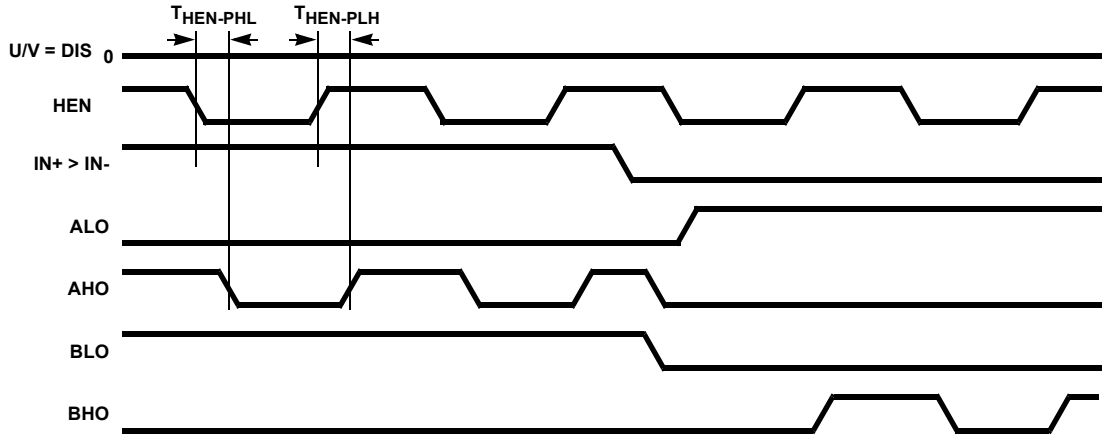



FIGURE 2. HIGH SIDE CHOP MODE

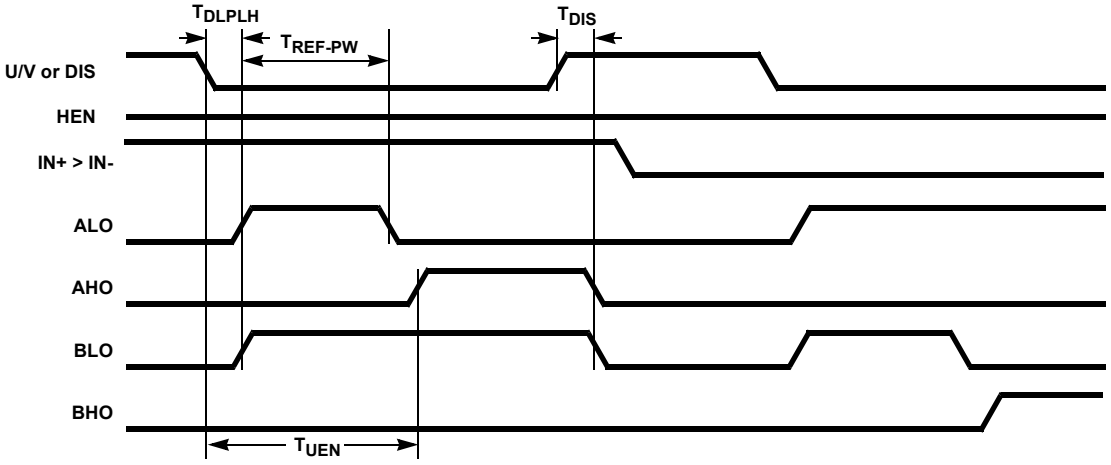



FIGURE 3. DISABLE FUNCTION

## *Typical Performance Curves* $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified

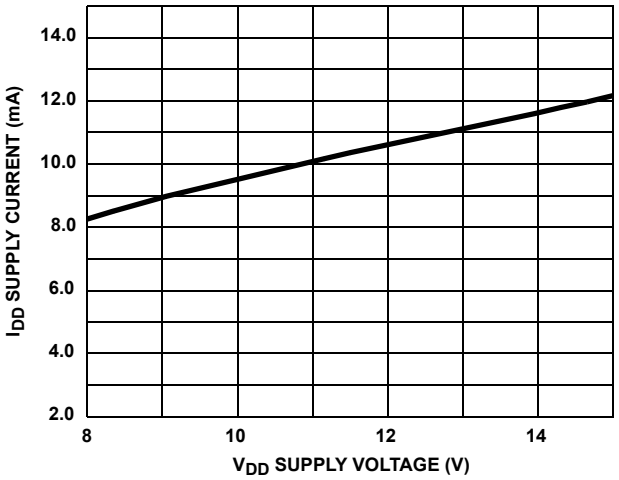



FIGURE 4. QUIESCENT $I_{DD}$ SUPPLY CURRENT vs $V_{DD}$ SUPPLY VOLTAGE

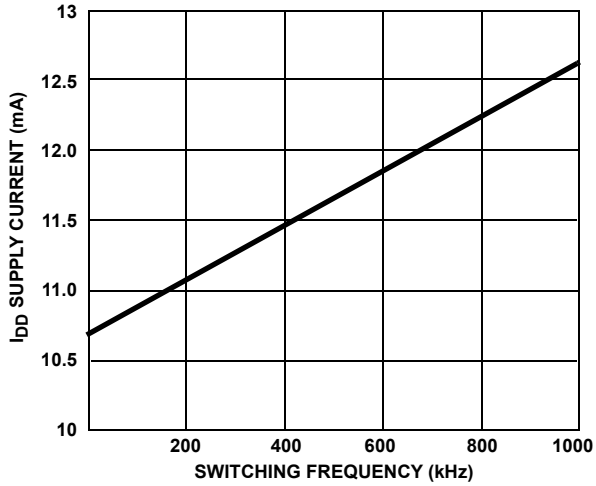



FIGURE 5. $I_{DDO}$ NO-LOAD $I_{DD}$ SUPPLY CURRENT vs FREQUENCY (kHz)

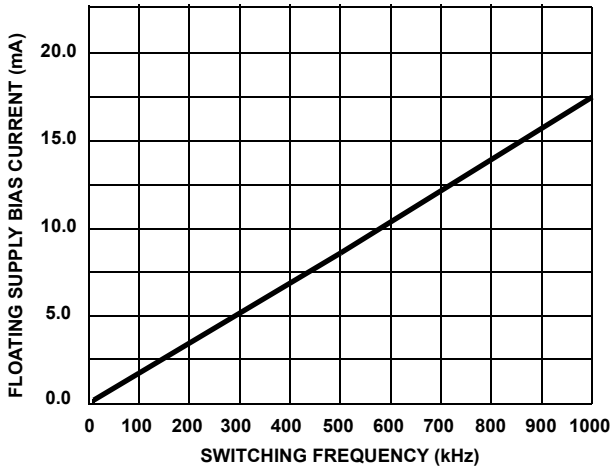



FIGURE 6. SIDE A, B FLOATING SUPPLY BIAS CURRENT vs FREQUENCY (LOAD = 1000pF)

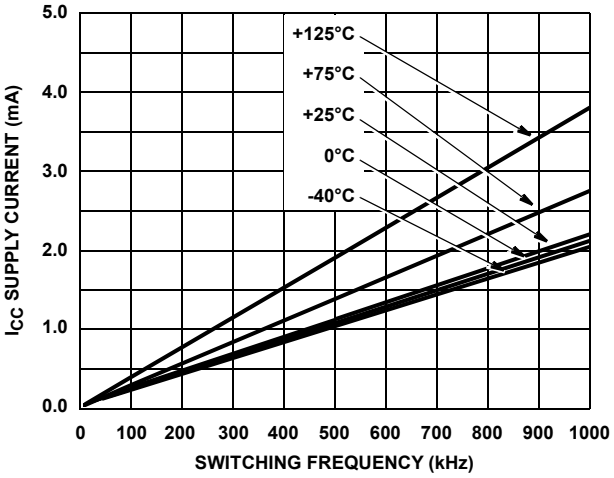



FIGURE 7. $I_{CCO}$, NO-LOAD $I_{CC}$ SUPPLY CURRENT vs FREQUENCY (kHz) TEMPERATURE

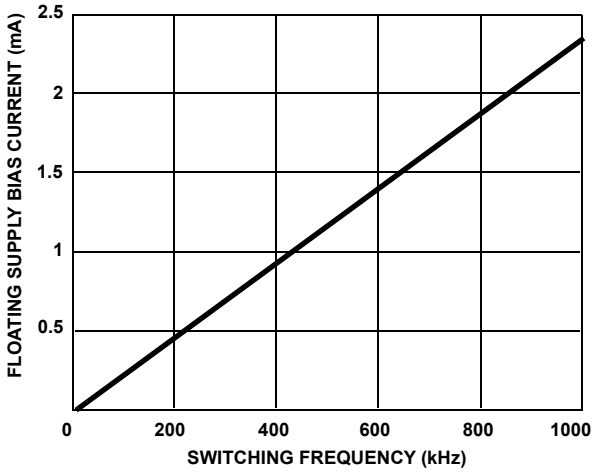



FIGURE 8. $I_{AHB}$, $I_{BHB}$ NO-LOAD FLOATING SUPPLY BIAS CURRENT vs FREQUENCY

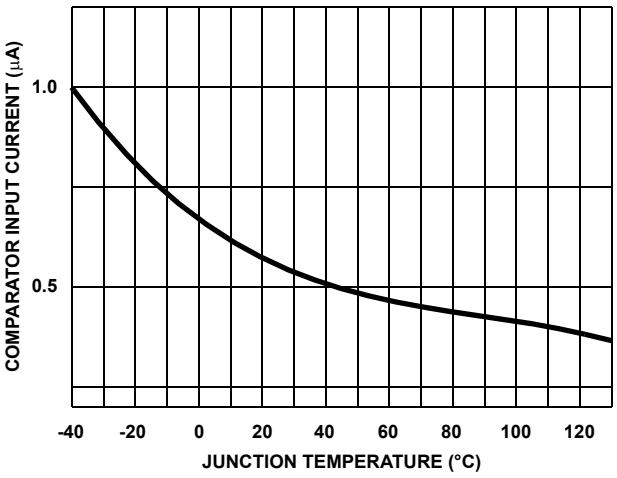



FIGURE 9. COMPARATOR INPUT CURRENT $I_L$ vs TEMPERATURE AT $V_{CM} = 5V$

## *Typical Performance Curves* $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 100K, and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

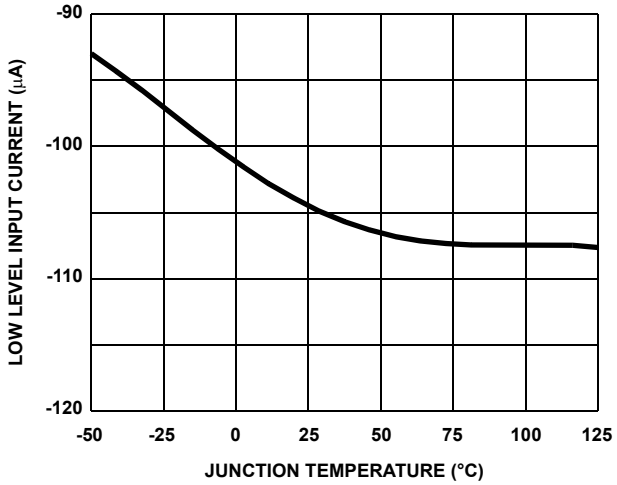



**FIGURE 10. DIS LOW LEVEL INPUT CURRENT $I_{IL}$ vs TEMPERATURE**

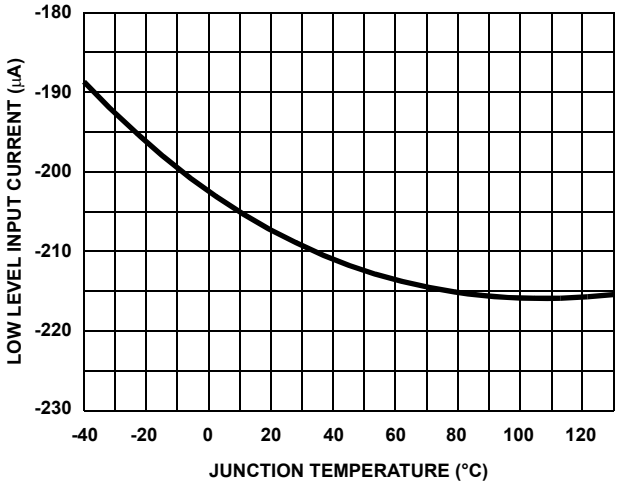



**FIGURE 11. HEN LOW LEVEL INPUT CURRENT $I_{IL}$ vs TEMPERATURE**

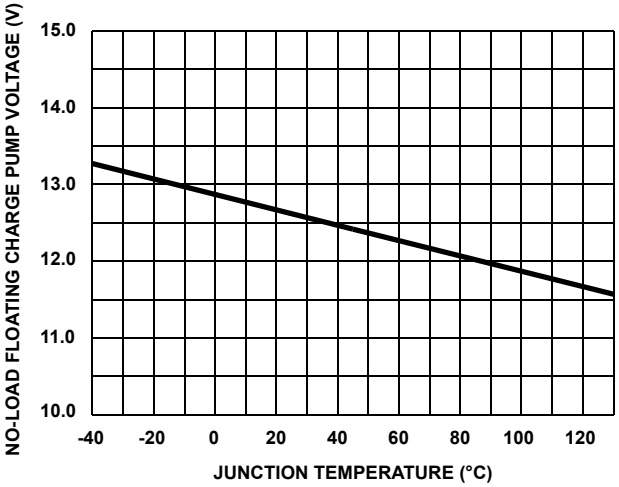



**FIGURE 12. AHB - AHS, BHB - BHS NO-LOAD CHARGE PUMP VOLTAGE vs TEMPERATURE**

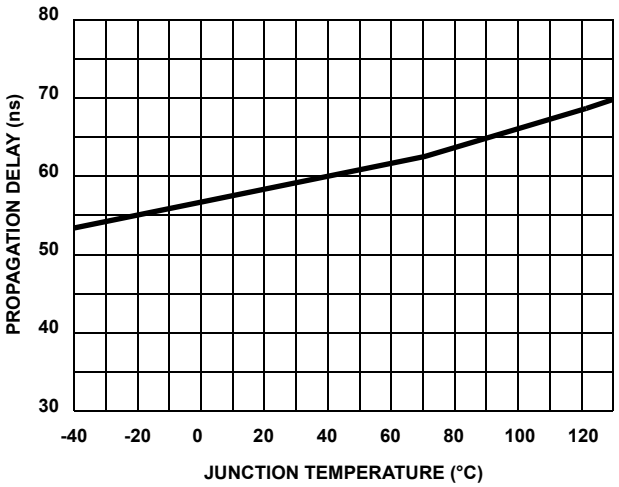



**FIGURE 13. UPPER DISABLE TURN-OFF PROPAGATION DELAY $T_{DISHIGH}$ vs TEMPERATURE**

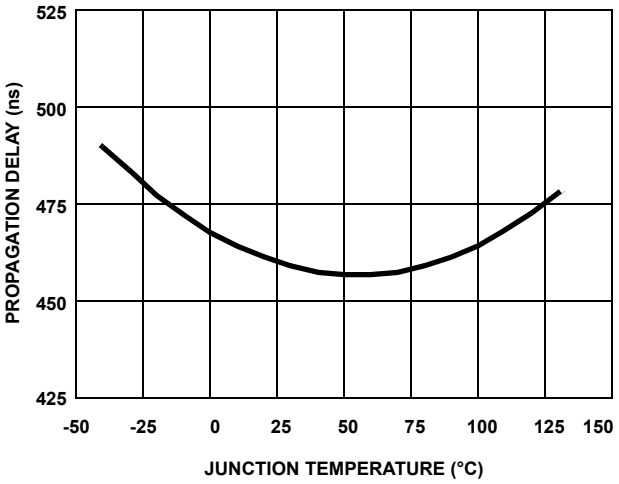



**FIGURE 14. DISABLE TO UPPER ENABLE $T_{UEN}$ PROPAGATION DELAY vs TEMPERATURE**

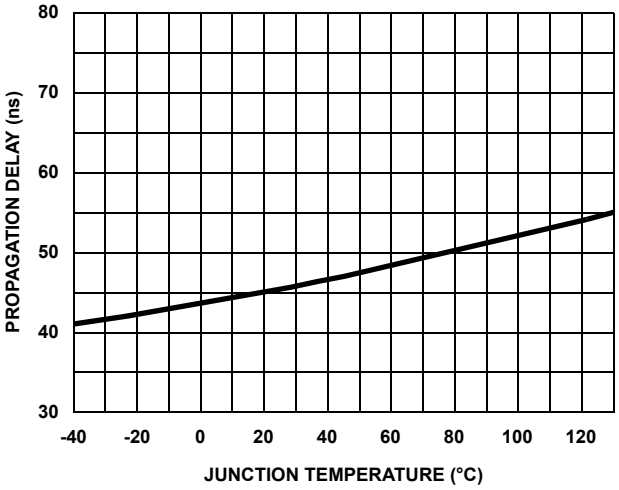



**FIGURE 15. LOWER DISABLE TURN-OFF PROPAGATION DELAY $T_{DISLOW}$ vs TEMPERATURE**

## *Typical Performance Curves* $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} =$ 10K, and $T_A = +25°C$, Unless Otherwise Specified

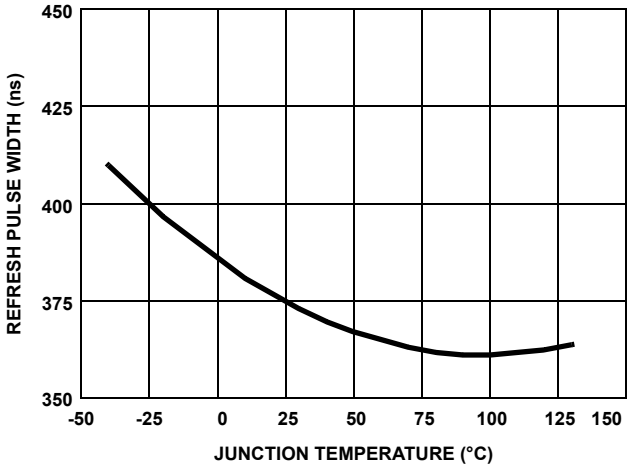



FIGURE 16. $T_{REF-PW}$ REFRESH PULSE WIDTH vs TEMPERATURE

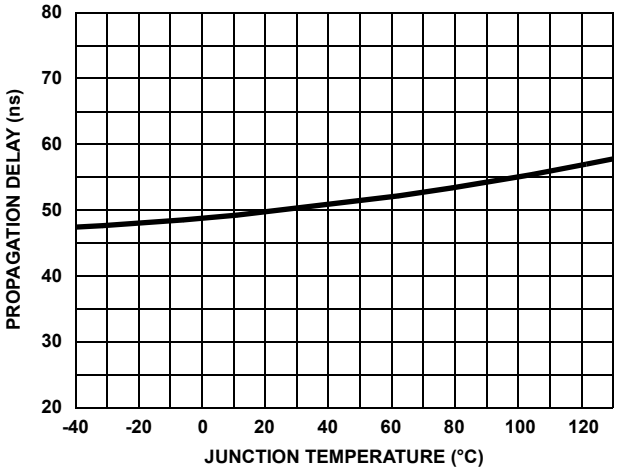



FIGURE 17. DISABLE TO LOWER ENABLE TDLPLH PROPAGATION DELAY vs TEMPERATURE

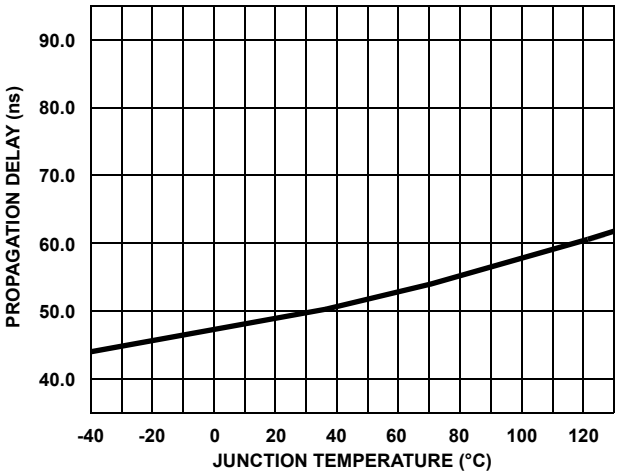



FIGURE 18. UPPER TURN-OFF PROPAGATION DELAY $T_{HPHL}$ vs TEMPERATURE

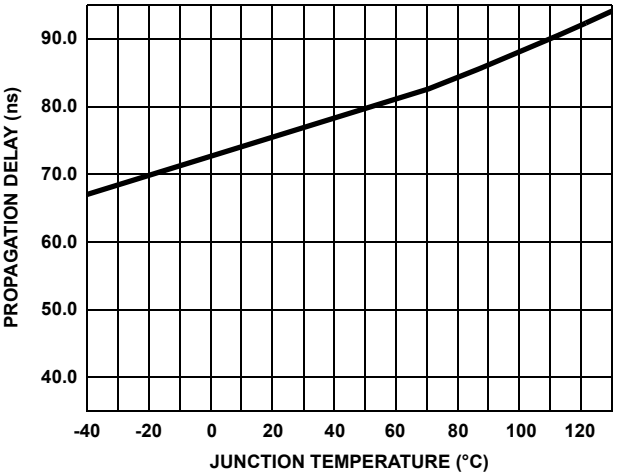



FIGURE 19. UPPER TURN-ON PROPAGATION DELAY THPLH vs TEMPERATURE

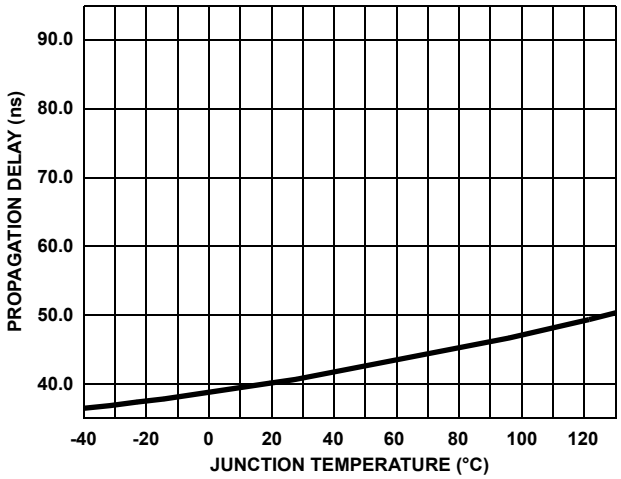



FIGURE 20. LOWER TURN-OFF PROPAGATION DELAY $T_{LPHL}$ vs TEMPERATURE

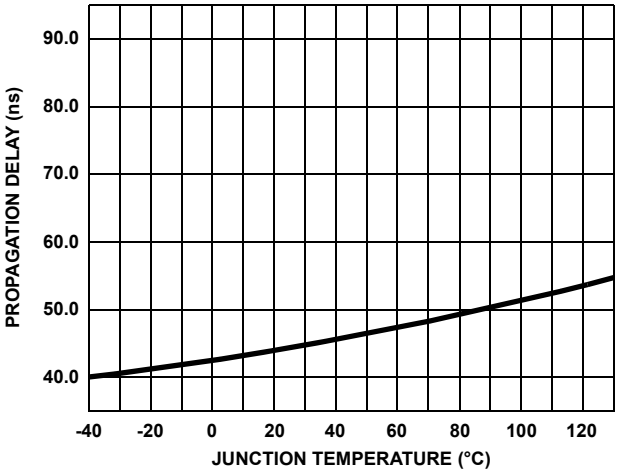



FIGURE 21. LOWER TURN-ON PROPAGATION DELAY $T_{LPLH}$ vs TEMPERATURE

## *Typical Performance Curves* $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified

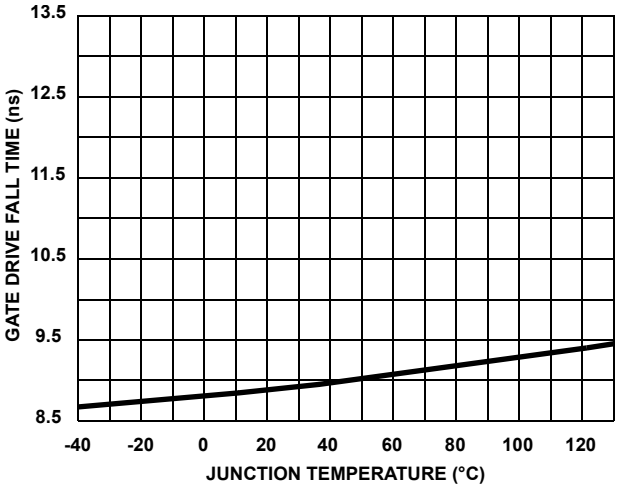



FIGURE 22. GATE DRIVE FALL TIME $T_F$ vs TEMPERATURE

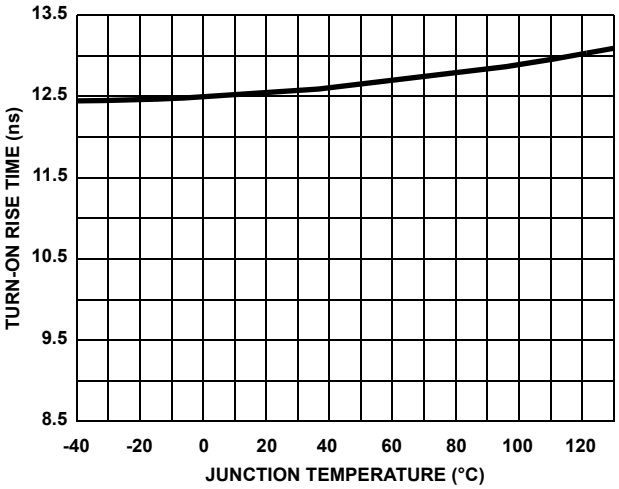



FIGURE 23. GATE DRIVE RISE TIME $T_R$ vs TEMPERATURE

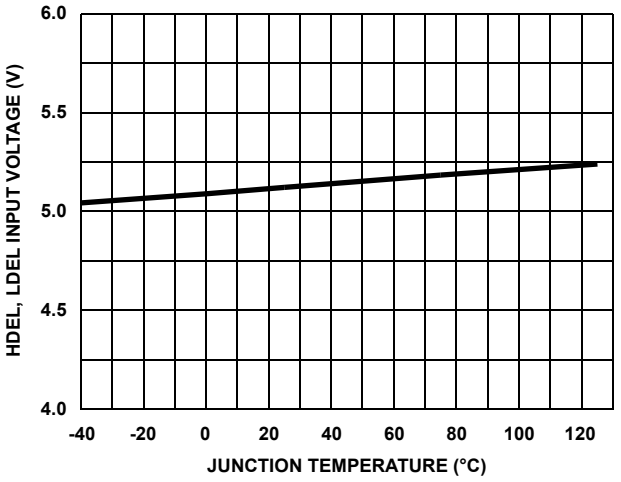



FIGURE 24. $V_{LDEL}$, $V_{HDEL}$ VOLTAGE vs TEMPERATURE

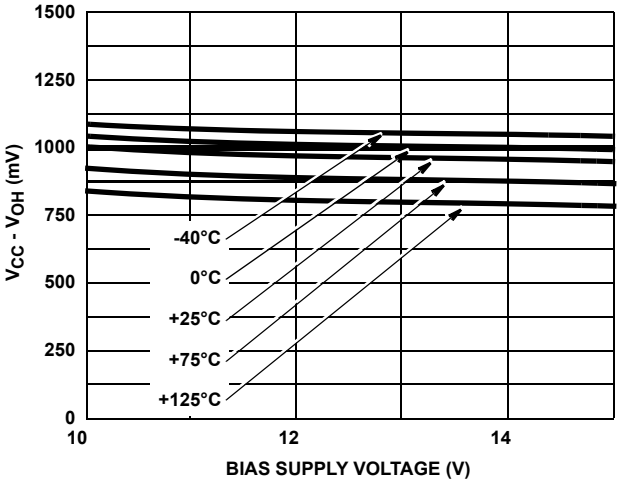



FIGURE 25. HIGH LEVEL OUTPUT VOLTAGE, $V_{CC} - V_{OH}$ vs BIAS SUPPLY AND TEMPERATURE AT 100µA

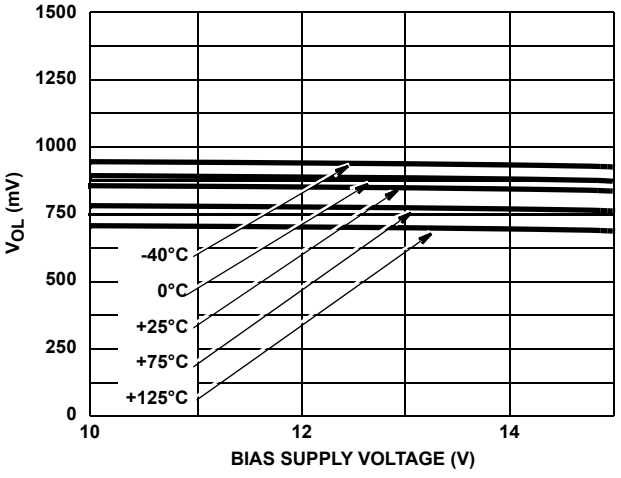



FIGURE 26. LOW LEVEL OUTPUT VOLTAGE $V_{OL}$ vs BIAS SUPPLY AND TEMPERATURE AT 100µA

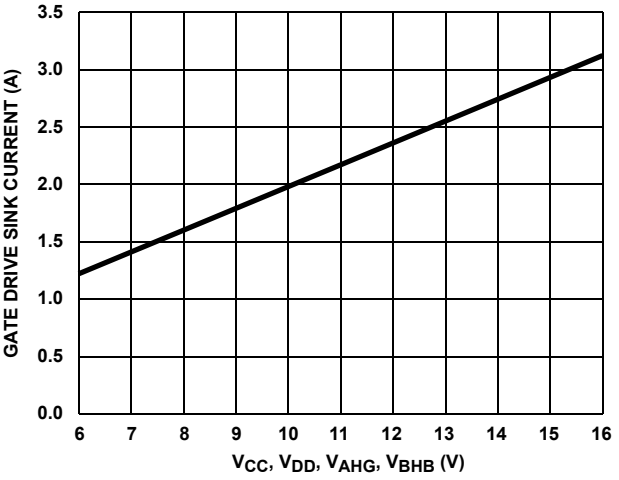



FIGURE 27. PEAK PULLDOWN CURRENT $I_O$. BIAS SUPPLY VOLTAGE

## *Typical Performance Curves* $V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V$, $V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V$, $R_{HDEL} = R_{LDEL} = 100K$, and $T_A = +25°C$, Unless Otherwise Specified **(Continued)**

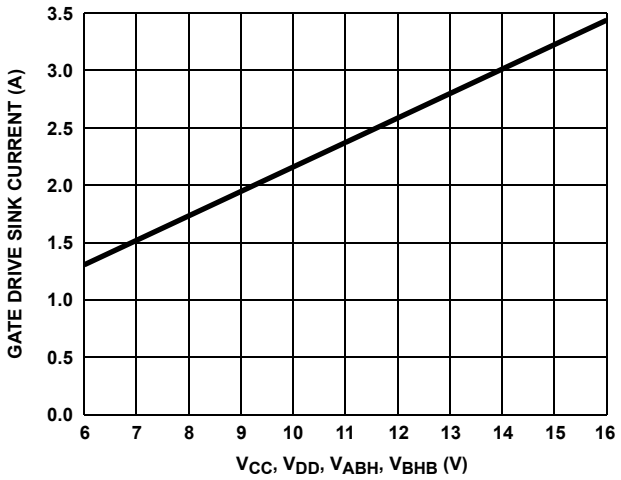



FIGURE 28. PEAK PULLUP CURRENT $I_{O+}$ vs SUPPLY VOLTAGE

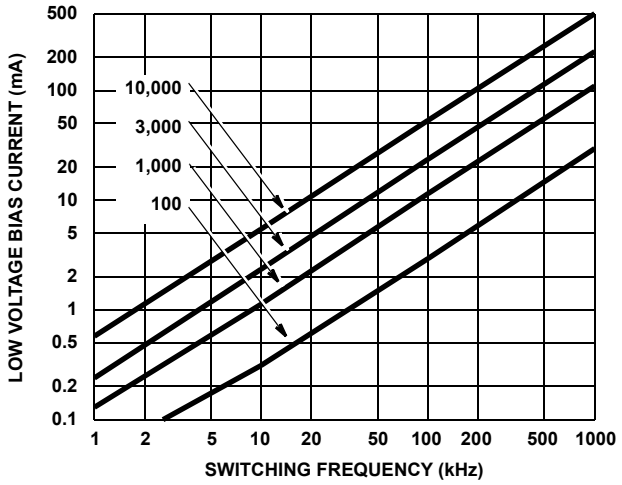



FIGURE 29. LOW VOLTAGE BIAS CURRENT $I_{DD}$ AND $I_{CC}$ (LESS QUIESCENT COMPONENT) vs FREQUENCY AND GATE LOAD CAPACITANCE

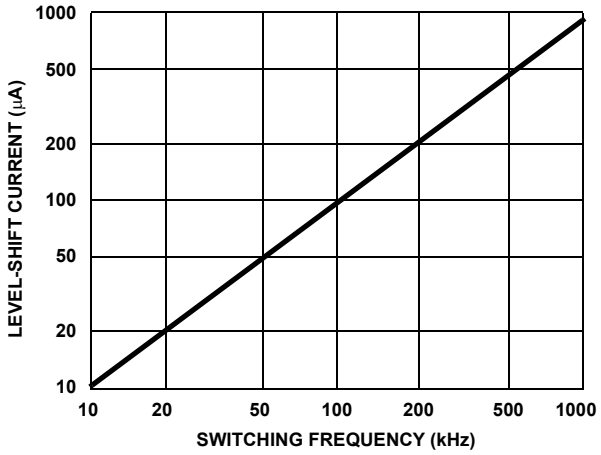



FIGURE 30. HIGH VOLTAGE LEVEL-SHIFT CURRENT vs FREQUENCY AND BUS VOLTAGE

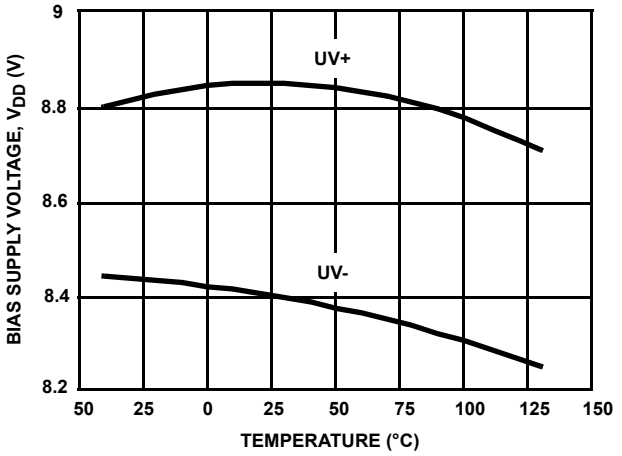



FIGURE 31. UNDERVOLTAGE LOCKOUT vs TEMPERATURE

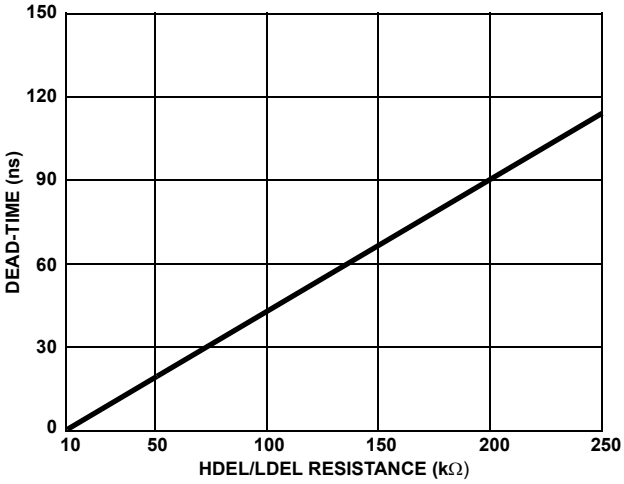
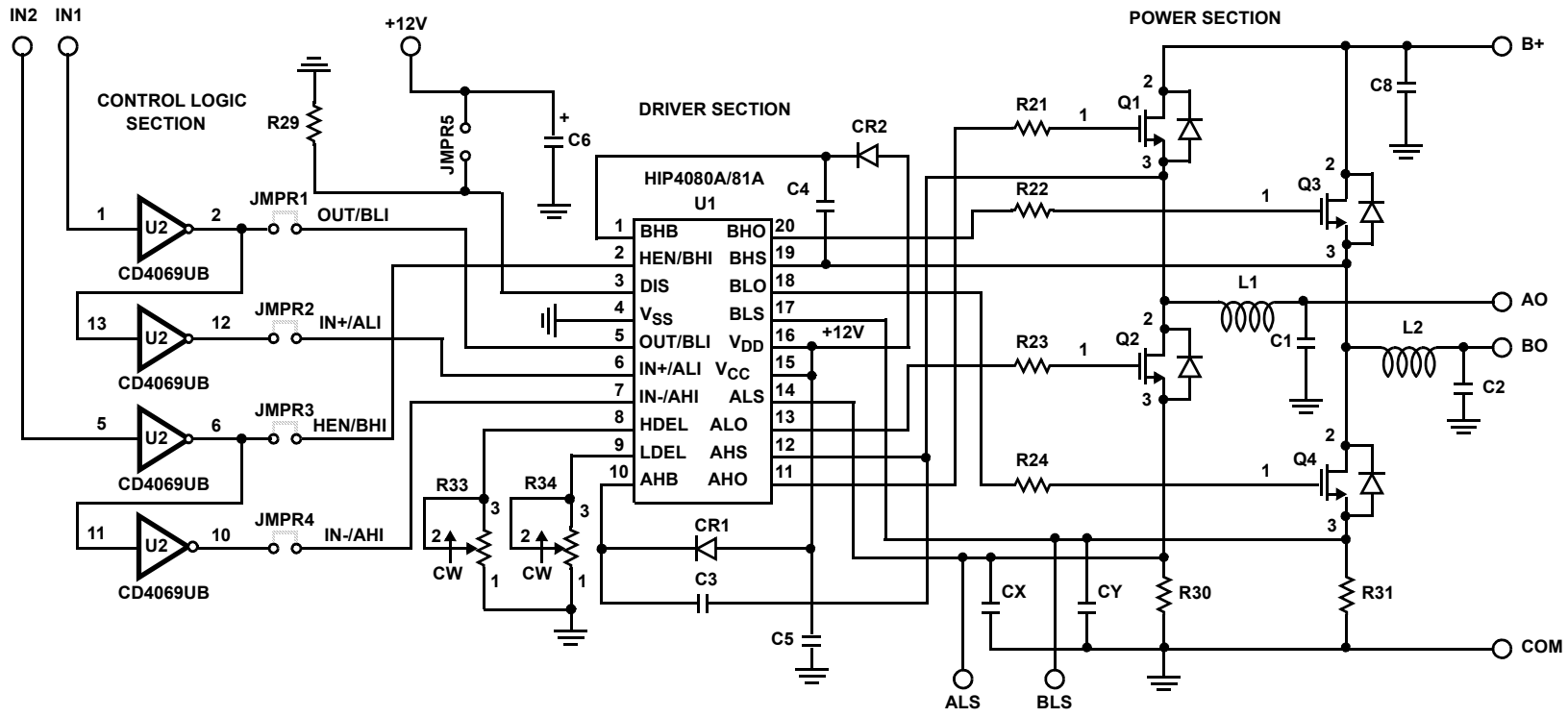



FIGURE 32. MINIMUM DEAD-TIME vs DEL RESISTANCE




NOTES:

1. DEVICE CD4069UB PIN 7 = COM. PIN 14 = +12V.
2. COMPONENTS L1, L2, C1, C2, CX, CY, R30, R31, ARE NOT SUPPLIED. REFER TO APPLICATION NOTE FOR HELP IN DETERMINING JMPR1 - JMPR4 JUMPER LOCATIONS.

FIGURE 33. HIP4080A EVALUATION PC BOARD SCHEMATIC

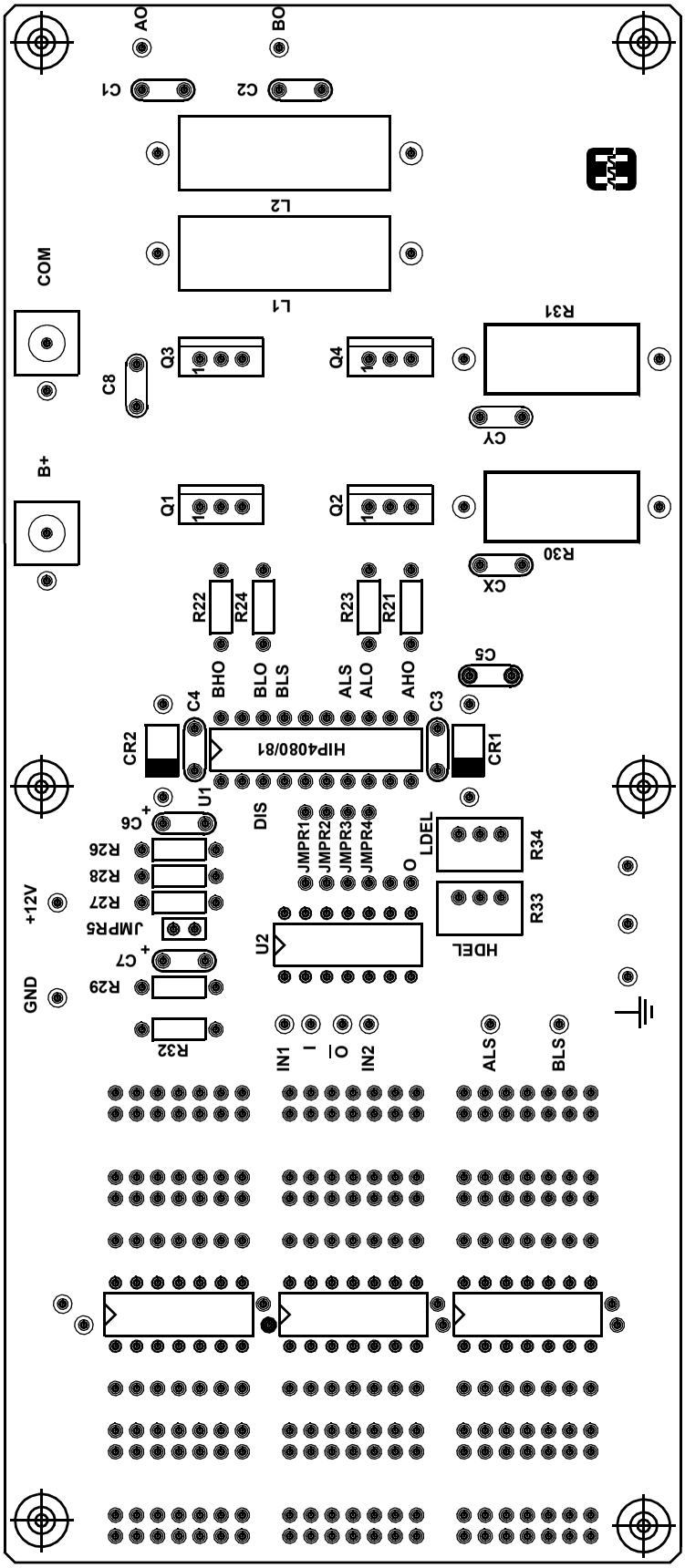


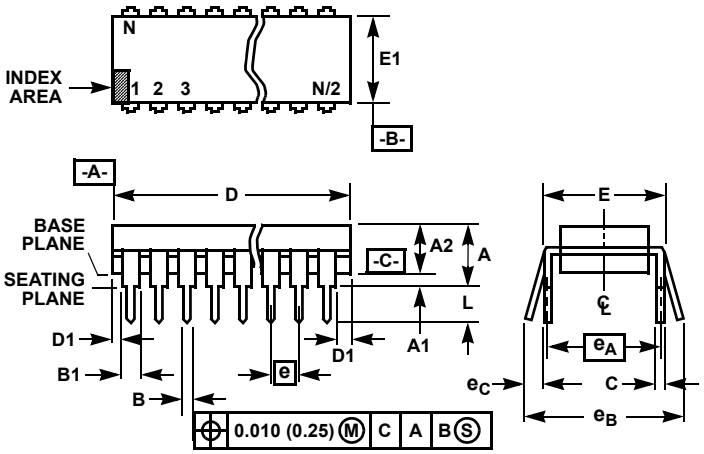

FIGURE 33. HIP4080A EVALUATION BOARD SILKSCREEN

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| Dec 11, 2019 | FN3658.8 | Removed retired parts.<br>Added Revision History section.<br>Updated POD M20.3 to the latest revision. Changes are as follows:<br>Rev 2. - Removed “u” symbol from drawing (overlaps the “a” on Side View).<br>Rev 3. - Top View:<br>Corrected "7.50 BSC" to "7.60/7.40" (no change from rev 2; error was introduced in conversion)<br>Changed "10.30 BSC" to "10.65/10.00" (no change from rev 2; error was introduced in conversion)<br>Side View:<br>Changed "12.80 BSC" to "13.00/12.60" (no change from rev 2; error was introduced in conversion)<br>Changed "2.65 max" to "2.65/2.35" (no change from rev 2; error was introduced in conversion)<br>Changed Note 1 from "ANSI Y14.5M-1982." to "ASME Y14.5M-1994"<br>Updated to new POD format by moving dimensions from table onto drawing and adding land pattern<br>Updated disclaimer. |

## *Package Outline Drawings*




NOTES:

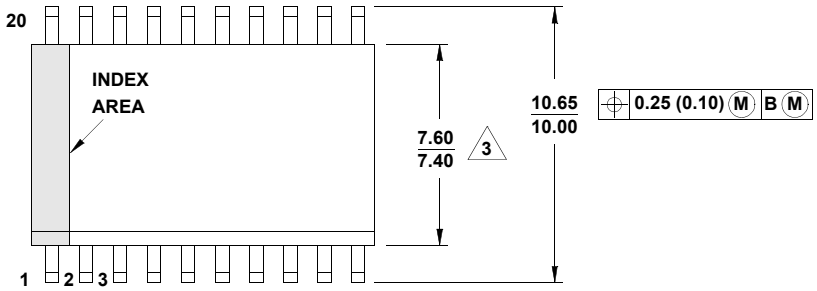
3. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
4. Dimensioning and tolerancing per ANSI Y14.5M-1982.
5. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
6. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
7. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
8. E and $e_A$ are measured with the leads constrained to be perpendicular to datum -C-.
9. $e_B$ and $e_C$ are measured at the lead tips with the leads unconstrained. $e_C$ must be zero or greater.
10. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
11. N is the maximum number of terminal positions.
12. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE (PDIP)

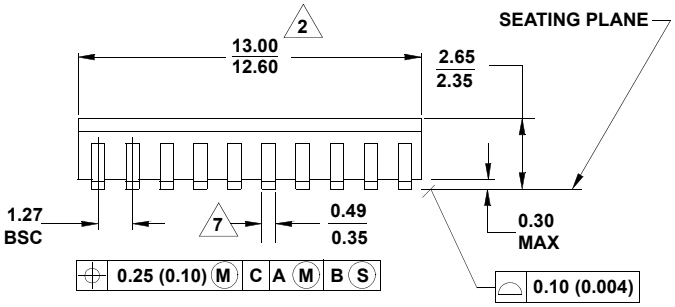
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.55 | 1.77 | 8 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.980 | 1.060 | 24.89 | 26.9 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| $e_A$ | 0.300 BSC | | 7.62 BSC | | 6 |
| $e_B$ | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 20 | | 20 | | 9 |

Rev. 0 12/93

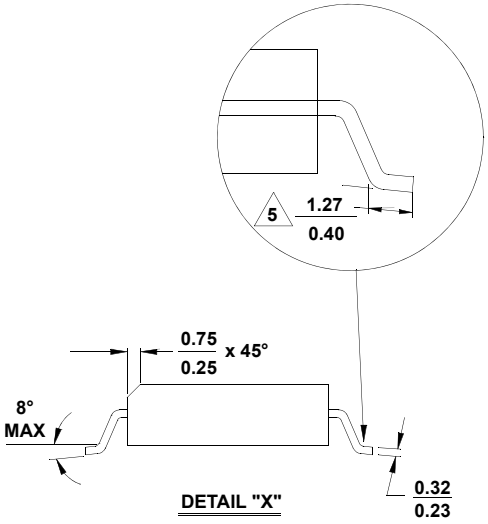
**M20.3**
**20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)**
**Rev 3, 2/11**



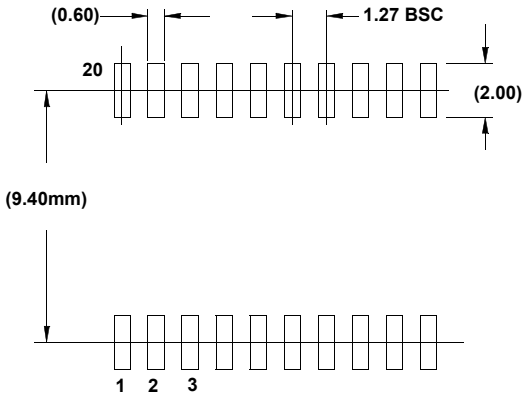

TOP VIEW




SIDE VIEW




DETAIL "X"




TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Dimension does not include interlead lash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Dimension is the length of terminal for soldering to a substrate.
6. Terminal numbers are shown for reference only.
7. The lead width as measured 0.36mm (0.14 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
8. Controlling dimension: MILLIMETER.
9. Dimensions in ( ) for reference only.
10. JEDEC reference drawing number: MS-013-AC.

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(Rev.4.0-1 November 2017)

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Стандарт Электрон Связь

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