

## 2.7V 10-Bit A/D Converter with SPI™ Serial Interface

### Features

- 10-bit resolution
- $\pm 1$  LSB max DNL
- $\pm 1$  LSB max INL
- On-chip sample and hold
- SPI™ serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 200 kps sampling rate at 5V
- 75 kps sampling rate at 2.7V
- Low power CMOS technology
  - 5 nA typical standby current, 2  $\mu$ A max
  - 500  $\mu$ A max active current at 5V
- Industrial temp range: -40°C to +85°C
- 8-pin PDIP, SOIC, MSOP and TSSOP packages

### Applications

- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

### Description

The Microchip Technology Inc. MCP3001 is a successive approximation 10-bit A/D converter (ADC) with on-board sample and hold circuitry. The device provides a single pseudo-differential input. Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) are both specified at  $\pm 1$  LSB max. Communication with the device is done using a simple serial interface compatible with the SPI protocol. The device is capable of sample rates up to 200 kps at a clock rate of 2.8 MHz. The MCP3001 operates over a broad voltage range (2.7V - 5.5V). Low current design permits operation with a typical standby current of only 5 nA and a typical active current of 400  $\mu$ A. The device is offered in 8-pin PDIP, MSOP, TSSOP and 150 mil SOIC packages.

### Package Types

#### PDIP, MSOP, SOIC, TSSOP

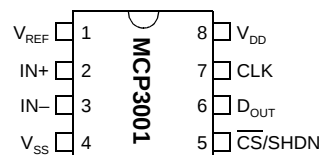
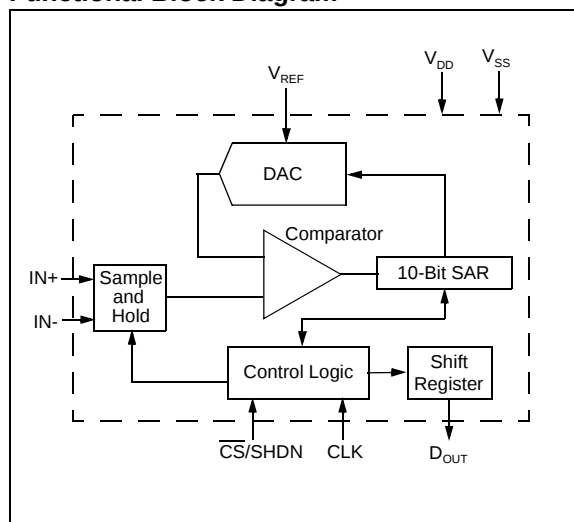


Illustration not to scale

### Functional Block Diagram



# MCP3001

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Maximum Ratings\*

$V_{DD}$  ..... 7.0V

All inputs and outputs w.r.t.  $V_{SS}$  ..... -0.6V to  $V_{DD}$  +0.6V

Storage temperature ..... -65°C to +150°C

Ambient temp. with power applied ..... -65°C to +125°C

ESD protection on all pins (HBM)..... > 4kV

\*Notice: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## PIN FUNCTION TABLE

| Name                 | Function                   |
|----------------------|----------------------------|
| $V_{DD}$             | +2.7V to 5.5V Power Supply |
| $V_{SS}$             | Ground                     |
| IN+                  | Positive Analog Input      |
| IN-                  | Negative Analog Input      |
| CLK                  | Serial Clock               |
| $D_{OUT}$            | Serial Data Out            |
| $\overline{CS}/SHDN$ | Chip Select/Shutdown Input |
| $V_{REF}$            | Reference Voltage Input    |

## ELECTRICAL CHARACTERISTICS

All parameters apply at  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $V_{REF} = 5V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $f_{SAMPLE} = 200$  kps and  $f_{CLK} = 14 * f_{SAMPLE}$ , unless otherwise noted. Typical values apply for  $V_{DD} = 5V$ ,  $T_{AMB} = 25^{\circ}C$ , unless otherwise noted.

| Parameter                              | Sym          | Min  | Typ         | Max       | Units              | Conditions                                           |
|----------------------------------------|--------------|------|-------------|-----------|--------------------|------------------------------------------------------|
| <b>Conversion Rate:</b>                |              |      |             |           |                    |                                                      |
| Conversion Time                        | $t_{CONV}$   | —    | —           | 10        | clock cycles       |                                                      |
| Analog Input Sample Time               | $t_{SAMPLE}$ | 1.5  |             |           | clock cycles       |                                                      |
| Throughput Rate                        | $f_{SAMPLE}$ | —    | —           | 200<br>75 | kps<br>kps         | $V_{DD} = V_{REF} = 5V$<br>$V_{DD} = V_{REF} = 2.7V$ |
| <b>DC Accuracy:</b>                    |              |      |             |           |                    |                                                      |
| Resolution                             |              | 10   |             |           | bits               |                                                      |
| Integral Nonlinearity                  | INL          | —    | $\pm 0.5$   | $\pm 1$   | LSB                |                                                      |
| Differential Nonlinearity              | DNL          | —    | $\pm 0.25$  | $\pm 1$   | LSB                | No missing codes over temperature                    |
| Offset Error                           |              | —    | —           | $\pm 1.5$ | LSB                |                                                      |
| Gain Error                             |              | —    | —           | $\pm 1$   | LSB                |                                                      |
| <b>Dynamic Performance:</b>            |              |      |             |           |                    |                                                      |
| Total Harmonic Distortion              | THD          | —    | -76         | —         | dB                 | $V_{IN} = 0.1V$ to $4.9V$ @1 kHz                     |
| Signal to Noise and Distortion (SINAD) | SINAD        | —    | 61          | —         | dB                 | $V_{IN} = 0.1V$ to $4.9V$ @1 kHz                     |
| Spurious Free Dynamic Range            | SFDR         | —    | 80          | —         | dB                 | $V_{IN} = 0.1V$ to $4.9V$ @1 kHz                     |
| <b>Reference Input:</b>                |              |      |             |           |                    |                                                      |
| Voltage Range                          | $V_{REF}$    | 0.25 | —           | $V_{DD}$  | V                  | <b>Note 2</b>                                        |
| Current Drain                          | $I_{REF}$    | —    | 90<br>0.001 | 150<br>3  | $\mu A$<br>$\mu A$ | $\overline{CS} = V_{DD} = 5V$                        |

**Note 1:** This parameter is guaranteed by characterization and not 100% tested.

**2:** See graph that relates linearity performance to  $V_{REF}$  level.

**3:** Because the sample cap will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

All parameters apply at  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $V_{REF} = 5V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $f_{SAMPLE} = 200$  ksp/s and  $f_{CLK} = 14 \cdot f_{SAMPLE}$ , unless otherwise noted. Typical values apply for  $V_{DD} = 5V$ ,  $T_{AMB} = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                     | Sym               | Min             | Typ   | Max             | Units         | Conditions                                                        |
|-----------------------------------------------|-------------------|-----------------|-------|-----------------|---------------|-------------------------------------------------------------------|
| <b>Temperature Ranges:</b>                    |                   |                 |       |                 |               |                                                                   |
| Specified Temperature Range                   | $T_A$             | -40             | —     | +85             | $^{\circ}C$   |                                                                   |
| Operating Temperature Range                   | $T_A$             | -40             | —     | +85             | $^{\circ}C$   |                                                                   |
| Storage Temperature Range                     | $T_A$             | -65             | —     | +150            | $^{\circ}C$   |                                                                   |
| <b>Thermal Package Resistance:</b>            |                   |                 |       |                 |               |                                                                   |
| Thermal Resistance, 8L-PDIP                   | $\theta_{JA}$     | —               | 85    | —               | $^{\circ}C/W$ |                                                                   |
| Thermal Resistance, 8L-SOIC                   | $\theta_{JA}$     | —               | 163   | —               | $^{\circ}C/W$ |                                                                   |
| Thermal Resistance, 8L-MSOP                   | $\theta_{JA}$     | —               | 206   | —               | $^{\circ}C/W$ |                                                                   |
| Thermal Resistance, 8L-TSSOP                  | $\theta_{JA}$     | —               | —     | —               | $^{\circ}C/W$ |                                                                   |
| <b>Analog Inputs:</b>                         |                   |                 |       |                 |               |                                                                   |
| Input Voltage Range (IN+)                     | IN+               | IN-             | —     | $V_{REF} + IN-$ | V             |                                                                   |
| Input Voltage Range (IN-)                     | IN-               | $V_{SS} - 100$  | —     | $V_{SS} + 100$  | mV            |                                                                   |
| Leakage Current                               |                   | —               | 0.001 | $\pm 1$         | $\mu A$       |                                                                   |
| Switch Resistance                             | $R_{SS}$          | —               | 1K    | —               | $\Omega$      | See Figure 4-1                                                    |
| Sample Capacitor                              | $C_{SAMPLE}$      | —               | 20    | —               | pF            | See Figure 4-1                                                    |
| <b>Digital Input/Output:</b>                  |                   |                 |       |                 |               |                                                                   |
| Data Coding Format                            |                   | Straight Binary |       |                 |               |                                                                   |
| High Level Input Voltage                      | $V_{IH}$          | $0.7 V_{DD}$    | —     | —               | V             |                                                                   |
| Low Level Input Voltage                       | $V_{IL}$          | —               | —     | $0.3 V_{DD}$    | V             |                                                                   |
| High Level Output Voltage                     | $V_{OH}$          | 4.1             | —     | —               | V             | $I_{OH} = -1$ mA, $V_{DD} = 4.5V$                                 |
| Low Level Output Voltage                      | $V_{OL}$          | —               | —     | 0.4             | V             | $I_{OL} = 1$ mA, $V_{DD} = 4.5V$                                  |
| Input Leakage Current                         | $I_{LI}$          | -10             | —     | 10              | $\mu A$       | $V_{IN} = V_{SS}$ or $V_{DD}$                                     |
| Output Leakage Current                        | $I_{LO}$          | -10             | —     | 10              | $\mu A$       | $V_{OUT} = V_{SS}$ or $V_{DD}$                                    |
| Pin Capacitance (all inputs/outputs)          | $C_{IN}, C_{OUT}$ | —               | —     | 10              | pF            | $V_{DD} = 5.0V$ (Note 1)<br>$T_{AMB} = 25^{\circ}C$ , $f = 1$ MHz |
| <b>Timing Parameters:</b>                     |                   |                 |       |                 |               |                                                                   |
| Clock Frequency                               | $f_{CLK}$         | —               | —     | 2.8<br>1.05     | MHz<br>MHz    | $V_{DD} = 5V$ (Note 3)<br>$V_{DD} = 2.7V$ (Note 3)                |
| Clock High Time                               | $t_{HI}$          | 160             | —     | —               | ns            |                                                                   |
| Clock Low Time                                | $t_{LO}$          | 160             | —     | —               | ns            |                                                                   |
| $\overline{CS}$ Fall To First Rising CLK Edge | $t_{SUCS}$        | 100             | —     | —               | ns            |                                                                   |
| CLK Fall To Output Data Valid                 | $t_{DO}$          | —               | —     | 125<br>200      | ns<br>ns      | $V_{DD} = 5V$ , See Figure 1-2<br>$V_{DD} = 2.7$ , See Figure 1-2 |
| CLK Fall To Output Enable                     | $t_{EN}$          | —               | —     | 125<br>200      | ns<br>ns      | $V_{DD} = 5V$ , See Figure 1-2<br>$V_{DD} = 2.7$ , See Figure 1-2 |
| $\overline{CS}$ Rise To Output Disable        | $t_{DIS}$         | —               | —     | 100             | ns            | See test circuits, Figure 1-2 (Note 1)                            |
| $\overline{CS}$ Disable Time                  | $t_{CSH}$         | 350             | —     | —               | ns            |                                                                   |
| $D_{OUT}$ Rise Time                           | $t_R$             | —               | —     | 100             | ns            | See test circuits, Figure 1-2 (Note 1)                            |
| $D_{OUT}$ Fall Time                           | $t_F$             | —               | —     | 100             | ns            | See test circuits, Figure 1-2 (Note 1)                            |

**Note 1:** This parameter is guaranteed by characterization and not 100% tested.

**2:** See graph that relates linearity performance to  $V_{REF}$  level.

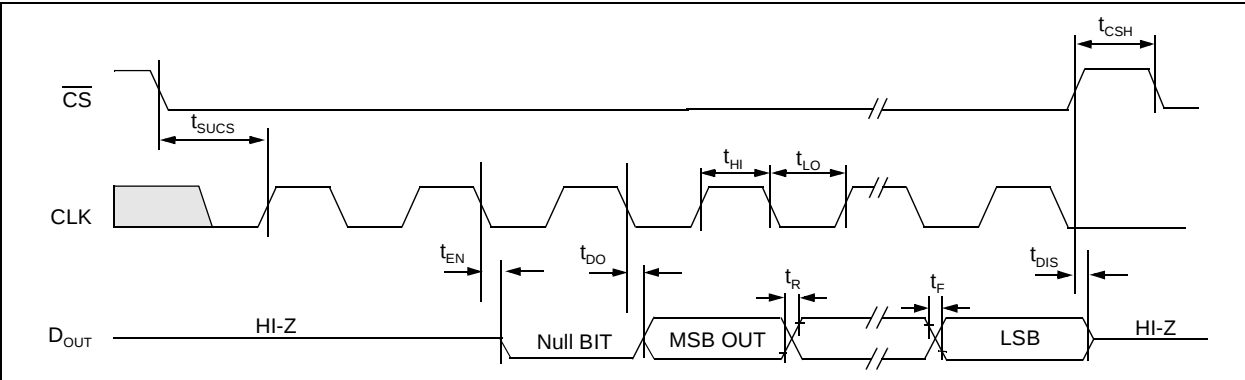
**3:** Because the sample cap will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

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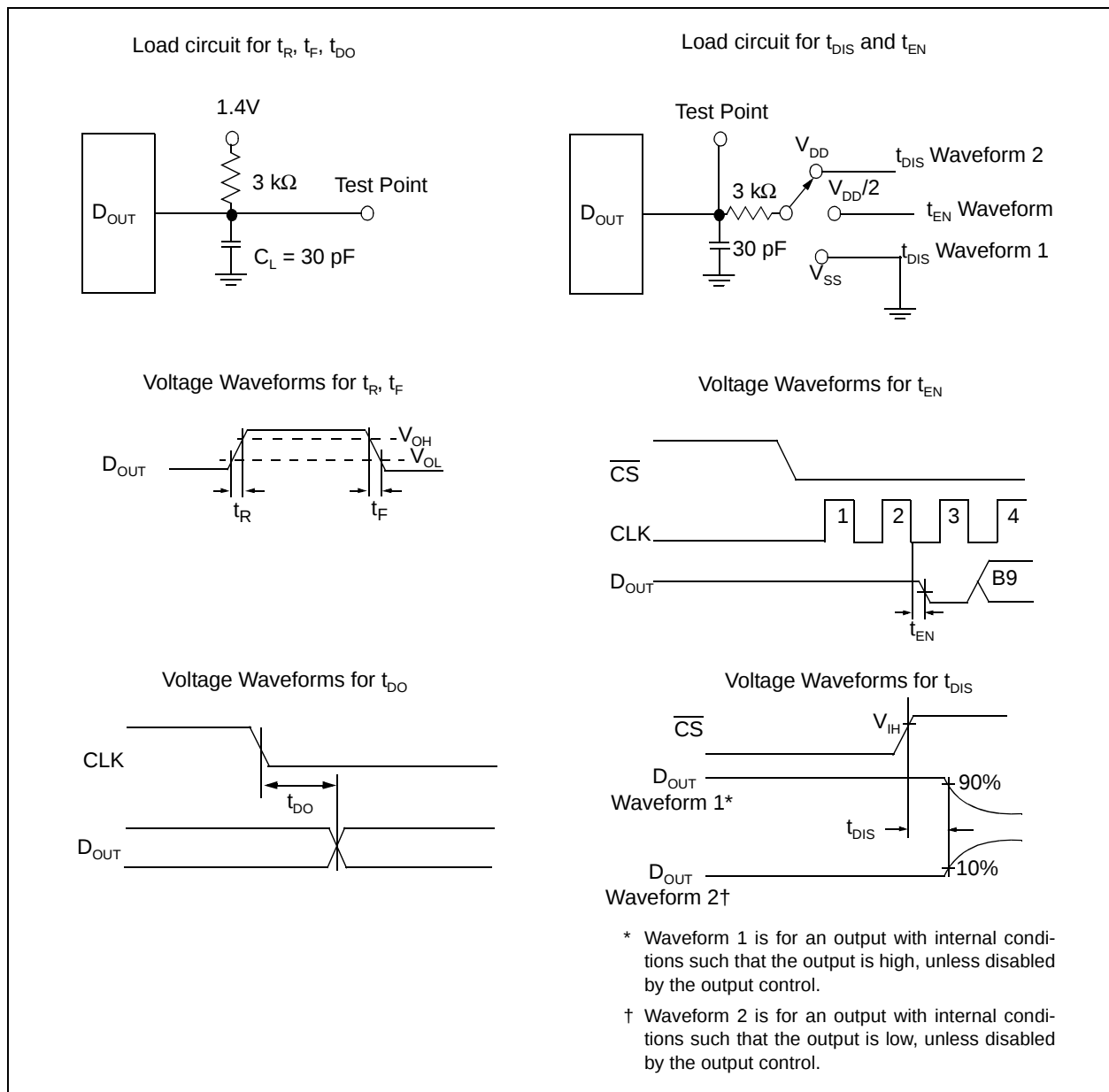
All parameters apply at  $V_{DD} = 5V$ ,  $V_{SS} = 0V$ ,  $V_{REF} = 5V$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $f_{SAMPLE} = 200$  ksp/s and  $f_{CLK} = 14 * f_{SAMPLE}$ , unless otherwise noted. Typical values apply for  $V_{DD} = 5V$ ,  $T_{AMB} = 25^{\circ}C$ , unless otherwise noted.

| Parameter                  | Sym       | Min | Typ        | Max | Units              | Conditions                                                                   |
|----------------------------|-----------|-----|------------|-----|--------------------|------------------------------------------------------------------------------|
| <b>Power Requirements:</b> |           |     |            |     |                    |                                                                              |
| Operating Voltage          | $V_{DD}$  | 2.7 | —          | 5.5 | V                  |                                                                              |
| Operating Current          | $I_{DD}$  | —   | 400<br>210 | 500 | $\mu A$<br>$\mu A$ | $V_{DD} = 5.0V$ , $D_{OUT}$ unloaded<br>$V_{DD} = 2.7V$ , $D_{OUT}$ unloaded |
| Standby Current            | $I_{DDS}$ | —   | 0.005      | 2   | $\mu A$            | $\overline{CS} = V_{DD} = 5.0V$                                              |

- Note 1:** This parameter is guaranteed by characterization and not 100% tested.
- 2:** See graph that relates linearity performance to  $V_{REF}$  level.
- 3:** Because the sample cap will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.



**FIGURE 1-1:** Serial Timing.

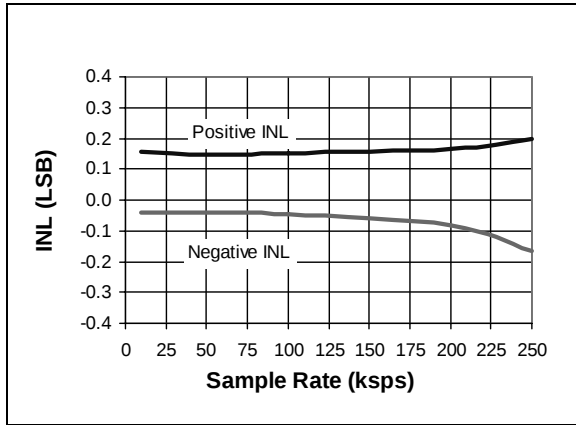


**FIGURE 1-2:** Test Circuits.

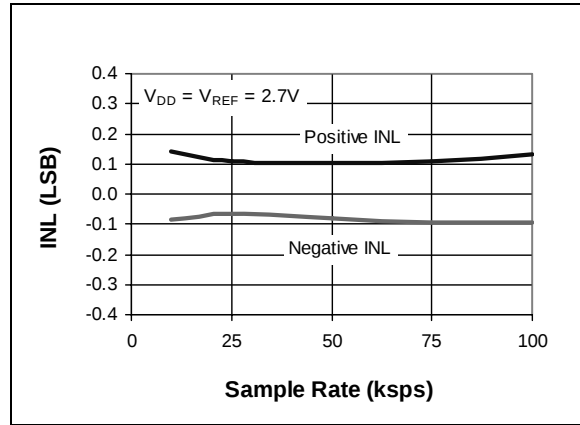
## 2.0 TYPICAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

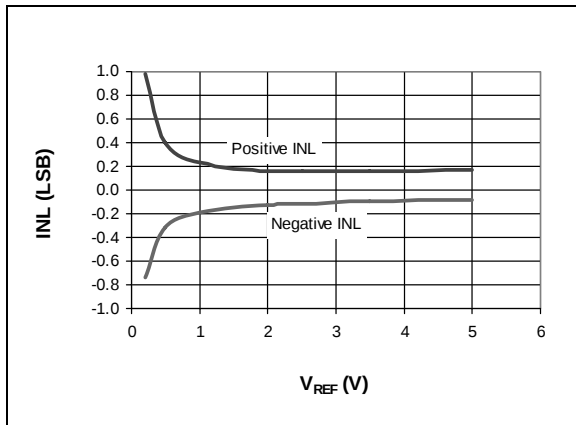
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $f_{SAMPLE} = 200$  kpsps,  $f_{CLK} = 14 \times \text{Sample Rate}$ ,  $T_A = 25^\circ C$



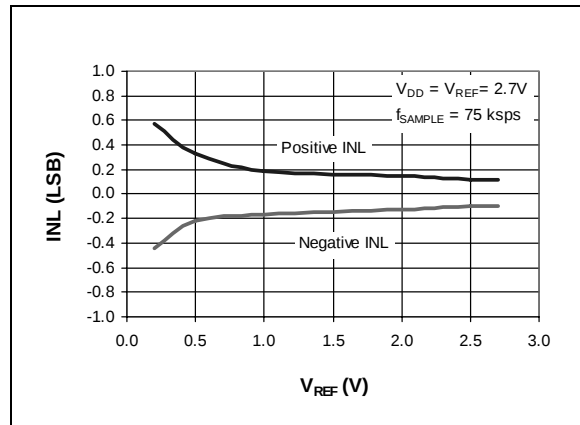
**FIGURE 2-1:** Integral Nonlinearity (INL) vs. Sample Rate.



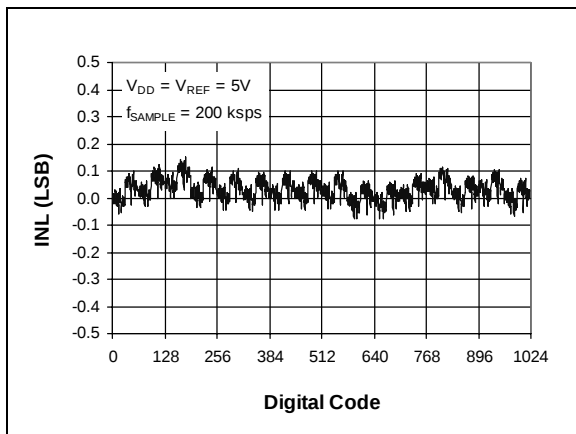
**FIGURE 2-4:** Integral Nonlinearity (INL) vs. Sample Rate ( $V_{DD} = 2.7V$ ).



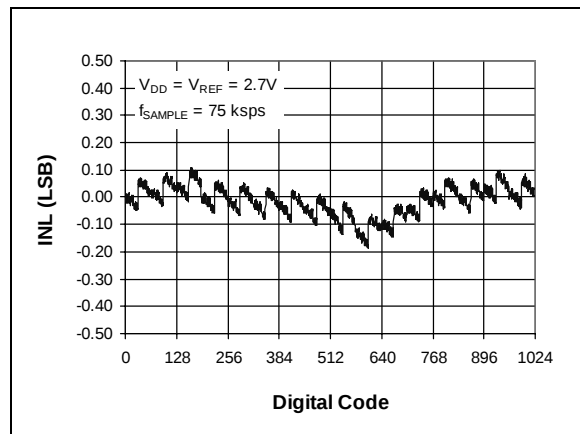
**FIGURE 2-2:** Integral Nonlinearity (INL) vs.  $V_{REF}$



**FIGURE 2-5:** Integral Nonlinearity (INL) vs.  $V_{REF}$  ( $V_{DD} = 2.7V$ ).

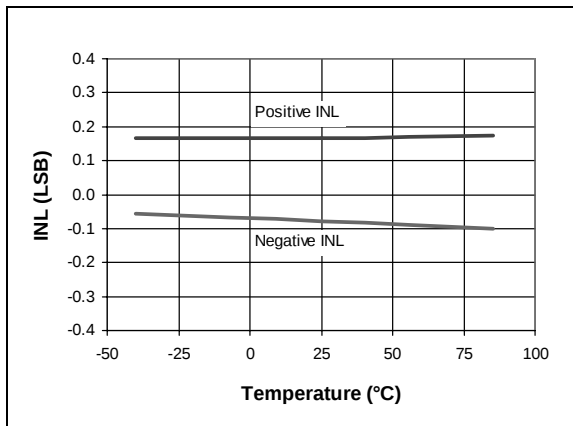


**FIGURE 2-3:** Integral Nonlinearity (INL) vs. Code (Representative Part).

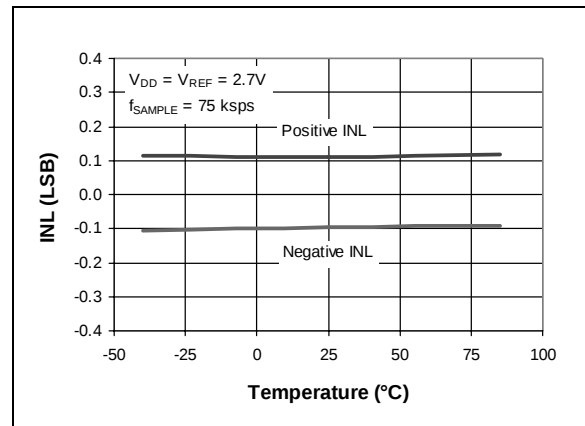


**FIGURE 2-6:** Integral Nonlinearity (INL) vs. Code (Representative Part,  $V_{DD} = 2.7V$ ).

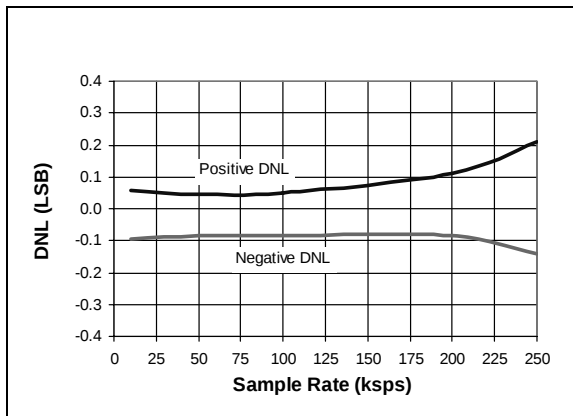
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $f_{SAMPLE} = 200$  kpsps,  $f_{CLK} = 14 \times \text{Sample Rate}$ ,  $T_A = 25^\circ\text{C}$



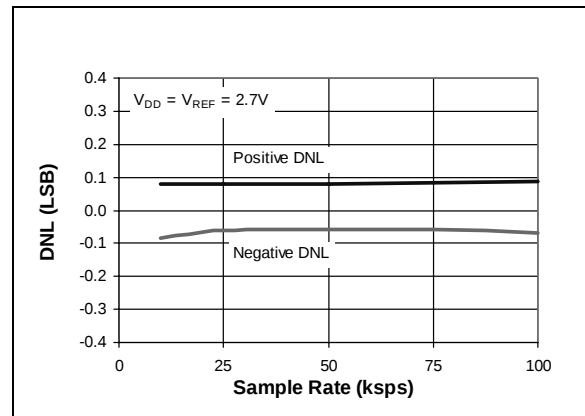
**FIGURE 2-7:** Integral Nonlinearity (INL) vs. Temperature.



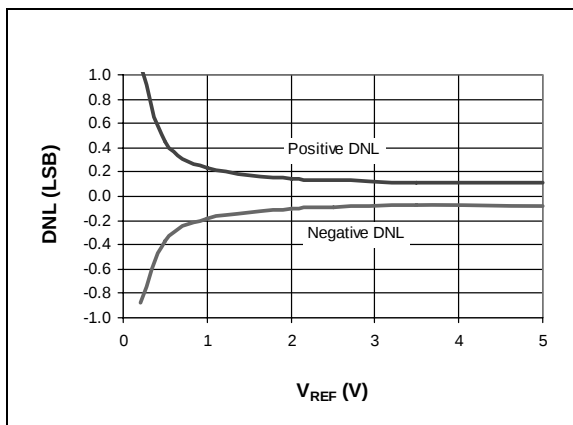
**FIGURE 2-10:** Integral Nonlinearity (INL) vs. Temperature ( $V_{DD} = 2.7V$ ).



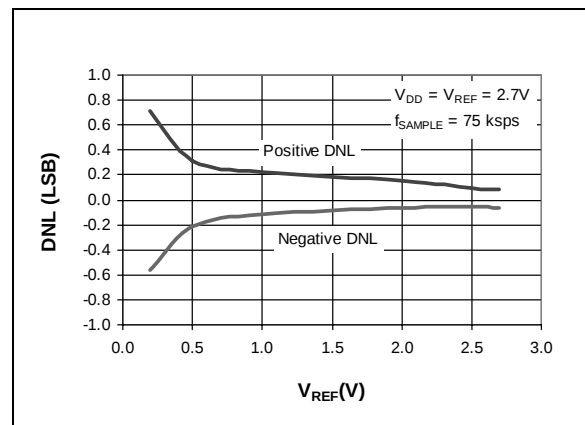
**FIGURE 2-8:** Differential Nonlinearity (DNL) vs. Sample Rate.



**FIGURE 2-11:** Differential Nonlinearity (DNL) vs. Sample Rate ( $V_{DD} = 2.7V$ ).



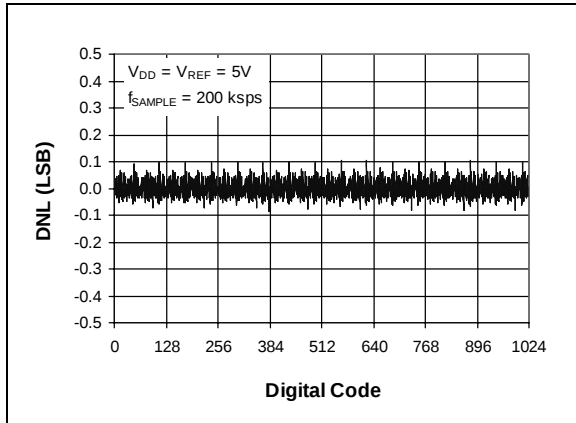
**FIGURE 2-9:** Differential Nonlinearity (DNL) vs.  $V_{REF}$ .



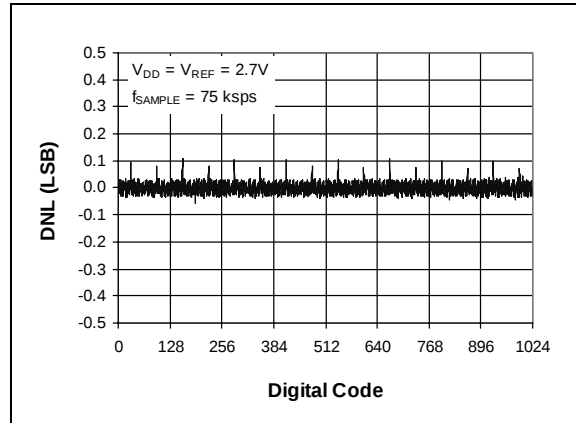
**FIGURE 2-12:** Differential Nonlinearity (DNL) vs.  $V_{REF}$  ( $V_{DD} = 2.7V$ ).

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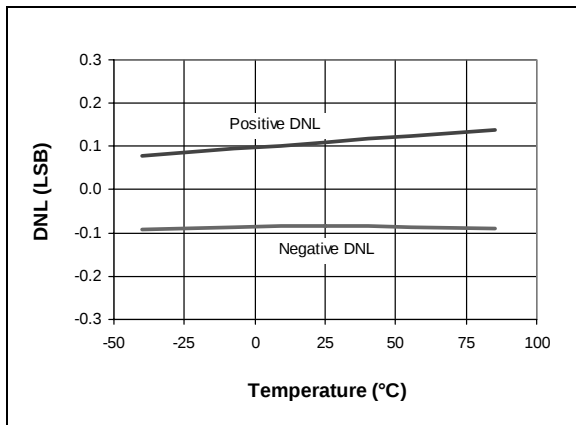
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $f_{SAMPLE} = 200$  kpsps,  $f_{CLK} = 14 \times \text{Sample Rate}$ ,  $T_A = 25^\circ\text{C}$



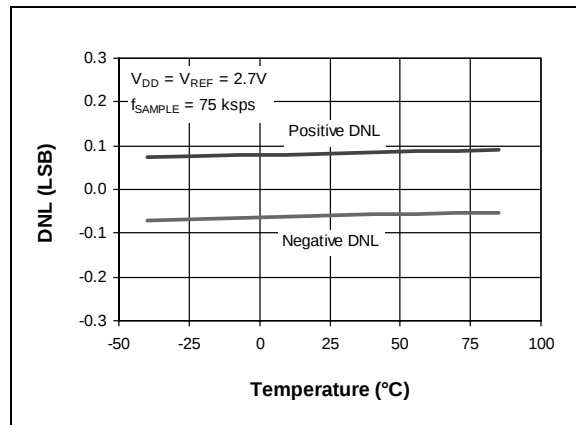
**FIGURE 2-13:** Differential Nonlinearity (DNL) vs. Code (Representative Part).



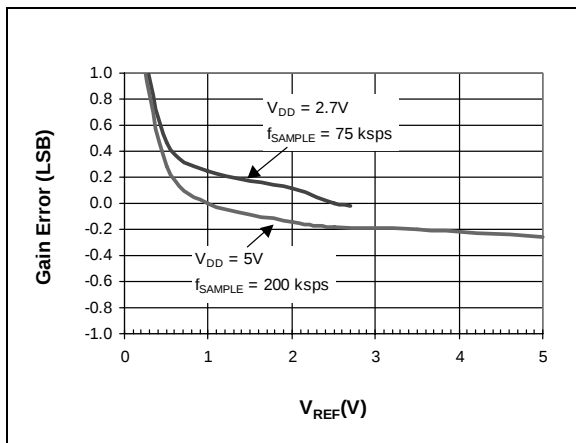
**FIGURE 2-16:** Differential Nonlinearity (DNL) vs. Code (Representative Part,  $V_{DD} = 2.7V$ ).



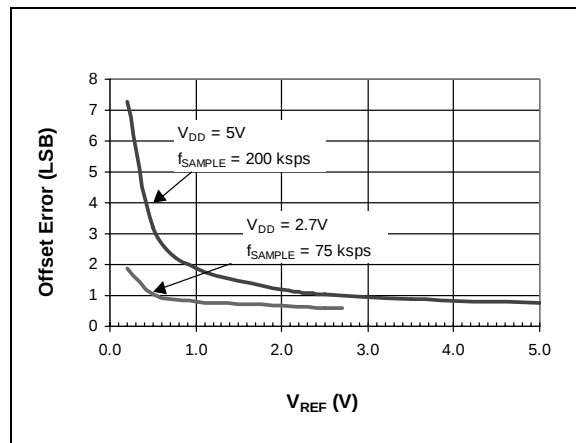
**FIGURE 2-14:** Differential Nonlinearity (DNL) vs. Temperature.



**FIGURE 2-17:** Differential Nonlinearity (DNL) vs. Temperature ( $V_{DD} = 2.7V$ ).

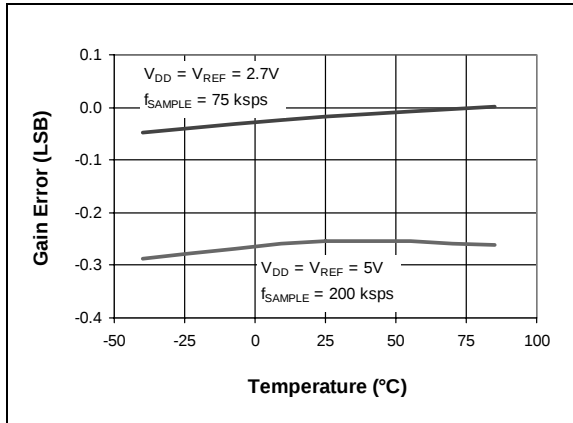


**FIGURE 2-15:** Gain Error vs.  $V_{REF}$ .

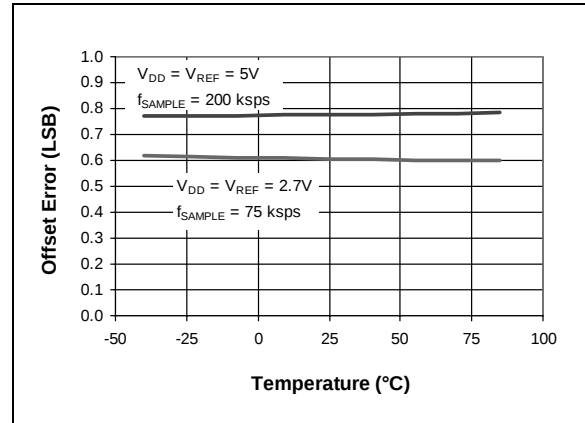


**FIGURE 2-18:** Offset Error vs.  $V_{REF}$ .

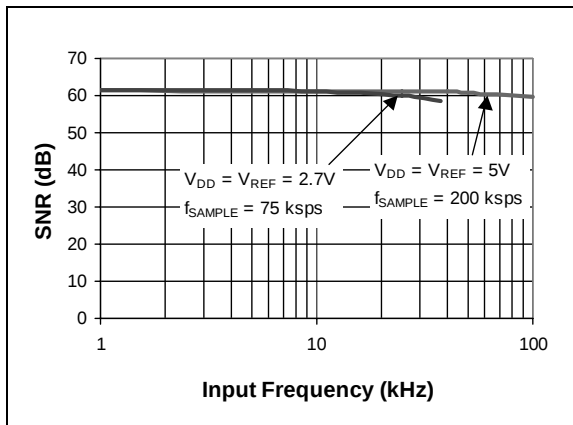
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $f_{SAMPLE} = 200$  kpsps,  $f_{CLK} = 14 \times \text{Sample Rate}$ ,  $T_A = 25^\circ C$



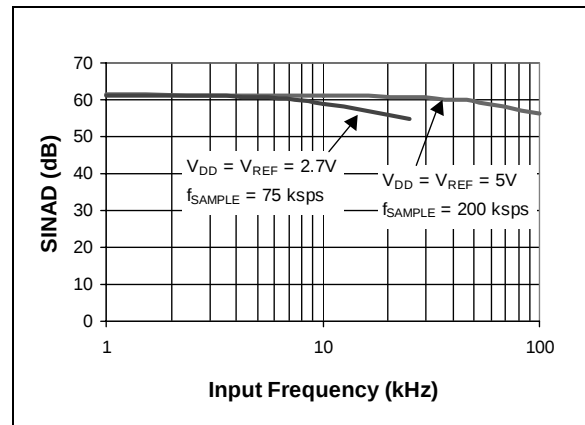
**FIGURE 2-19:** Gain Error vs. Temperature.



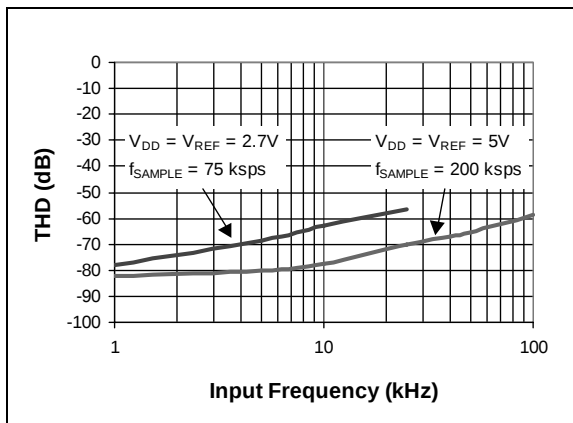
**FIGURE 2-22:** Offset Error vs. Temperature.



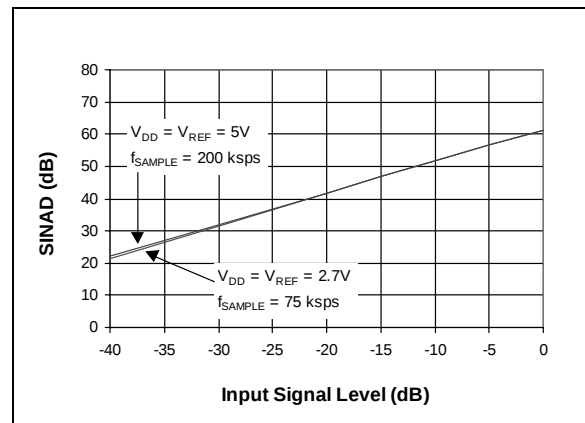
**FIGURE 2-20:** Signal to Noise Ratio (SNR) vs. Input Frequency.



**FIGURE 2-23:** Signal to Noise Ratio and Distortion (SINAD) vs. Input Frequency.



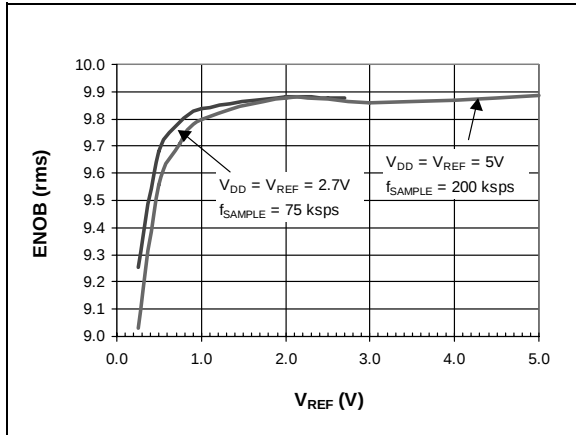
**FIGURE 2-21:** Total Harmonic Distortion (THD) vs. Input Frequency.



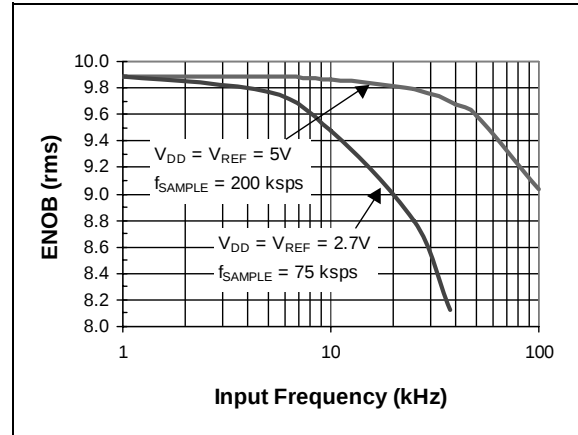
**FIGURE 2-24:** Signal to Noise and Distortion (SINAD) vs. Input Signal Level.

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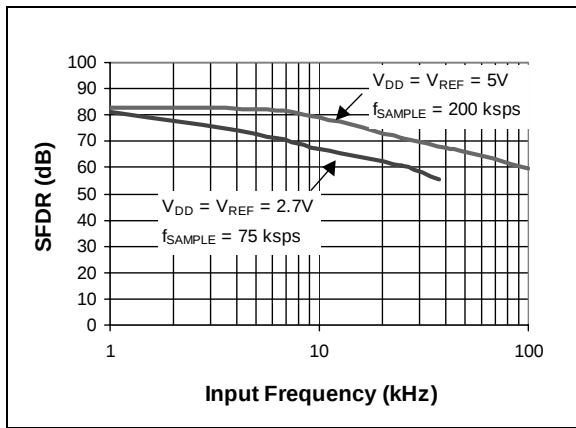
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $f_{SAMPLE} = 200$  kps,  $f_{CLK} = 14 \times \text{Sample Rate}$ ,  $T_A = 25^\circ C$



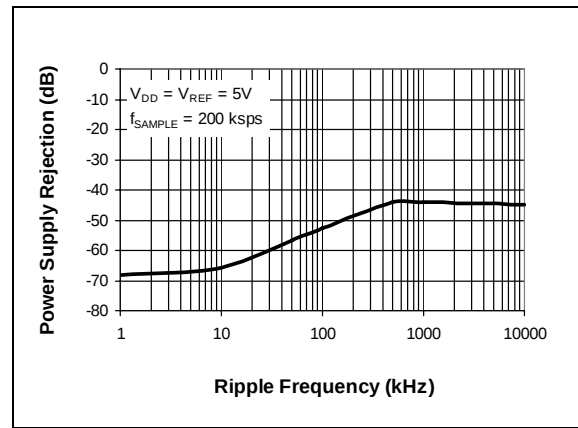
**FIGURE 2-25:** Effective Number of Bits (ENOB) vs.  $V_{REF}$ .



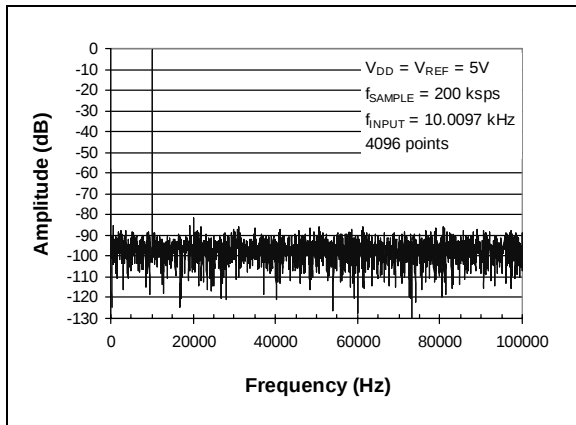
**FIGURE 2-28:** Effective Number of Bits (ENOB) vs. Input Frequency.



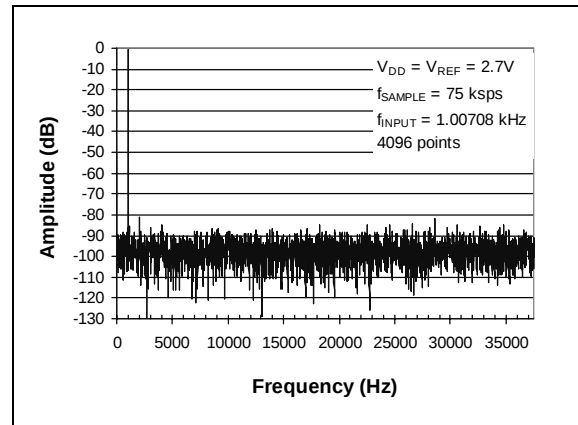
**FIGURE 2-26:** Spurious Free Dynamic Range (SFDR) vs. Input Frequency.



**FIGURE 2-29:** Power Supply Rejection (PSR) vs. Ripple Frequency.

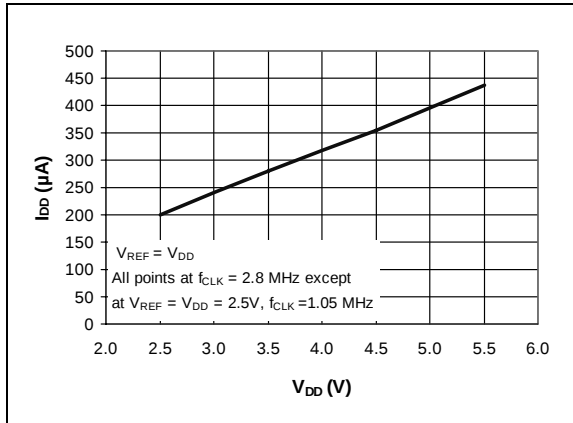


**FIGURE 2-27:** Frequency Spectrum of 10 kHz Input (Representative Part).

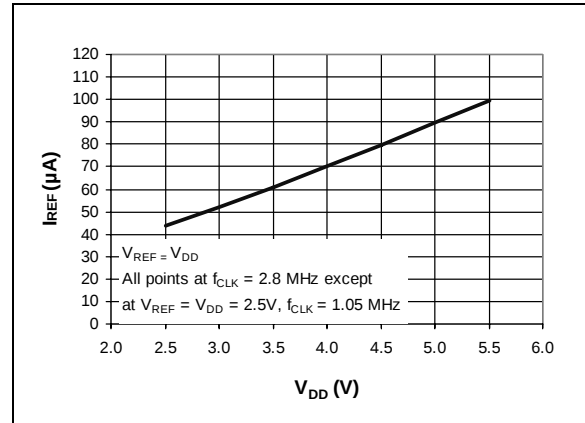


**FIGURE 2-30:** Frequency Spectrum of 1 kHz Input (Representative Part,  $V_{DD} = 2.7V$ ).

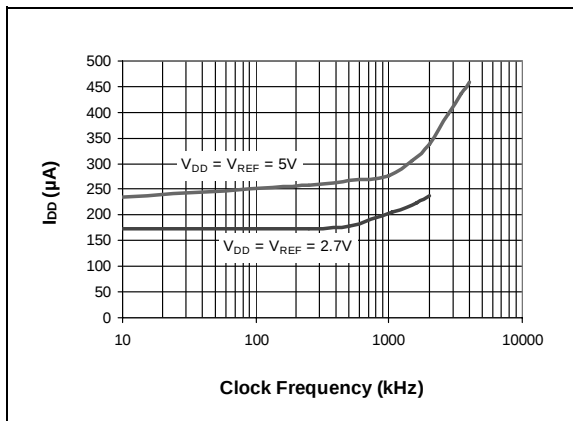
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $f_{SAMPLE} = 200$  ksp/s,  $f_{CLK} = 14 \times \text{Sample Rate}$ ,  $T_A = 25^\circ C$



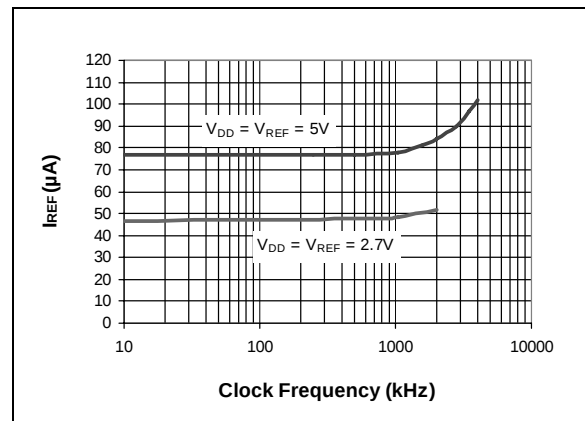
**FIGURE 2-31:**  $I_{DD}$  vs.  $V_{DD}$ .



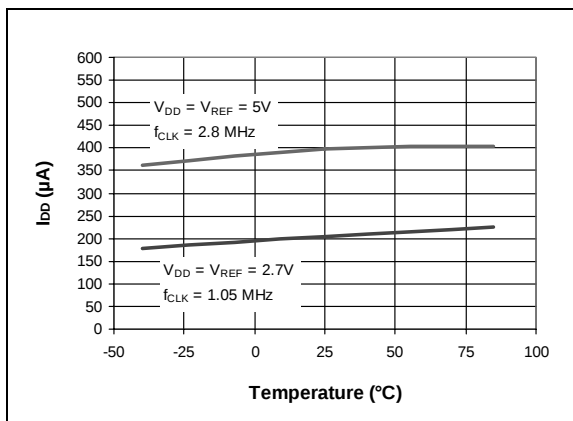
**FIGURE 2-34:**  $I_{REF}$  vs.  $V_{DD}$ .



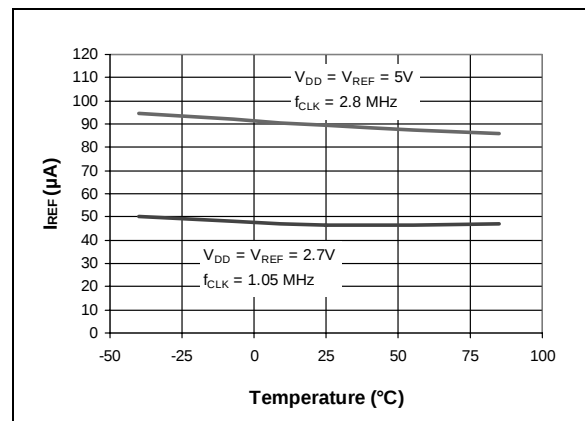
**FIGURE 2-32:**  $I_{DD}$  vs. Clock Frequency.



**FIGURE 2-35:**  $I_{REF}$  vs. Clock Frequency.



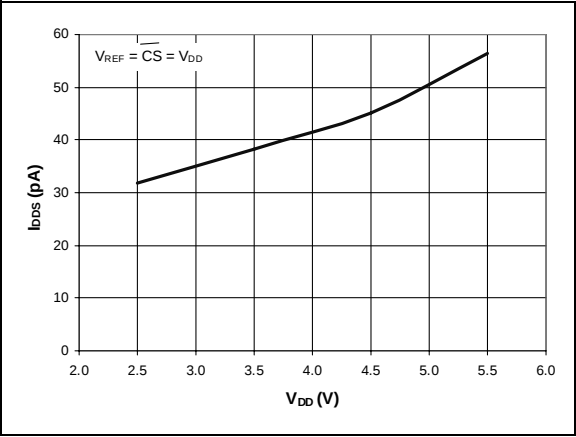
**FIGURE 2-33:**  $I_{DD}$  vs. Temperature.



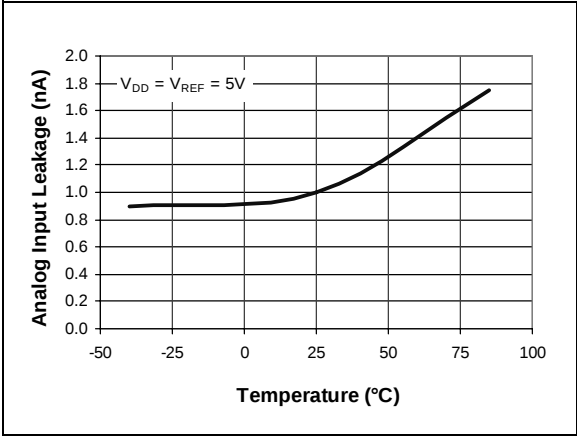
**FIGURE 2-36:**  $I_{REF}$  vs. Temperature.

# MCP3001

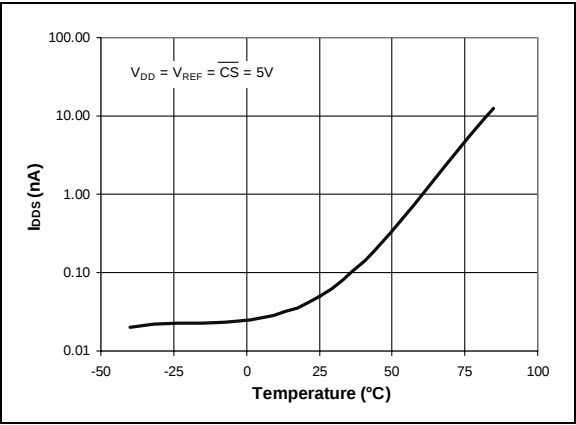
**Note:** Unless otherwise indicated,  $V_{DD} = V_{REF} = 5V$ ,  $f_{SAMPLE} = 200\text{ kSPS}$ ,  $f_{CLK} = 14 \times \text{Sample Rate}$ ,  $T_A = 25^\circ\text{C}$



**FIGURE 2-37:**  $I_{DDS}$  vs.  $V_{DD}$ .



**FIGURE 2-39:** Analog Input Leakage Current vs. Temperature.



**FIGURE 2-38:**  $I_{DDS}$  vs. Temperature.

## 3.0 PIN DESCRIPTIONS

### 3.1 IN+

Positive analog input. This input can vary from IN- to  $V_{REF} + IN-$ .

### 3.2 IN-

Negative analog input. This input can vary  $\pm 100$  mV from  $V_{SS}$ .

### 3.3 $\overline{CS}/SHDN$ (Chip Select/Shutdown)

The  $\overline{CS}/SHDN$  pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The  $\overline{CS}/SHDN$  pin must be pulled high between conversions.

### 3.4 CLK (Serial Clock)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See Section 6.2 for constraints on clock speed.

### 3.5 Dout (Serial Data output)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

## 4.0 DEVICE OPERATION

The MCP3001 A/D converter employs a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the first rising edge of the serial clock after  $\overline{CS}$  has been pulled low. Following this sample time, the input switch of the converter opens and the device uses the collected charge on the internal sample and hold capacitor to produce a serial 10-bit digital output code. Conversion rates of 200 ksp/s are possible on the MCP3001. See Section 6.2 for information on minimum clock rates. Communication with the device is done using a 3-wire SPI-compatible interface.

### 4.1 Analog Inputs

The MCP3001 provides a single pseudo-differential input. The IN+ input can range from IN- to  $(V_{REF} + IN-)$ . The IN- input is limited to  $\pm 100$  mV from the  $V_{SS}$  rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

For the A/D Converter to meet specification, the charge holding capacitor,  $C_{SAMPLE}$  must be given enough time to acquire a 10-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

In this diagram, it is shown that the source impedance ( $R_S$ ) adds to the internal sampling switch, ( $R_{SS}$ ) impedance, directly affecting the time that is required to charge the capacitor,  $C_{SAMPLE}$ . Consequently, a larger source impedance increases the offset, gain, and integral linearity errors of the conversion.

Ideally, the impedance of the signal source should be near zero. This is achievable with an operational amplifier such as the MCP601, which has a closed loop output impedance of tens of ohms. The adverse affects of higher source impedances are shown in Figure 4-2.

If the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than  $\{[V_{REF} + (IN-)] - 1 \text{ LSB}\}$ , then the output code will be 3FFh. If the voltage level at IN- is more than 1 LSB below  $V_{SS}$ , then the voltage level at the IN+ input will have to go below  $V_{SS}$  to see the 000h output code. Conversely, if IN- is more than 1 LSB above  $V_{SS}$ , then the 3FFh code will not be seen unless the IN+ input level goes above  $V_{REF}$  level.

### 4.2 Reference Input

The reference input ( $V_{REF}$ ) determines the analog input voltage range and the LSB size, as shown below.

$$LSB \text{ Size} = \frac{V_{REF}}{1024}$$

As the reference input is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D Converter is a function of the analog input signal and the reference input as shown below.

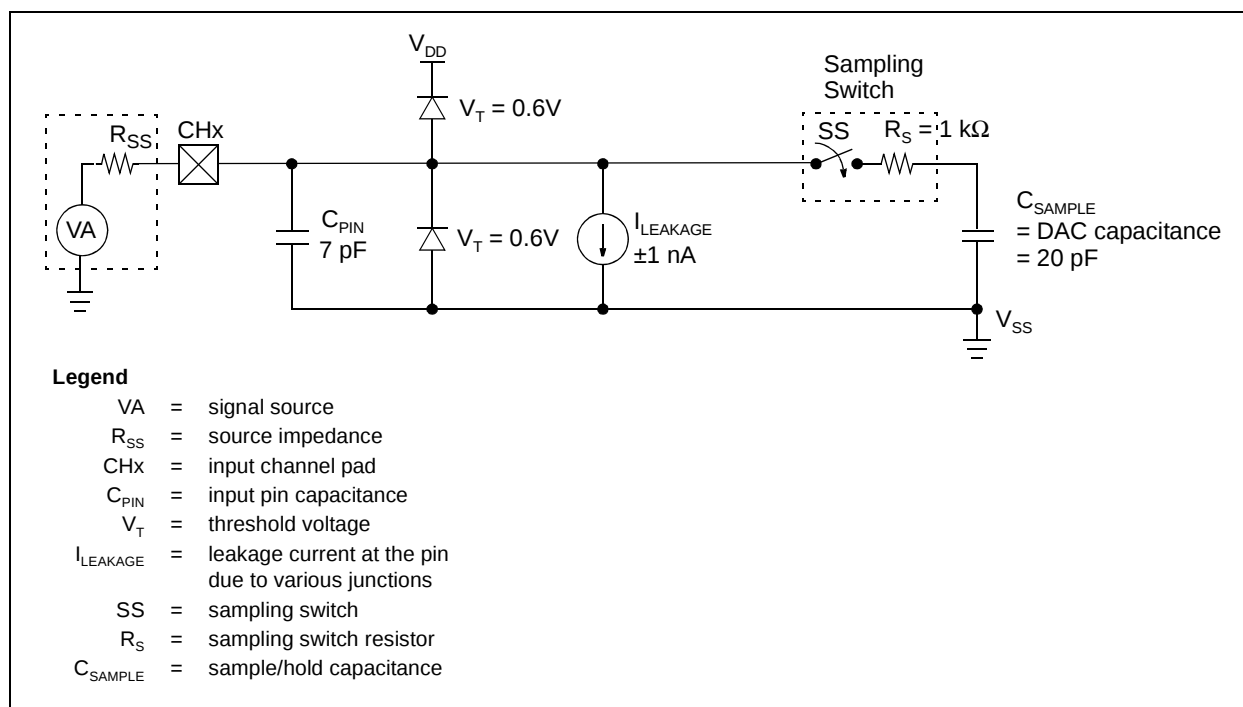
$$Digital \text{ Output Code} = \frac{1024 * V_{IN}}{V_{REF}}$$

where:

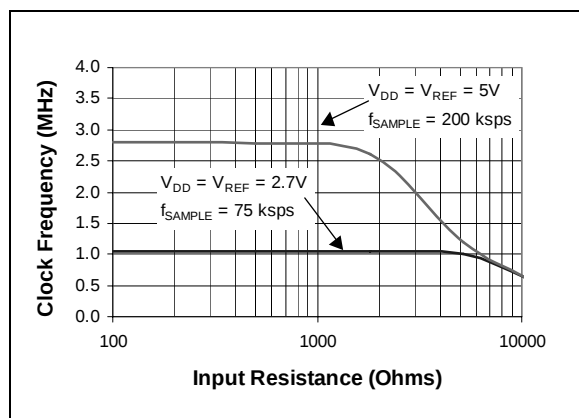
$$V_{IN} = \text{analog input voltage} = V(IN+) - V(IN-)$$

$$V_{REF} = \text{reference voltage}$$

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the operation of the ADC.



**FIGURE 4-1:** Analog Input Model.



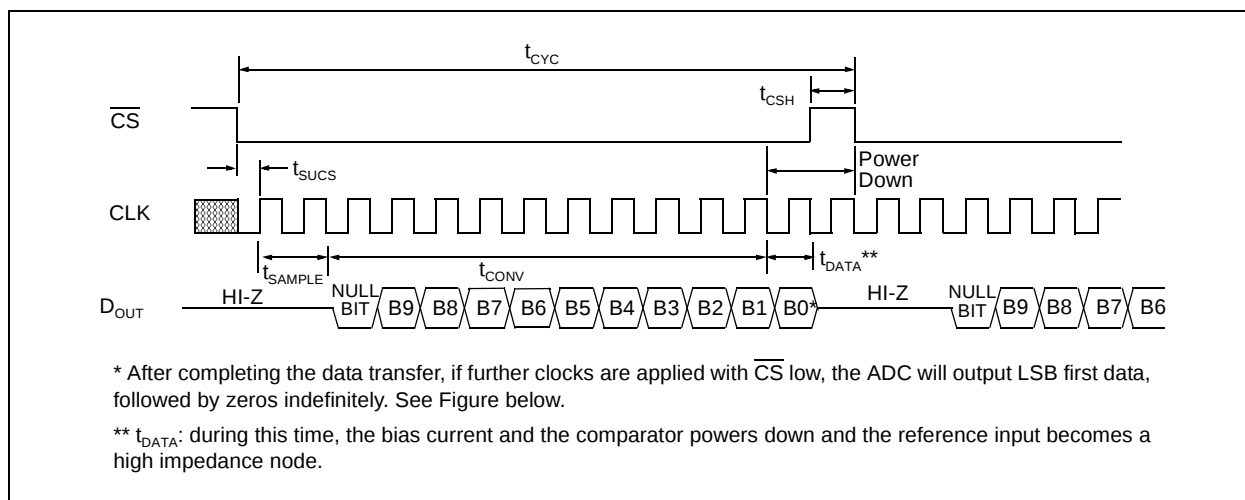
**FIGURE 4-2:** Maximum Clock Frequency vs. Input Resistance ( $R_S$ ) to maintain less than a 0.1LSB deviation in INL from nominal conditions.

## 5.0 SERIAL COMMUNICATIONS

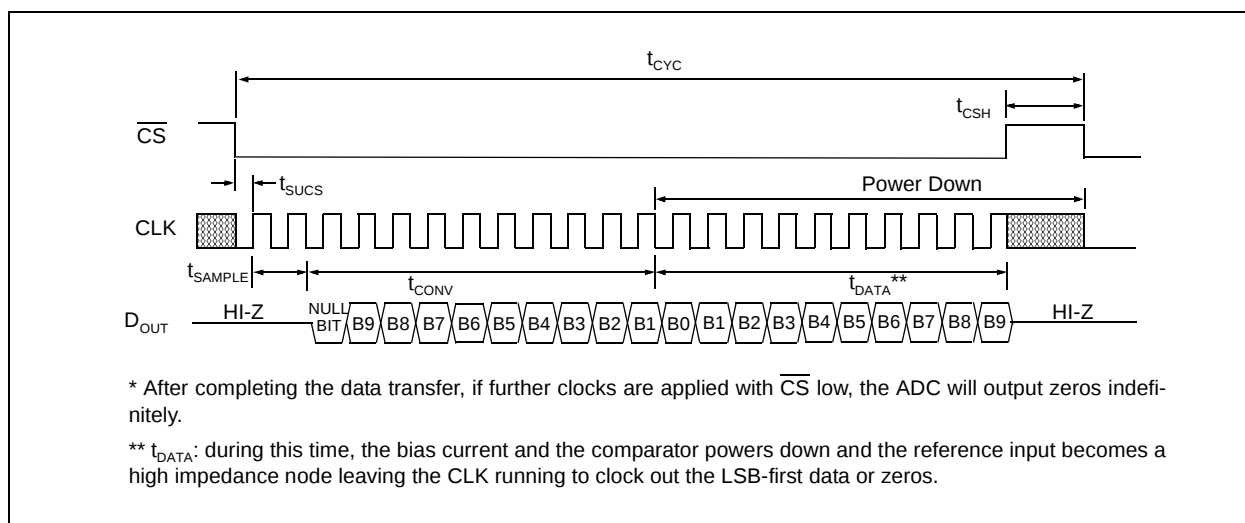
Communication with the device is done using a standard SPI compatible serial interface. Initiating communication with the MCP3001 begins with the  $\overline{CS}$  going low. If the device was powered up with the  $\overline{CS}$  pin low, it must be brought high and back low to initiate communication. The device will begin to sample the analog input on the first rising edge after  $\overline{CS}$  goes low. The sample period will end in the falling edge of the second clock, at which time the device will output a low null bit. The next 10 clocks will output the result of the conversion with MSB first, as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 10 data bits have been transmitted and the

device continues to receive clocks while the  $\overline{CS}$  is held low, the device will output the conversion result LSB first, as shown in Figure 5-2. If more clocks are provided to the device while  $\overline{CS}$  is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If it is desired, the  $\overline{CS}$  can be raised to end the conversion period at any time during the transmission. Faster conversion rates can be obtained by using this technique if not all the bits are captured before starting a new cycle. Some system designers use this method by capturing only the highest order 8 bits and 'throwing away' the lower 2 bits.



**FIGURE 5-1:** Communication with MCP3001 (MSB first Format).



**FIGURE 5-2:** Communication with MCP3001 (LSB first Format).

# MCP3001

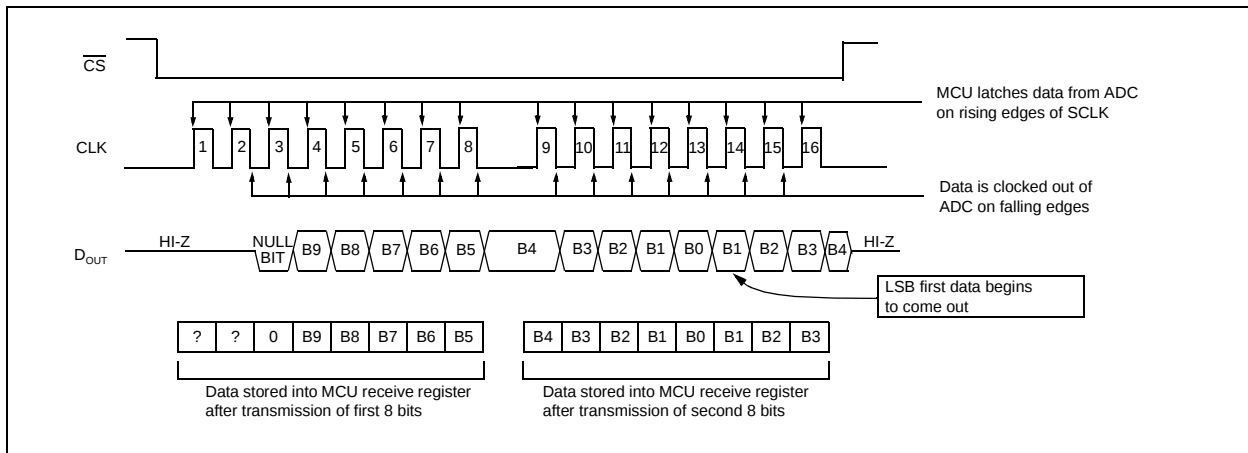
## 6.0 APPLICATIONS INFORMATION

### 6.1 Using the MCP3001 with Microcontroller SPI Ports

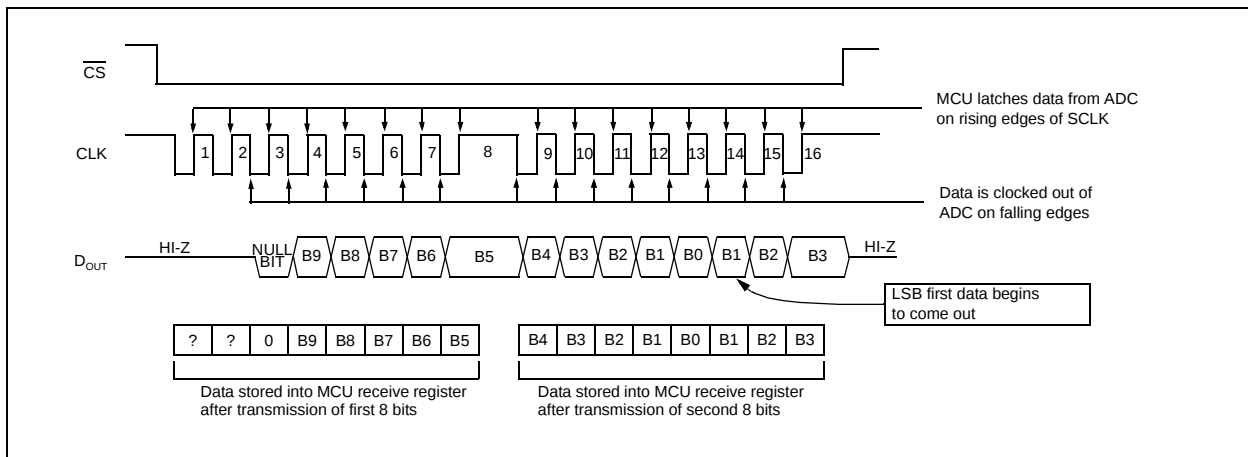
With most microcontroller SPI ports, it is required to clock out eight bits at a time. If this is the case, it will be necessary to provide more clocks than are required for the MCP3001. As an example, Figure 6-1 and Figure 6-2 show how the MCP3001 can be interfaced to a microcontroller with a standard SPI port. Since the MCP3001 always clocks data out on the falling edge of clock, the MCU SPI port must be configured to match this operation. SPI Mode 0,0 (clock idles low) and SPI Mode 1,1 (clock idles high) are both compatible with the MCP3001. Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the CLK from the microcontroller idles in the 'low' state. As shown in the diagram, the MSB is clocked out of the ADC on the falling edge of the third clock pulse. After the first eight clocks have been sent to the device, the microcontrol-

ler's receive buffer will contain two unknown bits (the output is at high impedance for the first two clocks), the null bit and the highest order five bits of the conversion. After the second eight clocks have been sent to the device, the MCU receive register will contain the lowest order five bits and the B1-B4 bits repeated as the ADC has begun to shift out LSB first data with the extra clocks. Typical procedure would then call for the lower order byte of data to be shifted right by three bits to remove the extra B1-B4 bits. The B9-B5 bits are then rotated 3 bits to the right with B7-B5 rotating from the high order byte to the lower order byte. Easier manipulation of the converted data can be obtained by using this method.

Figure 6-2 shows SPI Mode 1,1 communication which requires that the clock idles in the high state. As with mode 0,0, the ADC outputs data on the falling edge of the clock and the MCU latches data from the ADC in on the rising edge of the clock.



**FIGURE 6-1:** SPI Communication with the MCP3001 using 8-bit segments (Mode 0,0: SCLK idles low).



**FIGURE 6-2:** SPI Communication with the MCP3001 using 8-bit segments (Mode 1,1: SCLK idles high).

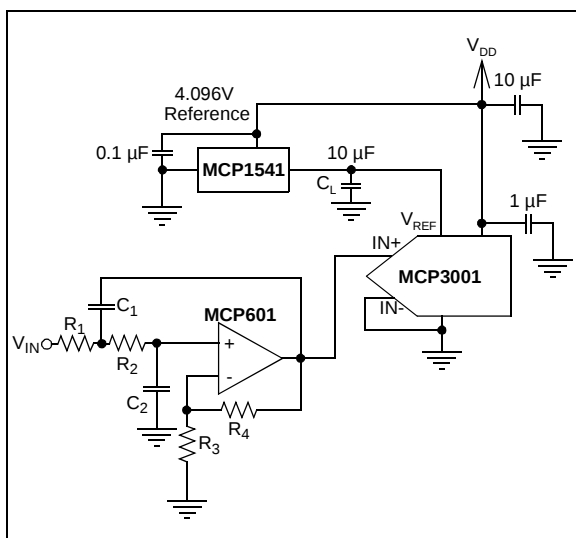
## 6.2 Maintaining Minimum Clock Speed

When the MCP3001 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample cap while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample cap for 700  $\mu$ s at  $V_{DD} = 2.7V$  and 1.5 ms at  $V_{DD} = 5V$ . This means that at  $V_{DD} = 2.7V$ , the time it takes to transmit the first 14 clocks must not exceed 700  $\mu$ s. Failure to meet this criterion may induce linearity errors into the conversion outside the rated specifications.

## 6.3 Buffering/Filtering the Analog Inputs

If the signal source for the ADC is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur. See Figure 4-2. It is also recommended that a filter be used to eliminate any signals that may be aliased back into the conversion results. This is illustrated in Figure 6-3 where an op amp is used to drive, filter and gain the analog input of the MCP3001. This amplifier provides a low impedance source for the converter input and a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip's interactive FilterLab™ software. FilterLab will calculate capacitor and resistor values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see the application note AN699 "Anti-Aliasing Analog Filters for Data Acquisition Systems."



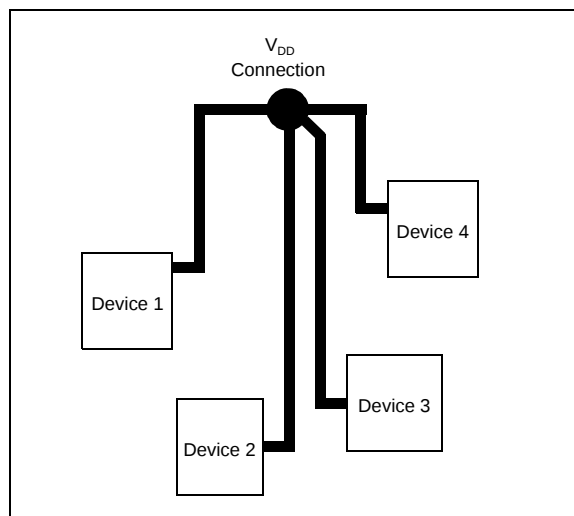
**FIGURE 6-3:** The MCP601 operational amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3001.

## 6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 1  $\mu$ F is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing  $V_{DD}$  connections to devices in a "star" configuration can also reduce noise by eliminating current return paths and associated errors. See Figure 6-4. For more information on layout tips when using ADC, refer to AN-688 "Layout Tips for 12-Bit A/D Converter Applications".



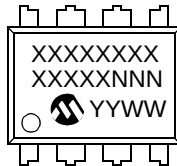
**FIGURE 6-4:**  $V_{DD}$  traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.

# MCP3001

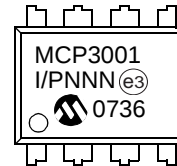
## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

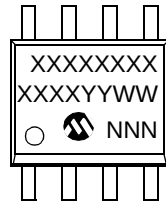
8-Lead PDIP (300 mil)



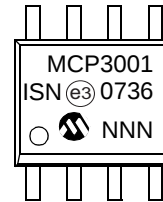
Example:



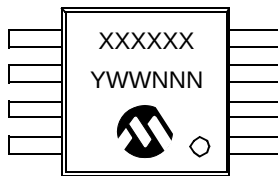
8-Lead SOIC (150 mil)



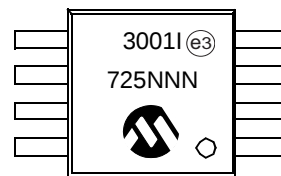
Example:



8-Lead MSOP



Example:



8-Lead TSSOP



Example:

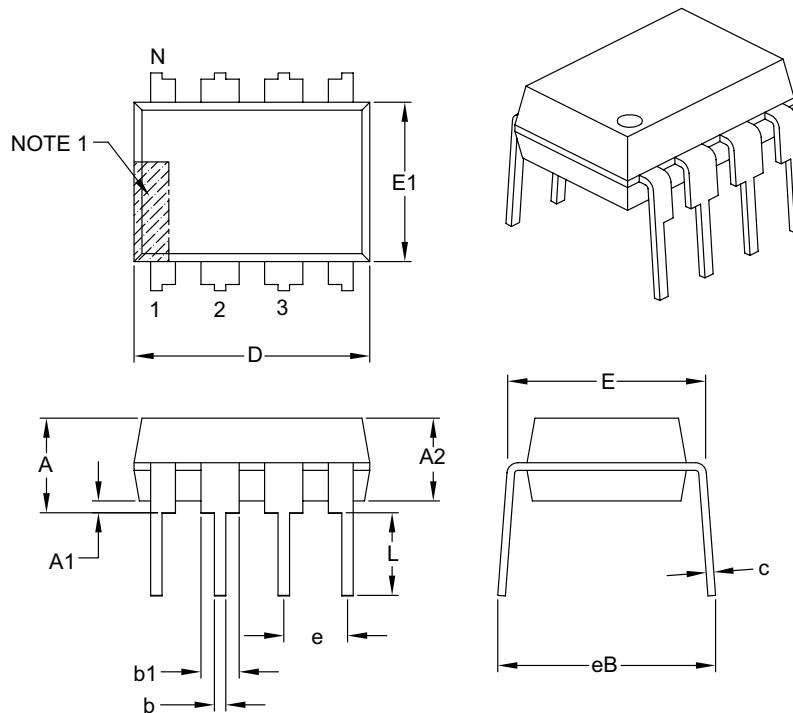


|                |        |                                                                                                                  |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| <b>Legend:</b> | XX...X | Customer-specific information                                                                                    |
|                | Y      | Year code (last digit of calendar year)                                                                          |
|                | YY     | Year code (last 2 digits of calendar year)                                                                       |
|                | WW     | Week code (week of January 1 is week '01')                                                                       |
|                | NNN    | Alphanumeric traceability code                                                                                   |
|                | (e3)   | Pb-free JEDEC designator for Matte Tin (Sn)                                                                      |
|                | *      | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units                      |    | INCHES   |      |      |
|----------------------------|----|----------|------|------|
| Dimension Limits           |    | MIN      | NOM  | MAX  |
| Number of Pins             | N  | 8        |      |      |
| Pitch                      | e  | .100 BSC |      |      |
| Top to Seating Plane       | A  | –        | –    | .210 |
| Molded Package Thickness   | A2 | .115     | .130 | .195 |
| Base to Seating Plane      | A1 | .015     | –    | –    |
| Shoulder to Shoulder Width | E  | .290     | .310 | .325 |
| Molded Package Width       | E1 | .240     | .250 | .280 |
| Overall Length             | D  | .348     | .365 | .400 |
| Tip to Seating Plane       | L  | .115     | .130 | .150 |
| Lead Thickness             | c  | .008     | .010 | .015 |
| Upper Lead Width           | b1 | .040     | .060 | .070 |
| Lower Lead Width           | b  | .014     | .018 | .022 |
| Overall Row Spacing §      | eB | –        | –    | .430 |

### Notes:

- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

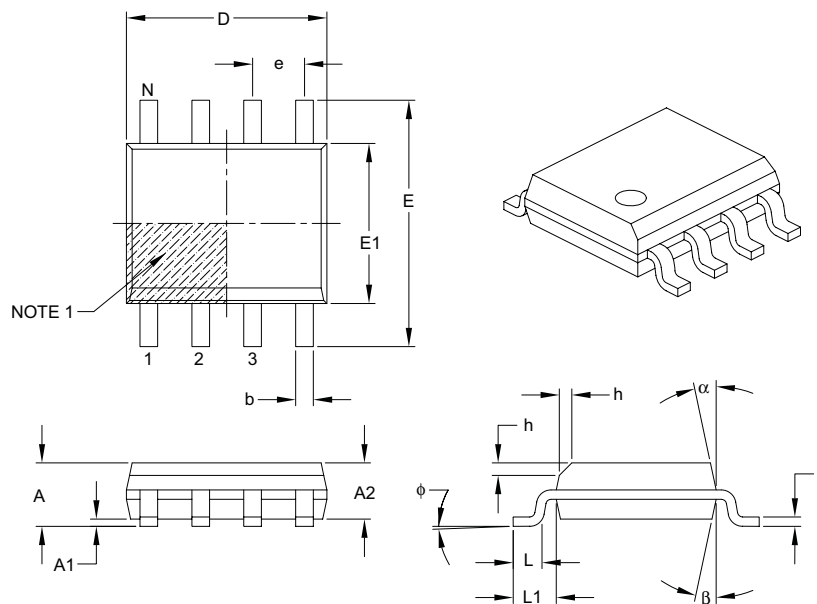
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

# MCP3001

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |     |      |
|--------------------------|-------|-------------|-----|------|
|                          |       | MIN         | NOM | MAX  |
| Number of Pins           | N     | 8           |     |      |
| Pitch                    | e     | 1.27 BSC    |     |      |
| Overall Height           | A     | –           | –   | 1.75 |
| Molded Package Thickness | A2    | 1.25        | –   | –    |
| Standoff §               | A1    | 0.10        | –   | 0.25 |
| Overall Width            | E     | 6.00 BSC    |     |      |
| Molded Package Width     | E1    | 3.90 BSC    |     |      |
| Overall Length           | D     | 4.90 BSC    |     |      |
| Chamfer (optional)       | h     | 0.25        | –   | 0.50 |
| Foot Length              | L     | 0.40        | –   | 1.27 |
| Footprint                | L1    | 1.04 REF    |     |      |
| Foot Angle               | φ     | 0°          | –   | 8°   |
| Lead Thickness           | c     | 0.17        | –   | 0.25 |
| Lead Width               | b     | 0.31        | –   | 0.51 |
| Mold Draft Angle Top     | α     | 5°          | –   | 15°  |
| Mold Draft Angle Bottom  | β     | 5°          | –   | 15°  |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

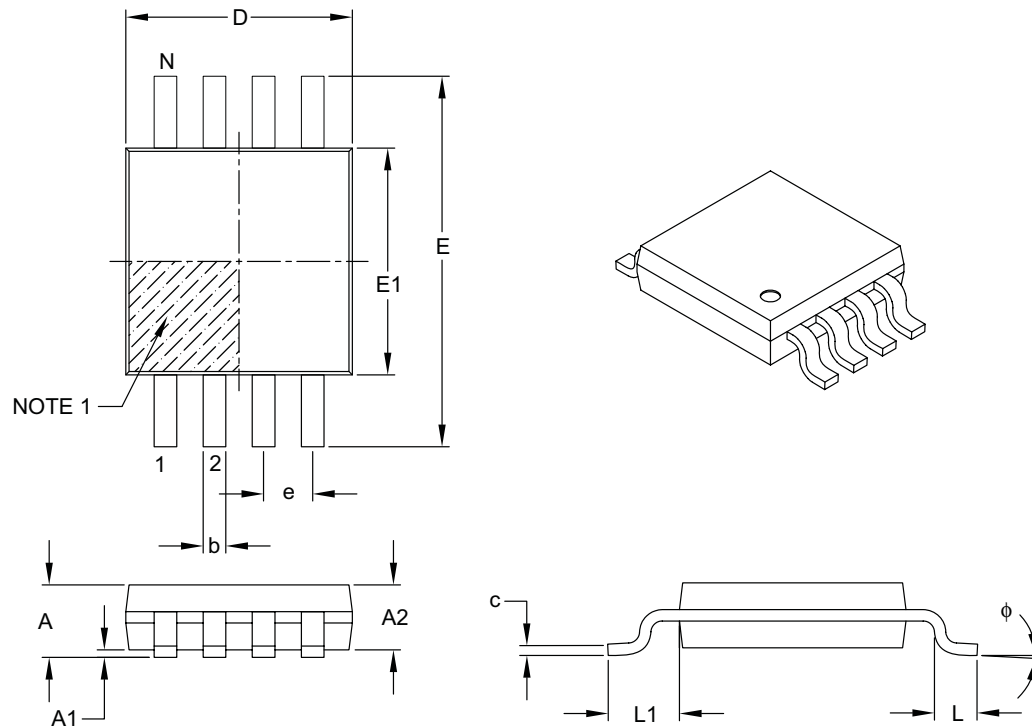
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |      |      |
|--------------------------|-------|-------------|------|------|
|                          |       | MIN         | NOM  | MAX  |
| Number of Pins           | N     | 8           |      |      |
| Pitch                    | e     | 0.65 BSC    |      |      |
| Overall Height           | A     | –           | –    | 1.10 |
| Molded Package Thickness | A2    | 0.75        | 0.85 | 0.95 |
| Standoff                 | A1    | 0.00        | –    | 0.15 |
| Overall Width            | E     | 4.90 BSC    |      |      |
| Molded Package Width     | E1    | 3.00 BSC    |      |      |
| Overall Length           | D     | 3.00 BSC    |      |      |
| Foot Length              | L     | 0.40        | 0.60 | 0.80 |
| Footprint                | L1    | 0.95 REF    |      |      |
| Foot Angle               | φ     | 0°          | –    | 8°   |
| Lead Thickness           | c     | 0.08        | –    | 0.23 |
| Lead Width               | b     | 0.22        | –    | 0.40 |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

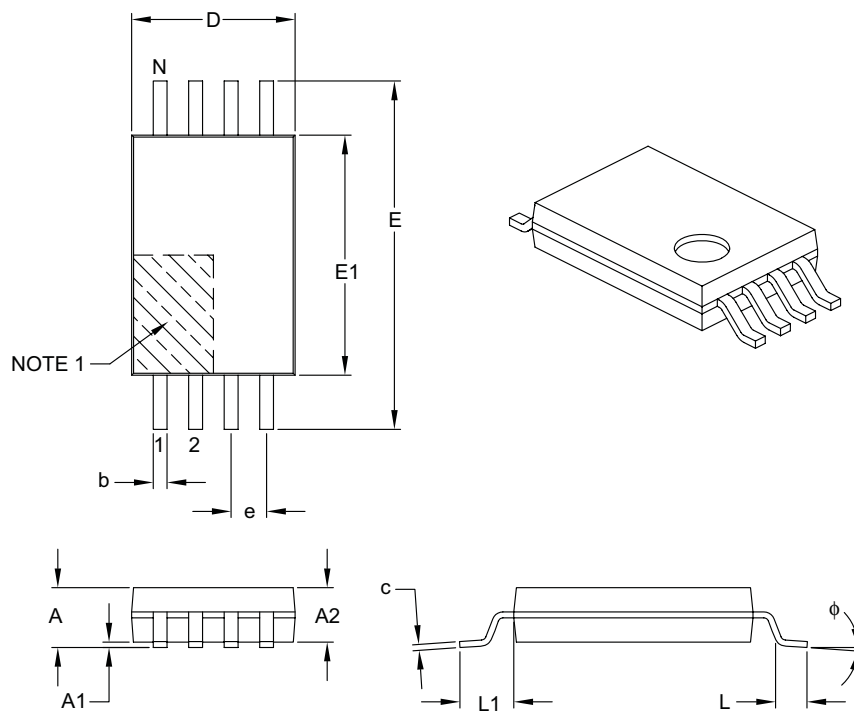
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

# MCP3001

## 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits         | Units | MILLIMETERS |      |      |
|--------------------------|-------|-------------|------|------|
|                          |       | MIN         | NOM  | MAX  |
| Number of Pins           | N     | 8           |      |      |
| Pitch                    | e     | 0.65 BSC    |      |      |
| Overall Height           | A     | –           | –    | 1.20 |
| Molded Package Thickness | A2    | 0.80        | 1.00 | 1.05 |
| Standoff                 | A1    | 0.05        | –    | 0.15 |
| Overall Width            | E     | 6.40 BSC    |      |      |
| Molded Package Width     | E1    | 4.30        | 4.40 | 4.50 |
| Molded Package Length    | D     | 2.90        | 3.00 | 3.10 |
| Foot Length              | L     | 0.45        | 0.60 | 0.75 |
| Footprint                | L1    | 1.00 REF    |      |      |
| Foot Angle               | φ     | 0°          | –    | 8°   |
| Lead Thickness           | c     | 0.09        | –    | 0.20 |
| Lead Width               | b     | 0.19        | –    | 0.30 |

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

## APPENDIX A: REVISION HISTORY

### Revision C (January 2007)

This revision includes updates to the packaging diagrams.

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**NOTES:**



# MCP3001

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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