

**STRUCTURE** Silicon Monolithic Integrated Circuit

**PRODUCT NAME** BU9735K

**FUNCTION** 72 Segment Driver

- Display data RAM (DDRAM): 18 × 4bit (72 MAX Segment)

**FEATURE** • Duty Ratio: 1/4

- LCD Driving Voltage Circuit On-Chip (1/3bias)

○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C, VSS=0V)

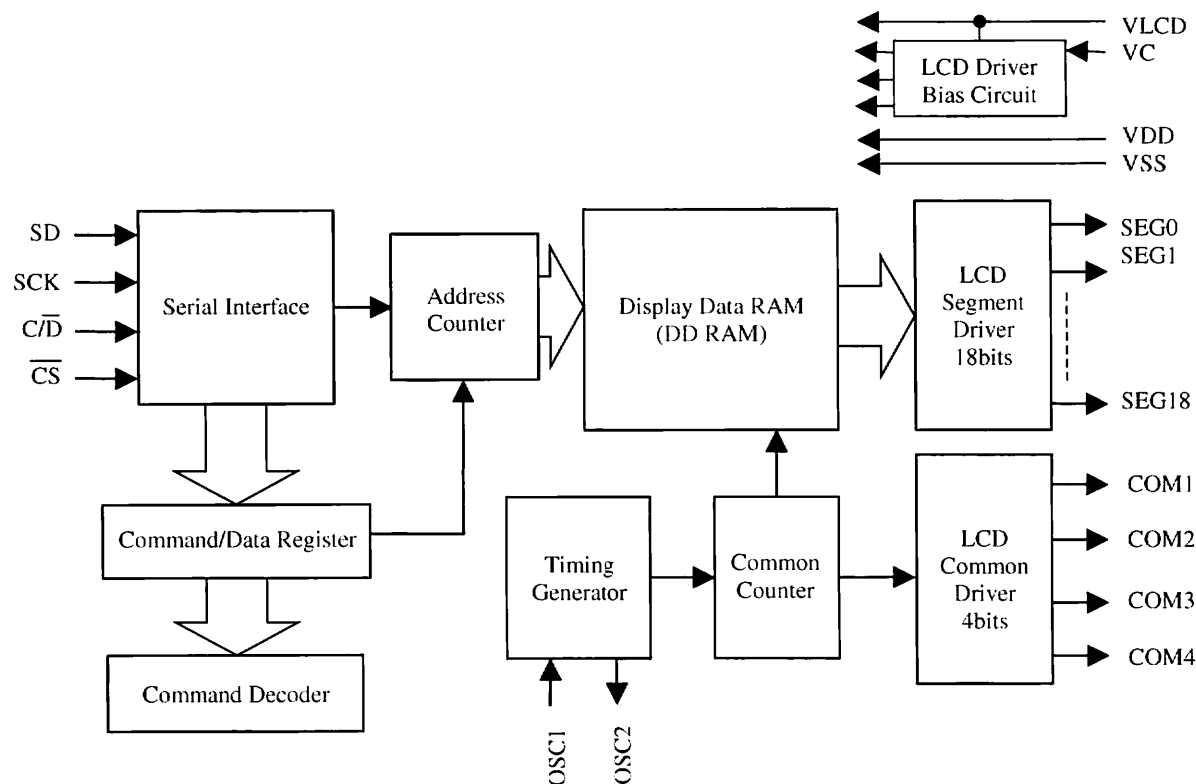
Parameter	Symbol	Limits	Unit
Supply voltage 1	VDD	-0.3 ~ +7.0	V
Supply voltage 2	VLCD	-0.3 ~ +7.0	V
Power dissipation	Pd	400 *1	mW
Operating Temperature	Topr	-40 ~ +85	°C
Surrounding Temperature	Tstg	-55 ~ +125	°C
DC Input Voltage	VIN	-0.3 ~ VDD+0.3	V
DC Output Voltage	VOUT	-0.3 ~ VDD+0.3	V

\*1: Power dissipation is done at 4.0mW/°C for operation above Ta ≥ 25°C.

○ RECOMMENDED OPERATING RANGE (Ta=25°C, VSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage 1	VDD	2.2	-	5.5	V	
Supply voltage 2	VLCD	2.5	-	5.5	V	Following relation must be maintained. VLCD ≥ VC ≥ VSS
Oscillating Frequency	fOSC	-	36	-	kHz	Rf=470k Ω

○ BLOCK DIAGRAM



○ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Unless Otherwise Specified VDD=2.2V~5.5V, VSS=0V, Ta=25°C)

Parameter	Symbol	Rating			Unit	Condition	Terminal
		Min.	Typ.	Max.			
“H” Input Voltage	VIH1	$0.8 \times VDD$	-	VDD	V		OSC1, SD, SCK, C/D, CS
“L” Input Voltage	VIL1	0	-	$0.2 \times VDD$	V		
LCD Driver On-Resistance *2	RON	-	-	30	kΩ	$ \Delta VON =0.1V$	SEG0~18, COM1~4
“H” Input Current	I <sub>IH</sub>	-2	-	-	μA	V <sub>IN</sub> =VDD	OSC1, SD, SCK, C/D, CS
“L” Input Current	I <sub>IL</sub>	-	-	2	μA	V <sub>IN</sub> =0	OSC1, SD, SCK, C/D, CS
Input Capacitance	CI	-	5	-	pF		SD, SCK, C/D, CS
Operating Current	IDD	-	0.05	1	μA	Display OFF *3	VDD
		-	30	70	μA	Display ON *3	
		-	80	200	μA	Accessing *4	

\*2: LCD Driver On-Resistance doesn't include Internal Power Supply Impedance.

\*3: VLCD=VDD, Rf=470kΩ, All Input Pin except OSC1 connect VDD or VSS.

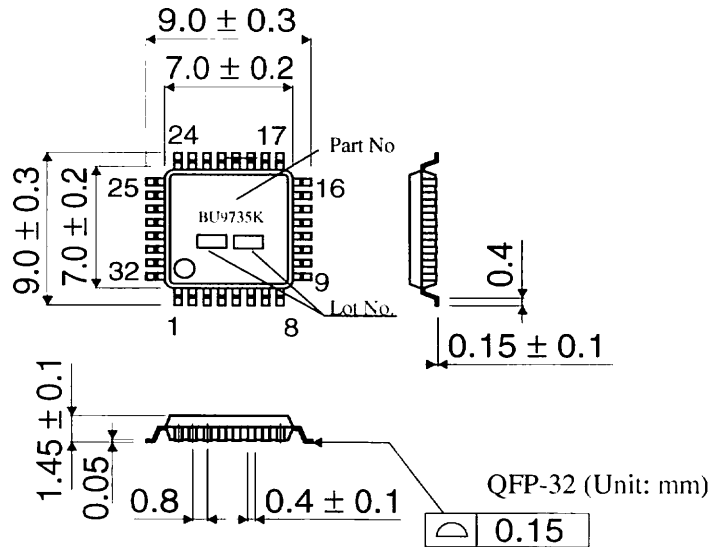
\*4: VLCD=VDD, Rf=470kΩ, fSCK=200kHz.

AC CHARACTERISTICS (Unless Otherwise Specified VDD=2.2V~5.5V、Ta=25°C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
SCK Rise Time	tTLH	-	-	100	ns	
SCK Fall Time	tTHL	-	-	100	ns	
SCK Cycle Time	tCYC	800	-	-	ns	
Command Wait Time	tWAIT	800	-	-	ns	
"H" SCK Pulse Width	tWH1	300	-	-	ns	
"L" SCK Pulse Width	tWL1	300	-	-	ns	
Data Set Up Time	tSU1	100	-	-	ns	
Data Hold Time	tH1	100	-	-	ns	
"H" $\overline{CS}$ Pulse Width	tWH2	300	-	-	ns	
"L" $\overline{CS}$ Pulse Width	tWL2	6400	-	-	ns	
$\overline{CS}$ Set Up Time	tSU2	100	-	-	ns	
$\overline{CS}$ Hold Time	tH2	100	-	-	ns	
$\overline{C/D}$ Set Up Time	tSU3	100	-	-	ns	
$\overline{C/D}$ Hold Time	tH3	100	-	-	ns	Reference rise 8 <sup>th</sup> Clock of SCK
$\overline{C/D}$ - $\overline{CS}$ Time *5	tCCH	100	-	-	ns	Reference rise $\overline{CS}$
$\overline{C/D}$ - SCK Time *5	tSCH	100	-	-	ns	Reference Fall 8 <sup>th</sup> Clock of SCK
Display start delay time						

\*5: Either of Them are Good enough.

○ Outline drawing



○ Terminal number, terminal name

Terminal No.	Terminal name	Terminal No.	Terminal name	Terminal No.	Terminal name	Terminal No.	Terminal name
1	OSC1	9	$\overline{CS}$	17	SEG3	25	SEG11
2	OSC2	10	$\overline{C/D}$	18	SEG4	26	SEG12
3	VSS	11	COM1	19	SEG5	27	SEG13
4	VC	12	COM2	20	SEG6	28	SEG14
5	VLCD	13	COM3	21	SEG7	29	SEG15
6	VDD	14	COM4	22	SEG8	30	SEG16
7	SCK	15	SEG1	23	SEG9	31	SEG17
8	SD	16	SEG2	24	SEG10	32	SEG18

○ Cautions on use

- (1) **Absolute Maximum Ratings**  
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.
- (2) **Operating conditions**  
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.
- (3) **Reverse connection of power supply connector**  
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.
- (4) **Power supply line**  
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.  
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.
- (5) **GND voltage**  
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.
- (6) **Short circuit between terminals and erroneous mounting**  
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.
- (7) **Operation in strong electromagnetic field**  
Be noted that using ICs in the strong electromagnetic field can malfunction them.
- (8) **Inspection with set PCB**  
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.
- (9) **Input terminals**  
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.
- (10) **Ground wiring pattern**  
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.
- (11) **External capacitor**  
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.
- (12) **No Connecting input terminals**  
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

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