

# MC74VHC4051, MC74VHC4052, MC74VHC4053

## Analog Multiplexers / Demultiplexers High-Performance Silicon-Gate CMOS

The MC74VHC4051, MC74VHC4052 and MC74VHC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from  $V_{CC}$  to  $V_{EE}$ ).

The VHC4051, VHC4052 and VHC4053 are identical in pinout to the high-speed HC4051A, HC4052A and HC4053A, and the metal-gate MC14051B, MC14052B and MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance ( $R_{on}$ ) is more linear over input voltage than  $R_{on}$  of metal-gate CMOS analog switches.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ( $V_{CC} - V_{EE}$ ) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ( $V_{CC} - GND$ ) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- Chip Complexity: VHC4051 — 184 FETs or 46 Equivalent Gates  
VHC4052 — 168 FETs or 42 Equivalent Gates  
VHC4053 — 156 FETs or 39 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



ON Semiconductor

<http://onsemi.com>

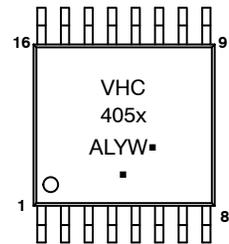
### MARKING DIAGRAMS



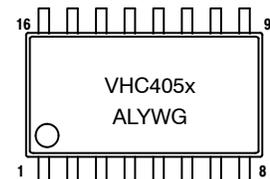
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOIC EIAJ-16  
M SUFFIX  
CASE 966



VHC405x = Specific Device Code  
(x = 1, 2 or 3)

A = Assembly Location

L, WL = Wafer Lot

Y, YY = Year

W, WW = Work Week

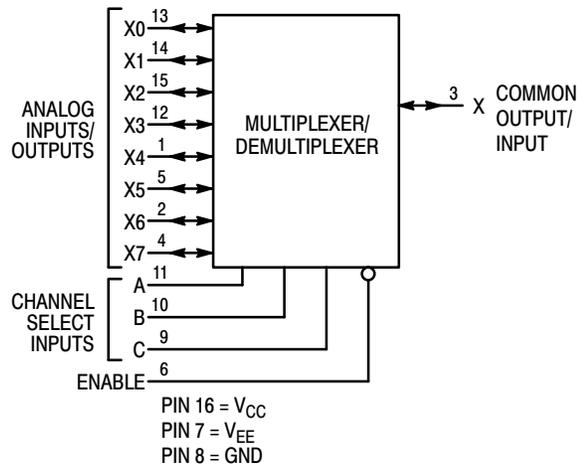
G or ▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

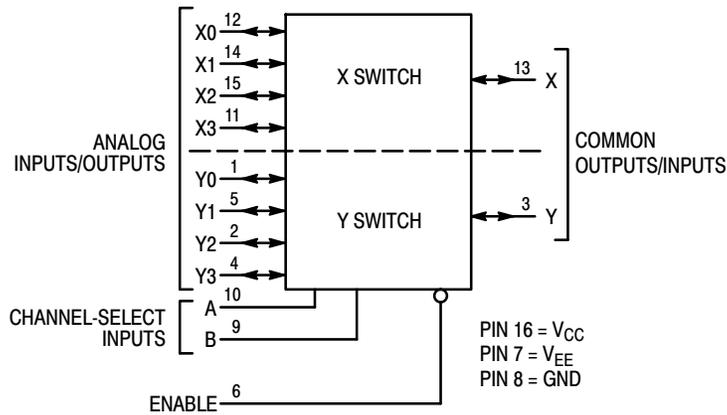
See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

**MC74VHC4051, MC74VHC4052, MC74VHC4053**



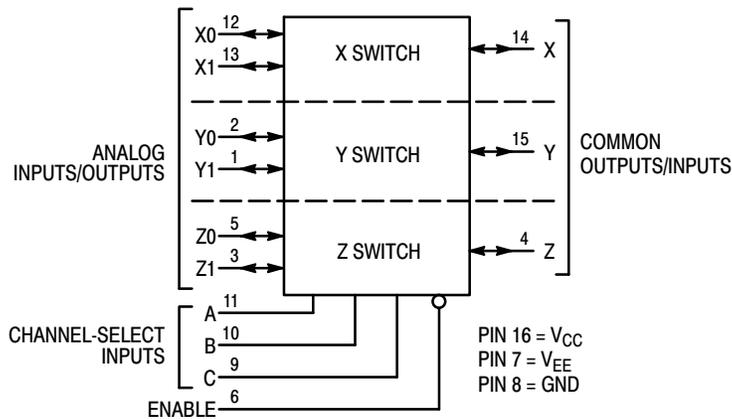
**MC74VHC4051**

**Single-Pole, 8-Position Plus Common Off**



**MC74VHC4052**

**Double-Pole, 4-Position Plus Common Off**



NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

**MC74VHC4053**

**Triple Single-Pole, Double-Position Plus Common Off**

**Figure 1. Logic Diagrams**

# MC74VHC4051, MC74VHC4052, MC74VHC4053

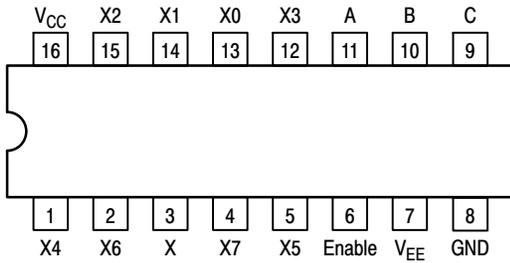


Figure 2. Pinout: MC74VHC4051 (Top View)

FUNCTION TABLE – MC74VHC4051

| Control Inputs |        |   |   | ON Channels |
|----------------|--------|---|---|-------------|
| Enable         | Select |   |   |             |
|                | C      | B | A |             |
| L              | L      | L | L | X0          |
| L              | L      | L | H | X1          |
| L              | L      | H | L | X2          |
| L              | L      | H | H | X3          |
| L              | H      | L | L | X4          |
| L              | H      | L | H | X5          |
| L              | H      | H | L | X6          |
| L              | H      | H | H | X7          |
| H              | X      | X | X | NONE        |

X = Don't Care

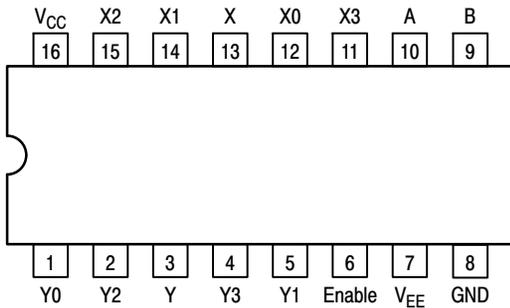


Figure 3. Pinout: MC74VHC4052 (Top View)

FUNCTION TABLE – MC74VHC4052

| Control Inputs |        |   |      | ON Channels |  |
|----------------|--------|---|------|-------------|--|
| Enable         | Select |   |      |             |  |
|                | B      | A |      |             |  |
| L              | L      | L | Y0   | X0          |  |
| L              | L      | H | Y1   | X1          |  |
| L              | H      | L | Y2   | X2          |  |
| L              | H      | H | Y3   | X3          |  |
| H              | X      | X | NONE |             |  |

X = Don't Care

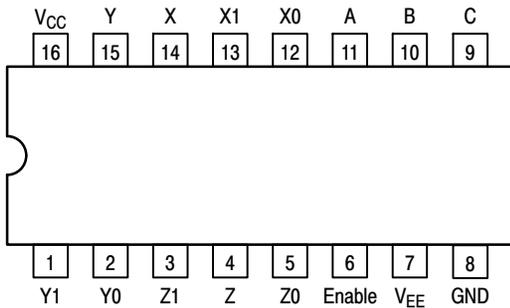


Figure 4. Pinout: MC74VHC4053 (Top View)

FUNCTION TABLE – MC74VHC4053

| Control Inputs |        |   |   | ON Channels |    |    |
|----------------|--------|---|---|-------------|----|----|
| Enable         | Select |   |   |             |    |    |
|                | C      | B | A |             |    |    |
| L              | L      | L | L | Z0          | Y0 | X0 |
| L              | L      | L | H | Z0          | Y0 | X1 |
| L              | L      | H | L | Z0          | Y1 | X0 |
| L              | L      | H | H | Z0          | Y1 | X1 |
| L              | H      | L | L | Z1          | Y0 | X0 |
| L              | H      | L | H | Z1          | Y0 | X1 |
| L              | H      | H | L | Z1          | Y1 | X0 |
| L              | H      | H | H | Z1          | Y1 | X1 |
| H              | X      | X | X | NONE        |    |    |

X = Don't Care

# MC74VHC4051, MC74VHC4052, MC74VHC4053

## MAXIMUM RATINGS\*

| Symbol    | Parameter   | Value                               | Unit |
|-----------|---|-------------------------------------|------|
| $V_{CC}$  | Positive DC Supply Voltage (Referenced to GND)<br>(Referenced to $V_{EE}$ ) | - 0.5 to + 7.0<br>- 0.5 to + 14.0   | V    |
| $V_{EE}$  | Negative DC Supply Voltage (Referenced to GND)                              | - 7.0 to + 5.0                      | V    |
| $V_{IS}$  | Analog Input Voltage  | $V_{EE} - 0.5$ to<br>$V_{CC} + 0.5$ | V    |
| $V_{in}$  | Digital Input Voltage (Referenced to GND)                                   | - 0.5 to $V_{CC} + 0.5$             | V    |
| I         | DC Current, Into or Out of Any Pin  | $\pm 25$                            | mA   |
| $P_D$     | Power Dissipation in Still Air<br>SOIC Package†<br>TSSOP Package†           | 500<br>450                          | mW   |
| $T_{stg}$ | Storage Temperature Range   | - 65 to + 150                       | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds                             | 260                                 | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol     | Parameter   | Min                             | Max                       | Unit |
|------------|---|---------------------------------|---------------------------|------|
| $V_{CC}$   | Positive DC Supply Voltage (Referenced to GND)<br>(Referenced to $V_{EE}$ ) | 2.0<br>2.0                      | 6.0<br>12.0               | V    |
| $V_{EE}$   | Negative DC Supply Voltage, Output (Referenced to GND)                      | - 6.0                           | GND                       | V    |
| $V_{IS}$   | Analog Input Voltage  | $V_{EE}$                        | $V_{CC}$                  | V    |
| $V_{in}$   | Digital Input Voltage (Referenced to GND)                                   | GND                             | $V_{CC}$                  | V    |
| $V_{IO}^*$ | Static or Dynamic Voltage Across Switch                                     |                                 | 1.2                       | V    |
| $T_A$      | Operating Temperature Range, All Package Types                              | - 55                            | + 125                     | °C   |
| $t_r, t_f$ | Input Rise/Fall Time<br>(Channel Select or Enable Inputs)                   | $V_{CC} = 2.0$ V<br>0<br>0<br>0 | 1000<br>800<br>500<br>400 | ns   |

\*For voltage drops across switch greater than 1.2V (switch on), excessive  $V_{CC}$  current may be drawn; i.e., the current out of the switch may contain both  $V_{CC}$  and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

# MC74VHC4051, MC74VHC4052, MC74VHC4053

## DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = \text{GND}$ , Except Where Noted

| Symbol   | Parameter   | Condition   | $V_{CC}$<br>V | Guaranteed Limit |       |        | Unit |
|----------|---|---|---------------|------------------|-------|--------|------|
|          |   |   |               | -55 to 25°C      | ≤85°C | ≤125°C |      |
| $V_{IH}$ | Minimum High-Level Input Voltage, Channel-Select or Enable Inputs | $R_{on} = \text{Per Spec}$  | 2.0           | 1.50             | 1.50  | 1.50   | V    |
|          |   |   | 3.0           | 2.10             | 2.10  | 2.10   |      |
|          |   |   | 4.5           | 3.15             | 3.15  | 3.15   |      |
|          |   |   | 6.0           | 4.20             | 4.20  | 4.20   |      |
| $V_{IL}$ | Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs  | $R_{on} = \text{Per Spec}$  | 2.0           | 0.5              | 0.5   | 0.5    | V    |
|          |   |   | 3.0           | 0.9              | 0.9   | 0.9    |      |
|          |   |   | 4.5           | 1.35             | 1.35  | 1.35   |      |
|          |   |   | 6.0           | 1.8              | 1.8   | 1.8    |      |
| $I_{in}$ | Maximum Input Leakage Current, Channel-Select or Enable Inputs    | $V_{in} = V_{CC}$ or GND,<br>$V_{EE} = -6.0 \text{ V}$  | 6.0           | ± 0.1            | ± 1.0 | ± 1.0  | μA   |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package)                    | Channel Select, Enable and<br>$V_{IS} = V_{CC}$ or GND; $V_{EE} = \text{GND}$<br>$V_{IO} = 0 \text{ V}$ $V_{EE} = -6.0$ | 6.0           | 1                | 10    | 40     | μA   |
|          |   |   | 6.0           | 4                | 40    | 80     |      |

## DC ELECTRICAL CHARACTERISTICS Analog Section

| Symbol          | Parameter  | Test Conditions   | $V_{CC}$<br>V                                       | $V_{EE}$<br>V   | Guaranteed Limit |        |         | Unit |     |
|-----------------|--|---|---|---|------------------|--------|---------|------|-----|
|                 |  |   |   |   | - 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |     |
| $R_{on}$        | Maximum "ON" Resistance  | $V_{in} = V_{IL}$ or $V_{IH}$<br>$V_{IS} = V_{CC}$ to $V_{EE}$<br>$I_S \leq 2.0 \text{ mA}$<br>(Figures 5 through 11)             | 3.0   | 0.0   | 200              | 240    | 320     | Ω    |     |
|                 |  |   | 4.5   | 0.0   | 160              | 200    | 280     |      |     |
|                 |  | 4.5   | - 4.5   | 120   | 150              | 170    |         |      |     |
|                 |  | 6.0   | - 6.0   | 100   | 125              | 140    |         |      |     |
|                 |  | $V_{in} = V_{IL}$ or $V_{IH}$<br>$V_{IS} = V_{CC}$ or $V_{EE}$ (Endpoints)<br>$I_S \leq 2.0 \text{ mA}$<br>(Figures 5 through 11) | 3.0   | 0.0   | 150              | 180    | 230     |      |     |
|                 |  |   | 4.5   | 0.0   | 110              | 140    | 190     |      |     |
| $\Delta R_{on}$ | Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package | $V_{in} = V_{IL}$ or $V_{IH}$<br>$V_{IS} = 1/2 (V_{CC} - V_{EE})$<br>$I_S \leq 2.0 \text{ mA}$                                    | 3.0   | 0.0   | 40               | 50     | 80      | Ω    |     |
|                 |  |   | 4.5   | 0.0   | 20               | 25     | 40      |      |     |
|                 |  |   | 4.5   | - 4.5   | 10               | 15     | 18      |      |     |
|                 |  |   | 6.0   | - 6.0   | 10               | 12     | 14      |      |     |
| $I_{off}$       | Maximum Off-Channel Leakage Current, Any One Channel                               | $V_{in} = V_{IL}$ or $V_{IH}$ ;<br>$V_{IO} = V_{CC} - V_{EE}$ ;<br>Switch Off (Figure 12)   | 6.0   | - 6.0   | 0.1              | 0.5    | 1.0     | μA   |     |
|                 |  |   | Maximum Off-Channel Leakage Current, Common Channel | $V_{in} = V_{IL}$ or $V_{IH}$ ;<br>$V_{IO} = V_{CC} - V_{EE}$ ;<br>Switch Off (Figure 13) | 6.0              | - 6.0  | 0.2     |      | 2.0 |
|                 | VHC4052  | 6.0   |   |   | - 6.0            | 0.1    | 1.0     |      | 2.0 |
| $I_{on}$        | Maximum On-Channel Leakage Current, Channel-to-Channel                             | $V_{in} = V_{IL}$ or $V_{IH}$ ;<br>Switch-to-Switch =<br>$V_{CC} - V_{EE}$ ; (Figure 14)  | VHC4051   | 6.0   | - 6.0            | 0.2    | 2.0     | 4.0  | μA  |
|                 |  |   | VHC4052   | 6.0   | - 6.0            | 0.1    | 1.0     | 2.0  |     |
|                 |  |   | VHC4053   | 6.0   | - 6.0            | 0.1    | 1.0     | 2.0  |     |

# MC74VHC4051, MC74VHC4052, MC74VHC4053

## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter  | V <sub>CC</sub><br>V   | Guaranteed Limit |       |        | Unit |
|--|--|--|------------------|-------|--------|------|
|  |  |  | -55 to 25°C      | ≤85°C | ≤125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Channel-Select to Analog Output<br>(Figures 18, 19) | 2.0  | 270              | 320   | 350    | ns   |
|  |  | 3.0  | 90               | 110   | 125    |      |
|  |  | 4.5  | 59               | 79    | 85     |      |
|  |  | 6.0  | 45               | 65    | 75     |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Analog Input to Analog Output<br>(Figures 20, 21)   | 2.0  | 40               | 60    | 70     | ns   |
|  |  | 3.0  | 25               | 30    | 32     |      |
|  |  | 4.5  | 12               | 15    | 18     |      |
|  |  | 6.0  | 10               | 13    | 15     |      |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Enable to Analog Output<br>(Figures 22, 23)         | 2.0  | 160              | 200   | 220    | ns   |
|  |  | 3.0  | 70               | 95    | 110    |      |
|  |  | 4.5  | 48               | 63    | 76     |      |
|  |  | 6.0  | 39               | 55    | 63     |      |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Enable to Analog Output<br>(Figures 22, 23)         | 2.0  | 245              | 315   | 345    | ns   |
|  |  | 3.0  | 115              | 145   | 155    |      |
|  |  | 4.5  | 49               | 69    | 83     |      |
|  |  | 6.0  | 39               | 58    | 67     |      |
| C <sub>in</sub>                        | Maximum Input Capacitance, Channel-Select or Enable Inputs                     |  | 10               | 10    | 10     | pF   |
| C <sub>I/O</sub>                       | Maximum Capacitance<br>(All Switches Off)                                      | Analog I/O   | 35               | 35    | 35     | pF   |
|  |  | Common O/I: VHC4051  | 130              | 130   | 130    |      |
|  |  | VHC4052  | 80               | 80    | 80     |      |
|  |  | VHC4053  | 50               | 50    | 50     |      |
|  | Feedthrough  |  | 1.0              | 1.0   | 1.0    |      |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Figure 25)*                                     | Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V |                  |       | pF     |      |
|  |  | VHC4051  | 45               |       |        |      |
|  |  | VHC4052  | 80               |       |        |      |
|  |  | VHC4053  | 45               |       |        |      |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74VHC4051, MC74VHC4052, MC74VHC4053

## ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

| Symbol | Parameter   | Condition  | V <sub>CC</sub><br>V | V <sub>EE</sub><br>V | Limit* |     |     | Unit             |
|--------|---|--|----------------------|----------------------|--------|-----|-----|------------------|
|        |   |  |                      |                      | 25°C   |     |     |                  |
| BW     | Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 15)          | f <sub>in</sub> = 1MHz Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>OS</sub> ; Increase f <sub>in</sub> Frequency Until dB Meter Reads -3dB; R <sub>L</sub> = 50Ω, C <sub>L</sub> = 10pF   | 2.25                 | -2.25                | '51    | '52 | '53 | MHz              |
|        |   |  | 4.50                 | -4.50                | 80     | 95  | 120 |                  |
|        |   |  | 6.00                 | -6.00                | 80     | 95  | 120 |                  |
| —      | Off-Channel Feedthrough Isolation (Figure 16)                                   | f <sub>in</sub> = Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>IS</sub><br>f <sub>in</sub> = 10kHz, R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF   | 2.25                 | -2.25                | -50    |     |     | dB               |
|        |   |  | 4.50                 | -4.50                | -50    |     |     |                  |
| —      | Feedthrough Noise. Channel-Select Input to Common I/O (Figure 17)               | V <sub>in</sub> ≤ 1MHz Square Wave (t <sub>r</sub> = t <sub>f</sub> = 6ns); Adjust R <sub>L</sub> at Setup so that I <sub>S</sub> = 0A; Enable = GND R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF  | 2.25                 | -2.25                | 25     |     |     | mV <sub>PP</sub> |
|        |   |  | 4.50                 | -4.50                | 105    |     |     |                  |
| —      | Crosstalk Between Any Two Switches (Figure 24) (Test does not apply to VHC4051) | f <sub>in</sub> = Sine Wave; Adjust f <sub>in</sub> Voltage to Obtain 0dBm at V <sub>IS</sub><br>f <sub>in</sub> = 10kHz, R <sub>L</sub> = 600Ω, C <sub>L</sub> = 50pF   | 2.25                 | -2.25                | -50    |     |     | dB               |
|        |   |  | 4.50                 | -4.50                | -50    |     |     |                  |
| —      | Crosstalk Between Any Two Switches (Figure 24) (Test does not apply to VHC4051) | f <sub>in</sub> = 1.0MHz, R <sub>L</sub> = 50Ω, C <sub>L</sub> = 10pF  | 2.25                 | -2.25                | -60    |     |     | dB               |
|        |   |  | 4.50                 | -4.50                | -60    |     |     |                  |
| THD    | Total Harmonic Distortion (Figure 26)   | f <sub>in</sub> = 1kHz, R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 50pF<br>THD = THD <sub>measured</sub> - THD <sub>source</sub><br>V <sub>IS</sub> = 4.0V <sub>PP</sub> sine wave<br>V <sub>IS</sub> = 8.0V <sub>PP</sub> sine wave<br>V <sub>IS</sub> = 11.0V <sub>PP</sub> sine wave | 2.25                 | -2.25                | 0.10   |     |     | %                |
|        |   |  | 4.50                 | -4.50                | 0.08   |     |     |                  |
| —      | Total Harmonic Distortion (Figure 26)   | f <sub>in</sub> = 1kHz, R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 50pF<br>THD = THD <sub>measured</sub> - THD <sub>source</sub><br>V <sub>IS</sub> = 4.0V <sub>PP</sub> sine wave<br>V <sub>IS</sub> = 8.0V <sub>PP</sub> sine wave<br>V <sub>IS</sub> = 11.0V <sub>PP</sub> sine wave | 6.00                 | -6.00                | 0.05   |     |     | %                |
|        |   |  | 6.00                 | -6.00                | 0.05   |     |     |                  |

\*Limits not tested. Determined by design and verified by qualification.

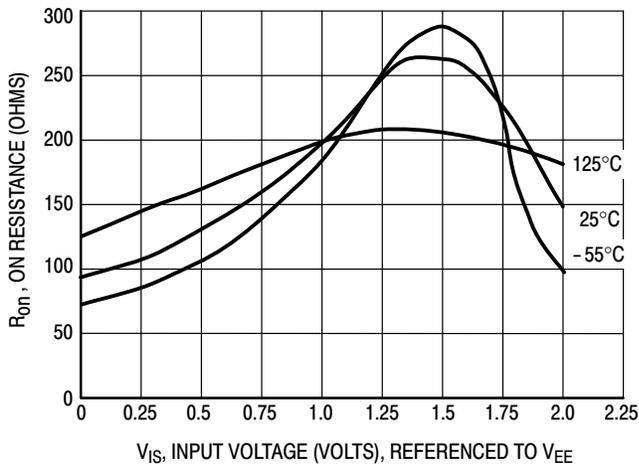


Figure 5. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 2.0 V

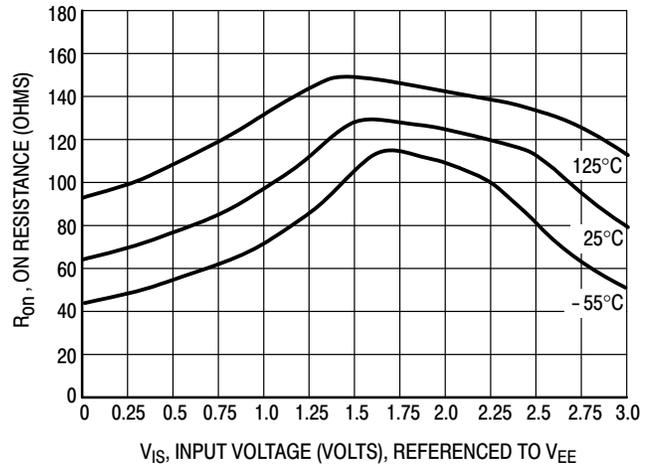


Figure 6. Typical On Resistance, V<sub>CC</sub> - V<sub>EE</sub> = 3.0 V

# MC74VHC4051, MC74VHC4052, MC74VHC4053

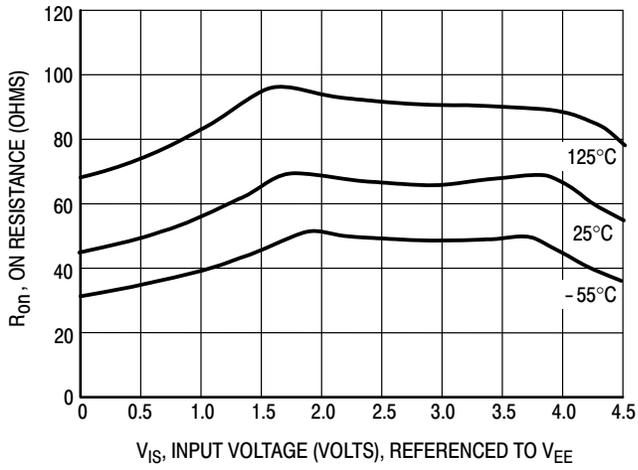


Figure 7. Typical On Resistance,  $V_{CC} - V_{EE} = 4.5$  V

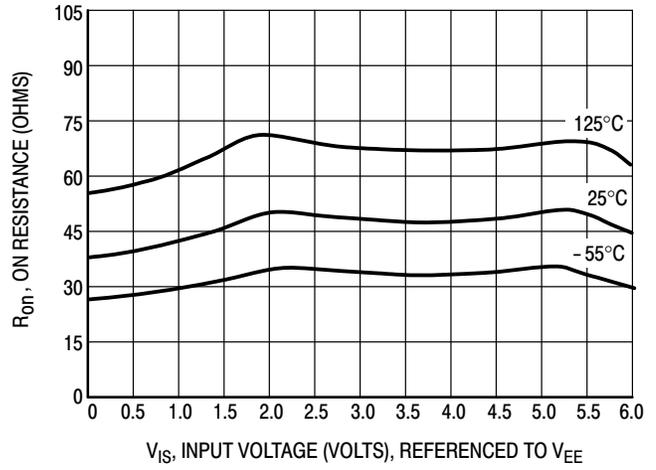


Figure 8. Typical On Resistance,  $V_{CC} - V_{EE} = 6.0$  V

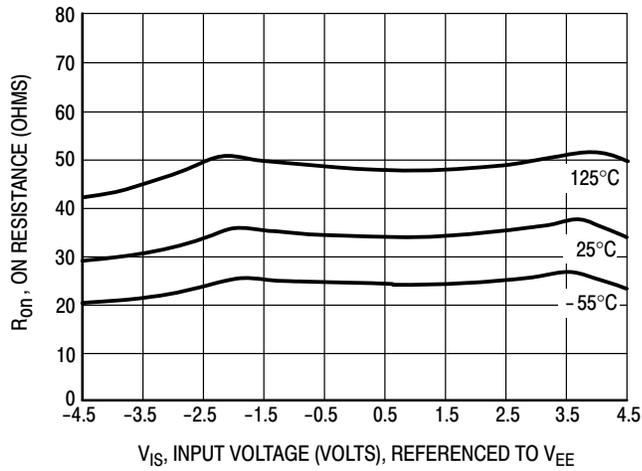


Figure 9. Typical On Resistance,  $V_{CC} - V_{EE} = 9.0$  V

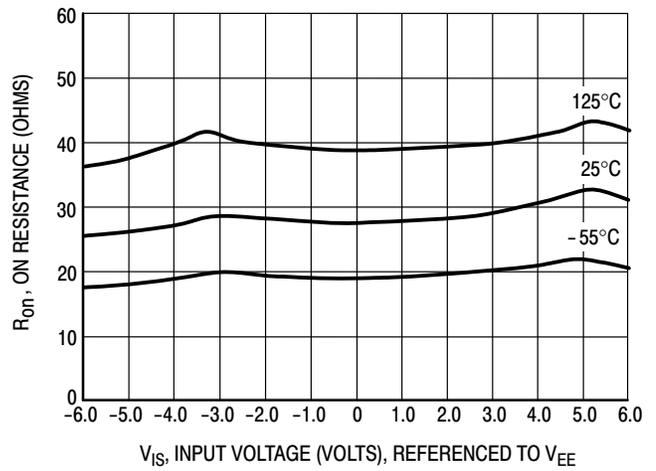


Figure 10. Typical On Resistance,  $V_{CC} - V_{EE} = 12.0$  V

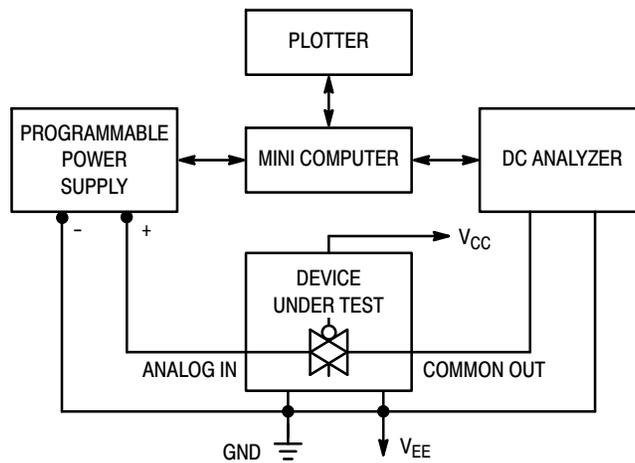


Figure 11. On Resistance Test Set-Up

MC74VHC4051, MC74VHC4052, MC74VHC4053

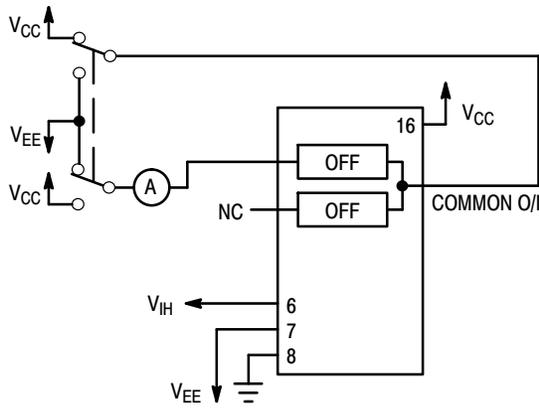


Figure 12. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

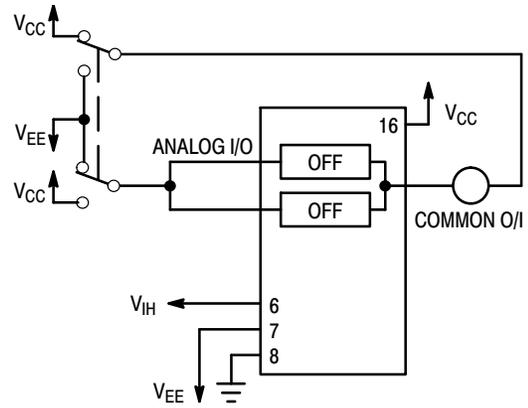


Figure 13. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

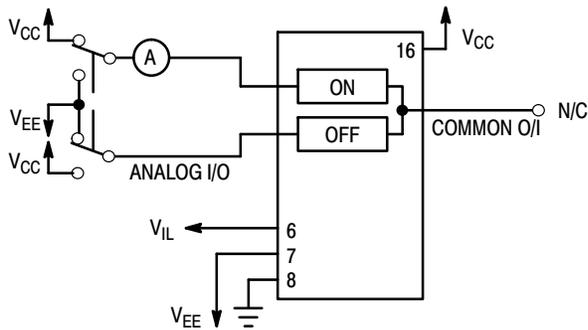
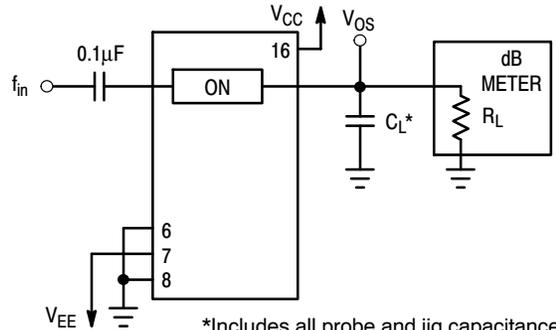
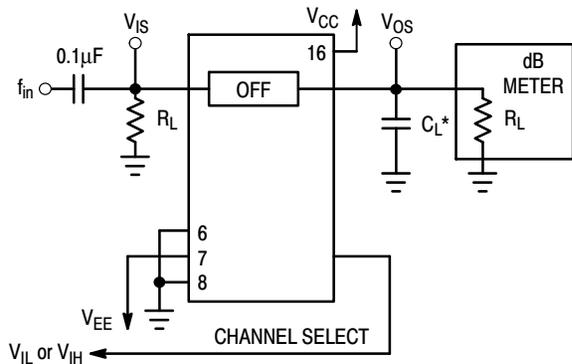


Figure 14. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up



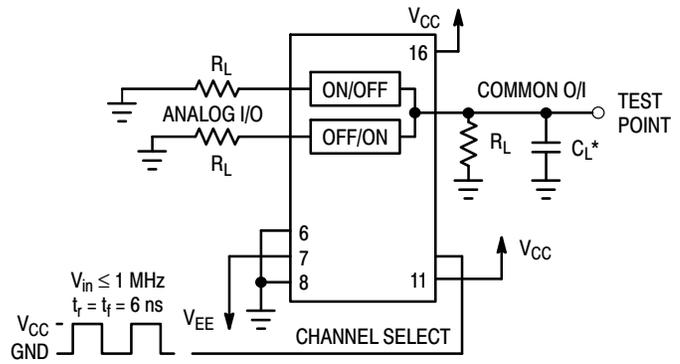
\*Includes all probe and jig capacitance

Figure 15. Maximum On Channel Bandwidth, Test Set-Up



\*Includes all probe and jig capacitance

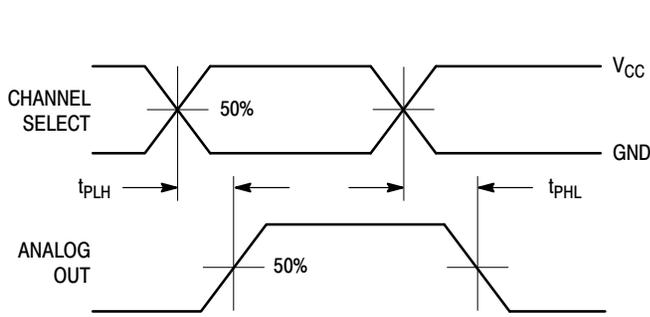
Figure 16. Off Channel Feedthrough Isolation, Test Set-Up



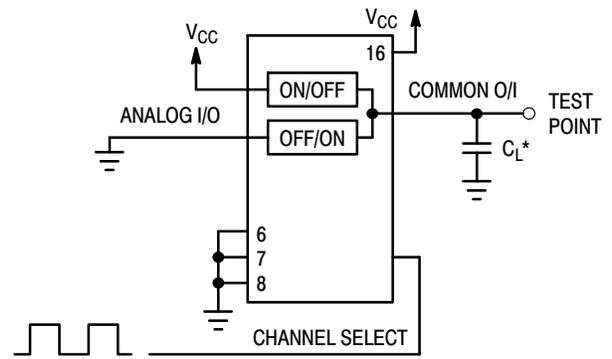
\*Includes all probe and jig capacitance

Figure 17. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

# MC74VHC4051, MC74VHC4052, MC74VHC4053

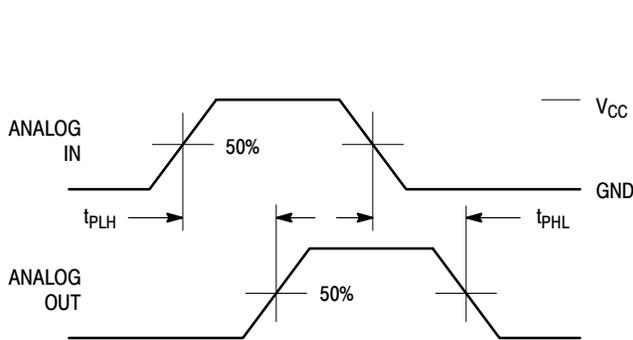


**Figure 18. Propagation Delays, Channel Select to Analog Out**

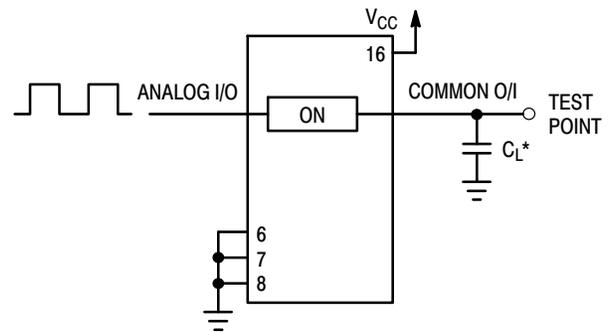


\*Includes all probe and jig capacitance

**Figure 19. Propagation Delay, Test Set-Up Channel Select to Analog Out**

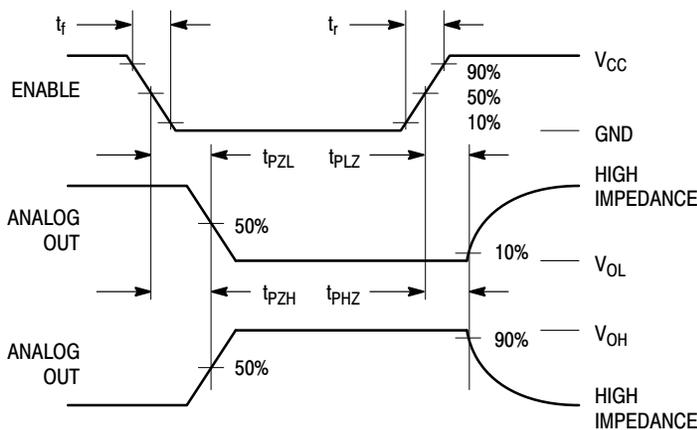


**Figure 20. Propagation Delays, Analog In to Analog Out**

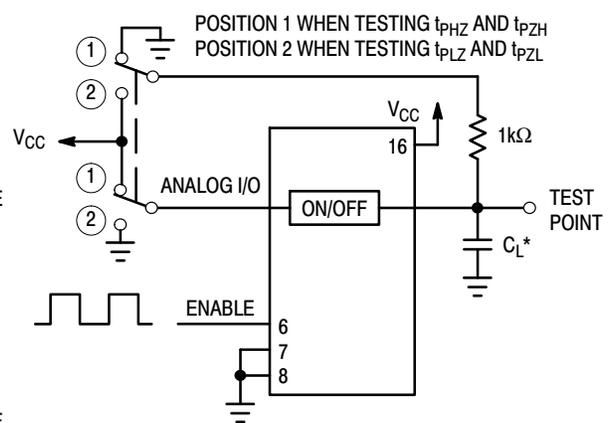


\*Includes all probe and jig capacitance

**Figure 21. Propagation Delay, Test Set-Up Analog In to Analog Out**

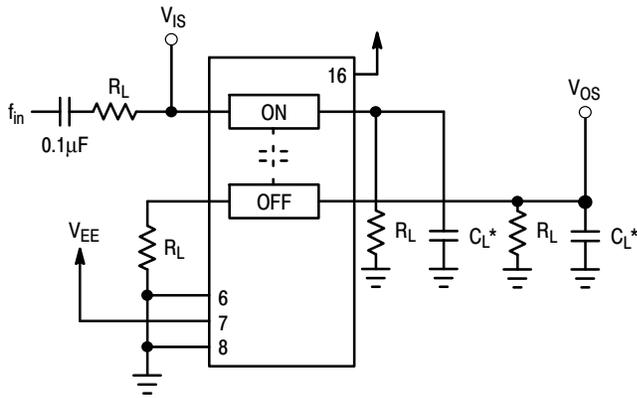


**Figure 22. Propagation Delays, Enable to Analog Out**



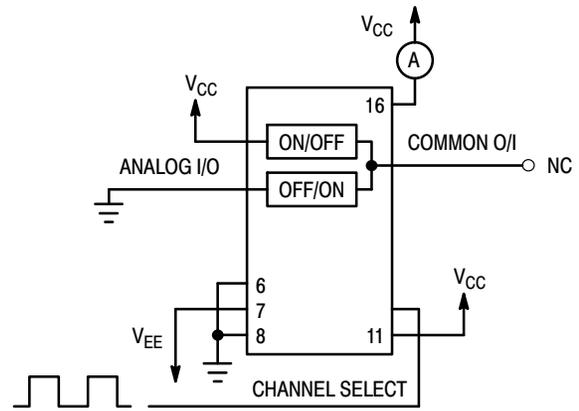
**Figure 23. Propagation Delay, Test Set-Up Enable to Analog Out**

## MC74VHC4051, MC74VHC4052, MC74VHC4053

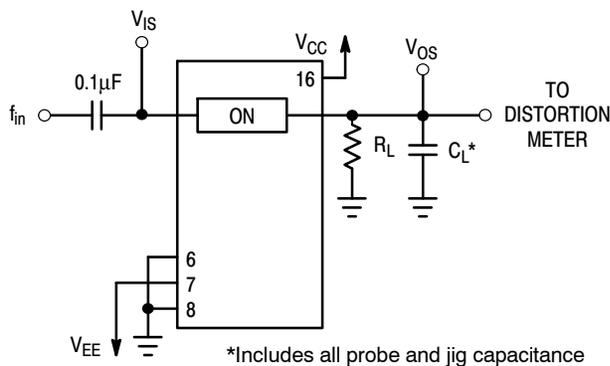


\*Includes all probe and jig capacitance

**Figure 24. Crosstalk Between Any Two Switches, Test Set-Up**

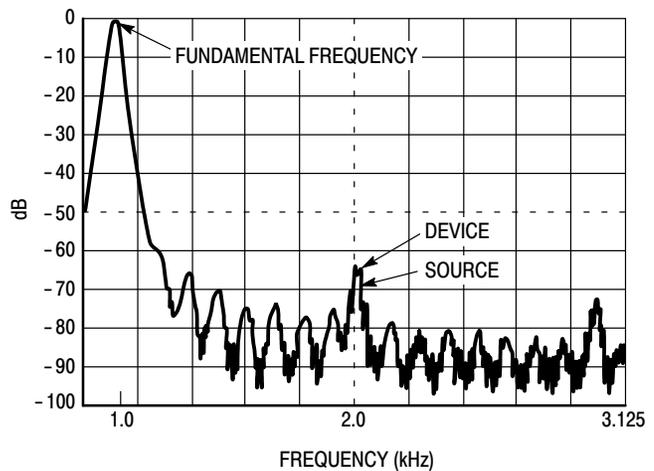


**Figure 25. Power Dissipation Capacitance, Test Set-Up**



\*Includes all probe and jig capacitance

**Figure 26. Total Harmonic Distortion, Test Set-Up**



**Figure 27. Plot, Harmonic Distortion**

## APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at  $V_{CC}$  or GND logic levels.  $V_{CC}$  being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5V = \text{logic high} \\ \text{GND} &= 0V = \text{logic low} \end{aligned}$$

The maximum analog voltage swings are determined by the supply voltages  $V_{CC}$  and  $V_{EE}$ . The positive peak analog voltage should not exceed  $V_{CC}$ . Similarly, the negative peak analog voltage should not go below  $V_{EE}$ . In this example, the difference between  $V_{CC}$  and  $V_{EE}$  is ten volts. Therefore, using the configuration of Figure 28, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

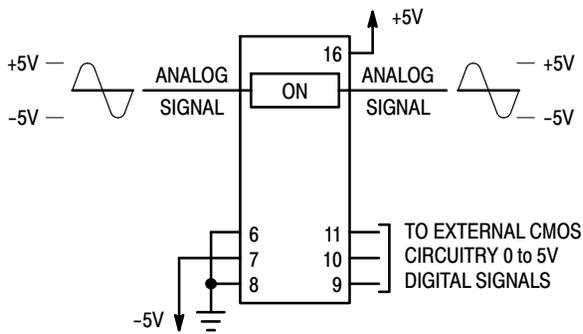
outputs to  $V_{CC}$  or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

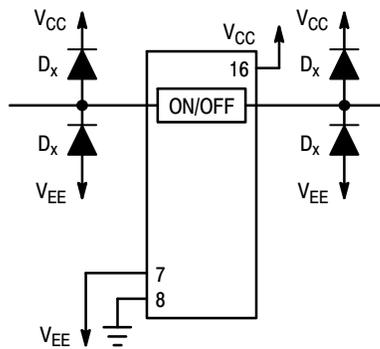
$$\begin{aligned} V_{CC} - \text{GND} &= 2 \text{ to } 6 \text{ volts} \\ V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ volts} \\ &\text{and } V_{EE} \leq \text{GND} \end{aligned}$$

When voltage transients above  $V_{CC}$  and/or below  $V_{EE}$  are anticipated on the analog channels, external Germanium or Schottky diodes ( $D_x$ ) are recommended as shown in Figure 29. These diodes should be able to absorb the maximum anticipated current surges during clipping.

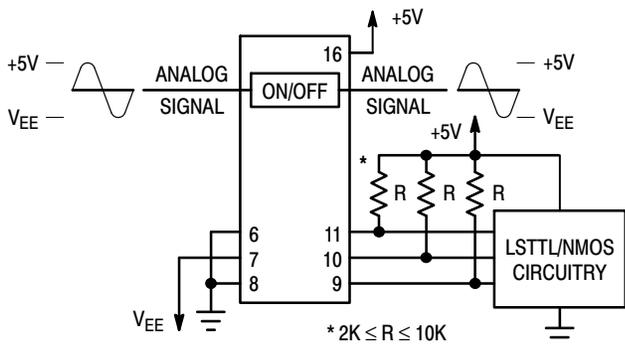
**MC74VHC4051, MC74VHC4052, MC74VHC4053**



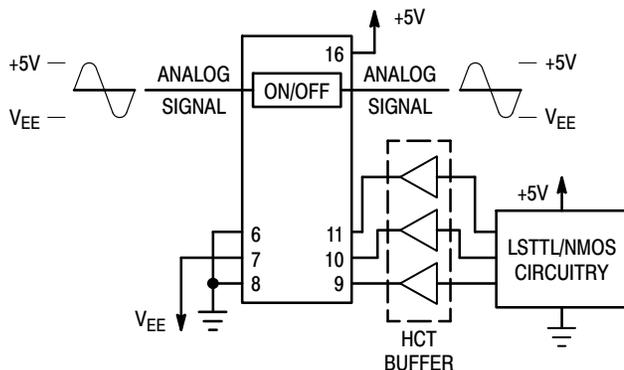
**Figure 28. Application Example**



**Figure 29. External Germanium or Schottky Clipping Diodes**

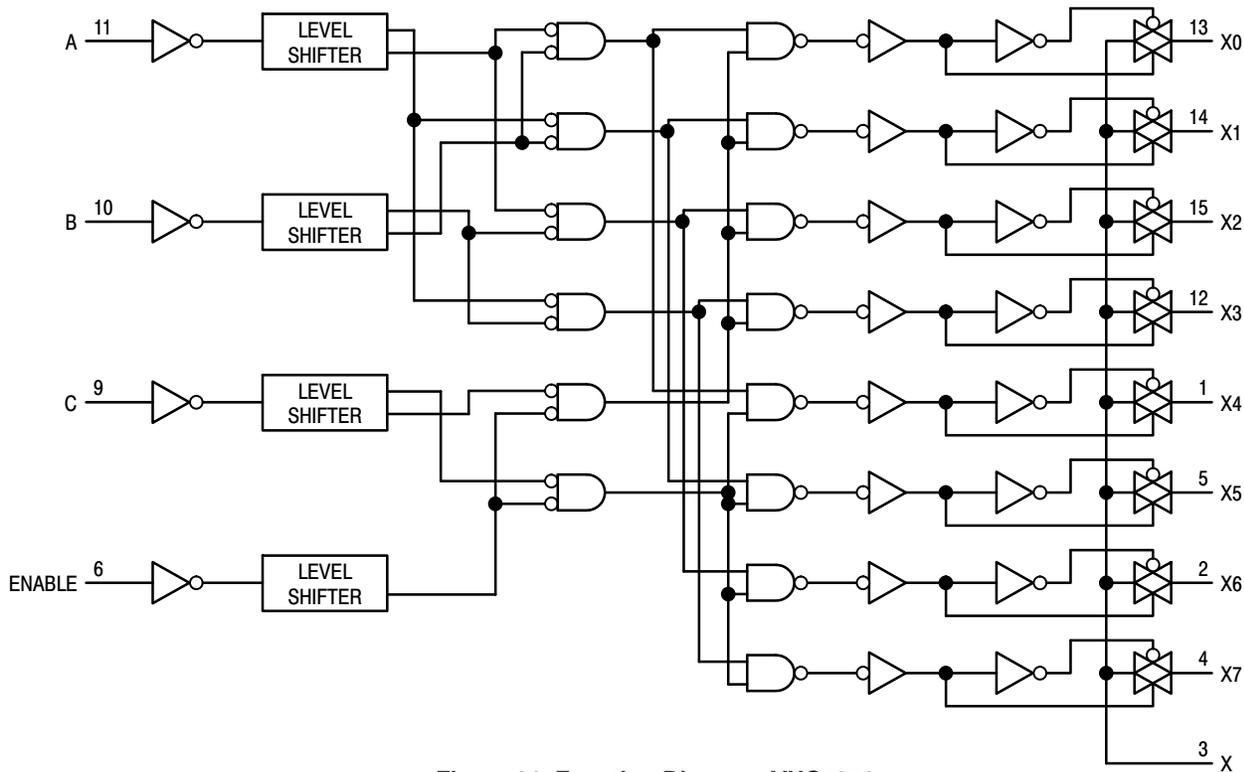


**a. Using Pull-Up Resistors**



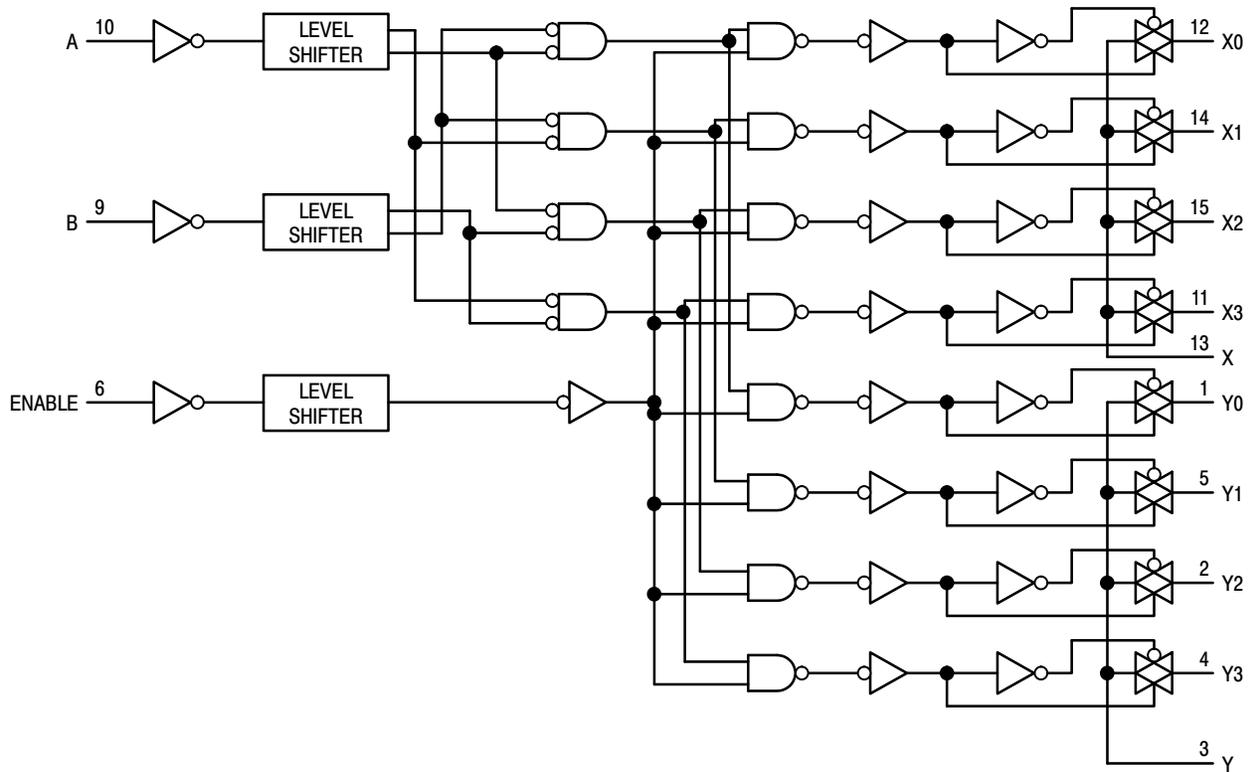
**b. Using HCT Interface**

**Figure 30. Interfacing LSTTL/NMOS to CMOS Inputs**

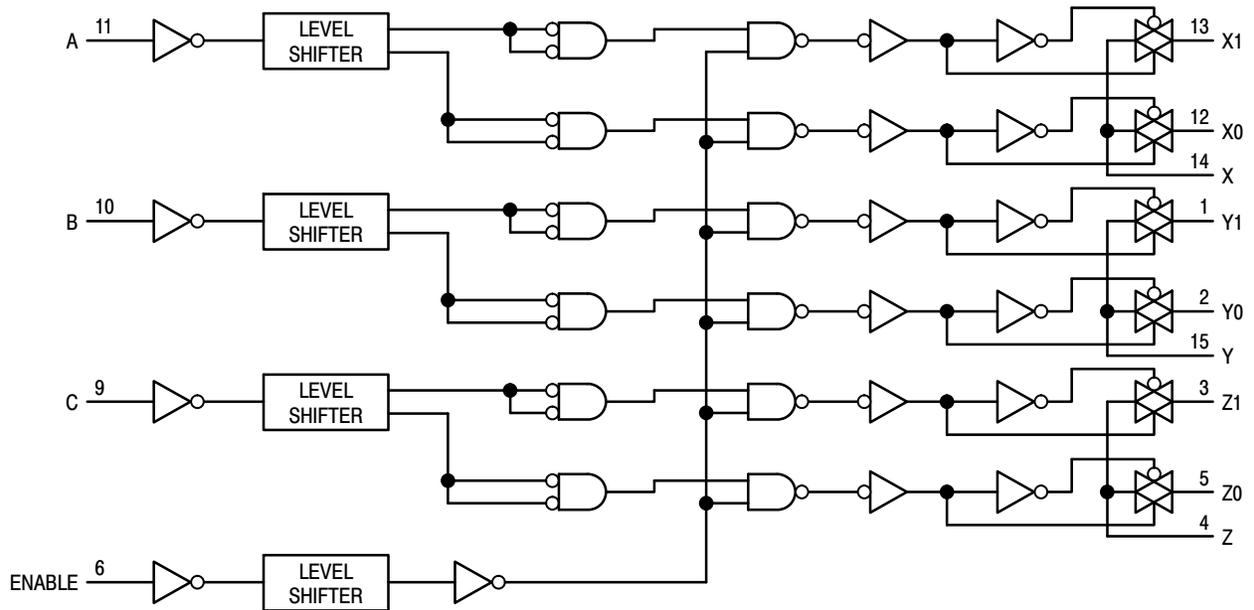


**Figure 31. Function Diagram, VHC4051**

**MC74VHC4051, MC74VHC4052, MC74VHC4053**



**Figure 33. Function Diagram, VHC4052**



**Figure 32. Function Diagram, VHC4053**

## MC74VHC4051, MC74VHC4052, MC74VHC4053

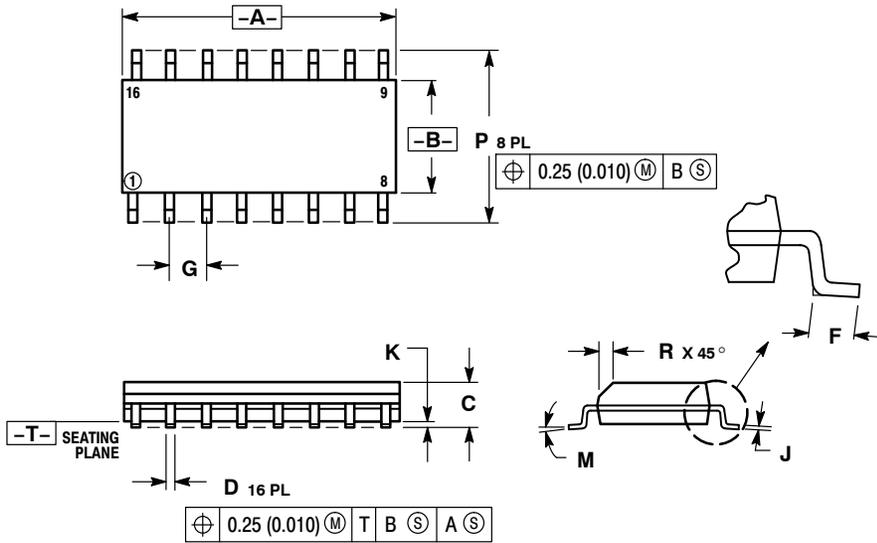
### ORDERING & SHIPPING INFORMATION

| Device           | Package   | Shipping                 |
|------------------|-----------|--------------------------|
| MC74VHC4051DR2G  | SOIC-16   | 2500 Units / Tape & Reel |
| MC74VHC4051DTR2G | TSSOP-16  | 2500 Units / Tape & Reel |
| MC74VHC4052DR2G  | SOIC-16   | 2500 Units / Tape & Reel |
| MC74VHC4052DTR2G | TSSOP-16  | 2500 Units / Tape & Reel |
| MC74VHC4053DR2G  | SOIC-16   | 2500 Units / Tape & Reel |
| MC74VHC4053DTR2G | TSSOP-16  | 2500 Units / Tape & Reel |
| MC74VHC4051MG    | SOEIAJ-16 | 50 Units / Rail          |
| MC74VHC4052MG    | SOEIAJ-16 | 50 Units / Rail          |
| MC74VHC4052MELG  | SOEIAJ-16 | 2000 Units / Reel        |
| MC74VHC4053MG    | SOEIAJ-16 | 50 Units / Rail          |

# MC74VHC4051, MC74VHC4052, MC74VHC4053

## PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

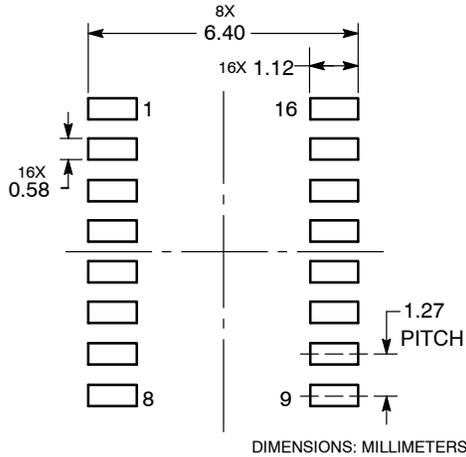


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0° 7°       |       | 0° 7°     |       |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

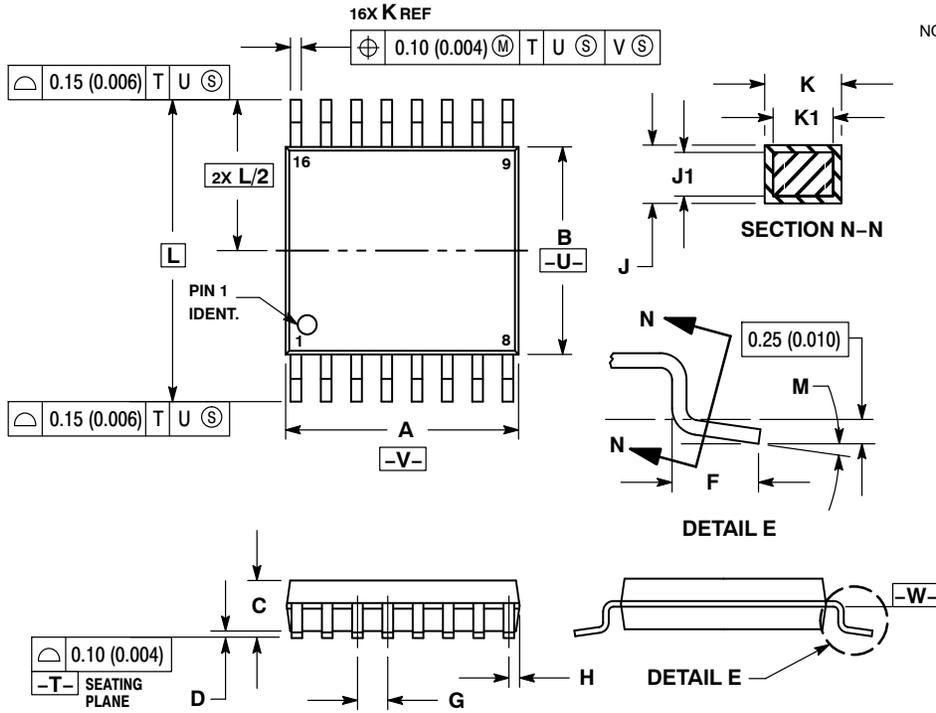
### SOLDERING FOOTPRINT



# MC74VHC4051, MC74VHC4052, MC74VHC4053

## PACKAGE DIMENSIONS

TSSOP-16  
CASE 948F-01  
ISSUE B

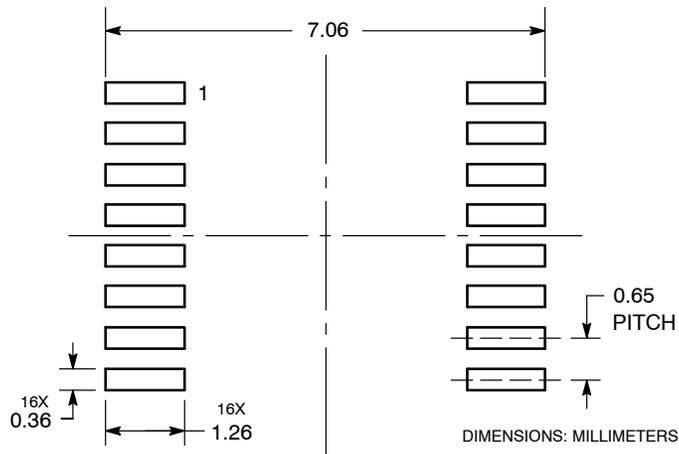


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

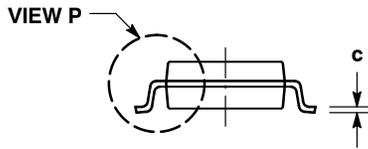
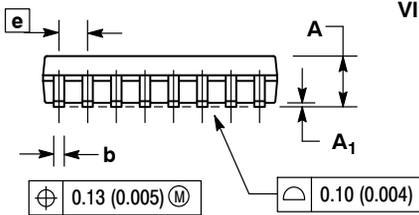
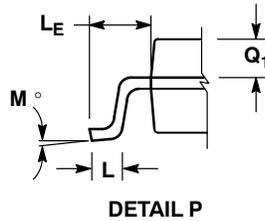
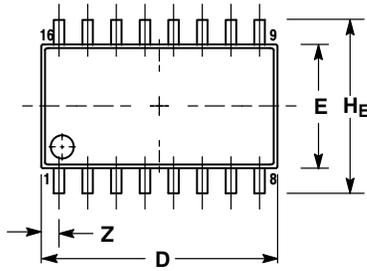
### SOLDERING FOOTPRINT



# MC74VHC4051, MC74VHC4052, MC74VHC4053

## PACKAGE DIMENSIONS

SOEIAJ-16  
CASE 966-01  
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.10        | 0.20  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| HE             | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| LE             | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.78  | ---       | 0.031 |

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative



## Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

### Наши контакты:

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331