

## Features

- Programmable Audio Output for Interfacing with Common Audio DAC
  - PCM Format Compatible
  - I<sup>2</sup>S Format Compatible
- 8-bit MCU C51 Core-based ( $F_{MAX} = 20$  MHz)
- 2304 Bytes of Internal RAM
- 64K Bytes of Code Memory
  - AT89C5132: Flash (100K Write/Erase Cycles)
- 4K Bytes of Boot Flash Memory (AT89C5132)
  - ISP: Download from USB or UART to any External Memory Cards
- USB Rev 1.1 Device Controller
  - “Full Speed” Data Transmission
- Built-in PLL
- MultiMedia Card<sup>®</sup> Interface Compatibility
- Atmel DataFlash<sup>®</sup> SPI Interface Compatibility
- IDE/ATAPI Interface
- 2 Channels 10-bit ADC, 8 kHz (8 True Bits)
  - Battery Voltage Monitoring
  - Voice Recording Controlled by Software
- Up to 44 Bits of General-purpose I/Os
  - 4-bit Interrupt Keyboard Port for a 4 x n Matrix
  - SmartMedia<sup>®</sup> Software Interface
- Two Standard 16-bit Timers/Counters
- Hardware Watchdog Timer
- Standard Full Duplex UART with Baud Rate Generator
- Two Wire Master and Slave Modes Controller
- SPI Master and Slave Modes Controller
- Power Management
  - Power-on Reset
  - Software Programmable MCU Clock
  - Idle Mode, Power-down Mode
- Operating Conditions
  - 3V,  $\pm 10\%$ , 25 mA Typical Operating at 25°C
  - Temperature Range: -40°C to +85°C
- Packages
  - TQFP80, PLCC84 (Development Board Only)
  - Dice

## Description

The AT89C5132 is a mass storage device controlling data exchange between various Flash modules, HDD and CD-ROM.

The AT89C5132 includes 64K Bytes of Flash memory and allows In-System Programming through an embedded 4K Bytes of Boot Flash Memory.

The AT89C5132 include 2304 Bytes of RAM memory.

The AT89C5132 provides all the necessary features for man-machine interface including, timers, keyboard port, serial or parallel interface (USB, SPI, IDE), ADC input, I<sup>2</sup>S output, and all external memory interface (NAND or NOR Flash, SmartMedia, MultiMedia, DataFlash cards).

## Typical Applications

- Flash Recorder/Writer
- PDA, Camera, Mobile Phone
- PC Add-on



## USB Microcontroller with 64K Bytes Flash Memory

## AT89C5132

## Preliminary

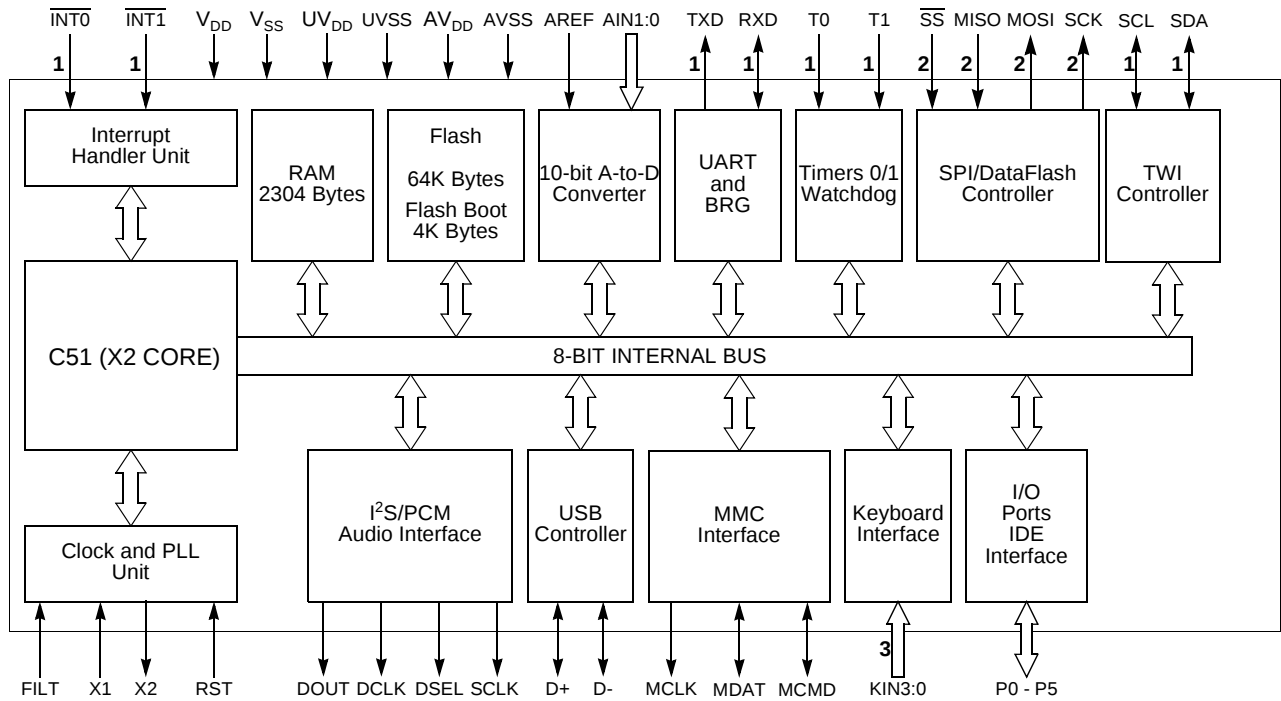
## Summary

Rev. 4173CS-USB-07/04



## Block Diagram

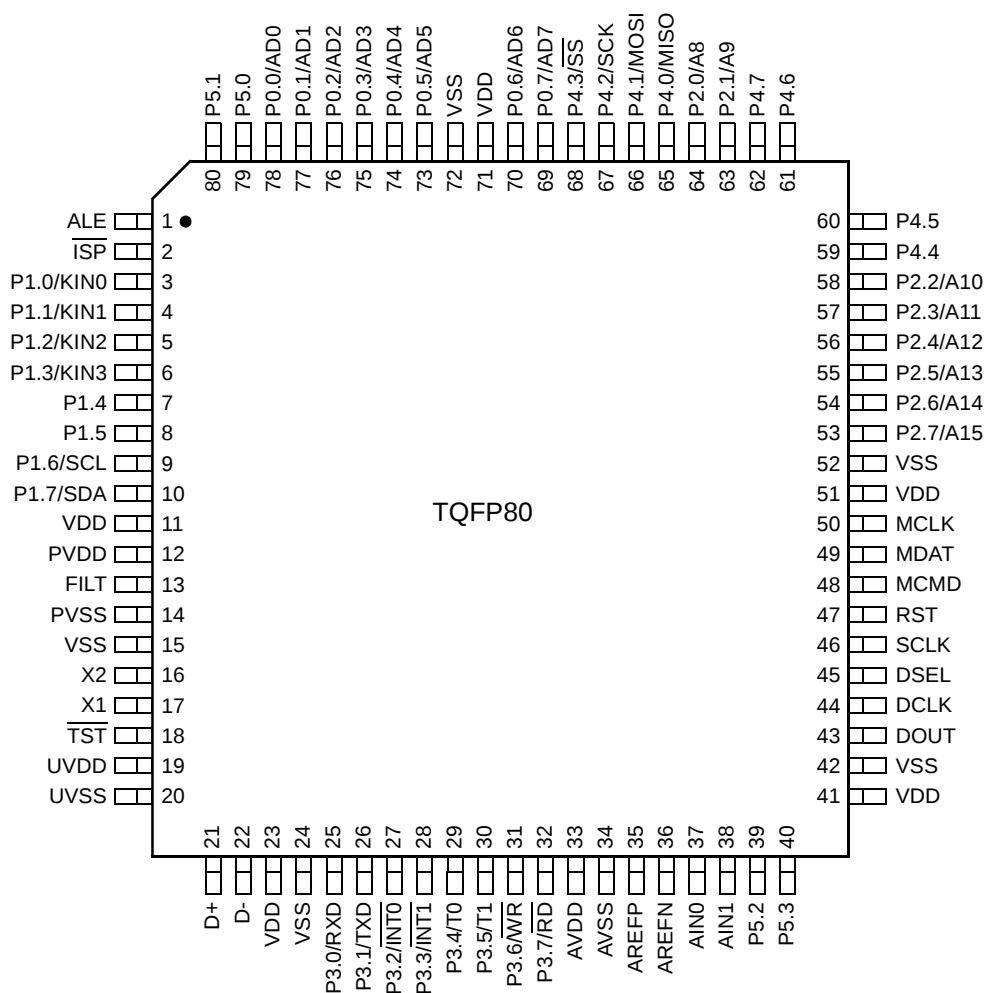
Figure 1. AT89C5132 Block Diagram



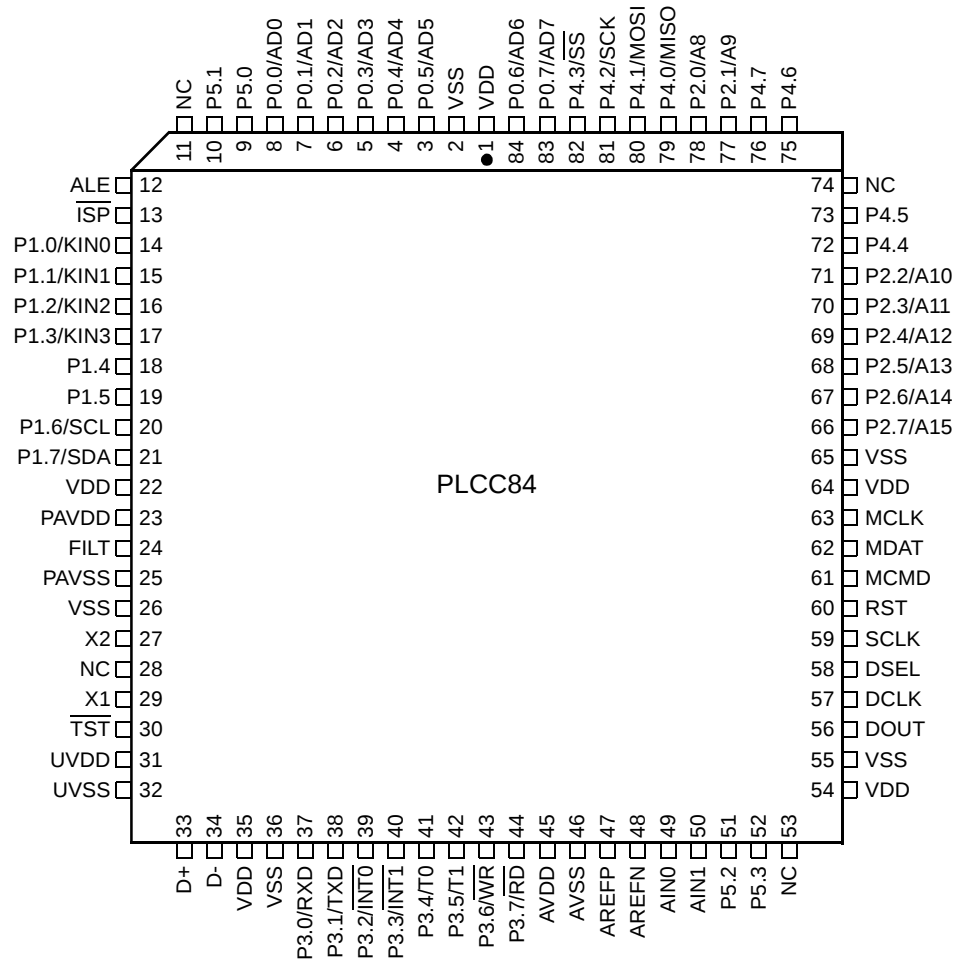
- Notes:
1. Alternate function of Port 3
  2. Alternate function of Port 4
  3. Alternate function of Port 1

## Pin Description

Figure 2. AT89C5132 80-pin TQFP Package



**Figure 3.** AT89C5132 84-pin PLCC <sup>(1)</sup>



Note: 1. For development board only.

## Signals

All the AT89C5132 signals are detailed by functionality in Table 1 to Table 15.

**Table 1.** Ports Signal Description

| Signal Name | Type | Description                                                                                                                                                                                                                                                            | Alternate Function                                                                         |
|-------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------|
| P0.7:0      | I/O  | <b>Port 0</b><br>P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to $V_{DD}$ or $V_{SS}$ . | AD7:0                                                                                      |
| P1.7:0      | I/O  | <b>Port 1</b><br>P1 is an 8-bit bidirectional I/O port with internal pull-ups.                                                                                                                                                                                         | KIN3:0<br>SCL<br>SDA                                                                       |
| P2.7:0      | I/O  | <b>Port 2</b><br>P2 is an 8-bit bidirectional I/O port with internal pull-ups.                                                                                                                                                                                         | A15:8                                                                                      |
| P3.7:0      | I/O  | <b>Port 3</b><br>P3 is an 8-bit bidirectional I/O port with internal pull-ups.                                                                                                                                                                                         | RXD<br>TXD<br>$\overline{\text{INT0}}$<br>INT1<br>T0<br>T1<br>$\overline{\text{WR}}$<br>RD |
| P4.7:0      | I/O  | <b>Port 4</b><br>P4 is an 8-bit bidirectional I/O port with internal pull-ups.                                                                                                                                                                                         | MISO<br>MOSI<br>SCK<br>$\overline{\text{SS}}$                                              |
| P5.3:0      | I/O  | <b>Port 5</b><br>P5 is a 4-bit bidirectional I/O port with internal pull-ups.                                                                                                                                                                                          | -                                                                                          |

**Table 2.** Clock Signal Description

| Signal Name | Type | Description                                                                                                                                                                                                                                                             | Alternate Function |
|-------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| X1          | I    | <b>Input to the on-chip inverting oscillator amplifier</b><br>To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing. | -                  |
| X2          | O    | <b>Output of the on-chip inverting oscillator amplifier</b><br>To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.                                                           | -                  |
| FILT        | I    | <b>PLL Low Pass Filter input</b><br>FILT receives the RC network of the PLL low pass filter.                                                                                                                                                                            | -                  |

**Table 3.** Timer 0 and Timer 1 Signal Description

| Signal Name              | Type | Description                                                                                                                                                                                                                                                                                                                                          | Alternate Function |
|--------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| $\overline{\text{INT0}}$ | I    | <b>Timer 0 Gate Input</b><br>INT0 serves as external run control for timer 0, when selected by GATE0 bit in TCON register.<br><b>External Interrupt 0</b><br>INT0 input sets IE0 in the TCON register. If bit IT0 in this register is set, bit IE0 is set by a falling edge on INT0#. If bit IT0 is cleared, bit IE0 is set by a low level on INT0#. | P3.2               |
| $\overline{\text{INT1}}$ | I    | <b>Timer 1 Gate Input</b><br>INT1 serves as external run control for timer 1, when selected by GATE1 bit in TCON register.<br><b>External Interrupt 1</b><br>INT1 input sets IE1 in the TCON register. If bit IT1 in this register is set, bit IE1 is set by a falling edge on INT1#. If bit IT1 is cleared, bit IE1 is set by a low level on INT1#. | P3.3               |
| T0                       | I    | <b>Timer 0 External Clock Input</b><br>When timer 0 operates as a counter, a falling edge on the T0 pin increments the count.                                                                                                                                                                                                                        | P3.4               |
| T1                       | I    | <b>Timer 1 External Clock Input</b><br>When timer 1 operates as a counter, a falling edge on the T1 pin increments the count.                                                                                                                                                                                                                        | P3.5               |

**Table 4.** Audio Interface Signal Description

| Signal Name | Type | Description                                                                                                                                      | Alternate Function |
|-------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| DCLK        | O    | <b>DAC Data Bit Clock</b>                                                                                                                        | -                  |
| DOUT        | O    | <b>DAC Audio Data</b>                                                                                                                            | -                  |
| DSEL        | O    | <b>DAC Channel Select Signal</b><br>DSEL is the sample rate clock output.                                                                        | -                  |
| SCLK        | O    | <b>DAC System Clock</b><br>SCLK is the oversampling clock synchronized to the digital audio data (DOUT) and the channel selection signal (DSEL). | -                  |

**Table 5.** USB Controller Signal Description

| Signal Name | Type | Description                                                                                                                          | Alternate Function |
|-------------|------|--------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| D+          | I/O  | <b>USB Positive Data Upstream Port</b><br>This pin requires an external 1.5 K $\Omega$ pull-up to $V_{DD}$ for full speed operation. | -                  |
| D-          | I/O  | <b>USB Negative Data Upstream Port</b>                                                                                               | -                  |

**Table 6.**

**Table 7. MultiMediaCard Interface Signal Description**

| Signal Name | Type | Description                                                                                                                                                                                                                 | Alternate Function |
|-------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| MCLK        | O    | <b>MMC Clock output</b><br>Data or command clock transfer.                                                                                                                                                                  | -                  |
| MCMD        | I/O  | <b>MMC Command line</b><br>Bidirectional command channel used for card initialization and data transfer commands. To avoid any parasitic current consumption, unused MCMD input must be polarized to $V_{DD}$ or $V_{SS}$ . | -                  |
| MDAT        | I/O  | <b>MMC Data line</b><br>Bidirectional data channel. To avoid any parasitic current consumption, unused MDAT input must be polarized to $V_{DD}$ or $V_{SS}$ .                                                               | -                  |

**Table 8. UART Signal Description**

| Signal Name | Type | Description                                                                                                                        | Alternate Function |
|-------------|------|------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| RXD         | I/O  | <b>Receive Serial Data</b><br>RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.   | P3.0               |
| TXD         | O    | <b>Transmit Serial Data</b><br>TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3. | P3.1               |

**Table 9. SPI Controller Signal Description**

| Signal Name     | Type | Description                                                                                                                                                                          | Alternate Function |
|-----------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| MISO            | I/O  | <b>SPI Master Input Slave Output Data Line</b><br>When in master mode, MISO receives data from the slave peripheral. When in slave mode, MISO outputs data to the master controller. | P4.0               |
| MOSI            | I/O  | <b>SPI Master Output Slave Input Data Line</b><br>When in master mode, MOSI outputs data to the slave peripheral. When in slave mode, MOSI receives data from the master controller. | P4.1               |
| SCK             | I/O  | <b>SPI Clock Line</b><br>When in master mode, SCK outputs clock to the slave peripheral. When in slave mode, SCK receives clock from the master controller.                          | P4.2               |
| $\overline{SS}$ | I    | <b>SPI Slave Select Line</b><br>When in controlled slave mode, $\overline{SS}$ enables the slave mode.                                                                               | P4.3               |

**Table 10. TWI Controller Signal Description**

| Signal Name | Type | Description                                                                                                                                                                                                   | Alternate Function |
|-------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| SCL         | I/O  | <b>TWI Serial Clock</b><br>When TWI controller is in master mode, SCL outputs the serial clock to the slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller. | P1.6               |
| SDA         | I/O  | <b>TWI Serial Data</b><br>SDA is the bidirectional Two Wire data line.                                                                                                                                        | P1.7               |

**Table 11.** A/D Converter Signal Description

| Signal Name | Type | Description                                                                                 | Alternate Function |
|-------------|------|---------------------------------------------------------------------------------------------|--------------------|
| AIN1:0      | I    | <b>A/D Converter Analog Inputs</b>                                                          | -                  |
| AREFP       | I    | <b>Analog Positive Voltage Reference Input</b>                                              | -                  |
| AREFN       | I    | <b>Analog Negative Voltage Reference Input</b><br>This pin is internally connected to AVSS. | -                  |

**Table 12.** Keypad Interface Signal Description

| Signal Name | Type | Description                                                                                                               | Alternate Function |
|-------------|------|---------------------------------------------------------------------------------------------------------------------------|--------------------|
| KIN3:0      | I    | <b>Keypad Input Lines</b><br>Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt. | P1.3:0             |

**Table 13.** External Access Signal Description

| Signal Name             | Type | Description                                                                                                                                                                                                                               | Alternate Function |
|-------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| A15:8                   | I/O  | <b>Address Lines</b><br>Upper address lines for the external bus.<br>Multiplexed higher address and data lines for the IDE interface.                                                                                                     | P2.7:0             |
| AD7:0                   | I/O  | <b>Address/Data Lines</b><br>Multiplexed lower address and data lines for the external memory or the IDE interface.                                                                                                                       | P0.7:0             |
| ALE                     | O    | <b>Address Latch Enable Output</b><br>ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A7:0. An external latch is used to demultiplex the address from address/data bus. | -                  |
| $\overline{\text{ISP}}$ | I/O  | <b>ISP Enable Input</b><br>This signal must be held to GND through a pull-down resistor at the falling reset to force execution of the internal bootloader.                                                                               | -                  |
| $\overline{\text{RD}}$  | O    | <b>Read Signal</b><br>Read signal asserted during external data memory read operation.                                                                                                                                                    | P3.7               |
| $\overline{\text{WR}}$  | O    | <b>Write Signal</b><br>Write signal asserted during external data memory write operation.                                                                                                                                                 | P3.6               |

**Table 14.** System Signal Description

| Signal Name      | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Alternate Function |
|------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| RST              | I    | <b>Reset Input</b><br>Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than $V_{IL}$ is applied, whether or not the oscillator is running.<br>This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and $V_{DD}$ .<br>Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation. | -                  |
| $\overline{TST}$ | I    | <b>Test Input</b><br>Test mode entry signal. This pin must be set to $V_{DD}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                           | -                  |

**Table 15.** Power Signal Description

| Signal Name | Type | Description                                                                | Alternate Function |
|-------------|------|----------------------------------------------------------------------------|--------------------|
| VDD         | PWR  | <b>Digital Supply Voltage</b><br>Connect these pins to +3V supply voltage. | -                  |
| VSS         | GND  | <b>Circuit Ground</b><br>Connect these pins to ground.                     | -                  |
| AVDD        | PWR  | <b>Analog Supply Voltage</b><br>Connect this pin to +3V supply voltage.    | -                  |
| AVSS        | GND  | <b>Analog Ground</b><br>Connect this pin to ground.                        | -                  |
| PVDD        | PWR  | <b>PLL Supply voltage</b><br>Connect this pin to +3V supply voltage.       | -                  |
| PVSS        | GND  | <b>PLL Circuit Ground</b><br>Connect this pin to ground.                   | -                  |
| UVDD        | PWR  | <b>USB Supply Voltage</b><br>Connect this pin to +3V supply voltage.       | -                  |
| UVSS        | GND  | <b>USB Ground</b><br>Connect this pin to ground.                           | -                  |



## Address Spaces

The AT8xC5132 derivatives implement four different address spaces:

- Program/Code Memory
- Boot Memory
- Data Memory
- Special Function Registers (SFRs)

### Code Memory

The AT89C5132 implements 64K Bytes of on-chip program/code memory in Flash technology.

The Flash memory increases ROM functionality by enabling in-circuit electrical erasure and programming. Thanks to the internal charge pump, the high voltage needed for programming or erasing Flash cells is generated on-chip using the standard  $V_{DD}$  voltage. Thus, the AT89C5132 can be programmed using only one voltage and allows in application software programming commonly known as IAP. Hardware programming mode is also available using specific programming tools.

### Boot Memory

The AT89C5132 implements 4K Bytes of on-chip boot memory provided in Flash technology. This boot memory is delivered programmed with a standard bootloader software allowing in system programming commonly known as ISP. It also contains some Application Programming Interfaces routines commonly known as API allowing user to develop his own bootloader.

### Data Memory

The AT89C5132 derivatives implement 2304 bytes of on-chip data RAM. This memory is divided in two separate areas:

- 256 bytes of on-chip RAM memory (standard C51 memory).
- 2048 bytes of on-chip expanded RAM memory (ERAM accessible via MOVX instructions).



## Peripherals

The AT8xC5132 peripherals are briefly described in the following sections. For further details on how to interface (hardware and software) to these peripherals, please refer to the AT8xC5132 complete datasheet.

### Clock Generator System

The AT8xC5132 internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

### Ports

The AT8xC5132 implement five 8-bit ports (P0 to P4) and one 4-bit port (P5). In addition to performing general-purpose I/Os, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bidirectional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/Os and alternate functions.

### Timers/Counters

The AT8xC5132 implement the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

### Watchdog Timer

The AT8xC5132 implement a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

### Audio Output Interface

The AT8xC5132 implements an audio output interface allowing the decoded audio bit-stream to be output in various formats. They are compatible with right and left justification PCM and I2S formats and the on-chip PLL allows connection of almost all commercial audio DAC families available on the market.

### Universal Serial Bus Interface

The AT8xC5132 implements a full-speed Universal Serial Bus Interface. The USB interface can be used for the following purposes:

- Download of files by supporting the USB mass storage class.
- In-System Programming by supporting the USB firmware upgrade class.

### MultiMedia Card Interface

The AT8xC5132 implements a MultiMedia Card (MMC) interface compliant to the V2.2 specification in MultiMedia Card mode. The MMC allows storage of files in removable Flash memory cards that can be easily plugged or removed from the application. It can also be used for In-System Programming.

### IDE/ATAPI Interface

The AT8xC5132 provide an IDE/ATAPI interface allowing connection of devices such as CD-ROM reader, CompactFlash™ cards, Hard Disk Drive, etc. It consists of a 16-bit bidirectional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interface but could be used for In-System Programming using CD-ROM.

**Serial I/O Interface**

The AT89C5132 implements a serial port with its own baud rate generator providing one single synchronous communication mode and three full-duplex Universal Asynchronous Receiver Transmitter (UART) communication modes. It is provided for the following purposes:

- In System Programming.
- Remote control of the AT89C5132 by a host.

**Serial Peripheral Interface**

The AT89C5132 implements a Serial Peripheral Interface (SPI) supporting master and slave modes. It is provided for the following purposes:

- Remote control of the AT89C5132 by a host.
- In System Programming.

**Two-wire Controller**

The AT89C5132 implements a 2-wire controller supporting the four standard master and slave modes with multimaster capability. It is provided for the following purposes:

- Connection of slave devices like LCD controller, audio DAC...
- Remote control of the AT89C5132 by a host.
- In System Programming.

**A/D Controller**

The AT89C5132 implements a 2-channel 10-bit (8 true bits) analog to digital converter (ADC). It is provided for the following purposes:

- Battery monitoring.
- Voice recording.
- Corded remote control.

## Electrical Characteristics

### Absolute Maximum Ratings

|                                            |                 |
|--------------------------------------------|-----------------|
| Storage Temperature .....                  | -65°C to +150°C |
| Voltage on any other Pin to $V_{SS}$ ..... | -0.3 to +4.0V   |
| $I_{OL}$ per I/O Pin .....                 | 5 mA            |
| Power Dissipation .....                    | 1 W             |
| Ambient Temperature Under Bias.....        | -40°C to +85°C  |
| $V_{DD}$ .....                             | 2.7V to 3.3V    |

NOTE:

Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

### DC Characteristics

#### Digital Logic

**Table 1.** Digital DC Characteristics

$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^\circ$  to  $+85^\circ C$

| Symbol    | Parameter                                                                                           | Min                      | Typ <sup>(1)</sup> | Max                      | Units   | Test Conditions        |
|-----------|-----------------------------------------------------------------------------------------------------|--------------------------|--------------------|--------------------------|---------|------------------------|
| $V_{IL}$  | Input Low Voltage                                                                                   | -0.5                     |                    | $0.2 \cdot V_{DD} - 0.1$ | V       |                        |
| $V_{IH1}$ | Input High Voltage (except RST, X1)                                                                 | $0.2 \cdot V_{DD} + 1.1$ |                    | $V_{DD}$                 | V       |                        |
| $V_{IH2}$ | Input High Voltage (RST, X1)                                                                        | $0.7 \cdot V_{DD}^{(2)}$ |                    | $V_{DD} + 0.5$           | V       |                        |
| $V_{OL1}$ | Output Low Voltage<br>(except P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)                    |                          |                    | 0.45                     | V       | $I_{OL} = 1.6$ mA      |
| $V_{OL2}$ | Output Low Voltage<br>(P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)                           |                          |                    | 0.45                     | V       | $I_{OL} = 3.2$ mA      |
| $V_{OH1}$ | Output High Voltage<br>(P1, P2, P3, P4 and P5)                                                      | $V_{DD} - 0.7$           |                    |                          | V       | $I_{OH} = -30$ $\mu A$ |
| $V_{OH2}$ | Output High Voltage<br>(P0, P2 address mode, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT, D+, D-) | $V_{DD} - 0.7$           |                    |                          | V       | $I_{OH} = -3.2$ mA     |
| $I_{IL}$  | Logical 0 Input Current (P1, P2, P3, P4 and P5)                                                     |                          |                    | -50                      | $\mu A$ | $V_{in} = 0.45$ V      |

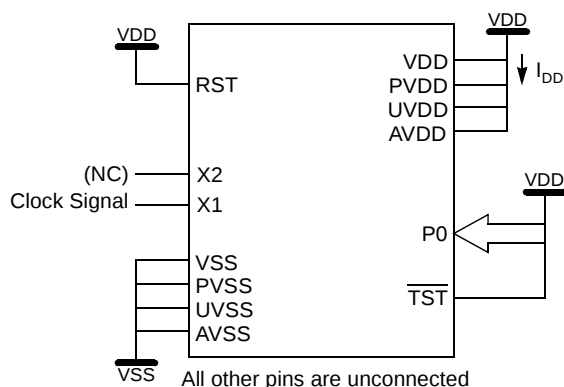
**Table 1.** Digital DC Characteristics

$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^\circ$  to  $+85^\circ C$

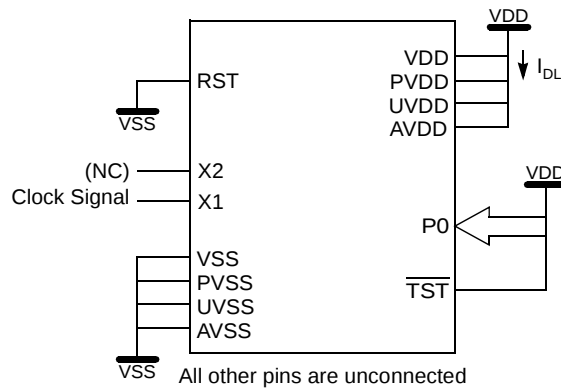
| Symbol    | Parameter                                                                 | Min | Typ <sup>(1)</sup> | Max                                                 | Units     | Test Conditions                                |
|-----------|---------------------------------------------------------------------------|-----|--------------------|-----------------------------------------------------|-----------|------------------------------------------------|
| $I_{LI}$  | Input Leakage Current (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT) |     |                    | 10                                                  | $\mu A$   | $0.45 < V_{IN} < V_{DD}$                       |
| $I_{TL}$  | Logical 1 to 0 Transition Current (P1, P2, P3, P4 and P5)                 |     |                    | -650                                                | $\mu A$   | $V_{in} = 2.0 V$                               |
| $R_{RST}$ | Pull-Down Resistor                                                        | 50  | 90                 | 200                                                 | $k\Omega$ |                                                |
| $C_{IO}$  | Pin Capacitance                                                           |     | 10                 |                                                     | $pF$      | $T_A = 25^\circ C$                             |
| $V_{RET}$ | $V_{DD}$ Data Retention Limit                                             |     |                    | 1.8                                                 | V         |                                                |
| $I_{DD}$  | Operating Current                                                         |     | (3)                | X1 / X2 mode<br>6.5 / 10.5<br>8 / 13.5<br>9.5 / 17  | $mA$      | $V_{DD} < 3.3 V$<br>12 MHz<br>16 MHz<br>20 MHz |
| $I_{DL}$  | Idle Mode Current                                                         |     | (3)                | X1 / X2 mode<br>5.3 / 8.1<br>6.4 / 10.3<br>7.5 / 13 | $mA$      | $V_{DD} < 3.3 V$<br>12 MHz<br>16 MHz<br>20 MHz |
| $I_{PD}$  | Power-Down Mode Current                                                   |     | 20                 | 500                                                 | $\mu A$   | $V_{RET} < V_{DD} < 3.3 V$                     |

- Notes:
1. Typical values are obtained using  $V_{DD} = 3 V$  and  $T_A = 25^\circ C$ . They are not tested and there is no guarantee on these values.
  2. Flash retention is guaranteed with the same formula for  $V_{DD}$  min down to 0V.
  3. See Table 154 for typical consumption in player mode.

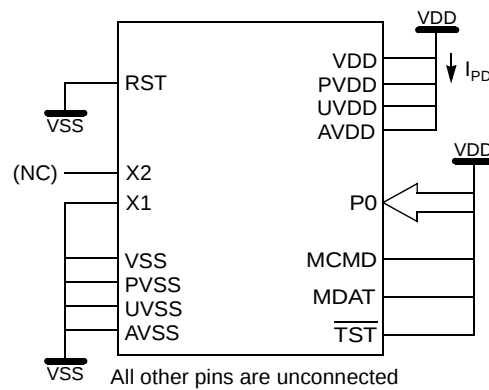
## $I_{DD}$ , $I_{DL}$ and $I_{PD}$ Test Conditions Figure 1. $I_{DD}$ Test Condition, Active Mode



**Figure 2.**  $I_{DL}$  Test Condition, Idle Mode



**Figure 3.**  $I_{PD}$  Test Condition, Power-Down Mode



## A-to-D Converter

**Table 2.** A-to-D Converter DC Characteristics

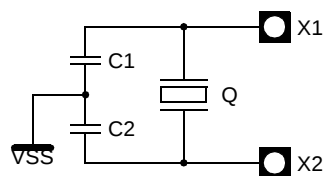
$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$

| Symbol     | Parameter                                     | Min              | Typ | Max            | Units      | Test Conditions                               |
|------------|-----------------------------------------------|------------------|-----|----------------|------------|-----------------------------------------------|
| $AV_{DD}$  | Analog Supply Voltage                         | 2.7              |     | 3.3            | V          |                                               |
| $AI_{DD}$  | Analog Operating Supply Current               |                  |     | 600            | $\mu A$    | $AV_{DD} = 3.3V$<br>$AIN1:0 = 0$ to $AV_{DD}$ |
| $AI_{PD}$  | Analog Standby Current                        |                  |     | 2              | $\mu A$    | $AV_{DD} = 3.3V$<br>$ADEN = 0$ or $PD = 1$    |
| $AV_{IN}$  | Analog Input Voltage                          | $AV_{SS}$        |     | $AV_{DD}$      | V          |                                               |
| $AV_{REF}$ | Reference Voltage<br>$A_{REFN}$<br>$A_{REFP}$ | $AV_{SS}$<br>2.4 |     | $AV_{DD}$<br>V | V<br>V     |                                               |
| $R_{REF}$  | AREF Input Resistance                         | 10               |     | 30             | k $\Omega$ | $T_A = 25^{\circ}C$                           |
| $C_{IA}$   | Analog Input capacitance                      |                  |     | 10             | pF         | $T_A = 25^{\circ}C$                           |

## Oscillator and Crystal

### Schematic

**Figure 4.** Crystal Connection



Note: For operation with most standard crystals, no external components are needed on X1 and X2. It may be necessary to add external capacitors on X1 and X2 to ground in special cases (max 10 pF). X1 and X2 may not be used to drive other circuits.

### Parameters

**Table 3.** Oscillator and Crystal Characteristics

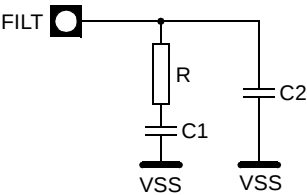
$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^{\circ}$  to  $+85^{\circ}C$

| Symbol   | Parameter                             | Min | Typ | Max | Unit     |
|----------|---------------------------------------|-----|-----|-----|----------|
| $C_{X1}$ | Internal Capacitance (X1 - $V_{SS}$ ) |     | 10  |     | pF       |
| $C_{X2}$ | Internal Capacitance (X2 - $V_{SS}$ ) |     | 10  |     | pF       |
| $C_L$    | Equivalent Load Capacitance (X1 - X2) |     | 5   |     | pF       |
| DL       | Drive Level                           |     |     | 50  | $\mu W$  |
| F        | Crystal Frequency                     |     |     | 20  | MHz      |
| RS       | Crystal Series Resistance             |     |     | 40  | $\Omega$ |
| CS       | Crystal Shunt Capacitance             |     |     | 6   | pF       |

# Phase Lock Loop

## Schematic

**Figure 5.** PLL Filter Connection



## Parameters

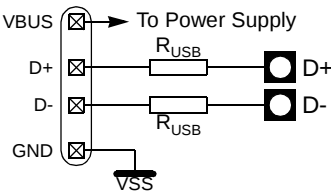
**Table 4.** PLL Filter Characteristics  
 $V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^{\circ}$  to  $+85^{\circ}C$

| Symbol | Parameter            | Min | Typ | Max | Unit     |
|--------|----------------------|-----|-----|-----|----------|
| R      | Filter Resistor      |     | 100 |     | $\Omega$ |
| C1     | Filter Capacitance 1 |     | 10  |     | nF       |
| C2     | Filter Capacitance 2 |     | 2.2 |     | nF       |

# USB Connection

## Schematic

**Figure 6.** USB Connection



## Parameters

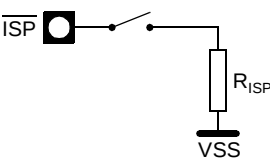
**Table 1.** USB Termination Characteristics  
 $V_{DD} = 2.7$  to  $3.3 V$ ,  $T_A = -40$  to  $+85^{\circ}C$

| Symbol    | Parameter                | Min | Typ | Max | Unit     |
|-----------|--------------------------|-----|-----|-----|----------|
| $R_{USB}$ | USB Termination Resistor |     | 27  |     | $\Omega$ |

# In-system Programming

## Schematic

**Figure 7.** ISP Pull-down Connection



## Parameters

**Table 5.** ISP Pull-Down Characteristics  
 $V_{DD} = 2.7$  to  $3.3 V$ ,  $T_A = -40^{\circ}$  to  $+85^{\circ}C$

| Symbol    | Parameter              | Min | Typ | Max | Unit       |
|-----------|------------------------|-----|-----|-----|------------|
| $R_{ISP}$ | ISP Pull-Down Resistor |     | 2.2 |     | k $\Omega$ |

## AC Characteristics

### External 8-bit Bus Cycles

#### Definition of Symbols

**Table 1.** External 8-bit Bus Cycles Timing Symbol Definitions

| Signals |                 | Conditions |                 |
|---------|-----------------|------------|-----------------|
| A       | Address         | H          | High            |
| D       | Data In         | L          | Low             |
| L       | ALE             | V          | Valid           |
| Q       | Data Out        | X          | No Longer Valid |
| R       | $\overline{RD}$ | Z          | Floating        |
| W       | $\overline{WR}$ |            |                 |

#### Timings

Test conditions: capacitive load on all pins = 50 pF.

**Table 2.** External 8-bit Bus Cycle – Data Read AC Timings

$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^\circ$  to  $+85^\circ C$

| Symbol     | Parameter                                    | Variable Clock<br>Standard Mode |                         | Variable Clock<br>X2 Mode |                           | Unit |
|------------|----------------------------------------------|---------------------------------|-------------------------|---------------------------|---------------------------|------|
|            |                                              | Min                             | Max                     | Min                       | Max                       |      |
| $T_{CLCL}$ | Clock Period                                 | 50                              |                         | 50                        |                           | ns   |
| $T_{LHLL}$ | ALE Pulse Width                              | $2 \cdot T_{CLCL} - 15$         |                         | $T_{CLCL} - 15$           |                           | ns   |
| $T_{AVLL}$ | Address Valid to ALE Low                     | $T_{CLCL} - 20$                 |                         | $0.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{LLAX}$ | Address hold after ALE Low                   | $T_{CLCL} - 20$                 |                         | $0.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{LLRL}$ | ALE Low to $\overline{RD}$ Low               | $3 \cdot T_{CLCL} - 30$         |                         | $1.5 \cdot T_{CLCL} - 30$ |                           | ns   |
| $T_{RLRH}$ | $\overline{RD}$ Pulse Width                  | $6 \cdot T_{CLCL} - 25$         |                         | $3 \cdot T_{CLCL} - 25$   |                           | ns   |
| $T_{RHLH}$ | $\overline{RD}$ high to ALE High             | $T_{CLCL} - 20$                 | $T_{CLCL} + 20$         | $0.5 \cdot T_{CLCL} - 20$ | $0.5 \cdot T_{CLCL} + 20$ | ns   |
| $T_{AVDV}$ | Address Valid to Valid Data In               |                                 | $9 \cdot T_{CLCL} - 65$ |                           | $4.5 \cdot T_{CLCL} - 65$ | ns   |
| $T_{AVRL}$ | Address Valid to $\overline{RD}$ Low         | $4 \cdot T_{CLCL} - 30$         |                         | $2 \cdot T_{CLCL} - 30$   |                           | ns   |
| $T_{RLDV}$ | $\overline{RD}$ Low to Valid Data            |                                 | $5 \cdot T_{CLCL} - 30$ |                           | $2.5 \cdot T_{CLCL} - 30$ | ns   |
| $T_{RLAZ}$ | $\overline{RD}$ Low to Address Float         |                                 | 0                       |                           | 0                         | ns   |
| $T_{RHDX}$ | Data Hold After $\overline{RD}$ High         | 0                               |                         | 0                         |                           | ns   |
| $T_{RHDZ}$ | Instruction Float After $\overline{RD}$ High |                                 | $2 \cdot T_{CLCL} - 25$ |                           | $T_{CLCL} - 25$           | ns   |

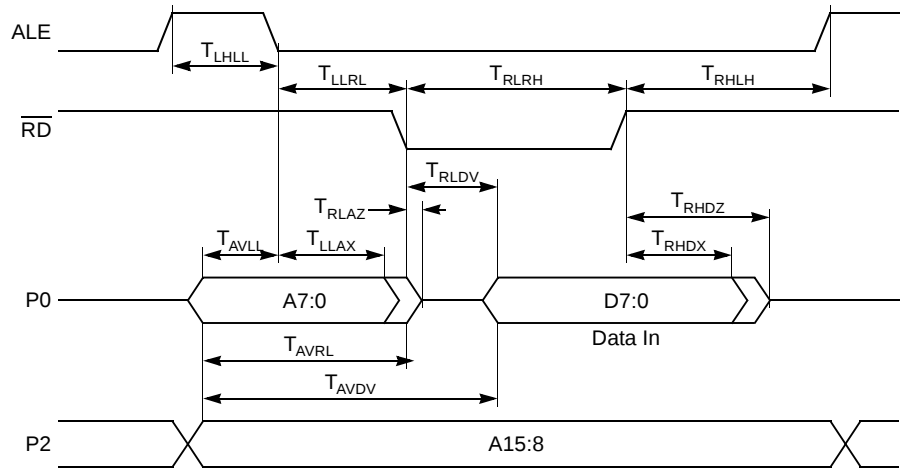
**Table 3.** External 8-bit Bus Cycle – Data Write AC Timings

$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^{\circ}$  to  $+85^{\circ}C$

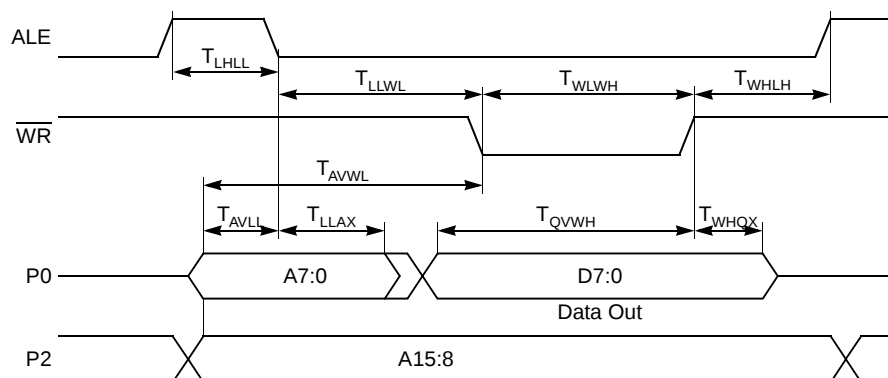
| Symbol     | Parameter                            | Variable Clock<br>Standard Mode |                 | Variable Clock<br>X2 Mode |                           | Unit |
|------------|--------------------------------------|---------------------------------|-----------------|---------------------------|---------------------------|------|
|            |                                      | Min                             | Max             | Min                       | Max                       |      |
| $T_{CLCL}$ | Clock Period                         | 50                              |                 | 50                        |                           | ns   |
| $T_{LHLL}$ | ALE Pulse Width                      | $2 \cdot T_{CLCL} - 15$         |                 | $T_{CLCL} - 15$           |                           | ns   |
| $T_{AVLL}$ | Address Valid to ALE Low             | $T_{CLCL} - 20$                 |                 | $0.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{LLAX}$ | Address hold after ALE Low           | $T_{CLCL} - 20$                 |                 | $0.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{LLWL}$ | ALE Low to $\overline{WR}$ Low       | $3 \cdot T_{CLCL} - 30$         |                 | $1.5 \cdot T_{CLCL} - 30$ |                           | ns   |
| $T_{WLWH}$ | $\overline{WR}$ Pulse Width          | $6 \cdot T_{CLCL} - 25$         |                 | $3 \cdot T_{CLCL} - 25$   |                           | ns   |
| $T_{WHLH}$ | $\overline{WR}$ High to ALE High     | $T_{CLCL} - 20$                 | $T_{CLCL} + 20$ | $0.5 \cdot T_{CLCL} - 20$ | $0.5 \cdot T_{CLCL} + 20$ | ns   |
| $T_{AVWL}$ | Address Valid to $\overline{WR}$ Low | $4 \cdot T_{CLCL} - 30$         |                 | $2 \cdot T_{CLCL} - 30$   |                           | ns   |
| $T_{QVWH}$ | Data Valid to $\overline{WR}$ High   | $7 \cdot T_{CLCL} - 20$         |                 | $3.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{WHQX}$ | Data Hold after $\overline{WR}$ High | $T_{CLCL} - 15$                 |                 | $0.5 \cdot T_{CLCL} - 15$ |                           | ns   |

## Waveforms

**Figure 1.** External 8-bit Bus Cycle – Data Read Waveforms



**Figure 2.** External 8-bit Bus Cycle – Data Write Waveforms



## External IDE 16-bit Bus Cycles

### Definition of Symbols

**Table 4.** External IDE 16-bit Bus Cycles Timing Symbol Definitions

| Signals |                 |
|---------|-----------------|
| A       | Address         |
| D       | Data In         |
| L       | ALE             |
| Q       | Data Out        |
| R       | $\overline{RD}$ |
| W       | $\overline{WR}$ |

| Conditions |                 |
|------------|-----------------|
| H          | High            |
| L          | Low             |
| V          | Valid           |
| X          | No Longer Valid |
| Z          | Floating        |

### Timings

Test conditions: capacitive load on all pins = 50 pF.

**Table 5.** External IDE 16-bit Bus Cycle – Data Read AC Timings

$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^\circ$  to  $+85^\circ C$

| Symbol     | Parameter                                    | Variable Clock<br>Standard Mode |                         | Variable Clock<br>X2 Mode |                           | Unit |
|------------|----------------------------------------------|---------------------------------|-------------------------|---------------------------|---------------------------|------|
|            |                                              | Min                             | Max                     | Min                       | Max                       |      |
| $T_{CLCL}$ | Clock Period                                 | 50                              |                         | 50                        |                           | ns   |
| $T_{LHLL}$ | ALE Pulse Width                              | $2 \cdot T_{CLCL} - 15$         |                         | $T_{CLCL} - 15$           |                           | ns   |
| $T_{AVLL}$ | Address Valid to ALE Low                     | $T_{CLCL} - 20$                 |                         | $0.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{LLAX}$ | Address hold after ALE Low                   | $T_{CLCL} - 20$                 |                         | $0.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{LLRL}$ | ALE Low to $\overline{RD}$ Low               | $3 \cdot T_{CLCL} - 30$         |                         | $1.5 \cdot T_{CLCL} - 30$ |                           | ns   |
| $T_{RLRH}$ | $\overline{RD}$ Pulse Width                  | $6 \cdot T_{CLCL} - 25$         |                         | $3 \cdot T_{CLCL} - 25$   |                           | ns   |
| $T_{RHLH}$ | $\overline{RD}$ high to ALE High             | $T_{CLCL} - 20$                 | $T_{CLCL} + 20$         | $0.5 \cdot T_{CLCL} - 20$ | $0.5 \cdot T_{CLCL} + 20$ | ns   |
| $T_{AVDV}$ | Address Valid to Valid Data In               |                                 | $9 \cdot T_{CLCL} - 65$ |                           | $4.5 \cdot T_{CLCL} - 65$ | ns   |
| $T_{AVRL}$ | Address Valid to $\overline{RD}$ Low         | $4 \cdot T_{CLCL} - 30$         |                         | $2 \cdot T_{CLCL} - 30$   |                           | ns   |
| $T_{RLDV}$ | $\overline{RD}$ Low to Valid Data            |                                 | $5 \cdot T_{CLCL} - 30$ |                           | $2.5 \cdot T_{CLCL} - 30$ | ns   |
| $T_{RLAZ}$ | $\overline{RD}$ Low to Address Float         |                                 | 0                       |                           | 0                         | ns   |
| $T_{RHDH}$ | Data Hold After $\overline{RD}$ High         | 0                               |                         | 0                         |                           | ns   |
| $T_{RHDZ}$ | Instruction Float After $\overline{RD}$ High |                                 | $2 \cdot T_{CLCL} - 25$ |                           | $T_{CLCL} - 25$           | ns   |

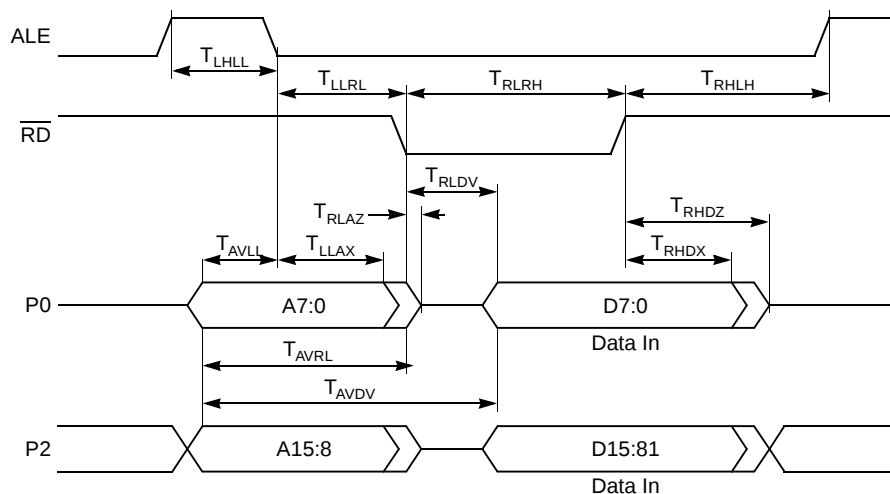
**Table 6.** External IDE 16-bit Bus Cycle – Data Write AC Timings

$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^\circ$  to  $+85^\circ C$

| Symbol     | Parameter                            | Variable Clock<br>Standard Mode |                 | Variable Clock<br>X2 Mode |                           | Unit |
|------------|--------------------------------------|---------------------------------|-----------------|---------------------------|---------------------------|------|
|            |                                      | Min                             | Max             | Min                       | Max                       |      |
| $T_{CLCL}$ | Clock Period                         | 50                              |                 | 50                        |                           | ns   |
| $T_{LHLL}$ | ALE Pulse Width                      | $2 \cdot T_{CLCL} - 15$         |                 | $T_{CLCL} - 15$           |                           | ns   |
| $T_{AVLL}$ | Address Valid to ALE Low             | $T_{CLCL} - 20$                 |                 | $0.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{LLAX}$ | Address hold after ALE Low           | $T_{CLCL} - 20$                 |                 | $0.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{LLWL}$ | ALE Low to $\overline{WR}$ Low       | $3 \cdot T_{CLCL} - 30$         |                 | $1.5 \cdot T_{CLCL} - 30$ |                           | ns   |
| $T_{WLWH}$ | $\overline{WR}$ Pulse Width          | $6 \cdot T_{CLCL} - 25$         |                 | $3 \cdot T_{CLCL} - 25$   |                           | ns   |
| $T_{WHLH}$ | $\overline{WR}$ High to ALE High     | $T_{CLCL} - 20$                 | $T_{CLCL} + 20$ | $0.5 \cdot T_{CLCL} - 20$ | $0.5 \cdot T_{CLCL} + 20$ | ns   |
| $T_{AVWL}$ | Address Valid to $\overline{WR}$ Low | $4 \cdot T_{CLCL} - 30$         |                 | $2 \cdot T_{CLCL} - 30$   |                           | ns   |
| $T_{QVWH}$ | Data Valid to $\overline{WR}$ High   | $7 \cdot T_{CLCL} - 20$         |                 | $3.5 \cdot T_{CLCL} - 20$ |                           | ns   |
| $T_{WHQX}$ | Data Hold after $\overline{WR}$ High | $T_{CLCL} - 15$                 |                 | $0.5 \cdot T_{CLCL} - 15$ |                           | ns   |

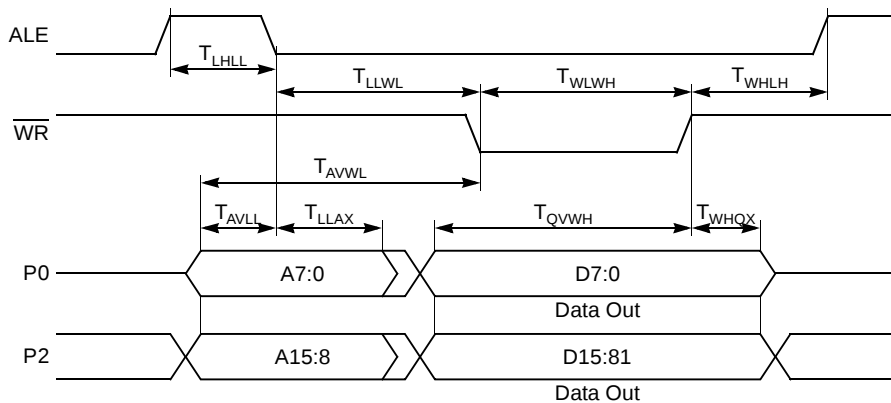
## Waveforms

**Figure 3.** External IDE 16-bit Bus Cycle – Data Read Waveforms



Note: D15:8 is written in DAT16H SFR.

**Figure 4.** External IDE 16-bit Bus Cycle – Data Write Waveforms



Note: D15:8 is the content of DAT16H SFR.

## SPI Interface

### Definition of Symbols

**Table 7.** SPI Interface Timing Symbol Definitions

| Signals |          |
|---------|----------|
| C       | Clock    |
| I       | Data In  |
| O       | Data Out |

| Conditions |                 |
|------------|-----------------|
| H          | High            |
| L          | Low             |
| V          | Valid           |
| X          | No Longer Valid |
| Z          | Floating        |

## Timings

**Table 8.** SPI Interface Master AC Timing

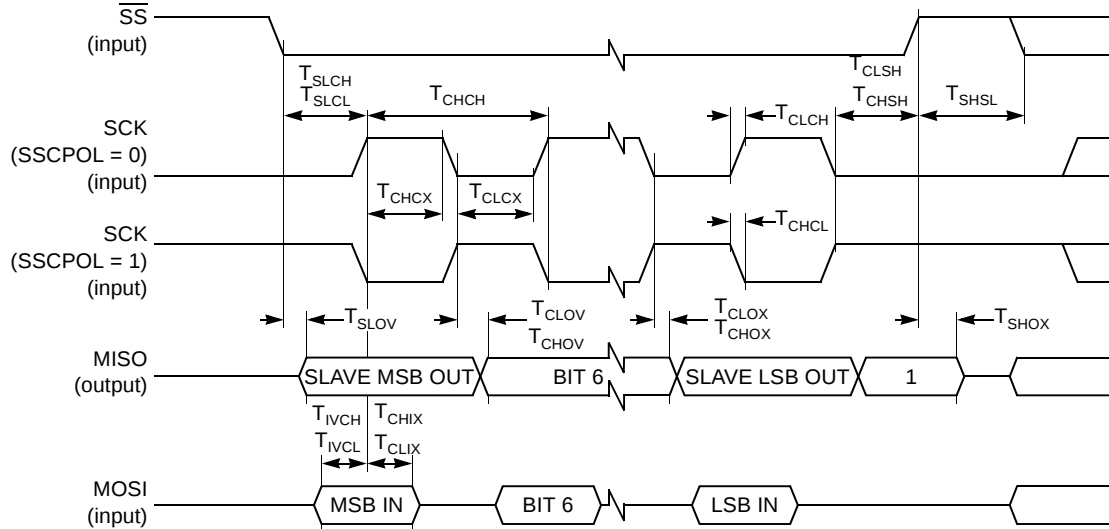
$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^\circ$  to  $+85^\circ C$

| Symbol               | Parameter                                   | Min | Max | Unit      |
|----------------------|---------------------------------------------|-----|-----|-----------|
| <b>Slave Mode</b>    |                                             |     |     |           |
| $T_{CHCH}$           | Clock Period                                | 8   |     | $T_{OSC}$ |
| $T_{CHCX}$           | Clock High Time                             | 3.2 |     | $T_{OSC}$ |
| $T_{CLCX}$           | Clock Low Time                              | 3.2 |     | $T_{OSC}$ |
| $T_{SLCH}, T_{SLCL}$ | $\overline{SS}$ Low to Clock edge           | 200 |     | ns        |
| $T_{IVCL}, T_{IVCH}$ | Input Data Valid to Clock Edge              | 100 |     | ns        |
| $T_{CLIX}, T_{CHIX}$ | Input Data Hold after Clock Edge            | 100 |     | ns        |
| $T_{CLOV}, T_{CHOV}$ | Output Data Valid after Clock Edge          |     | 100 | ns        |
| $T_{CLOX}, T_{CHOX}$ | Output Data Hold Time after Clock Edge      | 0   |     | ns        |
| $T_{CLSH}, T_{CHSH}$ | $\overline{SS}$ High after Clock Edge       | 0   |     | ns        |
| $T_{IVCL}, T_{IVCH}$ | Input Data Valid to Clock Edge              | 100 |     | ns        |
| $T_{CLIX}, T_{CHIX}$ | Input Data Hold after Clock Edge            | 100 |     | ns        |
| $T_{SLOV}$           | $\overline{SS}$ Low to Output Data Valid    |     | 130 | ns        |
| $T_{SHOX}$           | Output Data Hold after $\overline{SS}$ High |     | 130 | ns        |
| $T_{SHSL}$           | $\overline{SS}$ High to $\overline{SS}$ Low | (1) |     |           |
| $T_{ILIH}$           | Input Rise Time                             |     | 2   | $\mu s$   |
| $T_{IHIL}$           | Input Fall Time                             |     | 2   | $\mu s$   |
| $T_{OLOH}$           | Output Rise Time                            |     | 100 | ns        |
| $T_{OHOL}$           | Output Fall Time                            |     | 100 | ns        |
| <b>Master Mode</b>   |                                             |     |     |           |
| $T_{CHCH}$           | Clock Period                                | 4   |     | $T_{OSC}$ |
| $T_{CHCX}$           | Clock High Time                             | 1.6 |     | $T_{OSC}$ |
| $T_{CLCX}$           | Clock Low Time                              | 1.6 |     | $T_{OSC}$ |
| $T_{IVCL}, T_{IVCH}$ | Input Data Valid to Clock Edge              | 50  |     | ns        |
| $T_{CLIX}, T_{CHIX}$ | Input Data Hold after Clock Edge            | 50  |     | ns        |
| $T_{CLOV}, T_{CHOV}$ | Output Data Valid after Clock Edge          |     | 65  | ns        |
| $T_{CLOX}, T_{CHOX}$ | Output Data Hold Time after Clock Edge      | 0   |     | ns        |
| $T_{ILIH}$           | Input Data Rise Time                        |     | 2   | $\mu s$   |
| $T_{IHIL}$           | Input Data Fall Time                        |     | 2   | $\mu s$   |
| $T_{OLOH}$           | Output Data Rise Time                       |     | 50  | ns        |
| $T_{OHOL}$           | Output Data Fall Time                       |     | 50  | ns        |

Notes: 1. Value of this parameter depends on software.  
2. Test conditions: capacitive load on all pins = 100 pF

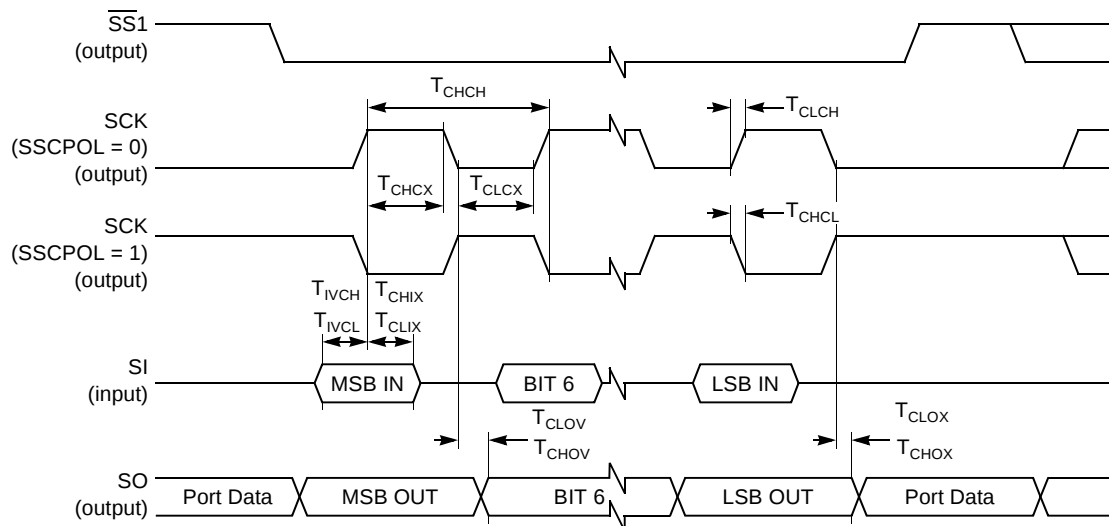
# Waveforms

**Figure 5. SPI Slave Waveforms (SSCPHA = 0)**



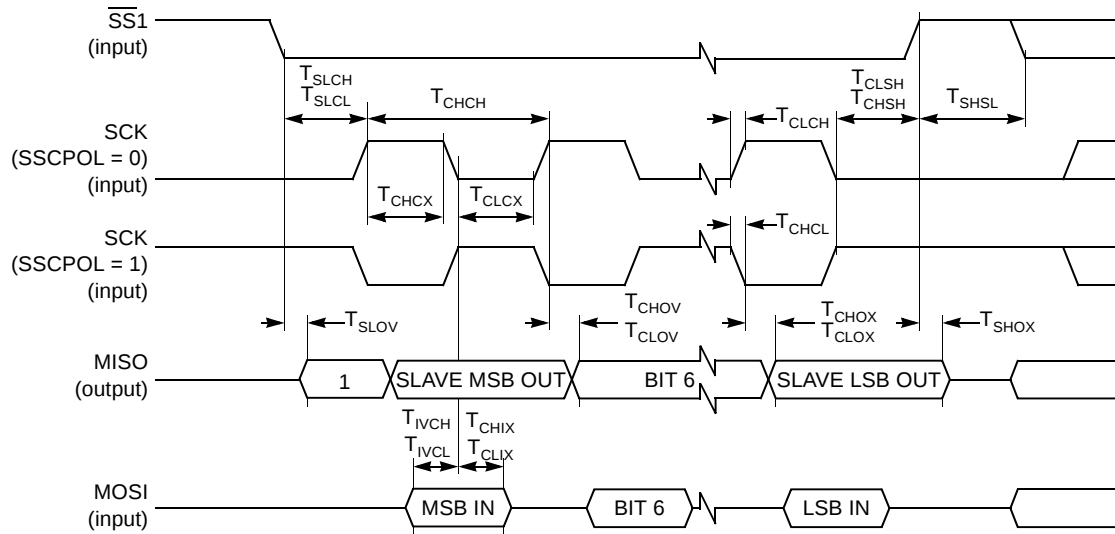
Note: 1. Not Defined but generally the MSB of the character which has just been received.

**Figure 6. SPI Slave Waveforms (SSCPHA = 1)**



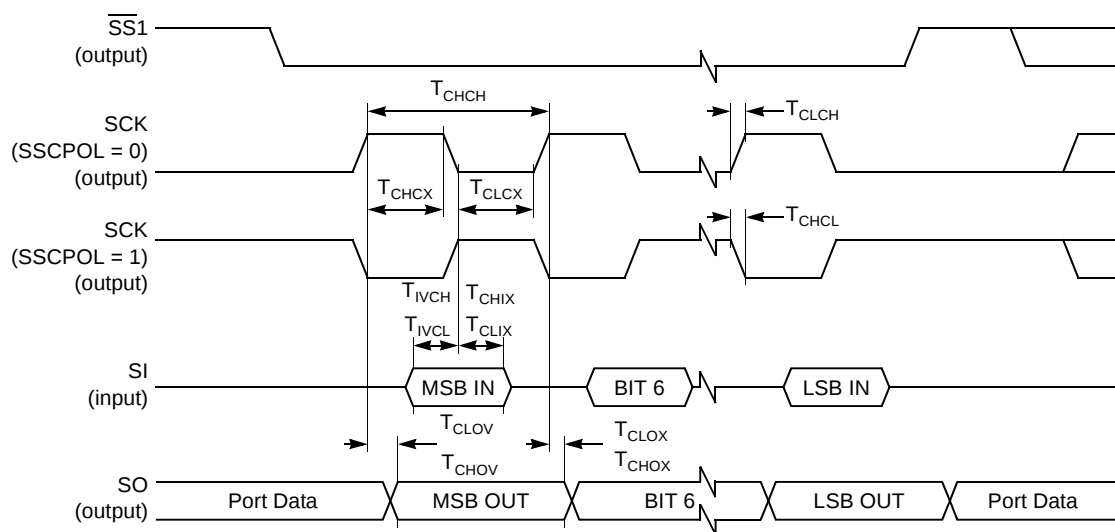
Note: 1. Not Defined but generally the LSB of the character which has just been received.

**Figure 7. SPI Master Waveforms (SSCPHA = 0)**



Note: 1.  $\overline{SS}$  handled by software using general purpose port pin.

**Figure 8. SPI Master Waveforms (SSCPHA = 1)**



Note: 1.  $\overline{SS}$  handled by software using general purpose port pin.

## Two-wire Interface

### Timings

**Table 1.** TWI Interface AC Timing

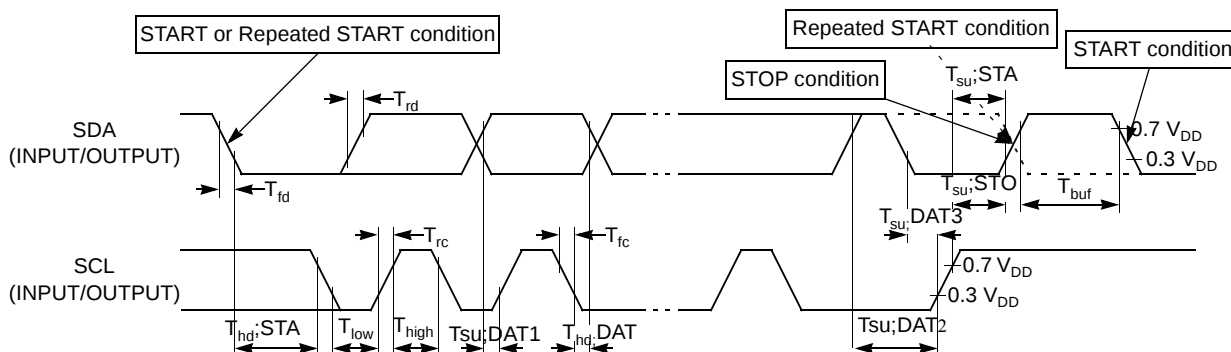
$V_{DD} = 2.7$  to  $3.3$  V,  $T_A = -40$  to  $+85^\circ\text{C}$

| Symbol         | Parameter                                         | INPUT<br>Min<br>Max       | OUTPUT<br>Min<br>Max               |
|----------------|---------------------------------------------------|---------------------------|------------------------------------|
| $T_{HD}; STA$  | Start condition hold time                         | $14 \cdot T_{CLCL}^{(4)}$ | $4.0 \mu\text{s}^{(1)}$            |
| $T_{LOW}$      | SCL low time                                      | $16 \cdot T_{CLCL}^{(4)}$ | $4.7 \mu\text{s}^{(1)}$            |
| $T_{HIGH}$     | SCL high time                                     | $14 \cdot T_{CLCL}^{(4)}$ | $4.0 \mu\text{s}^{(1)}$            |
| $T_{RC}$       | SCL rise time                                     | $1 \mu\text{s}$           | $_{(2)}$                           |
| $T_{FC}$       | SCL fall time                                     | $0.3 \mu\text{s}$         | $0.3 \mu\text{s}^{(3)}$            |
| $T_{SU}; DAT1$ | Data set-up time                                  | $250 \text{ ns}$          | $20 \cdot T_{CLCL}^{(4)} - T_{RD}$ |
| $T_{SU}; DAT2$ | SDA set-up time (before repeated START condition) | $250 \text{ ns}$          | $1 \mu\text{s}^{(1)}$              |
| $T_{SU}; DAT3$ | SDA set-up time (before STOP condition)           | $250 \text{ ns}$          | $8 \cdot T_{CLCL}^{(4)}$           |
| $T_{HD}; DAT$  | Data hold time                                    | $0 \text{ ns}$            | $8 \cdot T_{CLCL}^{(4)} - T_{FC}$  |
| $T_{SU}; STA$  | Repeated START set-up time                        | $14 \cdot T_{CLCL}^{(4)}$ | $4.7 \mu\text{s}^{(1)}$            |
| $T_{SU}; STO$  | STOP condition set-up time                        | $14 \cdot T_{CLCL}^{(4)}$ | $4.0 \mu\text{s}^{(1)}$            |
| $T_{BUF}$      | Bus free time                                     | $14 \cdot T_{CLCL}^{(4)}$ | $4.7 \mu\text{s}^{(1)}$            |
| $T_{RD}$       | SDA rise time                                     | $1 \mu\text{s}$           | $_{(2)}$                           |
| $T_{FD}$       | SDA fall time                                     | $0.3 \mu\text{s}$         | $0.3 \mu\text{s}^{(3)}$            |

- Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
  2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be  $< 1 \mu\text{s}$ .
  3. Spikes on the SDA and SCL lines with a duration of less than  $3 \cdot T_{CLCL}$  will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
  4.  $T_{CLCL} = T_{OSC}$  = one oscillator clock period.

### Waveforms

**Figure 9.** Two Wire Waveforms



## MMC Interface

### Definition of Symbols

**Table 9.** MMC Interface Timing Symbol Definitions

| Signals |          |
|---------|----------|
| C       | Clock    |
| D       | Data In  |
| O       | Data Out |

| Conditions |                 |
|------------|-----------------|
| H          | High            |
| L          | Low             |
| V          | Valid           |
| X          | No Longer Valid |

### Timings

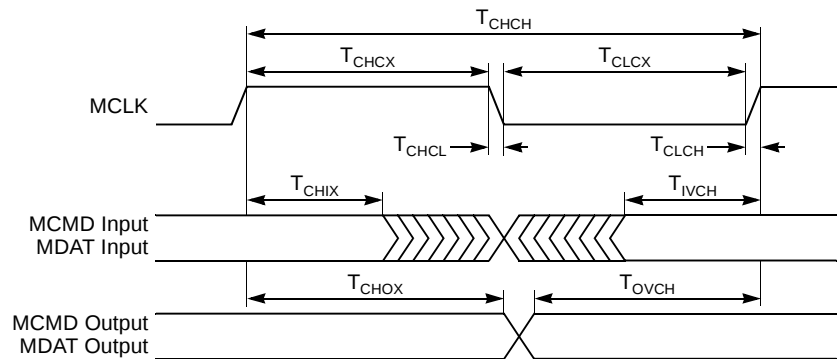
**Table 10.** MMC Interface AC Timings

$V_{DD} = 2.7$  to  $3.3$  V,  $T_A = -40$  to  $+85^\circ\text{C}$ ,  $CL \leq 100\text{pF}$  (10 cards)

| Symbol     | Parameter                         | Min | Max | Unit |
|------------|-----------------------------------|-----|-----|------|
| $T_{CHCH}$ | Clock Period                      | 50  |     | ns   |
| $T_{CHCX}$ | Clock High Time                   | 10  |     | ns   |
| $T_{CLCX}$ | Clock Low Time                    | 10  |     | ns   |
| $T_{CLCH}$ | Clock Rise Time                   |     | 10  | ns   |
| $T_{CHCL}$ | Clock Fall Time                   |     | 10  | ns   |
| $T_{DVCH}$ | Input Data Valid to Clock High    | 3   |     | ns   |
| $T_{CHDX}$ | Input Data Hold after Clock High  | 3   |     | ns   |
| $T_{CHOX}$ | Output Data Hold after Clock High | 5   |     | ns   |
| $T_{OVCH}$ | Output Data Valid to Clock High   | 5   |     | ns   |

### Waveforms

**Figure 10.** MMC Input Output Waveforms



## Audio Interface

### Definition of Symbols

**Table 11.** Audio Interface Timing Symbol Definitions

| Signals |             | Conditions |                 |
|---------|-------------|------------|-----------------|
| C       | Clock       | H          | High            |
| O       | Data Out    | L          | Low             |
| S       | Data Select | V          | Valid           |
|         |             | X          | No Longer Valid |

### Timings

**Table 12.** Audio Interface AC timings

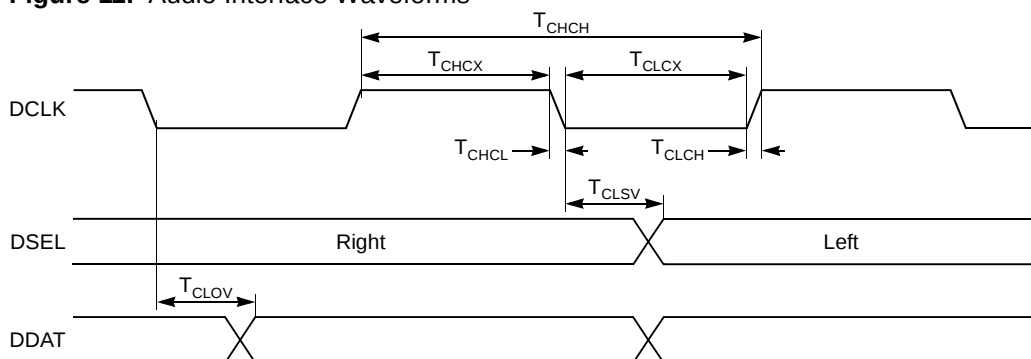
$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40$  to  $+85^{\circ}C$ ,  $CL \leq 30pF$

| Symbol     | Parameter                 | Min | Max                  | Unit |
|------------|---------------------------|-----|----------------------|------|
| $T_{CHCH}$ | Clock Period              |     | 325.5 <sup>(1)</sup> | ns   |
| $T_{CHCX}$ | Clock High Time           | 30  |                      | ns   |
| $T_{CLCX}$ | Clock Low Time            | 30  |                      | ns   |
| $T_{CLCH}$ | Clock Rise Time           |     | 10                   | ns   |
| $T_{CHCL}$ | Clock Fall Time           |     | 10                   | ns   |
| $T_{CLSV}$ | Clock Low to Select Valid |     | 10                   | ns   |
| $T_{CLOV}$ | Clock Low to Data Valid   |     | 10                   | ns   |

Note: 32-bit format with  $F_s = 48$  kHz.

### Waveforms

**Figure 11.** Audio Interface Waveforms



## Analog to Digital Converter

### Definition of Symbols

**Table 13.** Analog to Digital Converter Timing Symbol Definitions

| Signals |                              | Conditions |      |
|---------|------------------------------|------------|------|
| C       | Clock                        | H          | High |
| E       | Enable (ADEN bit)            | L          | Low  |
| S       | Start Conversion (ADSST bit) |            |      |

### Characteristics

**Table 2.** Analog to Digital Converter AC Characteristics

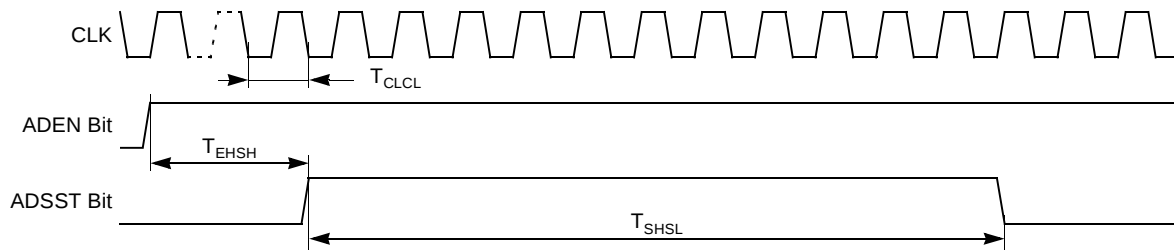
$V_{DD} = 2.7$  to  $3.3$  V,  $T_A = -40$  to  $+85^\circ\text{C}$

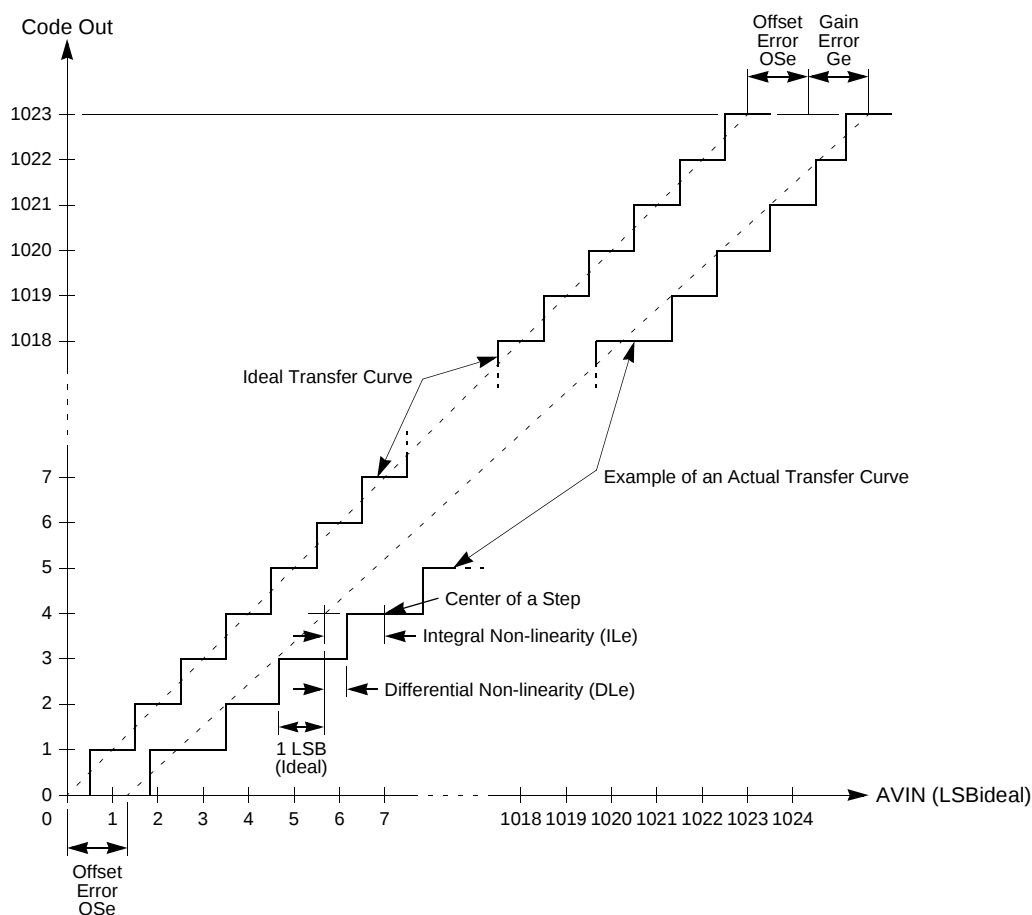
| Symbol     | Parameter                                          | Min | Max                 | Unit          |
|------------|----------------------------------------------------|-----|---------------------|---------------|
| $T_{CLCL}$ | Clock Period                                       | 4   |                     | $\mu\text{s}$ |
| $T_{EHS}$  | Start-up Time                                      |     | 4                   | $\mu\text{s}$ |
| $T_{SHSL}$ | Conversion Time                                    |     | $11 \cdot T_{CLCL}$ | $\mu\text{s}$ |
| DLe        | Differential non-linearity error <sup>(1)(2)</sup> |     | 1                   | LSB           |
| ILe        | Integral non-linearity error <sup>(1)(3)</sup>     |     | 2                   | LSB           |
| OSe        | Offset error <sup>(1)(4)</sup>                     |     | 4                   | LSB           |
| Ge         | Gain error <sup>(1)(5)</sup>                       |     | 4                   | LSB           |

- Notes:
1.  $V_{DD} = V_{REFP} = 3.0$  V,  $V_{SS} = V_{REFN} = 0$  V. ADC is monotonic with no missing code.
  2. The differential non-linearity is the difference between the actual step width and the ideal step width (see Figure 23).
  3. The integral non-linearity is the peak difference between the center of the actual step and the ideal transfer curve after appropriate adjustment of gain and offset errors (see Figure 23).
  4. The offset error is the absolute difference between the straight line which fits the actual transfer curve (after removing of gain error), and the straight line which fits the ideal transfer curve (see Figure 23).
  5. The gain error is the relative difference in percent between the straight line which fits the actual transfer curve (after removing of offset error), and the straight line which fits the ideal transfer curve (see Figure 23).

### Waveforms

**Figure 12.** Analog-to-Digital Converter Internal Waveforms



**Figure 13.** Analog-to-Digital Converter Characteristics

## Flash Memory

### Definition of Symbols

**Table 14.** Flash Memory Timing Symbol Definitions

| Signals |                         |
|---------|-------------------------|
| S       | $\overline{\text{ISP}}$ |
| R       | RST                     |
| B       | FBUSY flag              |

| Conditions |                 |
|------------|-----------------|
| L          | Low             |
| V          | Valid           |
| X          | No Longer Valid |

### Timings

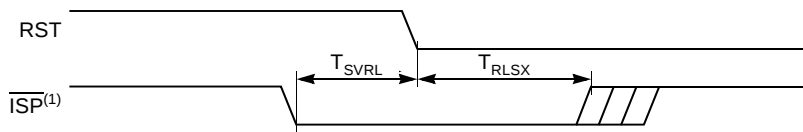
**Table 15.** Flash Memory AC Timing

$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40^\circ$  to  $+85^\circ C$

| Symbol     | Parameter                                         | Min  | Typ | Max | Unit  |
|------------|---------------------------------------------------|------|-----|-----|-------|
| $T_{SVRL}$ | Input $\overline{\text{ISP}}$ Valid to RST Edge   | 50   |     |     | ns    |
| $T_{RLSX}$ | Input $\overline{\text{ISP}}$ Hold after RST Edge | 50   |     |     | ns    |
| $T_{BHBL}$ | FLASH Internal Busy (Programming) Time            |      | 10  |     | ms    |
| $N_{FCY}$  | Number of Flash Write Cycles                      | 100K |     |     | Cycle |
| $T_{FDR}$  | Flash Data Retention Time                         | 10   |     |     | Year  |

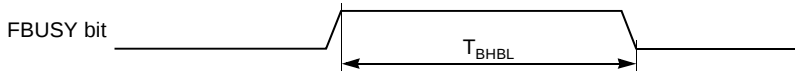
# Waveforms

**Figure 14.** Flash Memory – ISP Waveforms



Note: 1.  $\overline{\text{ISP}}$  must be driven through a pull-down resistor (see Section “In-system Programming”, page 22).

**Figure 15.** Flash Memory – Internal Busy Waveforms



# External Clock Drive and Logic Level References

## Definition of Symbols

**Table 16.** External Clock Timing Symbol Definitions

| Signals |       |
|---------|-------|
| C       | Clock |

| Conditions |                 |
|------------|-----------------|
| H          | High            |
| L          | Low             |
| X          | No Longer Valid |

## Timings

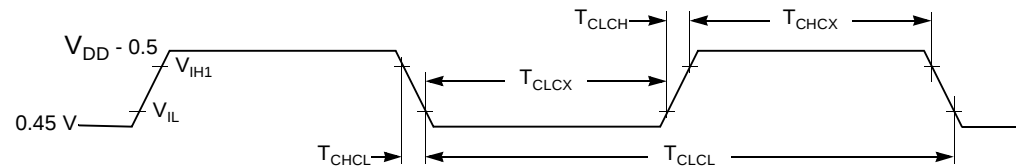
**Table 17.** External Clock AC Timings

$V_{DD} = 2.7$  to  $3.3V$ ,  $T_A = -40$  to  $+85^{\circ}C$

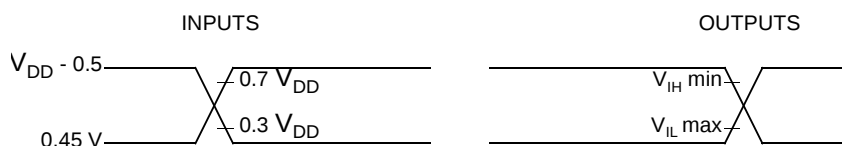
| Symbol     | Parameter               | Min | Max | Unit |
|------------|-------------------------|-----|-----|------|
| $T_{CLCL}$ | Clock Period            | 50  |     | ns   |
| $T_{CHCX}$ | High Time               | 10  |     | ns   |
| $T_{CLCX}$ | Low Time                | 10  |     | ns   |
| $T_{CLCH}$ | Rise Time               | 3   |     | ns   |
| $T_{CHCL}$ | Fall Time               | 3   |     | ns   |
| $T_{CR}$   | Cyclic Ratio in X2 Mode | 40  | 60  | %    |

# Waveforms

**Figure 16.** External Clock Waveform

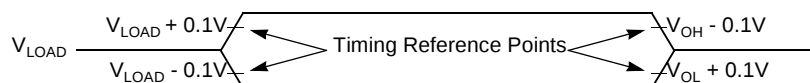


**Figure 17.** AC Testing Input/Output Waveforms



- Notes:
1. During AC testing, all inputs are driven at  $V_{DD} - 0.5V$  for a logic 1 and  $0.45V$  for a logic 0.
  2. Timing measurements are made on all outputs at  $V_{IH \text{ min}}$  for a logic 1 and  $V_{IL \text{ max}}$  for a logic 0.

**Figure 18.** Float Waveforms



- Note:
- For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading  $V_{OH}/V_{OL}$  level occurs with  $I_{OL}/I_{OH} = \pm 20 \text{ mA}$ .



## Ordering Information

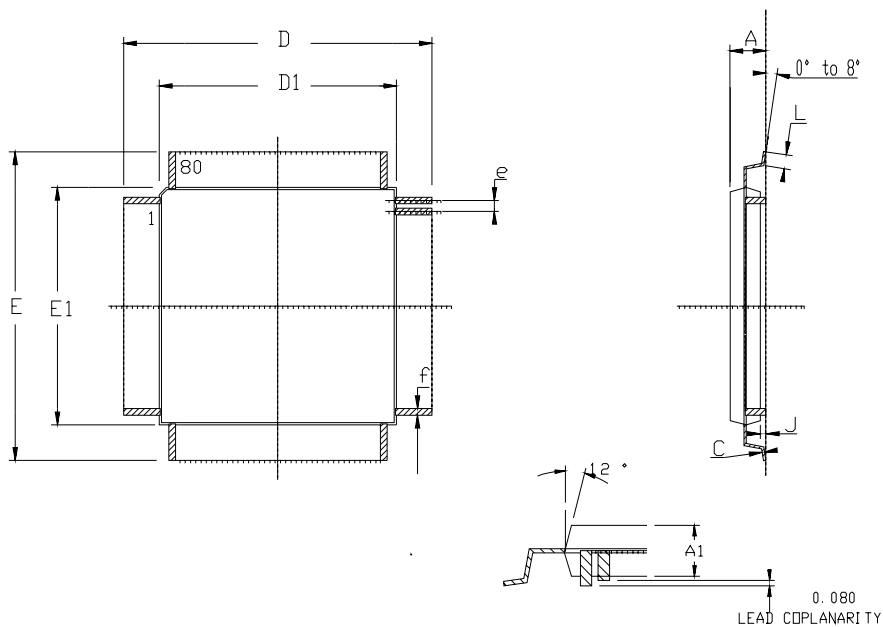
Possible Order Entries<sup>(1)</sup>

| Part Number     | Memory Size<br>(Bytes) | Supply<br>Voltage | Temperature<br>Range | Max<br>Frequency<br>(MHz) | Package | Packing | Product<br>Marking |
|-----------------|------------------------|-------------------|----------------------|---------------------------|---------|---------|--------------------|
| AT89C5132-ROTIL | 64K Flash              | 3V                | Industrial           | 40                        | TQFP80  | Tray    | 895132-IL          |

Note: 1. PLCC84 package only available for development board.

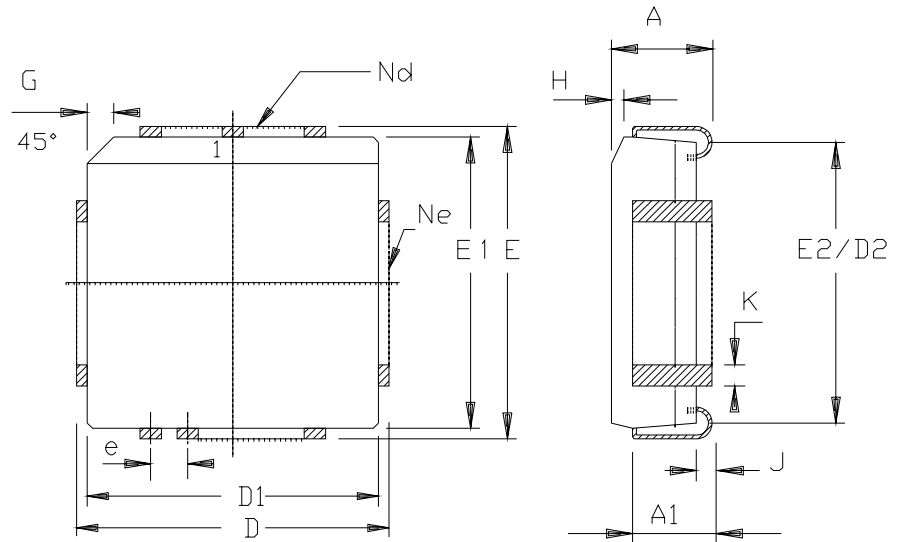
# Package Information

## TQFP80



|    | MM       |       | INCH      |      |
|----|----------|-------|-----------|------|
|    | Min      | Max   | Min       | Max  |
| A  | 1.40     | 1.60  | .055      | .063 |
| A1 | 1.35     | 1.45  | .053      | .057 |
| C  | 0.17 BSC |       | .007 BSC  |      |
| D  | 15.80    | 16.20 | .622      | .638 |
| D1 | 13.90    | 14.10 | .547      | .555 |
| E  | 15.80    | 16.20 | .622      | .638 |
| E1 | 13.90    | 14.10 | .547      | .555 |
| J  | 0.05     | 0.15  | .002      | .006 |
| L  | 0.45     | 0.75  | .018      | .030 |
| e  | 0.65 BSC |       | .0256 BSC |      |
| f  | 0.30 BSC |       | .012 BSC  |      |

# PLCC84



|         | MM     |        | INCH   |        |
|---------|--------|--------|--------|--------|
| A       | 4. 20  | 5. 08  | . 165  | . 200  |
| A1      | 2. 29  | 3. 30  | . 090  | . 130  |
| D       | 30. 10 | 30. 35 | 1. 185 | 1. 195 |
| D1      | 29. 21 | 29. 41 | 1. 150 | 1. 158 |
| D2      | 27. 69 | 28. 70 | 1. 090 | 1. 130 |
| E       | 30. 10 | 30. 35 | 1. 185 | 1. 195 |
| E1      | 29. 21 | 29. 41 | 1. 150 | 1. 158 |
| E2      | 27. 69 | 28. 70 | 1. 090 | 1. 130 |
| e       | 1. 27  | BSC    | . 050  | BSC    |
| G       | 1. 07  | 1. 22  | . 042  | . 048  |
| H       | 1. 07  | 1. 42  | . 042  | . 056  |
| J       | 0. 51  | -      | . 020  | -      |
| K       | 0. 33  | 0. 53  | . 013  | . 021  |
| Nd      | 21     |        | 21     |        |
| Ne      | 21     |        | 21     |        |
| PKG STD |        | 00     |        |        |

## Datasheet Change Log for AT89C5132

### Changes from 4173A-08/02 to 4173B-03/04

1. Supression of ROM product version.
2. Supression of TQFP64 package.

### Changes from 4173B-03/04 - 4173C - 07/04

1. Add USB connection schematic in USB section.
2. Add USB termination characteristics in DC Characteristics section.
3. Page access mode clarification in Data Memory section.



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