MAX14661

Beyond-the-Rails 16:2 Multiplexer

General Description

The MAX14661 is a serially controlled, dual-channel analog multiplexer allowing any of the 16 pins to be connected to either common pin simultaneously in any combination. The device features Beyond-the-Rails™ capability so that ±5.5V signals can be passed with any single supply between +1.6V and +5.5V.

The serial control is selectable between I²C and SPI. Both modes provide individual control of each independent switch so that any combination of switches can be applied. I²C mode provides two address-select pins allowing for addressing up to four devices on a single bus. The SPI mode includes a DOUT pin that can be used to chain multiple devices together with a single select signal.

The IC is available in a 28-pin (4mm x 4mm) TQFN package and is specified over the -40ºC to +85ºC extended temperature range. The AB_ and COM_ pins provide ±10kV ESD protection (HBM).

Applications

- System Diagnostics
- Data Acquisition
- I²C Signal Switching
- Audio Input Selection

Features and Benefits

- Beyond-the-Rails Technology Reduces Cost and Complexity
  - Switch ±5.5V Signals from a +1.6V Single Supply
  - Wide +1.6V to +5.5V Supply Range
  - Low 5.5Ω R_{ON} (typ) Across the Supply Range
- Flexible Multiplexing Enables Design Reuse
  - 16:2 Matrix Switch Multiplexer Connects Any Input Pin To Either Common Pin In Any Combination
  - Each Switch is Independently Controlled via I²C or SPI
  - Programmable Shadow Registers Allow Simultaneous Updating
- Low Distortion Switching Improves System Performance
  - Total Harmonic Distortion + Noise 0.005% (typ)
  - R_{ON} Flatness 2.5mΩ (typ) Across Complete Signal Range
- Integrated Protection for System Reliability
  - ±10kV HBM ESD Protection on all AB_ and COM_ Pins, Even When Powered Down

***Ordering Information* appears at end of data sheet.**

19-6739; Rev 2; 1/15

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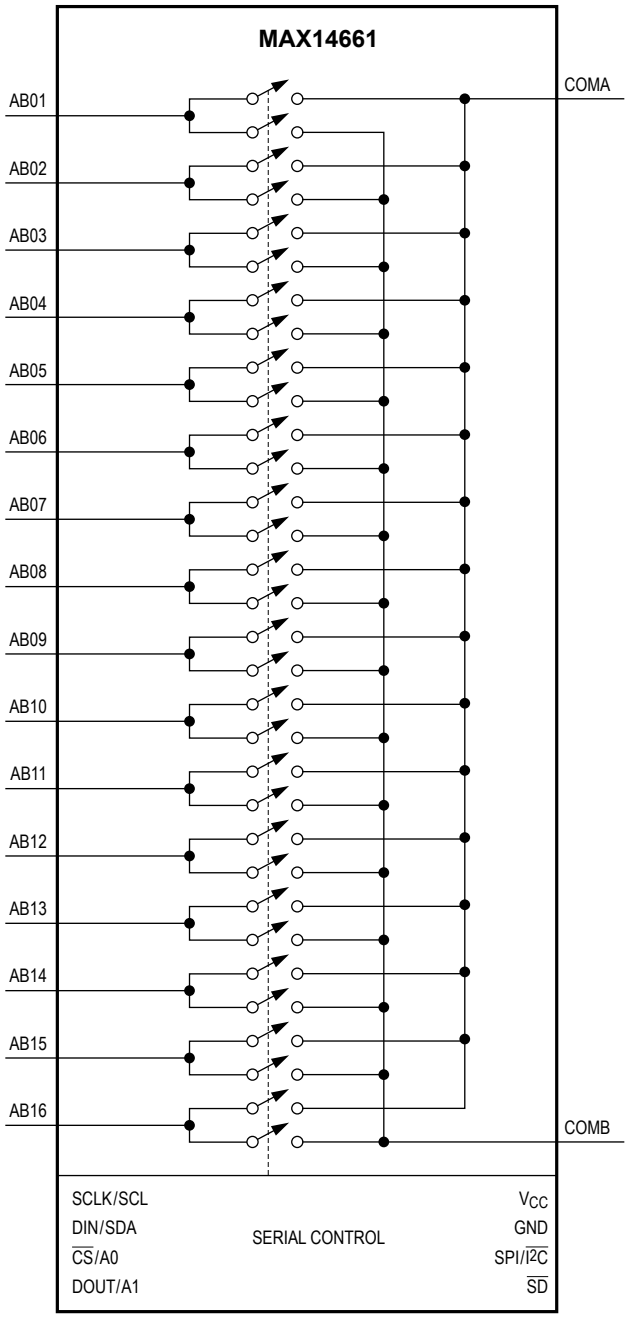
Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{CC}, DIN/SDA, SCLK/SCL, DOUT/A1, $\overline{CS}$/A0, $\overline{SD}$ ..... -0.3V to +6.0V
SPI/I^2C..... -0.3V to min (V_{CC} to +0.3V, 6V)
AB_, COM_ .....-6.0V to +6.0V
Continuous Current (AB_ or COM_ to any switch).....±50mA
Peak Current (AB_ or COM_ to any switch)
(pulsed at 1ms, maximum 10% duty cycle).....±100mA

Continuous Power Dissipation
28 TQFN (derate 28.6mW/ºC above +70ºC).....2285.7mW
Operating Temperature Range.....-40ºC to +85ºC
Maximum Junction Temperature .....+150ºC
Storage Temperature Range.....-65ºC to +150ºC
Lead Temperature (soldering, 10s) .....+300ºC
Soldering Temperature (reflow).....+260ºC

Package Thermal Characteristics (Note 1)

Junction-to-Case Thermal Resistance (θ_{JC})
TQFN.....3ºC/W

Junction-to-Ambient Thermal Resistance (θ_{JA})
TQFN.....35ºC/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = +1.6V to +5.5V, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25ºC, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power-Supply Range	V_{CC}		1.6		5.5	V
Power-Supply Rejection Ratio	PSRR	R_{COM} = 50Ω, V_{CC} = +3.3V ±0.1V, f = 10kHz		-84		dB
V_{CC} Supply Current	I_{CC}	V_{CC} = +3.3V, all switches on		675	1500	µA
		V_{CC} = +3.3V, two switches on		115	200	
		V_{CC} = +3.3V, $\overline{SD}$ = 0			1	
ANALOG SWITCH						
Analog Signal Range	$V_{AB\_}$, $V_{COM\_}$		-5.5		+5.5	V
Analog Signal Amplitude (Notes 3, 4)	V_{P-P}	V_{CC} > 2.5V			11	V
		f < 500kHz			11	
		V_{CC} < 2.5V, f > 500kHz			6	
On-Resistance	R_{ON}	V_{CC} = +5V			8	Ω
		V_{CC} = +1.8V			12	
On-Resistance Match between Channels	ΔR_{ON}	V_{CC} = 3.3V, between COM_ and AB_		0.25		Ω
On-Resistance Flatness	R_{FLAT}	V_{CC} = 3.3V, $I_{COM\_}$ = 10mA, $V_{COM\_}$ = -5.5V to +5.5V		25		mΩ
AB_, COM_ Off-Leakage Current	I_{OFF}	V_{CC} = 3.3V, switch open, $V_{COM\_}$ = -5.5V, +5.5V $V_{AB\_}$ = +5.5V, -5.5V, unconnected (Notes 3, 5)	-50		+50	nA

Electrical Characteristics (continued)

(V_{CC} = +1.6V to +5.5V, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25ºC, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AB_, COM_ On-Leakage Current	I_{ON}	V_{CC} = 3.3V, switch closed, $V_{COM\_}$ = $V_{AB\_}$ = ±5.5V (Notes 3, 5)	-50		+50	nA
DYNAMIC PERFORMACE (Notes 6, 7)						
Turn-Off Time	t_{OFF}	$V_{COM\_}$ = 3.0V, R_L = 100Ω, C_L = 33pF, open COM_ and AB_ together		5		µs
Break-Before-Make Time	t_{BBM}	$V_{COM\_}$ = 3.0V, R_L = 100Ω, C_L = 33pF, time for both switching channels are open during transition	0			µs
Turn-On Time	t_{ON}	$V_{COM\_}$ = 3.0V, R_L = 100Ω, C_L = 33pF; close AB_ and COMA or AB_ and COMB together		13	25	µs
Enable Time	t_{EN}	Time from when $\overline{SD}$ pin goes high to when the device is ready to listen for I²C/SPI comunications			300	µs
Bandwidth -3dB	BW	R_S = R_L = 50Ω (Notes 7, 8), $V_{COM\_}$ = $0.6V_{P-P}$		60		MHz
Total Harmonic Distortion Plus Noise	THD + N	f = 20Hz to 20kHz, $V_{COM\_}$ = $0.5V_{P-P}$, R_S = R_L = 50Ω, DC bias = 0		0.005		%
Off-Isolation	V_{ISO}	R_S = R_L = 50Ω, $V_{COM\_}$ = $0.6V_{P-P}$, f = 1MHz (Note 8)		-62		dB
Crosstalk	V_{CT}	R_S = R_L = 50Ω, V_{COM} = $0.6V_{P-P}$, f = 1MHz (Note 8)		-80		dB
Thermal Shutdown	T_{SDW}			150		ºC
Thermal Hysteresis	T_{HYST}			25		ºC
SPI TIMING CHARACTERISTICS (See Figure 12)						
SCLK Clock Period	t_{CH} + t_{CL}		95			ns
SCLK Pulse-Width High	t_{CH}		35			ns
SCLK Pulse-Width Low	t_{CL}		45			ns
$\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}		15			ns
DIN Hold Time	t_{DH}		15			ns
DIN Setup Time	t_{DS}		15			ns
Output Data Propagation Delay	t_{DO}	C_L = 15pF, V_{CC} ≥ 2.7V			40	ns
		C_L = 15pF, 1.6V ≤ V_{CC} < 2.7V			80	
DOUT Rise and Fall Times	t_{FT}	C_L = 15pF		10		ns
$\overline{CS}$ Hold Time	t_{CSH}		60			ns
I²C TIMING (See Figure 4)						
I²C Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs

Electrical Characteristics (continued)

(V_{CC} = +1.6V to +5.5V, T_A = -40ºC to +85ºC, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25ºC, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Valid to SCL Rise Time	$t_{SU:DAT}$	Write setup time	100			ns
Data Hold Time to SCL Fall	$t_{HD:DAT}$	Write hold time	0			ns
DIGITAL I/O						
Input Logic-High Voltage	V_{IH}		1.4			V
Input Logic-Low Voltage (DIN/SDA, SCLK/SCL, $\overline{CS}$/A0)	V_{IL_FAST}				0.5	V
Input Logic-Low Voltage (DOUT/A1 $\overline{SD}$)	V_{IL_SLOW}				0.4	V
Input Leakage Current	I_{IN}		-1		+1	µA
SPI/$\overline{I^2C}$ I²C Threshold	V_{I2C}				0.4	V
SPI/$\overline{I^2C}$ SPI Threshold	V_{SPI}		1.5			V
Output Logic Low (I²C mode)	V_{OL_I2C}	I_{SINK} = 3mA			0.4	V
SPI/$\overline{I^2C}$ SPI Supply Voltage	V_{OVDD}		1.5		5.5	V
Output Logic-Low (SPI Mode)	V_{OL_SPI}	I_{SINK} = 200µA			0.15 x V_{OVDD}	V
Output Logic-High (SPI Mode)	V_{OH_SPI}	I_{SOURCE} = 200µA	0.85 x V_{OVDD}			V
ESD PROTECTION						
All AB_ and COM_ Pins		HBM		±10		kV
All Others Pins		HBM		±2		kV

Note 2: All devices are 100% production tested at T_A = +25ºC. Specifications over temperature are guaranteed by design.
Note 3: Guaranteed by design.
Note 4: See the *Typical Operating Characteristics* Maximum Signal Amplitude vs. Supply Voltage for f > 500kHz for more details.
Note 5: Test circuit Figure 1.
Note 6: Test circuit Figure 2.
Note 7: Supply voltage and signal amplitude can affect the frequency response of the device. See amplitude frequency stability in the *Typical Operating Characteristics* for more details.
Note 8: Test circuit Figure 3.

Test Circuits/Timing Diagrams

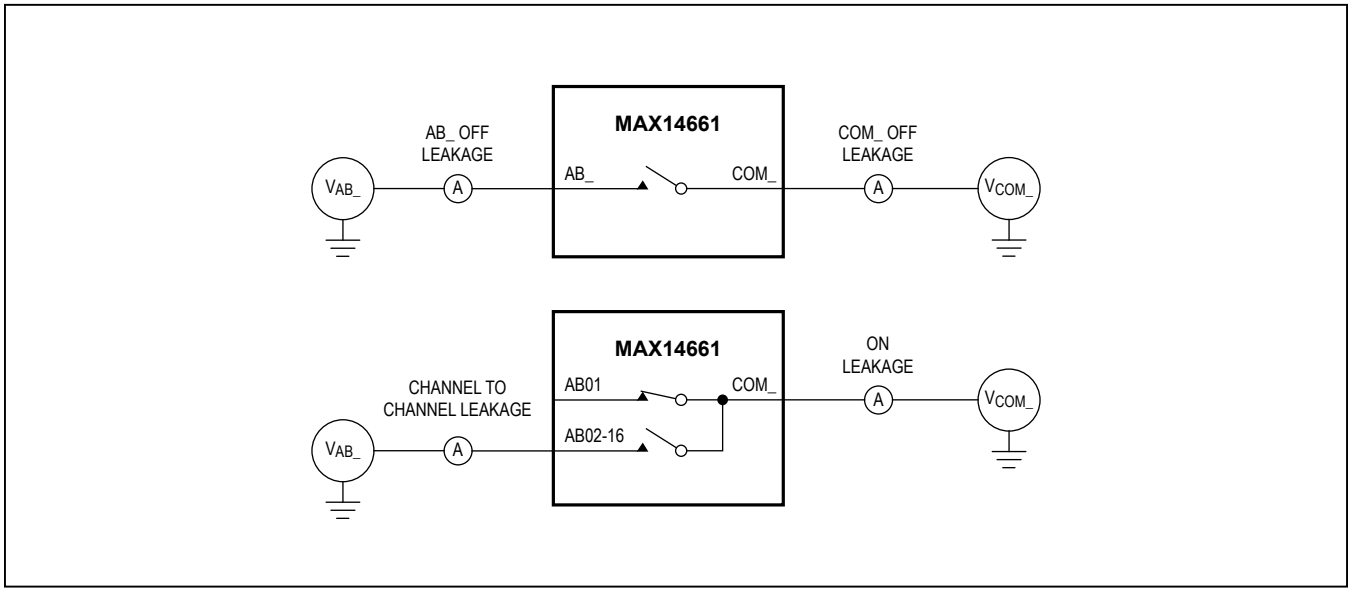


Figure 1. On-/Off-/Channel-to-Channel Leakage Current

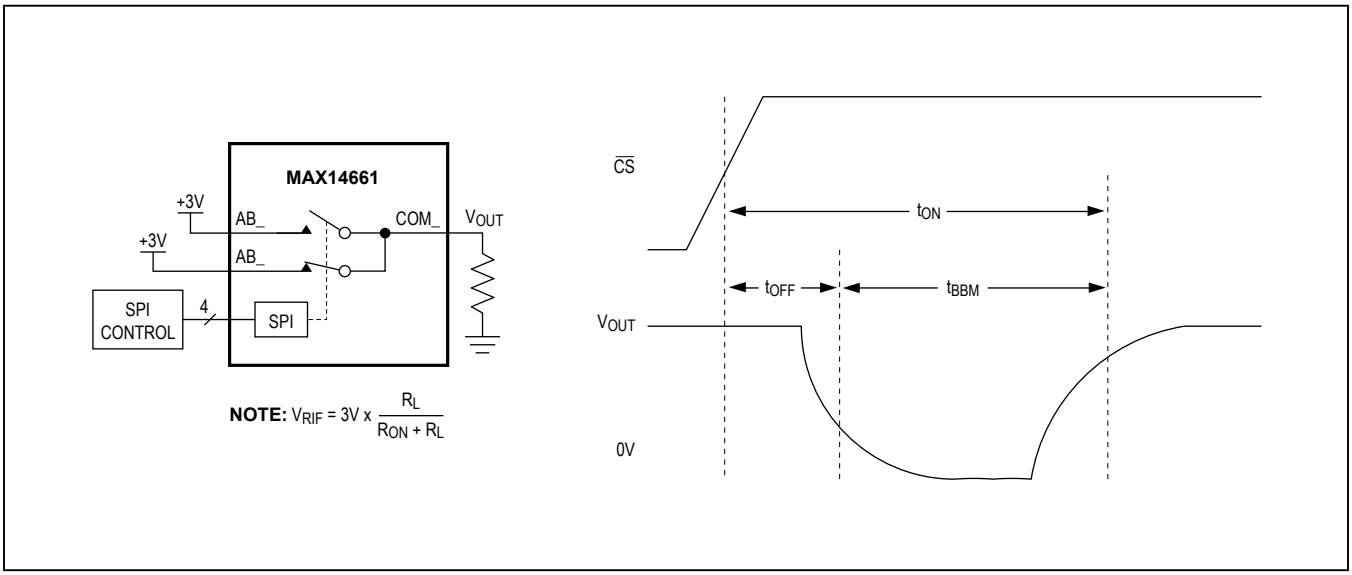


Figure 2. Turn-On/Turn-Off/Break-Before-Make

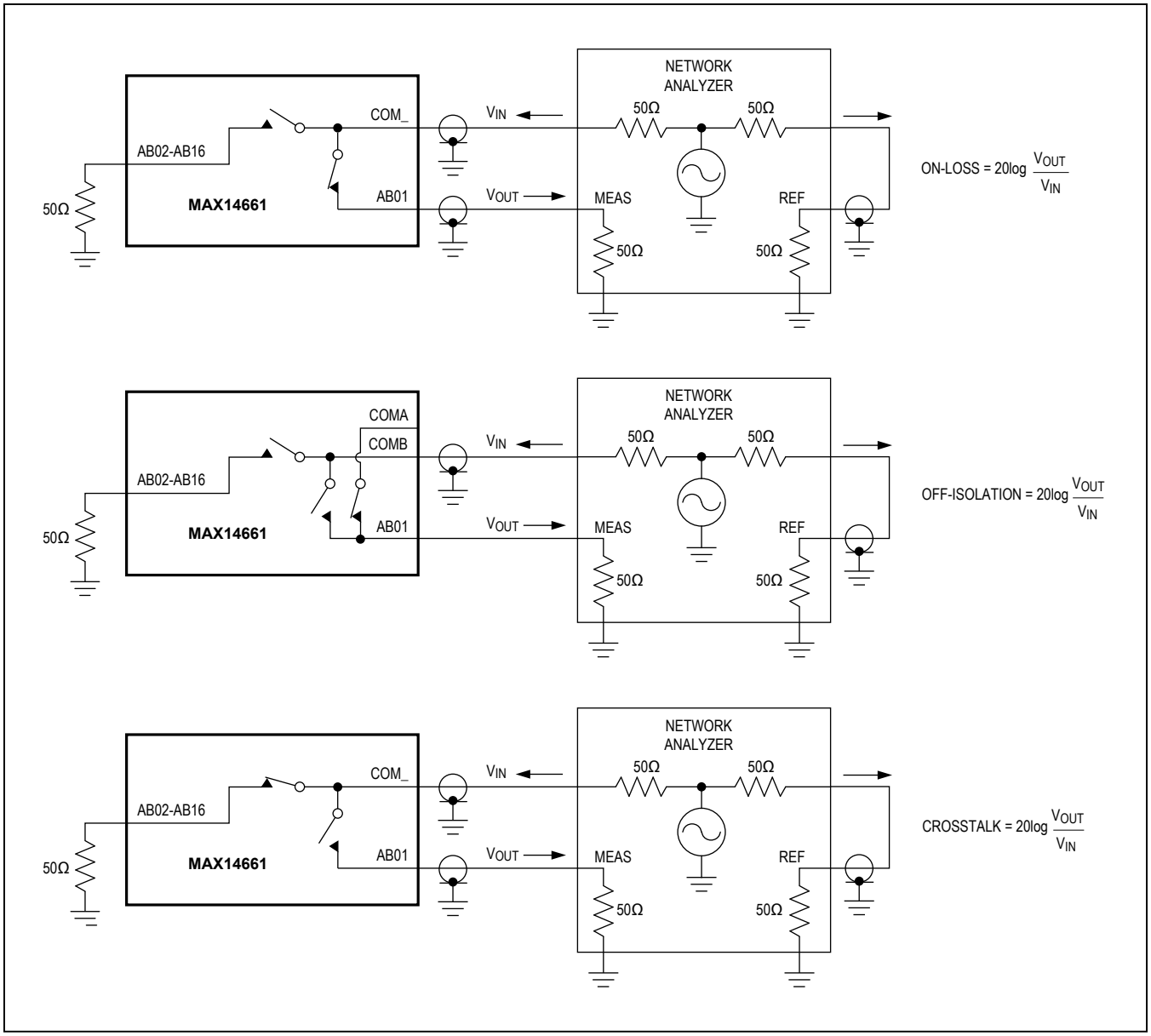
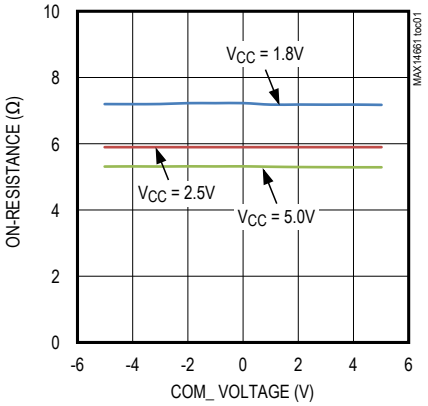


Figure 3. Insertion Loss, Off-Isolation, and Crosstalk

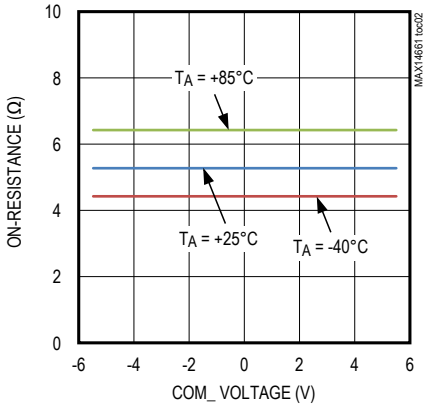
Typical Operating Characteristics

(V_{CC} = +1.6V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

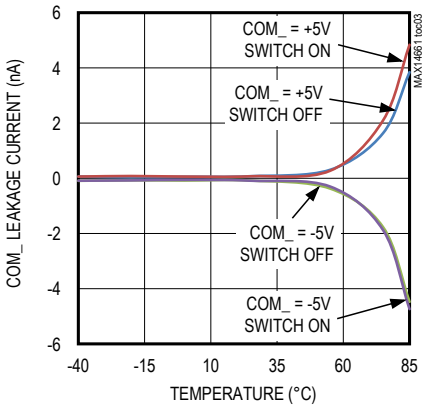
ON-RESISTANCE vs. COM_ VOLTAGE



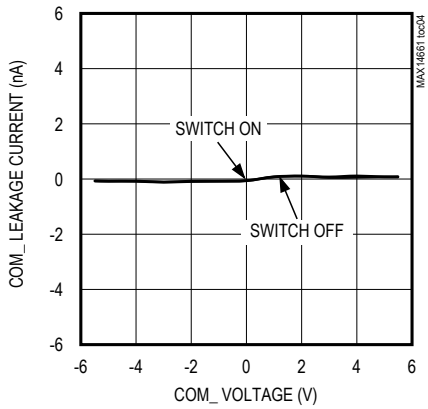
ON-RESISTANCE vs. COM_ VOLTAGE



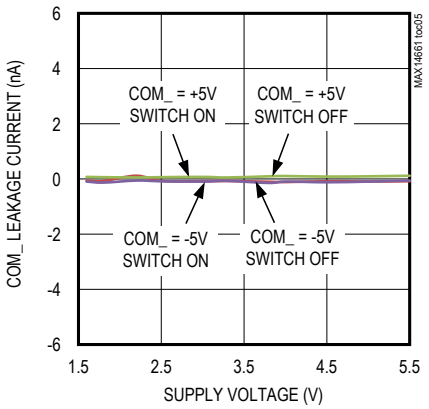
COM_ LEAKAGE CURRENT vs. TEMPERATURE



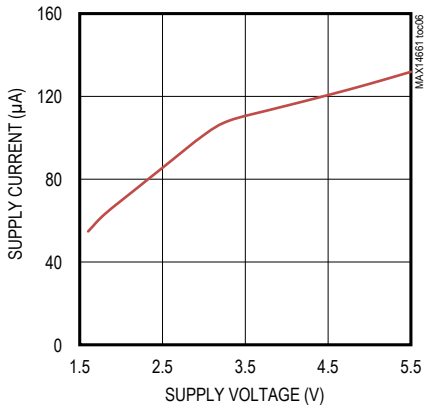
COM_ LEAKAGE CURRENT vs. COM_ VOLTAGE



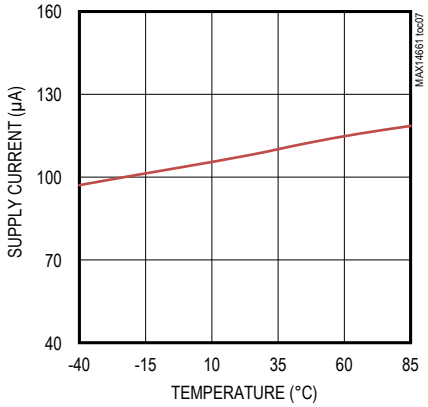
COM_ LEAKAGE CURRENT vs. SUPPLY VOLTAGE



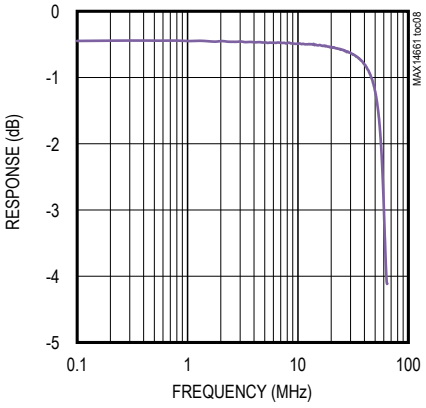
SUPPLY CURRENT vs. SUPPLY VOLTAGE (TWO SWITCHES ON)



SUPPLY CURRENT vs. TEMPERATURE (TWO SWITCHES ON)



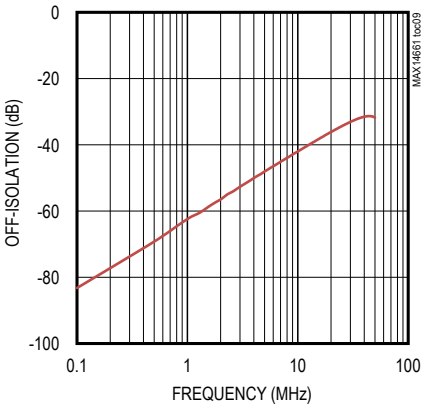
FREQUENCY RESPONSE



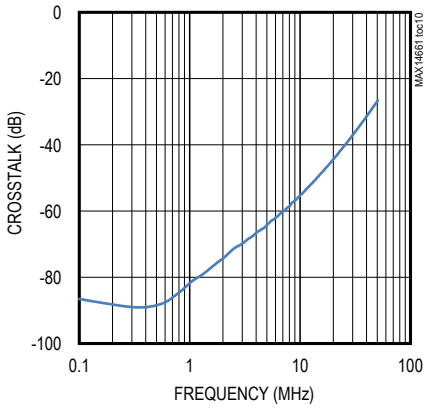
Typical Operating Characteristics (continued)

(V_{CC} = +1.6V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

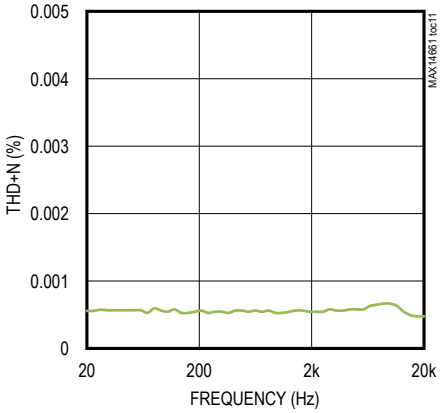
OFF-ISOLATION vs. FREQUENCY



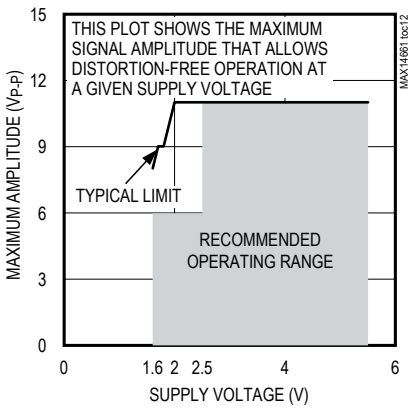
CROSSTALK vs. FREQUENCY



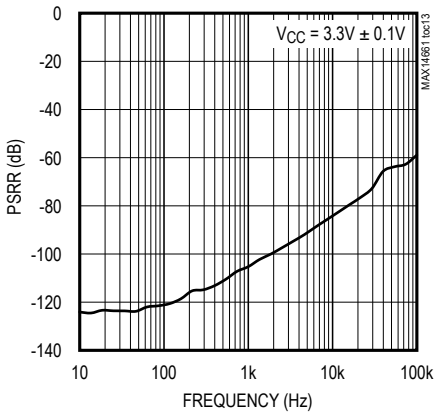
TOTAL HARMONIC DISTORTION + NOISE (THD+N) vs. FREQUENCY



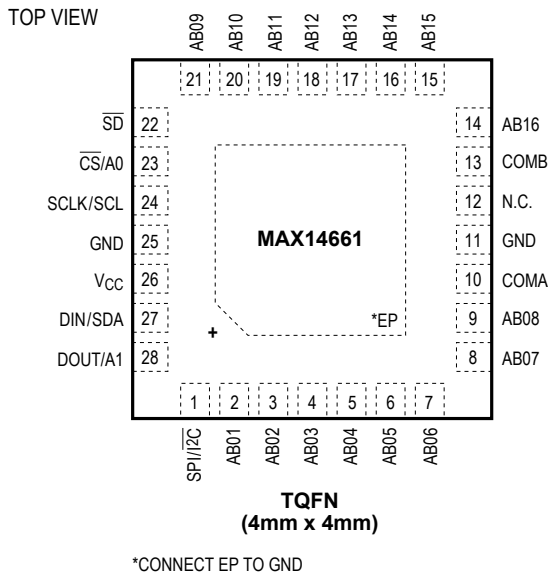
MAXIMUM SIGNAL AMPLITUDE vs. SUPPLY VOLTAGE f > 500kHz



PSRR vs. FREQUENCY



Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	SPI/ $\overline{I^2C}$	Serial Mode Select SPI (high) or I²C (low), Supply Input for DOUT
2	AB01	AB Connection to Switches 1A and 1B
3	AB02	AB Connection to Switches 2A and 2B
4	AB03	AB Connection to Switches 3A and 3B
5	AB04	AB Connection to Switches 4A and 4B
6	AB05	AB Connection to Switches 5A and 5B
7	AB06	AB Connection to Switches 6A and 6B
8	AB07	AB Connection to Switches 7A and 7B
9	AB08	AB Connection to Switches 8A and 8B
10	COMA	Common Connection to All A Switches

Pin Description (continued)

PIN	NAME	FUNCTION
11	GND	Ground
12	N.C.	Not Connected
13	COMB	Common Connection to All B Switches
14	AB16	AB Connection to Switches 16A and 16B
15	AB15	AB Connection to Switches 15A and 15B
16	AB14	AB Connection to Switches 14A and 14B
17	AB13	AB Connection to Switches 13A and 13B
18	AB12	AB Connection to Switches 12A and 12B
19	AB11	AB Connection to Switches 11A and 11B
20	AB10	AB Connection to Switches 10A and 10B
21	AB09	AB Connection to Switches 9A and 9B
22	$\overline{SD}$	Active-Low Shutdown/Low-Power Mode, Turns All Switches Off
23	$\overline{CS}$/A0	I2C Address Bit 0/SPI $\overline{CS}$ Signal
24	SCLK/SCL	I2C Serial Clock/SPI Serial Clock
25	GND	Ground
26	V_{CC}	Power-Supply Input
27	DIN/SDA	I2C Serial Data/SPI Data Input
28	DOUT/A1	I2C Address Bit 1/SPI Data Output
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Table 1. Register Map

ADDRESS	NAME	TYPE	DEFAULT	DESCRIPTION
0x00	DIR0	RW	0x00	Switches 8A–1A direct read/write access
0x01	DIR1	RW	0x00	Switches 16A–9A direct read/write access
0x02	DIR2	RW	0x00	Switches 8B–1B direct read/write access
0x03	DIR3	RW	0x00	Switches 16B–9B direct read/write access
0x10	SHDW0	RW	0x00	Switches 8A–1A shadow read/write access
0x11	SHDW1	RW	0x00	Switches 16A–9A shadow read/write access
0x12	SHDW2	RW	0x00	Switches 8B–1B shadow read/write access
0x13	SHDW3	RW	0x00	Switches 16B–9B shadow read/write access
0x14	CMD_A	RW	0x00	Set mux A command (reads 0x00)
0x15	CMD_B	RW	0x00	Set mux B command (reads 0x00)

Register Types: RW = Read/Write

Table 2. Detailed Register Map

DIR0 0x00								
BIT	7	6	5	4	3	2	1	0
BIT Name	Direct_SW8A–1A							
Reset Value	0	0	0	0	0	0	0	0
Description	Direct Register Data for SW8A–1A 0 = Switch open 1 = Switch closed							
DIR1 0x01								
BIT	7	6	5	4	3	2	1	0
BIT Name	Direct_SW16A–9A							
Reset Value	0	0	0	0	0	0	0	0
Description	Direct Register Data for SW16A–9A 0 = Switch open 1 = Switch closed							
DIR2 0x02								
BIT	7	6	5	4	3	2	1	0
BIT Name	Direct_SW8B–1B							
Reset Value	0	0	0	0	0	0	0	0
Description	Direct Register Data for SW8B–1B 0 = Switch open 1 = Switch closed							

Table 2. Detailed Register Map (continued)

DIR3 0x03								
BIT	7	6	5	4	3	2	1	0
BIT Name	Direct_SW16B–9B							
Reset Value	0	0	0	0	0	0	0	0
Description	Direct Register Data for SW16B–9B 0 = Switch open 1 = Switch closed							
SHDW0 0x10								
BIT	7	6	5	4	3	2	1	0
BIT Name	Shadow_SW8A–1A							
Reset Value	0	0	0	0	0	0	0	0
Description	Shadow Register Data for SW8A–1A; temporarily holding registers that support simultaneous updates. 0 = Switch open 1 = Switch closed							
SHDW1 0x11								
BIT	7	6	5	4	3	2	1	0
BIT Name	Shadow_SW16A–9A							
Reset Value	0	0	0	0	0	0	0	0
Description	Shadow Register Data for SW16A–9A; temporarily holding registers that support simultaneous updates. 0 = Switch open 1 = Switch closed							
SHDW2 0x12								
BIT	7	6	5	4	3	2	1	0
BIT Name	Shadow_SW8B–1B							
Reset Value	0	0	0	0	0	0	0	0
Description	Shadow Register Data for SW8B–1B; temporarily holding registers that support simultaneous updates. 0 = Switch open 1 = Switch closed							
SHDW3 0x13								
BIT	7	6	5	4	3	2	1	0
BIT Name	Shadow_SW16B–1B							
Reset Value	0	0	0	0	0	0	0	0
Description	Shadow Register Data for SW16B–9B; temporarily holding registers that support simultaneous updates. 0 = Switch open 1 = Switch closed							

Table 2. Detailed Register Map (continued)

CMD_A 0x14								
BIT	7	6	5	4	3	2	1	0
BIT Name	RFU	RFU	RFU	SelA				
Reset Value	0	0	0	0	0	0	0	0
Description	SelA 00000 = Enable only SW01A (0x0001) 00001 = Enable only SW02A (0x0002) 00010 = Enable only SW03A (0x0004) 00011 = Enable only SW04A (0x0008) 00100 = Enable only SW05A (0x0010) 00101 = Enable only SW06A (0x0020) 00110 = Enable only SW07A (0x0040) 00111 = Enable only SW08A (0x0080) 01000 = Enable only SW09A (0x0100) 01001 = Enable only SW10A (0x0200) 01010 = Enable only SW11A (0x0400) 01011 = Enable only SW12A (0x0800) 01100 = Enable only SW13A (0x1000) 01101 = Enable only SW14A (0x2000) 01110 = Enable only SW15A (0x4000) 01111 = Enable only SW16A (0x8000) 10000 = Disable all bank A switches (0x0000) 10001 = Copy A shadows registers (SHDW0 and SHDW1) to switches 10010 ..11111 = No change on bank A							
CMD_B 0x15								
BIT	7	6	5	4	3	2	1	0
BIT Name	RFU	RFU	RFU	SelB				
Reset Value	0	0	0	0	0	0	0	0
RFU = Reserved Description	SelB 00000 = Enable only SW01B (0x0001) 00001 = Enable only SW02B (0x0002) 00010 = Enable only SW03B (0x0004) 00011 = Enable only SW04B (0x0008) 00100 = Enable only SW05B (0x0010) 00101 = Enable only SW06B (0x0020) 00110 = Enable only SW07B (0x0040) 00111 = Enable only SW08B (0x0080) 01000 = Enable only SW09B (0x0100) 01001 = Enable only SW10B (0x0200) 01010 = Enable only SW11B (0x0400) 01011 = Enable only SW12B (0x0800) 01100 = Enable only SW13B (0x1000) 01101 = Enable only SW14B (0x2000) 01110 = Enable only SW15B (0x4000) 01111 = Enable only SW16B (0x8000) 10000 = Disable all bank B switches (0x0000) 10001 = Copy B shadows registers (SHDW2 and SHDW3) to switches 10010 .. 11111 = No change on bank B							

Detailed Description

Low-Power Shutdown

The device includes an active-low shutdown pin ($\overline{SD}$). When this pin is low, all registers are cleared and all switches are open. The serial interface is not functional when in shutdown. All switch connections are open and tolerant of the full ±5.5V specified signal range. In this mode the part consumes minimal power.

SPI Output Supply

The SPI/$\overline{I^2C}$ pin has a dual purpose. In addition to selecting which serial protocol the part uses, it also functions as the I/O voltage power pin for the SPI DOUT signal. This allows the user to set the output voltage independent of the device supply voltage.

I²C Serial Interface

Direct Access Registers

The direct access registers (DIR0–DIR3) allow the user to read or write the switches eight at a time. These register addresses support automatic incrementing so they can be read or written sequentially. The switches are updated after the last bit of the byte clocked in.

Shadow Registers

The shadow registers (SHDW0–SHDW3) provide storage for switch values to allow for simultaneous updates of the switches. Unlike the direct access registers, these registers have no immediate effect until the copy command is issued. The copy command has to be written in CMD_A and CMD_B registers. Simply write to the four registers with the desired state of each switch, and then write the appropriate command to registers CMD_A and CMD_B to simultaneously apply the values to the switches.

Set Mux Command Registers

The set mux command registers allow the user to easily select any one single switch in a bank. The CMD_A register allows the user to turn on one single switch in bank A, to open the entire bank A switches, to copy SHDW0 and SHDW1 registers to DIR0 and DIR1 registers, or to leave bank A as it is (no changes). Similarly, the CMD_B register allows the user to turn on one single switch in bank B, to open the entire bank B switches, to copy SHDW2 and SHDW3 registers to DIR2 and DIR3 registers, or to leave bank B as it is (no changes). The values apply to the switches after both registers (CMD_A and CMD_B) have been written. CMD_A and CMD_B are a single 16-bit register; therefore, CMD_A must be programmed before CMD_B.

Serial Addressing

When in I²C mode, the MAX14661 operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX14661 and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX14661 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 4).

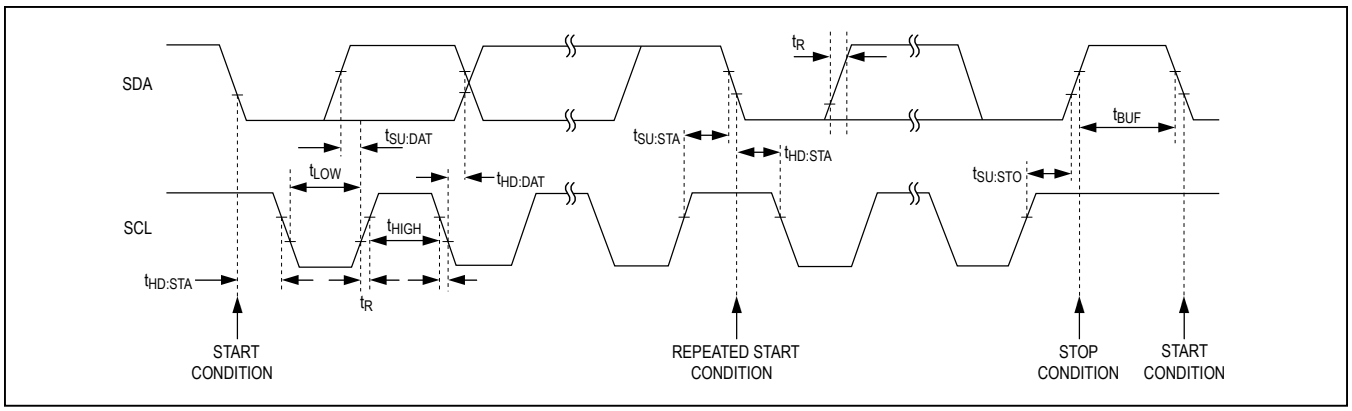


Figure 4. I²C Interface Timing Details

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 5). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 6). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 7), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14661, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the device did not pull SDA low, a not acknowledge is indicated.

Slave Address

The MAX14661 features a 7-bit slave address, configured by the A0 and A1 inputs. To select the slave address, connect A0 and A1 to GND or V_{CC}, as indicated in Table 3. The IC has four possible addresses, allowing up to four MAX14661 devices to share the same interface bus. The bit following a 7-bit slave address is the R/W bit, which is low for a write command and high for a read command.

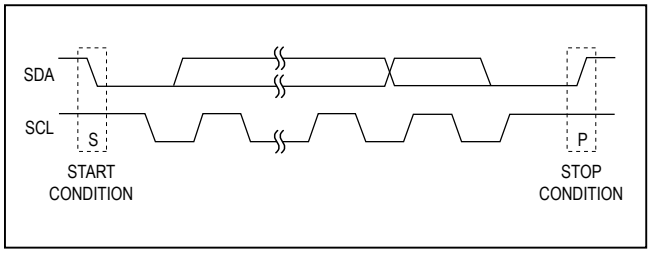


Figure 5. Start and Stop Conditions

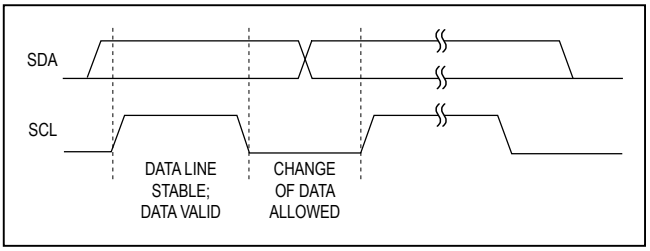


Figure 6. Bit Transfer

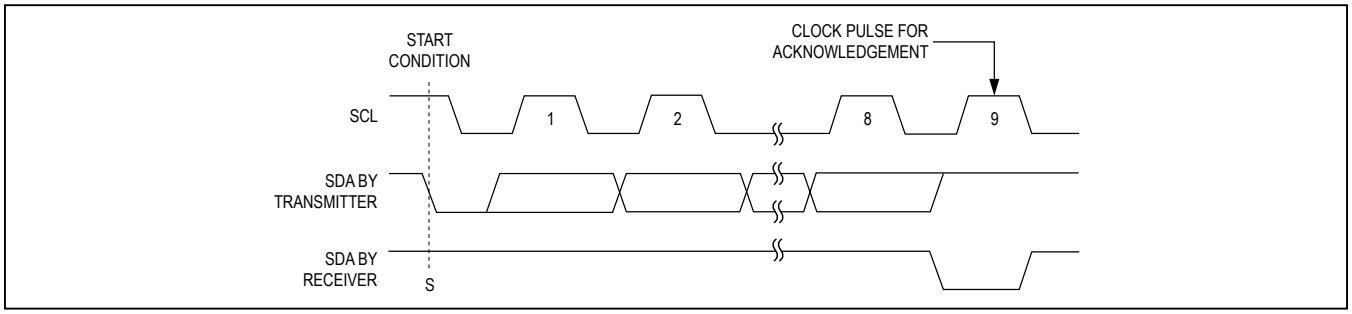


Figure 7. Acknowledge

Table 3. Slave Address Configuration

LOGIC INPUTS		I2C SLAVE ADDRESS									
A1	A0	A6	A5	A4	A3	A2	A1	A0	R/W	READ ADD	WRITE ADD
0	0	1	0	0	1	1	0	0	1/0	0X99	0X98
0	1	1	0	0	1	1	0	1	1/0	0X9B	0X9A
1	0	1	0	0	1	1	1	0	1/0	0X9D	0X9C
1	1	1	0	0	1	1	1	1	1/0	0X9F	0X9E

Bus Reset

The MAX14661 resets the bus with the I²C start condition for reads. When the R/$\overline{W}$ bit is set to 1, the device transmits data to the master, thus the master is reading from the device.

Format for Writing

A write to the MAX14661 comprises the transmission of the slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, then the device takes no further action beyond storing the register address. Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 8). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrement (Figure 9).

Format for Reading

The MAX14661 is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 10). The master can now read consecutive bytes from the device, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 11). Once the master sounds a NACK, the MAX14661 stops sending valid data.

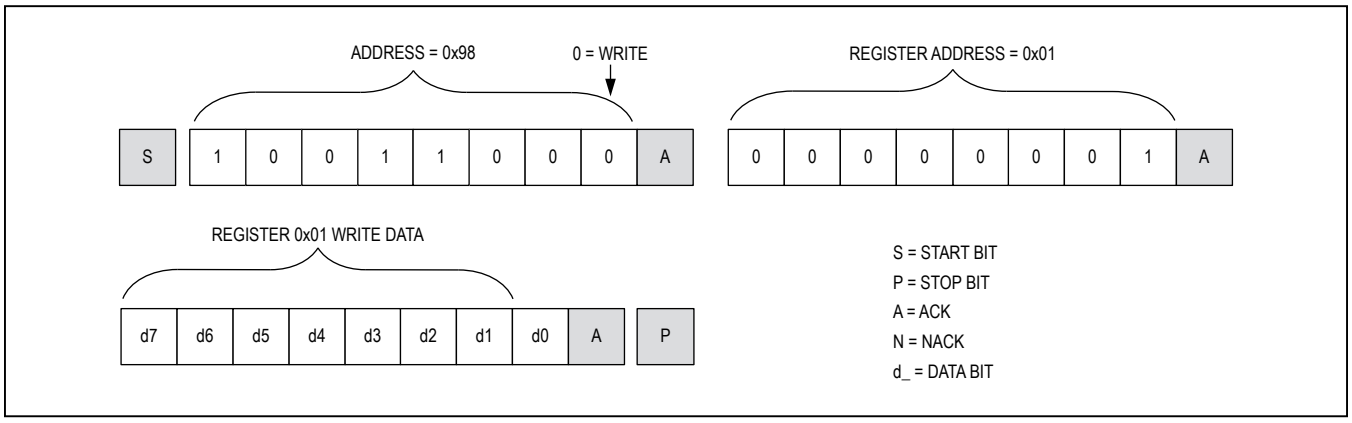


Figure 8. Format for I²C Write

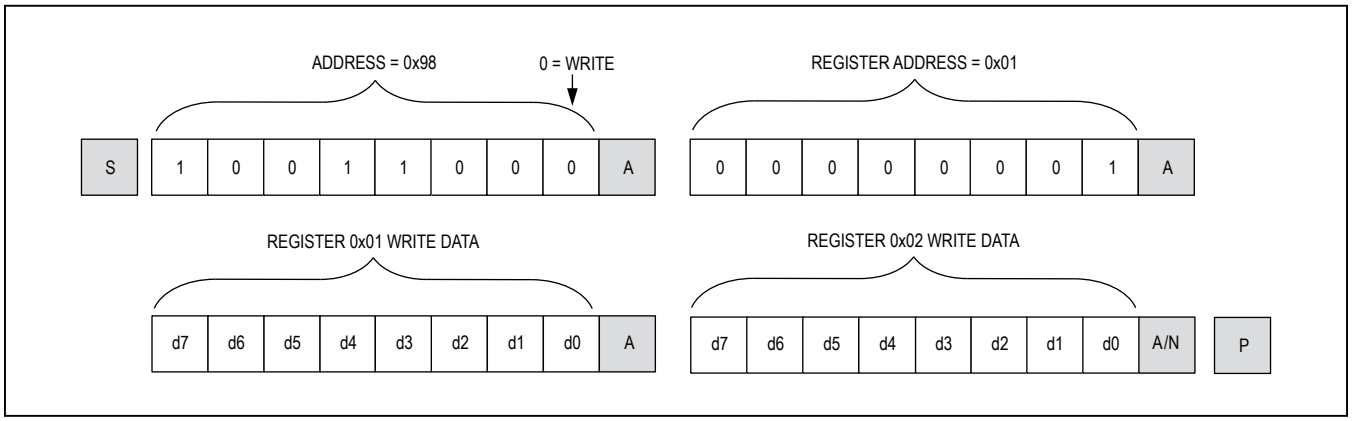


Figure 9. Format for Writing to Multiple Registers

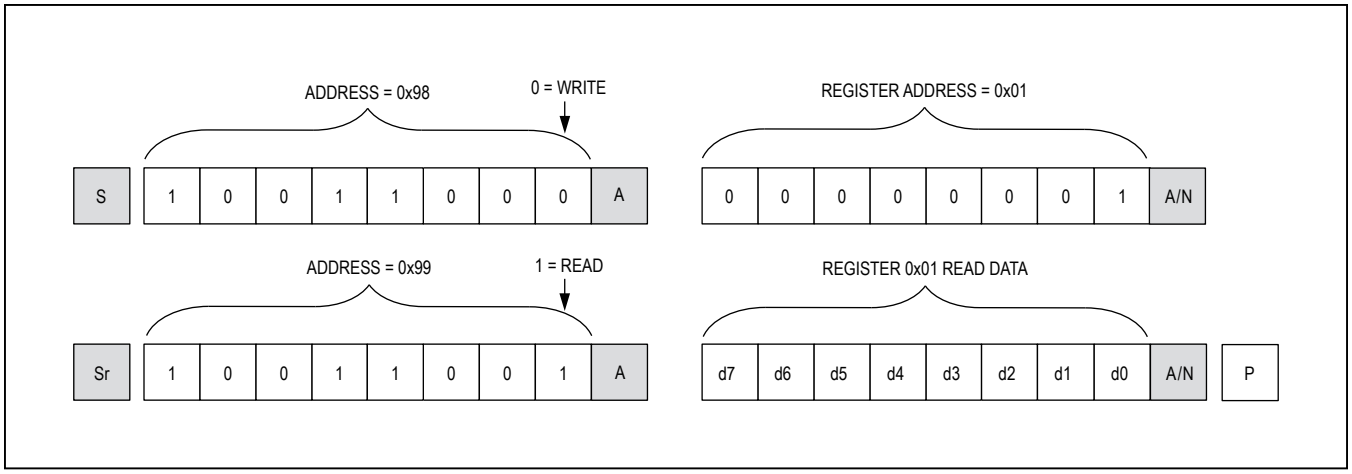


Figure 10. Format for Reads (Repeated Start)

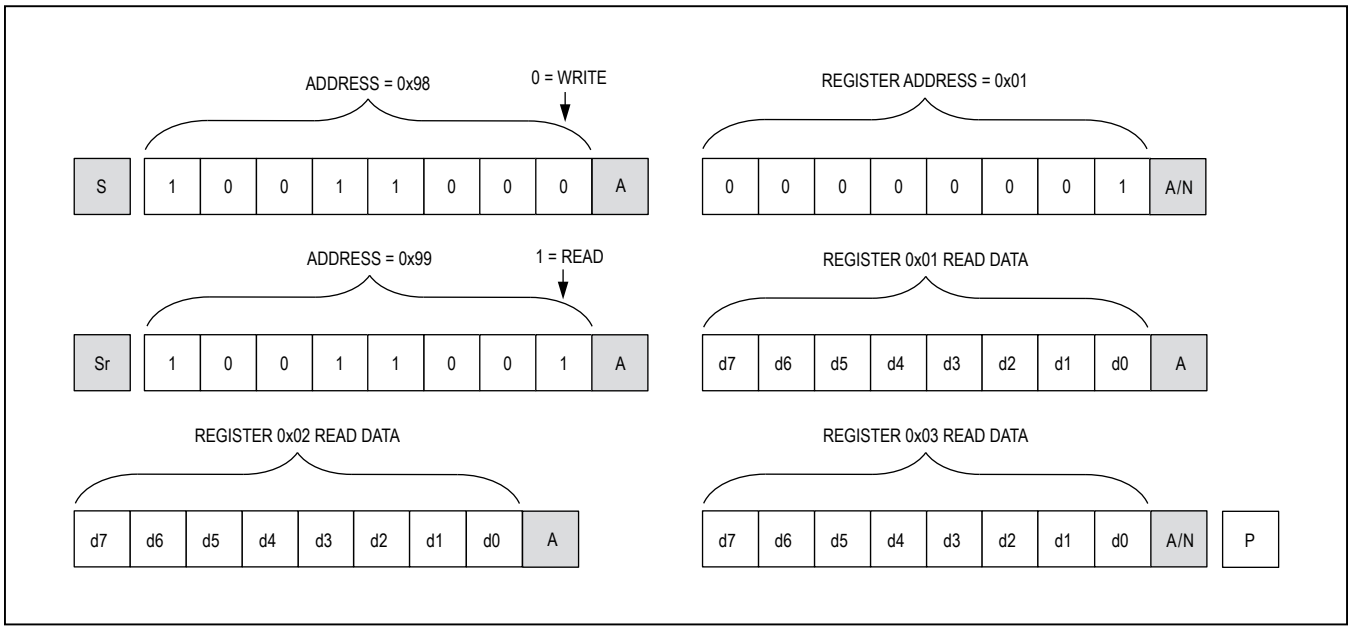


Figure 11. Format for Reading Multiple Registers

SPI Interface

In SPI mode, the device operates a shift register designed to work with common serial interfaces. The bits are shifted through so that a large serial chain can be made to minimize pins needed for a system with multiple devices. (See Figure 12.) This shift register is also designed to be compatible with common microcontroller SPI-type interfaces. The switches in the MAX14661 are all transitioned simultaneously. To update the switches in SPI mode, the user must shift in a bit with the desired state of each switch according to the data format listed in Table 4. The switches are updated at the rising edge of $\overline{CS}$ with the last 32 bits of data shifted in **only if the number of bits clocked in is greater than or equal to the number of switches (32)**. The DOUT pin is the serial output of the shift register. This outputs the data loaded into DIN, delayed by 32 clocks, and is intended for creating a serial daisy chain to minimize the number select lines required by the SPI interface. The first 32 bits out of DOUT after the falling edge of $\overline{CS}$ are the contents of the shift register prior to $\overline{CS}$ falling, followed by the data being clocked into DIN. The bits in the shift register are all zero when power is applied or after shutdown is released.

Note that the data in the shift register may not be the same as the state of the switches. The DOUT pin is intended for daisy chain applications and not for switch readback. Note for V_{CC} less than 2.7V, the DOUT propagation delay can limit the maximum SPI operating frequency. See Figures 12 and 13 for the SPI timing diagrams. The voltage level driven out by the DOUT buffer is set by the voltage applied to SPI/$\overline{I^2C}$. This allows the voltage to be independent from the supply voltage. While we expect the voltage at SPI/$\overline{I^2C}$ to be less than or equal to V_{CC} in most applications, it can be higher than V_{CC} as long as it does not exceed V_{CC} before V_{CC} has reached at least 1.8V.

Table 4. SPI Data Format

BYTE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
First	SW16B	SW15B	SW14B	SW13B	SW12B	SW11B	SW10B	SW09B
Second	SW08B	SW07B	SW06B	SW05B	SW04B	SW03B	SW02B	SW01B
Third	SW16A	SW15A	SW14A	SW13A	SW12A	SW11A	SW10A	SW09A
Fourth	SW08A	SW07A	SW06A	SW05A	SW04A	SW03A	SW02A	SW01A

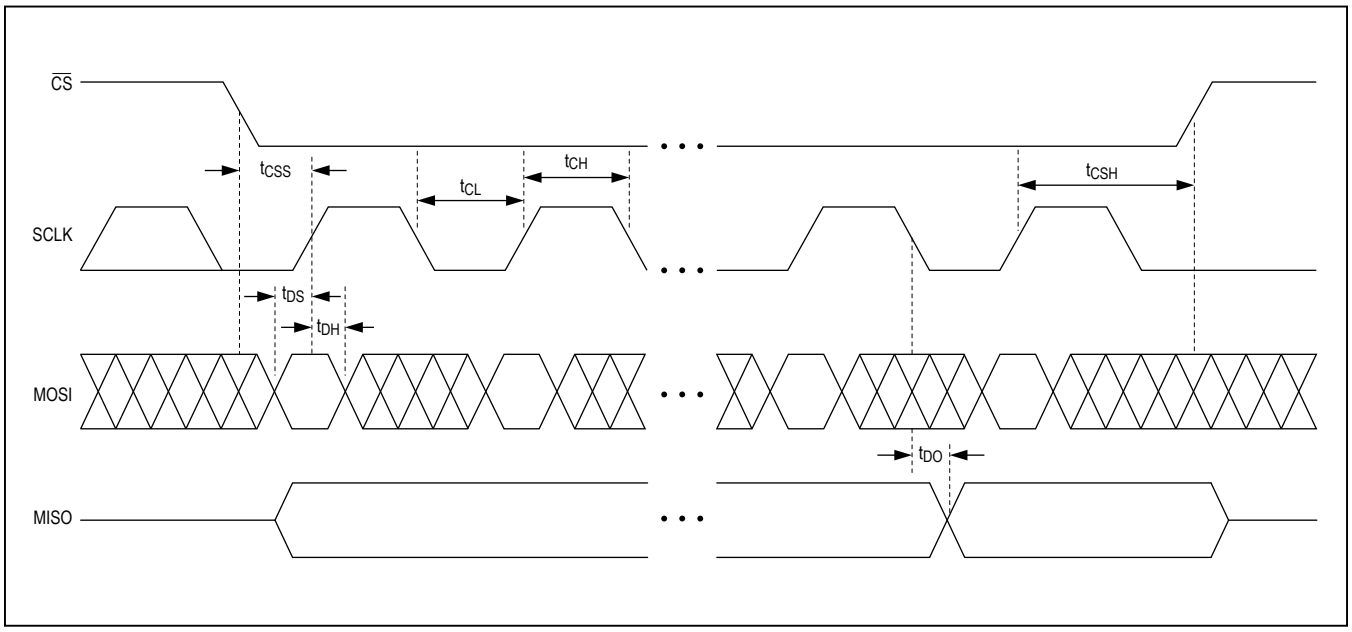


Figure 12. SPI Timing Details

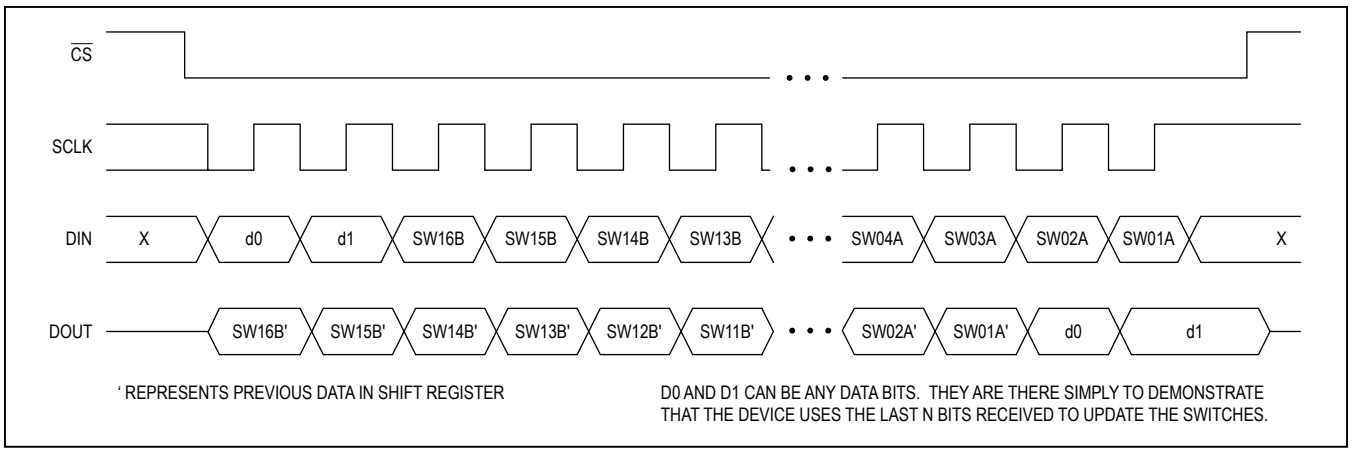


Figure 13. SPI Timing Diagram

Applications Information

Serial Bus Configurations

The MAX14661 was designed to support a wide variety of multiplexing applications. Multiple devices can be used in a system to expand the number of ports being multiplexed. With the two address-select pins provided in I²C mode, four devices can be attached to the same I²C bus simultaneously using only two pins. There are also several options for addressing multiple devices when using the SPI interface. Using only three pins on the microcontroller, as many devices as desired can be loaded by connecting all the CS and SCK pins in parallel and chaining the DOUT pin from one device to the DIN pin on the next. It is also acceptable to provide a separate $\overline{CS}$ pin for each device so that they can be individually addressed and loaded. Alternatively a separate data line can be used for each device to reduce the time required to load all the devices. Some of the options and tradeoffs are listed in Table 5, as well as example application diagrams in the *Typical Application Circuit*.

Table 5. Benefits and Limitations of Different Serial-Bus Configurations

SERIAL BUS	PINS	BENEFITS	LIMITATIONS
I²C (Figure 16)	2	Fewest Pins	Maximum four devices per bus, slow protocol, no simultaneous updates across all devices
SPI Daisy Chain (Figure 19)	3	Faster than I²C with only one additional pin, simultaneous updates across all devices in chain	n x 32 clocks required to load all devices
SPI Separate CS (Figure 17)	n+2	Common SPI implementation, quick for single device updates	n x 32 clocks required to load all devices, requires an additional pin per device, no simultaneous updates across all devices
SPI Separate Data (Figure 18)	n+2	Fastest loading for multiple devices, simultaneous updates across all devices	Requires an additional pin per device, may not be supported by SPI controller

Extended ESD

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (HBM) encountered during handling and assembly. AB_ and COM_ are further protected against ESD up to ±10kV (HBM) without damage. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14661 continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 14 shows the Human Body Model. Figure 15 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

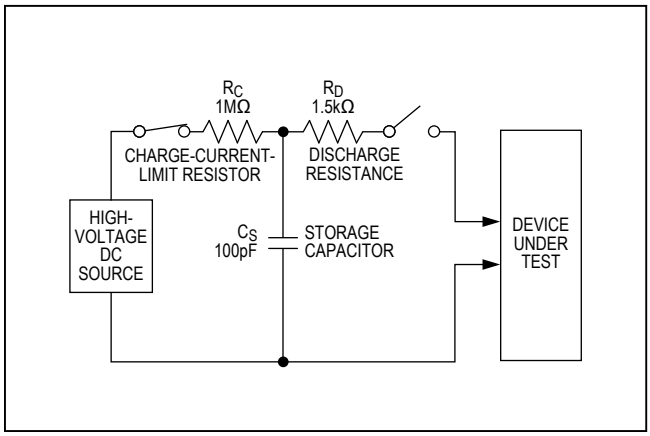


Figure 14. Human Body ESD Test Model

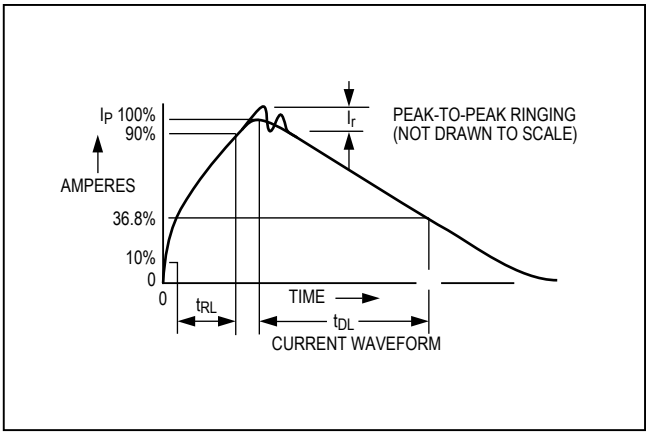


Figure 15. Human Body Current Waveform

Typical Application Circuit

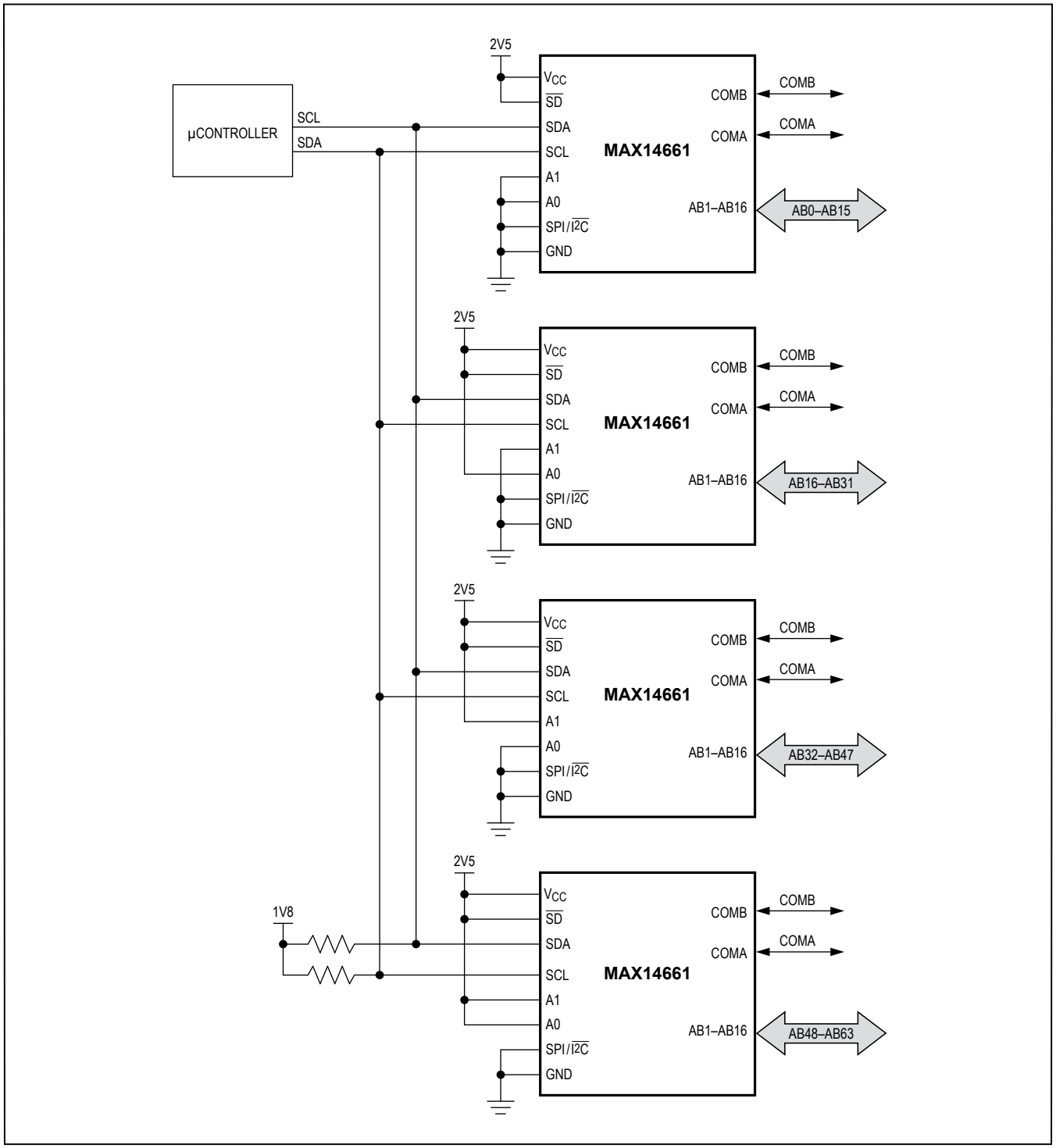


Figure 16. I²C Controlled 64:2 MUX

Typical Application Circuit (continued)

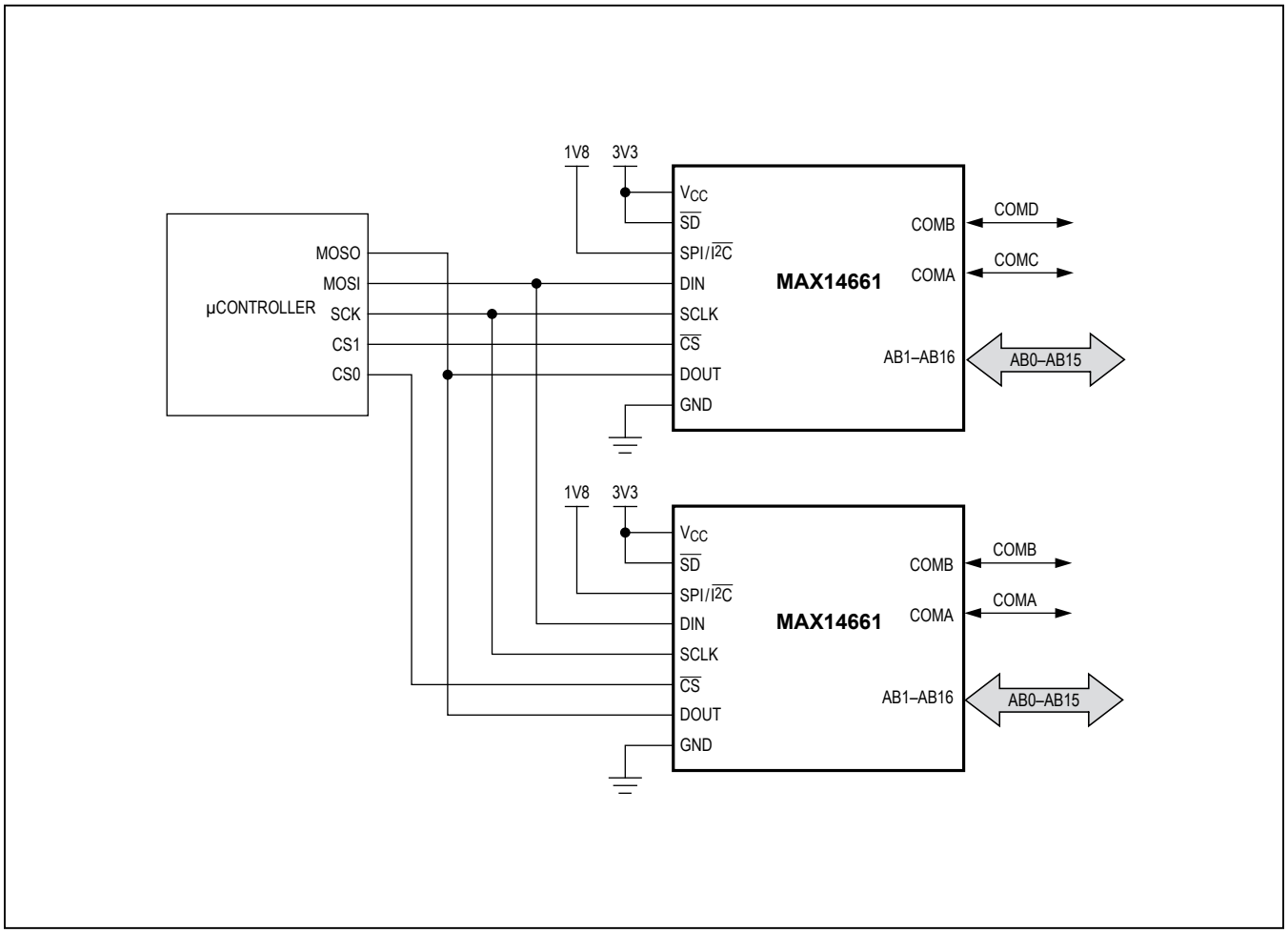


Figure 17. SPI Separate $\overline{CS}$ 16:4

Typical Application Circuit (continued)

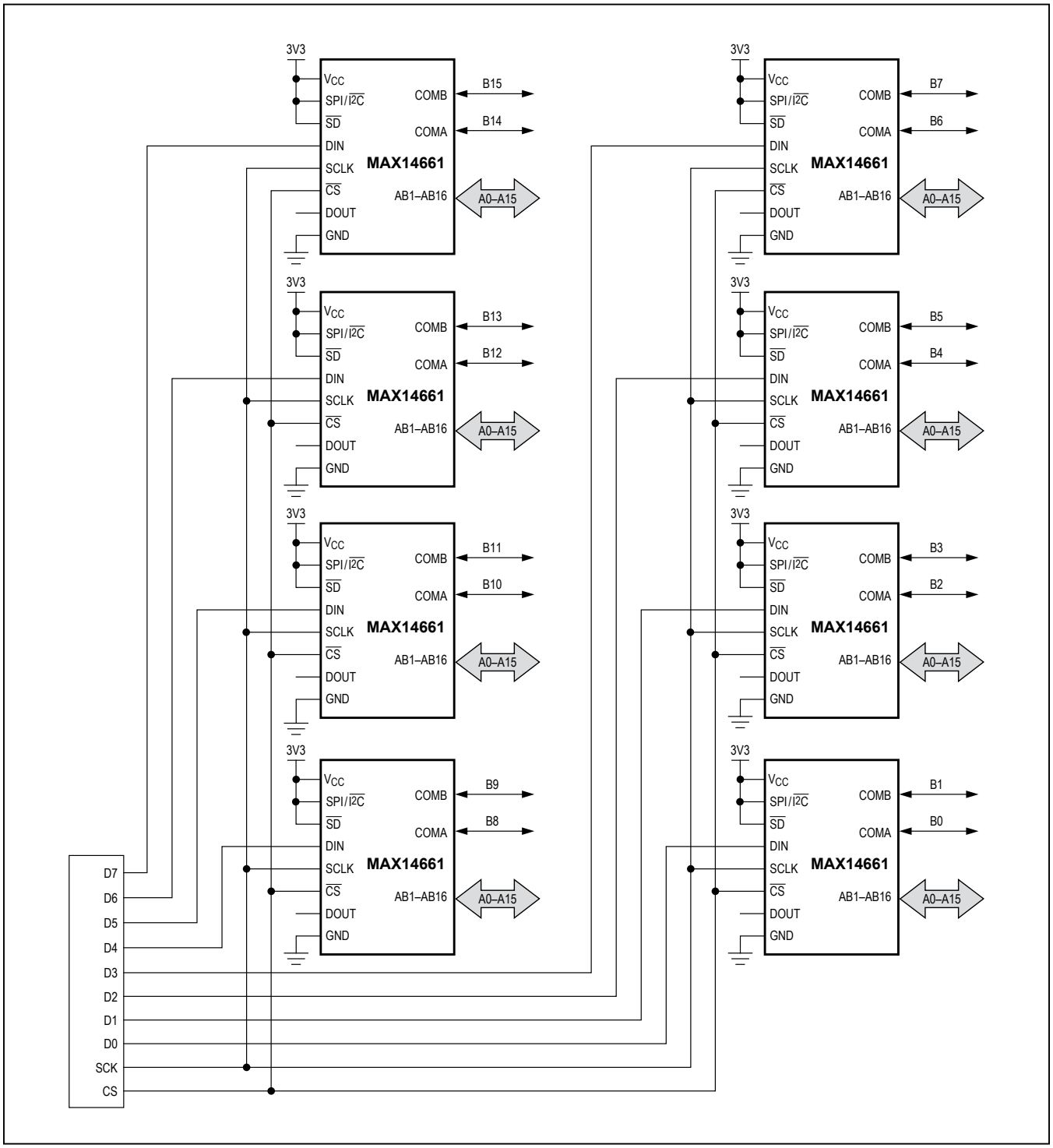


Figure 18. SPI Separate Data 16:16 MUX

Typical Application Circuit (continued)

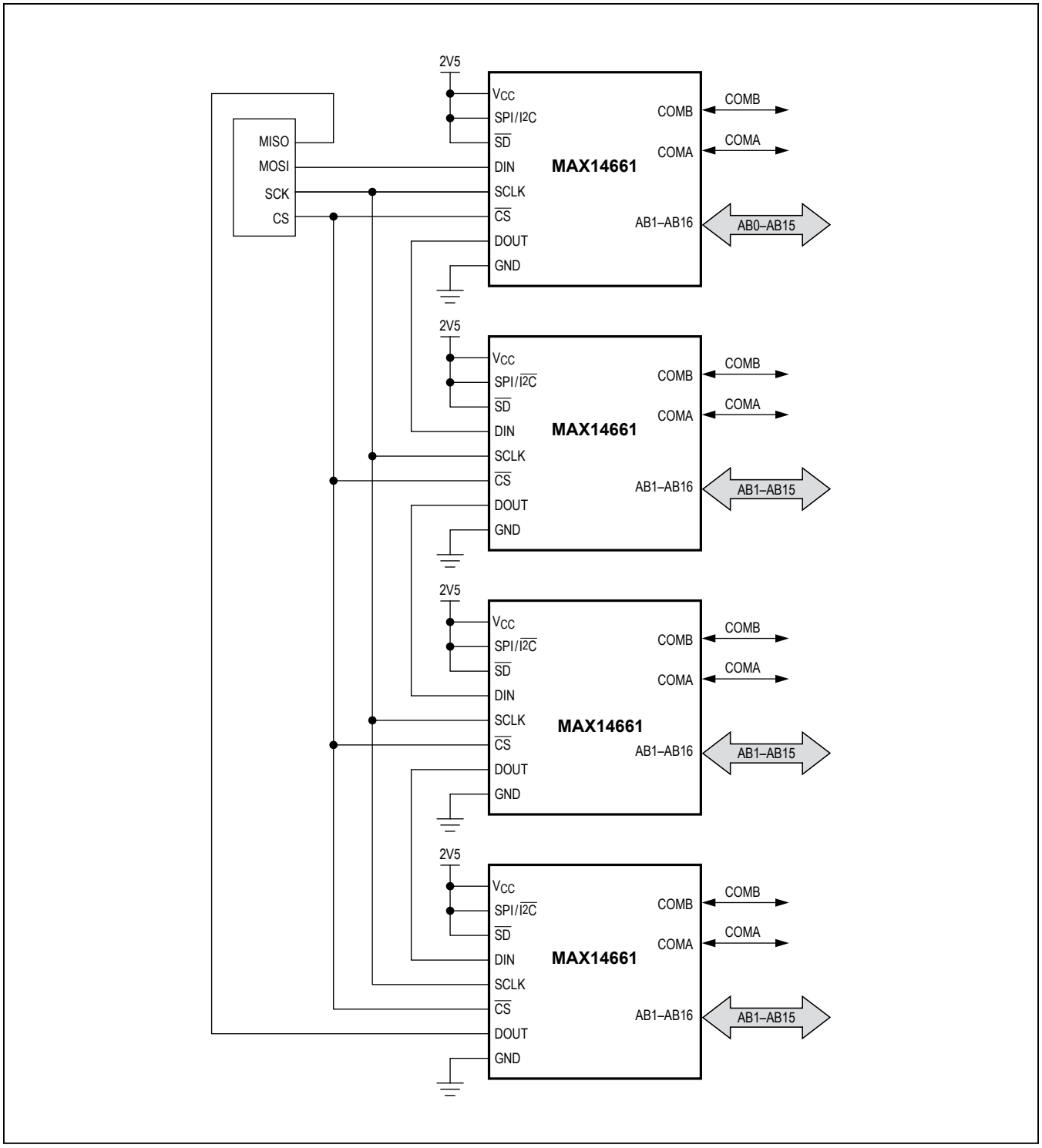


Figure 19. SPI Daisy Chain 256:2 MUX

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14661ETI+	-40°C to +85°C	28 TQFN 4mm x 4mm
MAX14661ETI+T	-40°C to +85°C	28 TQFN 4mm x 4mm

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and reel
**EP = Exposed Pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2844+1	21-0139	90-0035

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	—
1	1/14	Added MAX14661ETI+	26
2	1/15	Updated page 1 content	1

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