S-89130/89140 Series

MINI ANALOG SERIES
CMOS OPERATIONAL AMPLIFIER

The mini-analog series is a group of ICs that incorporate a general purpose analog circuit in a small package.
S-89130/89140 Series is a CMOS type operational amplifier that has a phase compensation circuit, and operates at a low voltage with low current consumption. S-89130/89140 Series can operate within a wide temperature range of −40°C to +125°C.
This product is a dual operational amplifier (two circuits).

■ Features

- Lower operating voltage : V_{DD} = 2.7 V to 5.5 V
- Low current consumption (per circuit) : I_{DD} = 1.00 mA typ. (S-89130 Series, V_{DD} = 5.0 V)
  I_{DD} = 0.27 mA typ. (S-89140 Series, V_{DD} = 5.0 V)
- Low input offset voltage : V_{IO} = 6.0 mV max. (S-89130 Series)
  V_{IO} = 7.0 mV max. (S-89140 Series)
- Operational temperature range : −40°C to +125°C
- No external capacitors required for internal phase compensation
- Lead-free (Sn 100%), halogen-free *1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

- Current sensing
- Signal amplification
- Buffer
- Active filter
- Electronics devices

■ Packages

- SNT-8A
- TMSOP-8

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

■ Block Diagram

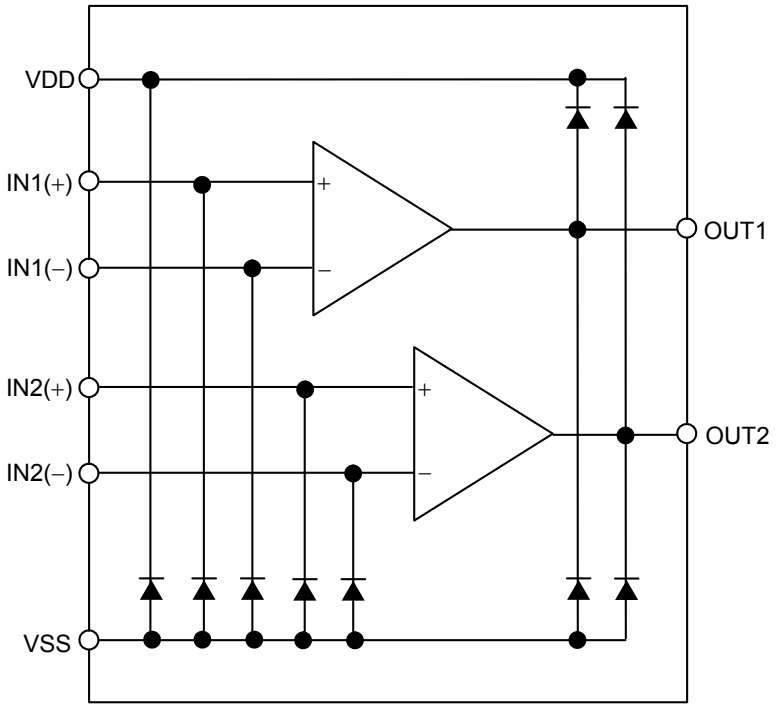
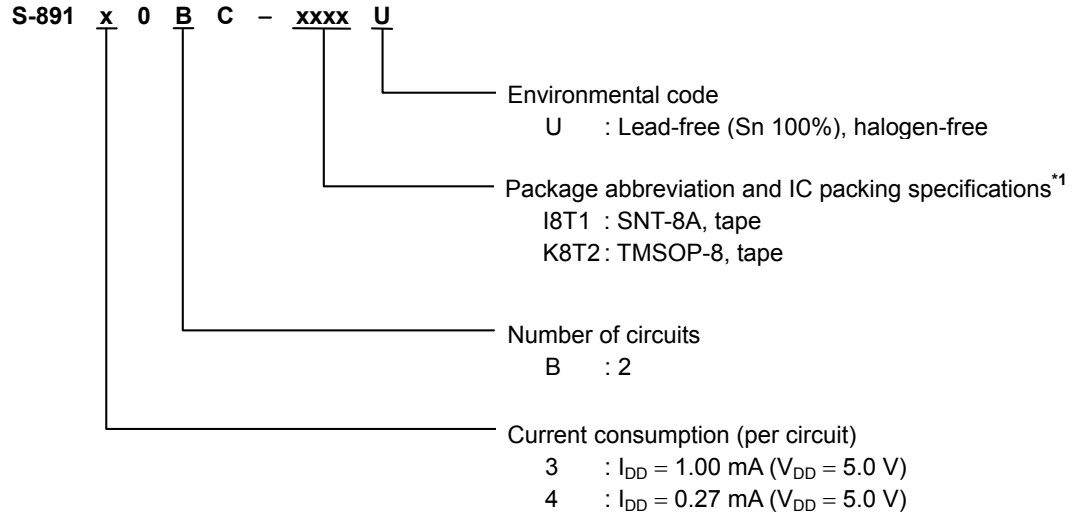


Figure 1

■ Product Name Structure

Users can select the product type for the S-89130/89140 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Packages**" regarding the package drawings and "**3. Product name list**" regarding the product type.

1. Product name



***1.** Refer to the tape specifications

2. Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–

3. Product name list

Table 1

Product name	Current consumption (per circuit)*1	Gain-bandwidth*1	Package
S-89130BC-I8T1U	1.00 mA	3.0 MHz	SNT-8A
S-89130BC-K8T2U	1.00 mA	3.0 MHz	TMSOP-8
S-89140BC-I8T1U	0.27 mA	1.0 MHz	SNT-8A
S-89140BC-K8T2U	0.27 mA	1.0 MHz	TMSOP-8

***1.** The value when V_{DD} = 5.0 V

■ Pin Configurations

1. SNT-8A

SNT-8A
Top view

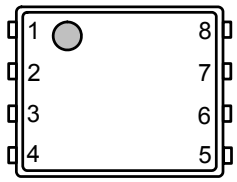


Figure 2

Table 2

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

2. TMSOP-8

TMSOP-8
Top view

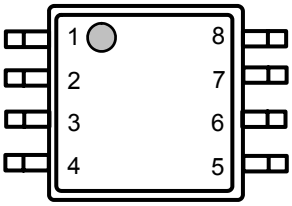


Figure 3

Table 3

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

■ Absolute Maximum Ratings

Table 4

(Ta = +25°C unless otherwise specified)

Parameter		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS} − 0.3 to V_{SS} + 7.0	V
Input voltage		$V_{IN(+)}$, $V_{IN(-)}$	V_{SS} − 0.3 to V_{SS} + 7.0	V
Output voltage		V_{OUT}	V_{SS} − 0.3 to V_{DD} + 0.3	V
Differential input voltage		V_{IND}	±7.0	V
Output pin current		I_{SOURCE}	20.0	mA
		I_{SINK}	20.0	mA
Power dissipation	SNT-8A	P_D	550[*1]	mW
	TMSOP-8		800[*1]	mW
Operating ambient temperature		T_{opr}	−40 to +125	°C
Junction temperature		T_j	−55 to +150	°C
Storage temperature		T_{stg}	−55 to +150	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

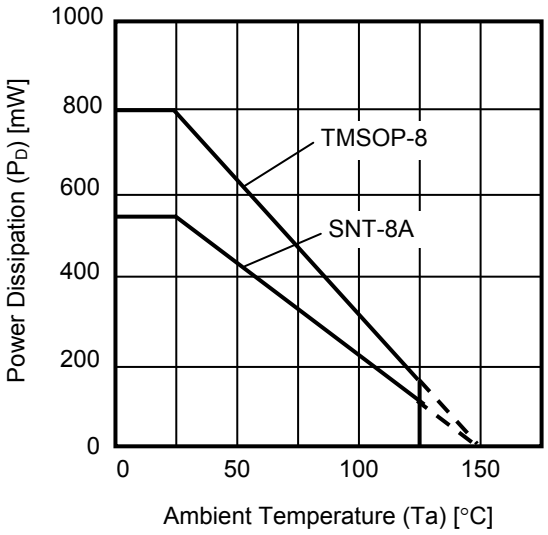


Figure 4 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. S-89130 Series

Table 5

(Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Range of operating power supply voltage	V_{DD}	–	2.7	–	5.5	V	–

1. 1 V_{DD} = 5.0 V

Table 6

DC Electrical Characteristics (V_{DD} = 5.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)	I_{DD}	$V_{CMR} = V_{OUT} = V_{DD} / 2$	–	1.00	1.25	mA	5
Input offset voltage	V_{IO}	$V_{CMR} = V_{DD} / 2$	−6.0	±3.0	+6.0	mV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = V_{DD} / 2$	–	±3	–	μV/°C	1
Input offset current	I_{IO}	–	–	1	–	pA	–
Input bias current	I_{BIAS}	–	–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–	−0.1	–	3.8	V	2
Voltage gain (open loop)	A_{VOL}	$V_{OUT} = V_{SS} + 0.5$ V to $V_{DD} - 0.5$ V $V_{CMR} = V_{DD} / 2$, R_L = 1.0 MΩ	88	110	–	dB	8
Maximum output swing voltage	V_{OH}	R_L = 1.0 MΩ	4.9	–	–	V	3
	V_{OL}	R_L = 1.0 MΩ	–	–	0.1	V	4
Common-mode input signal rejection ratio	CMRR	$V_{CMR} = V_{SS} - 0.1$ V to $V_{DD} - 1.2$ V	70	85	–	dB	2
Power supply voltage rejection ratio	PSRR	V_{DD} = 2.7 V to 5.5 V	70	90	–	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD} - 0.12$ V	5.0	–	–	mA	6
Sink current	I_{SINK}	V_{OUT} = 0.12 V	5.0	–	–	mA	7

Table 7

AC Electrical Characteristics (V_{DD} = 5.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 13)**	–	2.0	–	V/μs
Gain-bandwidth product	GBP	C_L = 0 pF	–	3.0	–	MHz

1. 2 V_{DD} = 2.7 V

Table 8

DC Electrical Characteristics (V_{DD} = 2.7 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)	I_{DD}	$V_{CMR} = V_{OUT} = V_{DD} / 2$	–	0.90	1.20	mA	5
Input offset voltage	V_{IO}	$V_{CMR} = V_{DD} / 2$	−6.0	±3.0	+6.0	mV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = V_{DD} / 2$	–	±3	–	μV/°C	1
Input offset current	I_{IO}	–	–	1	–	pA	–
Input bias current	I_{BIAS}	–	–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–	−0.1	–	1.5	V	2
Voltage gain (open loop)	A_{VOL}	$V_{OUT} = V_{SS}$ + 0.5 V to V_{DD} − 0.5 V $V_{CMR} = V_{DD} / 2$, R_L = 1.0 MΩ	80	110	–	dB	8
Maximum output swing voltage	V_{OH}	R_L = 1.0 MΩ	2.6	–	–	V	3
	V_{OL}	R_L = 1.0 MΩ	–	–	0.1	V	4
Common-mode input signal rejection ratio	CMRR	$V_{CMR} = V_{SS}$ − 0.1 V to V_{DD} − 1.2 V	65	85	–	dB	2
Power supply voltage rejection ratio	PSRR	V_{DD} = 2.7 V to 5.5 V	70	90	–	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD}$ − 0.12 V	5.0	–	–	mA	6
Sink current	I_{SINK}	V_{OUT} = 0.12 V	5.0	–	–	mA	7

Table 9

AC Electrical Characteristics (V_{DD} = 2.7 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 13)**	–	2.0	–	V/μs
Gain-bandwidth product	GBP	C_L = 0 pF	–	3.0	–	MHz

2. S-89140 Series

Table 10

(Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Range of operating power supply voltage	V_{DD}	–	2.7	–	5.5	V	–

2. 1 V_{DD} = 5.0 V

Table 11

DC Electrical Characteristics (V_{DD} = 5.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)	I_{DD}	$V_{CMR} = V_{OUT} = V_{DD} / 2$	–	0.27	0.35	mA	5
Input offset voltage	V_{IO}	$V_{CMR} = V_{DD} / 2$	−7.0	±3.0	+7.0	mV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = V_{DD} / 2$	–	±3	–	μV/°C	1
Input offset current	I_{IO}	–	–	1	–	pA	–
Input bias current	I_{BIAS}	–	–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–	−0.1	–	3.8	V	2
Voltage gain (open loop)	A_{VOL}	$V_{OUT} = V_{SS}$ + 0.5 V to V_{DD} − 0.5 V $V_{CMR} = V_{DD} / 2$, R_L = 1.0 MΩ	88	110	–	dB	8
Maximum output swing voltage	V_{OH}	R_L = 1.0 MΩ	4.9	–	–	V	3
	V_{OL}	R_L = 1.0 MΩ	–	–	0.1	V	4
Common-mode input signal rejection ratio	CMRR	$V_{CMR} = V_{SS}$ − 0.1 V to V_{DD} − 1.2 V	70	85	–	dB	2
Power supply voltage rejection ratio	PSRR	V_{DD} = 2.7 V to 5.5 V	70	90	–	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD}$ − 0.12 V	5.0	–	–	mA	6
Sink current	I_{SINK}	V_{OUT} = 0.12 V	5.0	–	–	mA	7

Table 12

AC Electrical Characteristics (V_{DD} = 5.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 13)**	–	0.5	–	V/μs
Gain-bandwidth product	GBP	C_L = 0 pF	–	1.0	–	MHz

2. 2 V_{DD} = 2.7 V

Table 13

DC Electrical Characteristics (V_{DD} = 2.7 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)	I_{DD}	$V_{CMR} = V_{OUT} = V_{DD} / 2$	–	0.25	0.33	mA	5
Input offset voltage	V_{IO}	$V_{CMR} = V_{DD} / 2$	−7.0	±3.0	+7.0	mV	1
Input offset voltage drift	$\frac{\Delta V_{IO}}{\Delta Ta}$	$V_{CMR} = V_{DD} / 2$	–	±3	–	μV/°C	1
Input offset current	I_{IO}	–	–	1	–	pA	–
Input bias current	I_{BIAS}	–	–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–	−0.1	–	1.5	V	2
Voltage gain (open loop)	A_{VOL}	$V_{OUT} = V_{SS}$ + 0.5 V to V_{DD} − 0.5 V $V_{CMR} = V_{DD} / 2$, R_L = 1.0 MΩ	80	110	–	dB	8
Maximum output swing voltage	V_{OH}	R_L = 1.0 MΩ	2.6	–	–	V	3
	V_{OL}	R_L = 1.0 MΩ	–	–	0.1	V	4
Common-mode input signal rejection ratio	CMRR	$V_{CMR} = V_{SS}$ − 0.1 V to V_{DD} − 1.2 V	65	85	–	dB	2
Power supply voltage rejection ratio	PSRR	V_{DD} = 2.7 V to 5.5 V	70	90	–	dB	1
Source current	I_{SOURCE}	$V_{OUT} = V_{DD}$ − 0.12 V	5.0	–	–	mA	6
Sink current	I_{SINK}	V_{OUT} = 0.12 V	5.0	–	–	mA	7

Table 14

AC Electrical Characteristics (V_{DD} = 2.7 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 13)**	–	0.5	–	V/μs
Gain-bandwidth product	GBP	C_L = 0 pF	–	1.0	–	MHz

■ Test Circuit (Per Circuit)

1. Power supply voltage rejection ratio, input offset voltage

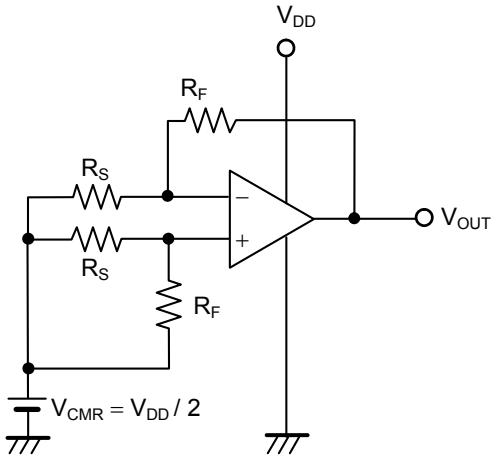


Figure 5

- **Power supply voltage rejection ratio (PSRR)**

  The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with V_{OUT} measured at each V_{DD}.

  Test conditions:
  V_{DD} = 2.7 V: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$,
  V_{DD} = 5.5 V: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$PSRR = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{\left(V_{OUT1} - \frac{V_{DD1}}{2}\right) - \left(V_{OUT2} - \frac{V_{DD2}}{2}\right)} \right| \times \frac{R_F + R_S}{R_S} \right)$$

- **Input offset voltage (V_{IO})**

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_F + R_S}$$

2. Common-mode input signal rejection ratio, common-mode input voltage range

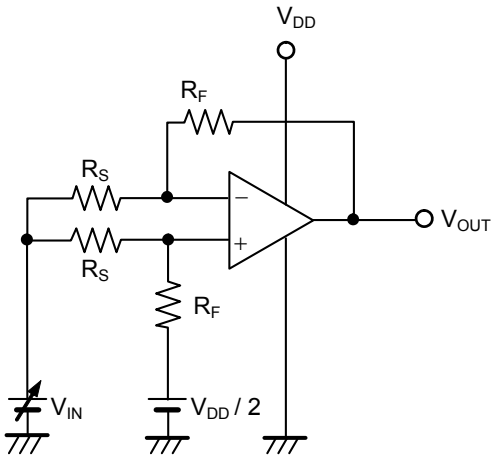


Figure 6

- **Common-mode input signal rejection ratio (CMRR)**

  The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with V_{OUT} measured at each V_{IN}.

  Test conditions:
  $V_{IN} = V_{CMR\ Max.}$: $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$,
  $V_{IN} = V_{CMR\ Min.}$: $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

$$CMRR = 20 \log \left(\left| \frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

- **Common-mode input voltage range (V_{CMR})**

  The common mode input voltage range (V_{CMR}) is the range of V_{IN} in which the common mode input signal rejection ratio (CMRR) is satisfied when V_{IN} is varied.

3. Maximum output swing voltage (V_{OH})

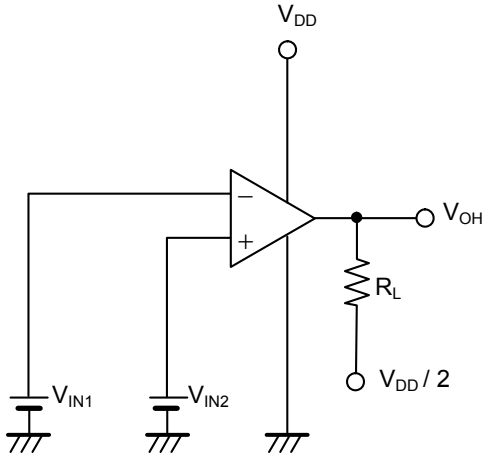


Figure 7

- **Maximum output swing voltage (V_{OH})**

Test conditions

$V_{IN1} = \frac{V_{DD}}{2} - 0.1$ V

$V_{IN2} = \frac{V_{DD}}{2} + 0.1$ V

$R_L = 1$ MΩ

4. Maximum output swing voltage (V_{OL})

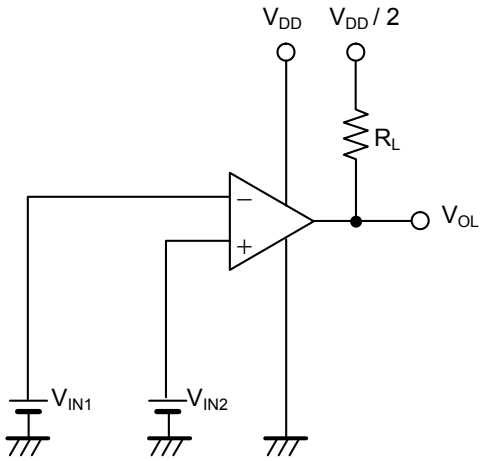


Figure 8

- **Maximum output swing voltage (V_{OL})**

Test conditions:

$V_{IN1} = \frac{V_{DD}}{2} + 0.1$ V

$V_{IN2} = \frac{V_{DD}}{2} - 0.1$ V

$R_L = 1$ MΩ

5. Current consumption

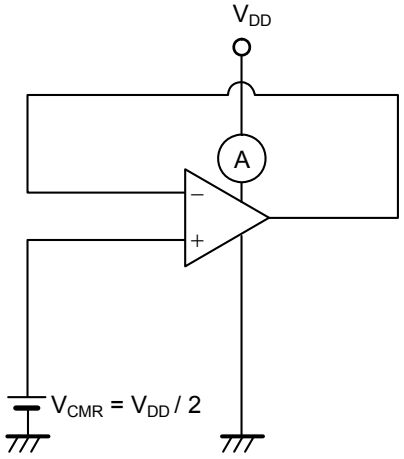


Figure 9

- **Current consumption (I_{DD})**

6. Source current

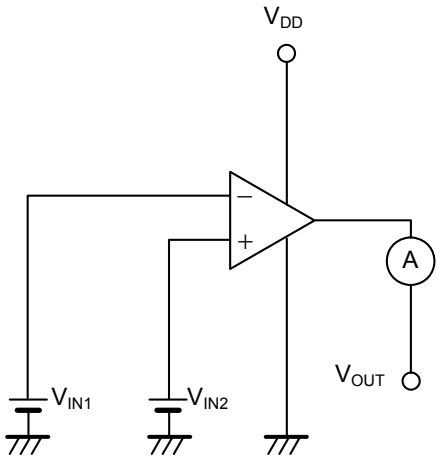


Figure 10

- **Source current (I_{SOURCE})**

  Test conditions:
  $V_{OUT} = V_{DD} - 0.12$ V
  $V_{IN1} = \frac{V_{DD}}{2} - 0.1$ V
  $V_{IN2} = \frac{V_{DD}}{2} + 0.1$ V

7. Sink current

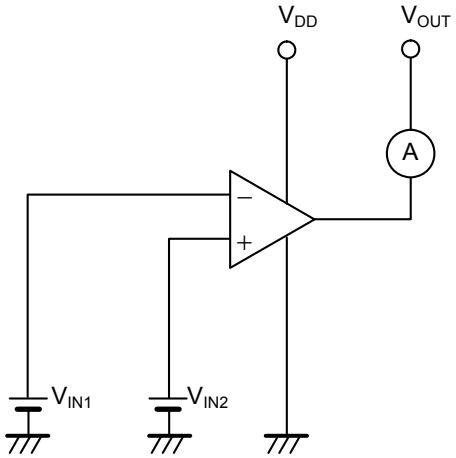


Figure 11

- **Sink current (I_{SINK})**

  Test conditions:
  $V_{OUT} = V_{SS} + 0.12$ V
  $V_{IN1} = \frac{V_{DD}}{2} + 0.1$ V
  $V_{IN2} = \frac{V_{DD}}{2} - 0.1$ V

8. Voltage gain (open loop)

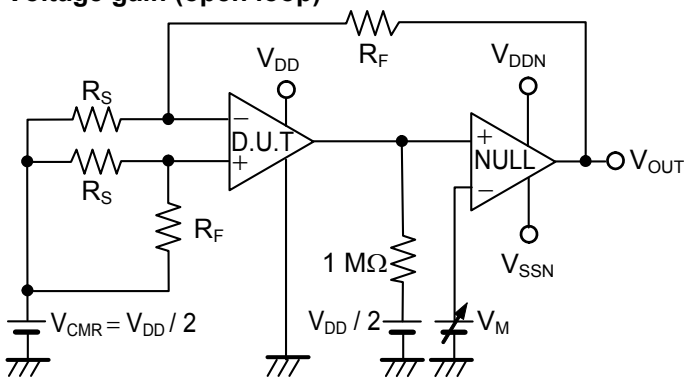


Figure 12

- **Voltage-gain (open loop) (A_{VOL})**

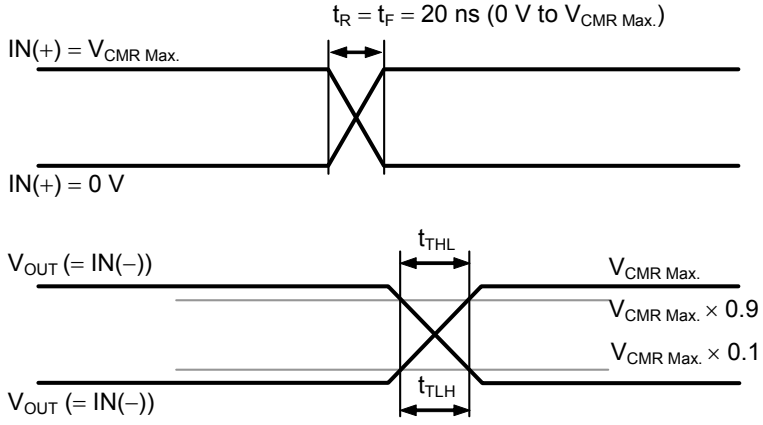
The voltage gain (A_{VOL}) can be calculated by the following expression, with measured V_{OUT} at each V_M.

Test conditions:
$V_M = V_{DD} - 0.5$ V: $V_M = V_{M1}$, $V_{OUT} = V_{OUT1}$,
$V_M = 0.5$ V: $V_M = V_{M2}$, $V_{OUT} = V_{OUT2}$

$$A_{VOL} = 20 \log \left(\left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

9. Slew rate (SR)

Measured by the voltage follower circuit.



$$SR = \frac{V_{CMR\ Max.} \times 0.8}{t_{TLH}}$$

$$SR = \frac{V_{CMR\ Max.} \times 0.8}{t_{THL}}$$

Figure 13

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.
- Use this IC with the output current 20 mA or less.
- This IC operates stably even directly connecting a load capacitance 100 pF or less to the output pin, as seen in **Figure 14**. When using a load capacitance 100 pF or larger, set a resistor 47 Ω or more, as seen in **Figure 15**. In case of connecting a filter for noise prevention, and using a load capacitance 100 pF or more, also set a resistor 47 Ω or more as seen in **Figure 16**.

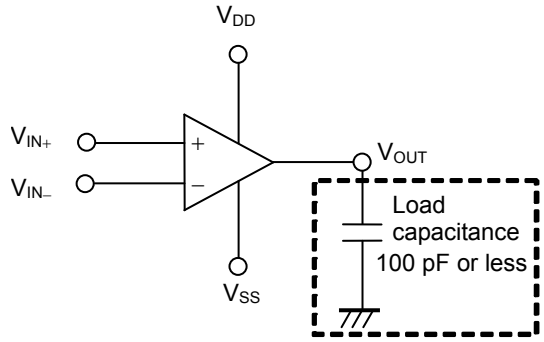


Figure 14

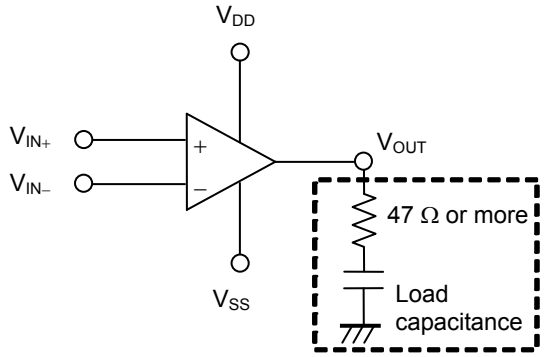


Figure 15

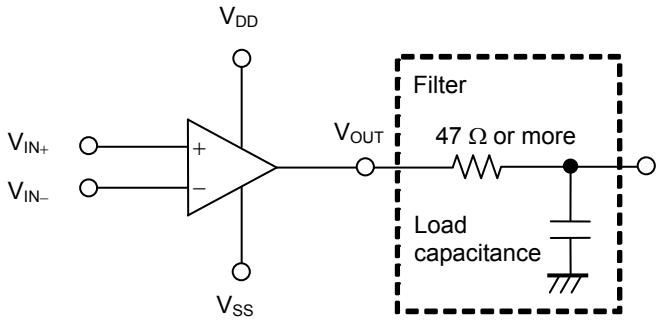


Figure 16

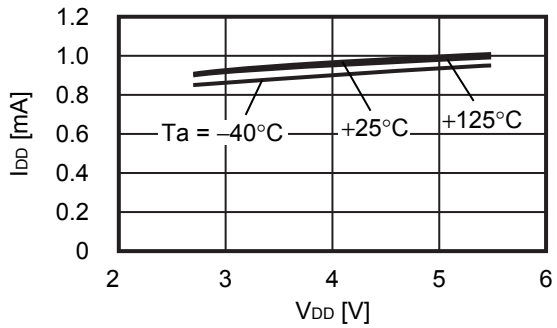
Caution **The above connection diagram and constant will not guarantee successful operation. Perform through evaluation using the actual application to set the constant.**

■ Characteristics (Typical Data)

1. Current consumption (per circuit) vs. Power supply voltage

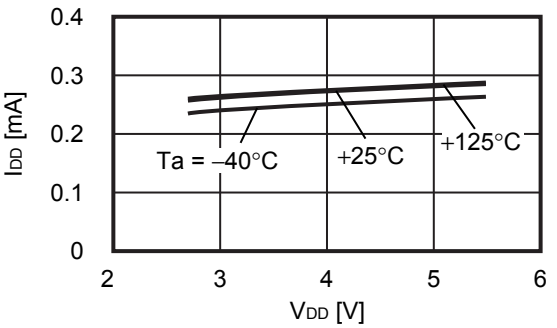
1. 1 S-89130 Series

I_{DD}–V_{DD}, V_{SS} = 0 V, V_{CMR} = V_{OUT} = V_{DD} / 2



1. 2 S-89140 Series

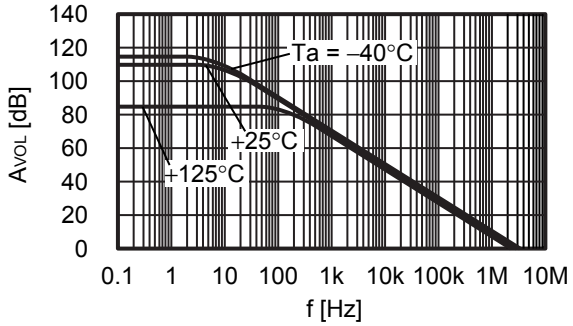
I_{DD}–V_{DD}, V_{SS} = 0 V, V_{CMR} = V_{OUT} = V_{DD} / 2



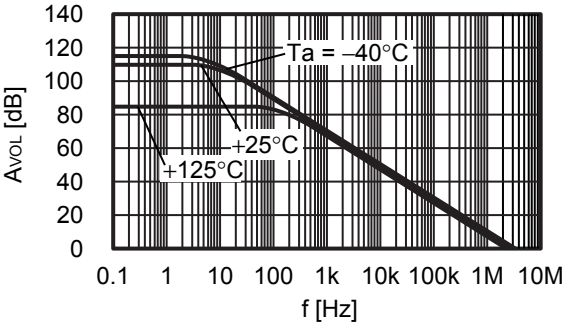
2. Voltage gain vs. Frequency

2. 1 S-89130 Series

A_{VOL}–f, V_{DD} = 2.7 V, V_{SS} = 0 V

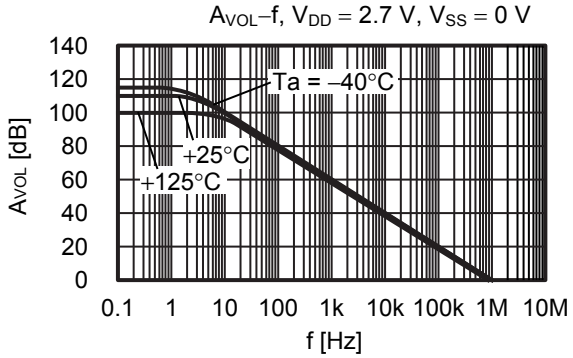


A_{VOL}–f, V_{DD} = 5.0 V, V_{SS} = 0 V

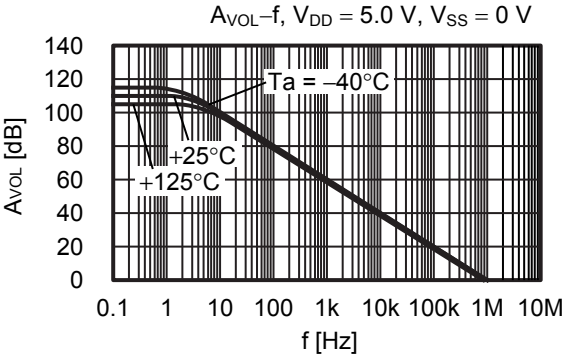


2. 2 S-89140 Series

A_{VOL}–f, V_{DD} = 2.7 V, V_{SS} = 0 V



A_{VOL}–f, V_{DD} = 5.0 V, V_{SS} = 0 V

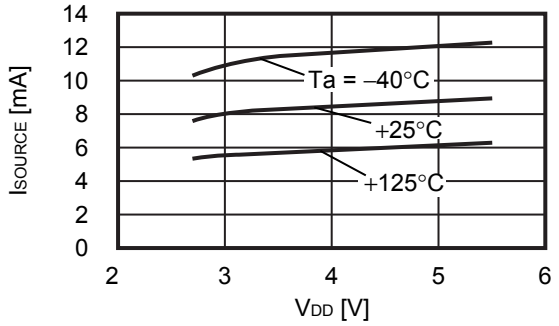


3. Output current

3. 1 I_{SOURCE} vs. Power supply voltage

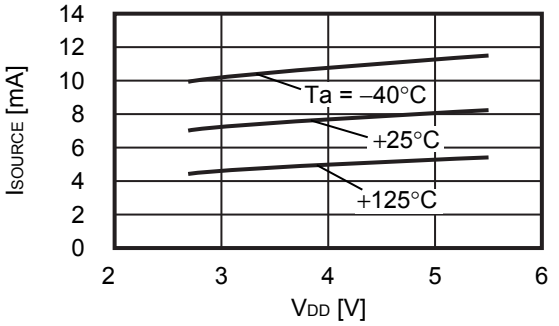
3. 1. 1 S-89130 Series

I_{SOURCE}–V_{DD}, V_{OUT} = V_{DD} – 0.12 V, V_{SS} = 0 V



3. 1. 2 S-89140 Series

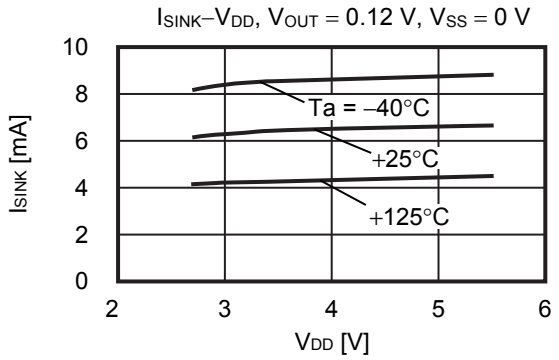
I_{SOURCE}–V_{DD}, V_{OUT} = V_{DD} – 0.12 V, V_{SS} = 0 V



3. 2 I_{SINK} vs. Power supply voltage

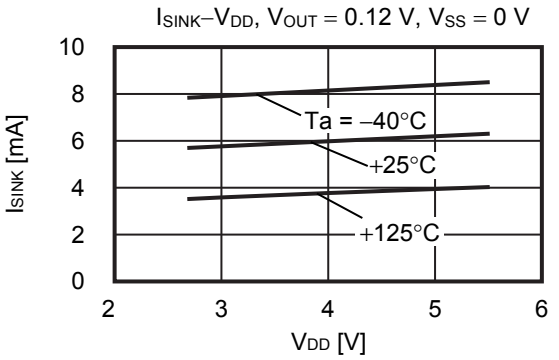
3. 2. 1 S-89130 Series

I_{SINK}–V_{DD}, V_{OUT} = 0.12 V, V_{SS} = 0 V



3. 2. 2 S-89140 Series

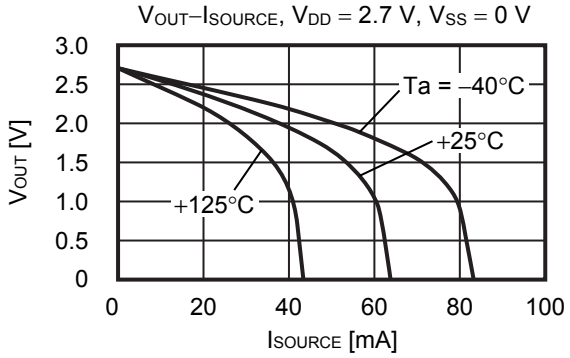
I_{SINK}–V_{DD}, V_{OUT} = 0.12 V, V_{SS} = 0 V



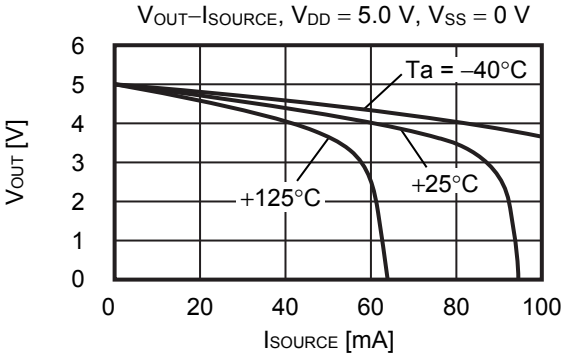
3. 3 Output voltage (V_{OUT}) vs. I_{SOURCE}

3. 3. 1 S-89130 Series

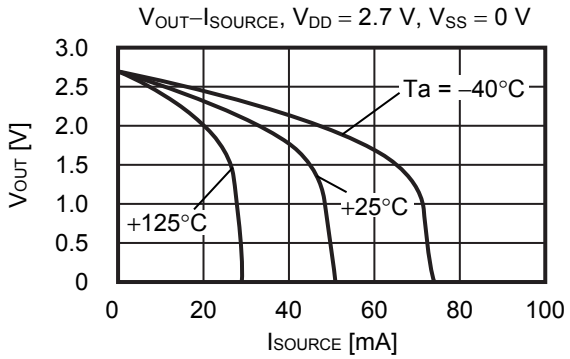
V_{OUT}–I_{SOURCE}, V_{DD} = 2.7 V, V_{SS} = 0 V

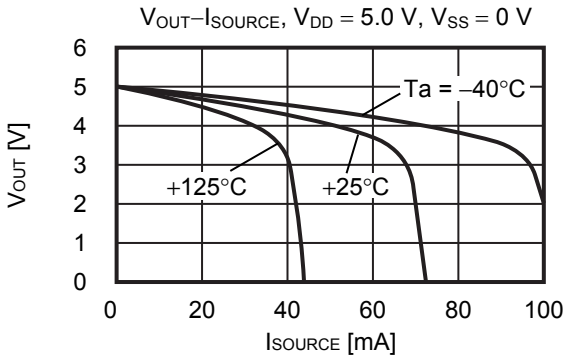


V_{OUT}–I_{SOURCE}, V_{DD} = 5.0 V, V_{SS} = 0 V



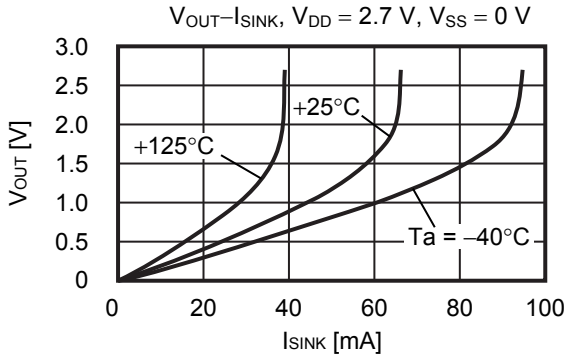
3. 3. 2 S-89140 Series

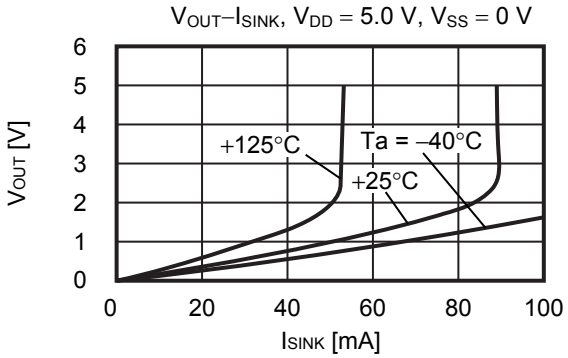




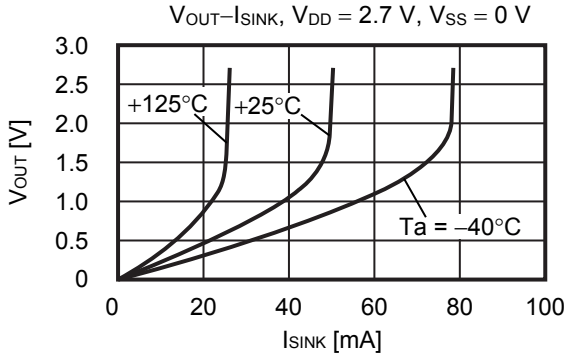
3. 4 Output voltage (V_{OUT}) vs. I_{SINK}

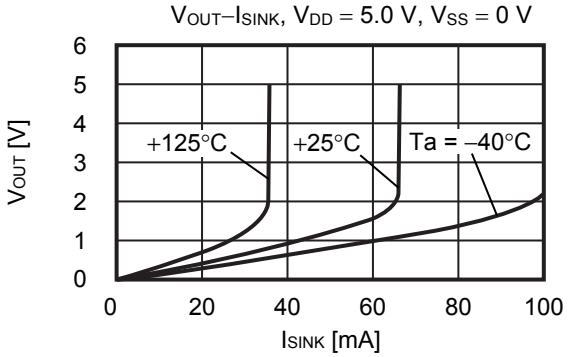
3. 4. 1 S-89130 Series





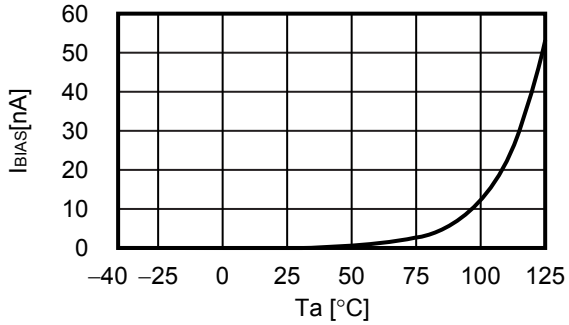
3. 4. 2 S-89140 Series

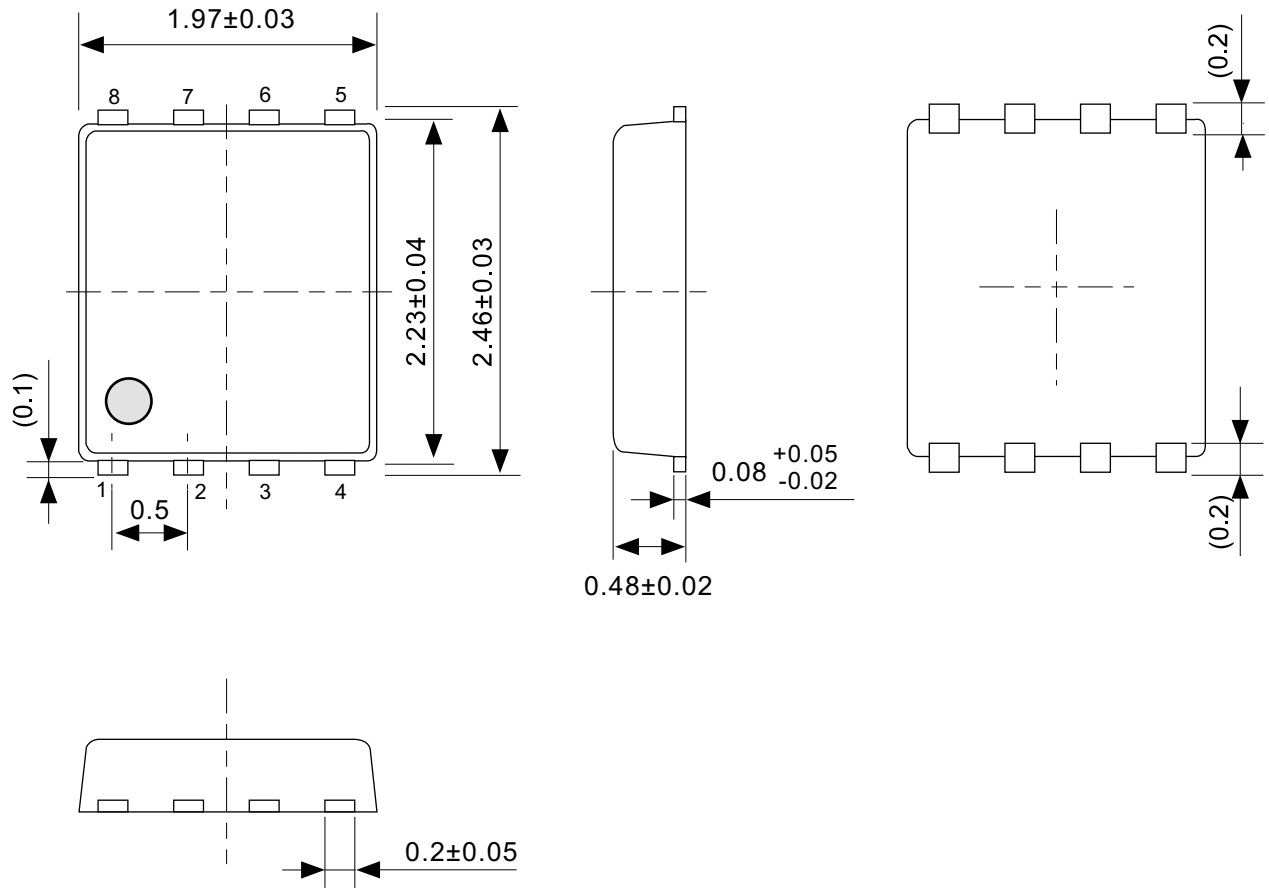




4. Input bias current vs. Temperature

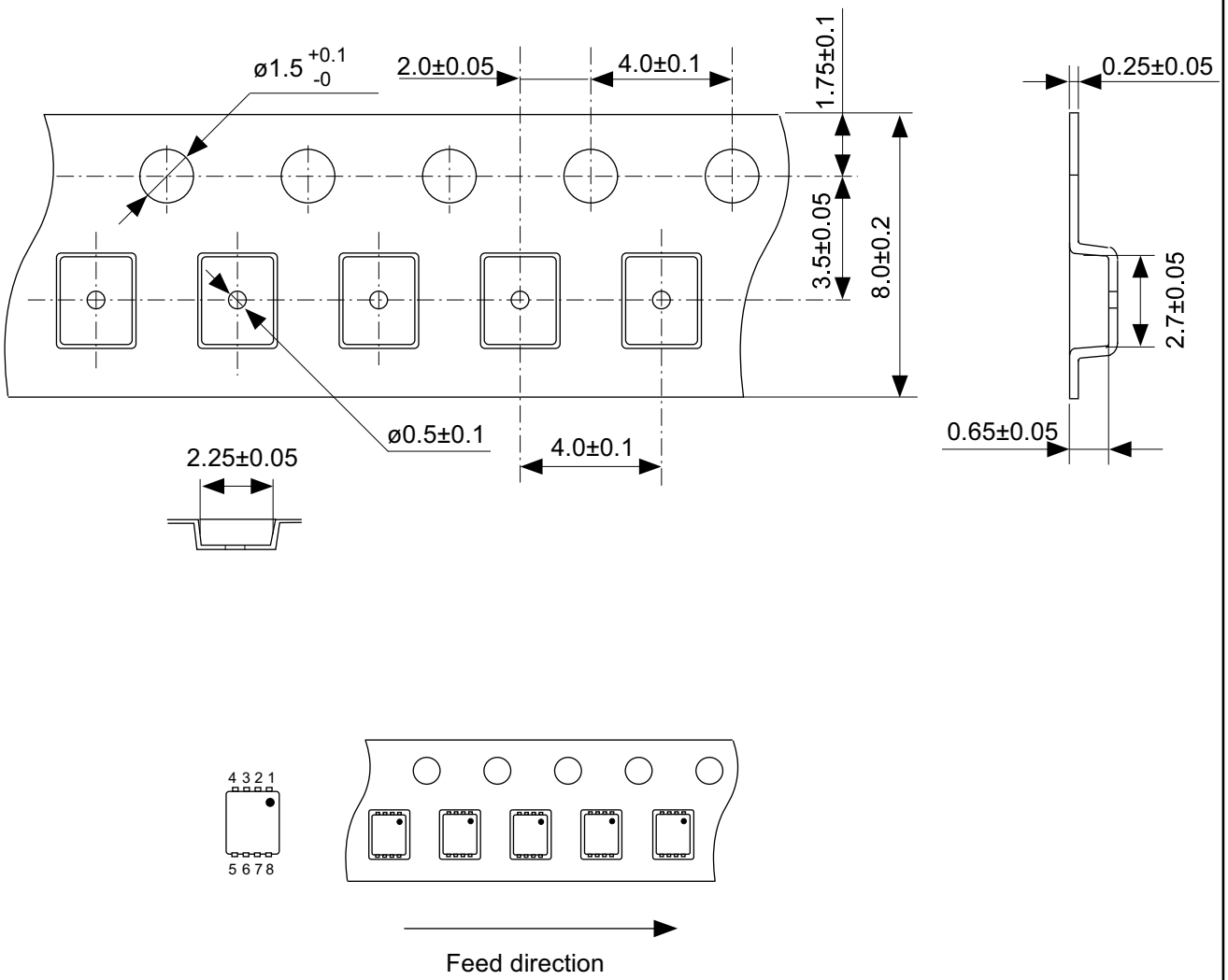
I_{BIAS}–Ta, V_{DD} = 5.0 V, V_{SS} = 0 V, V_{CMR} = V_{DD} / 2





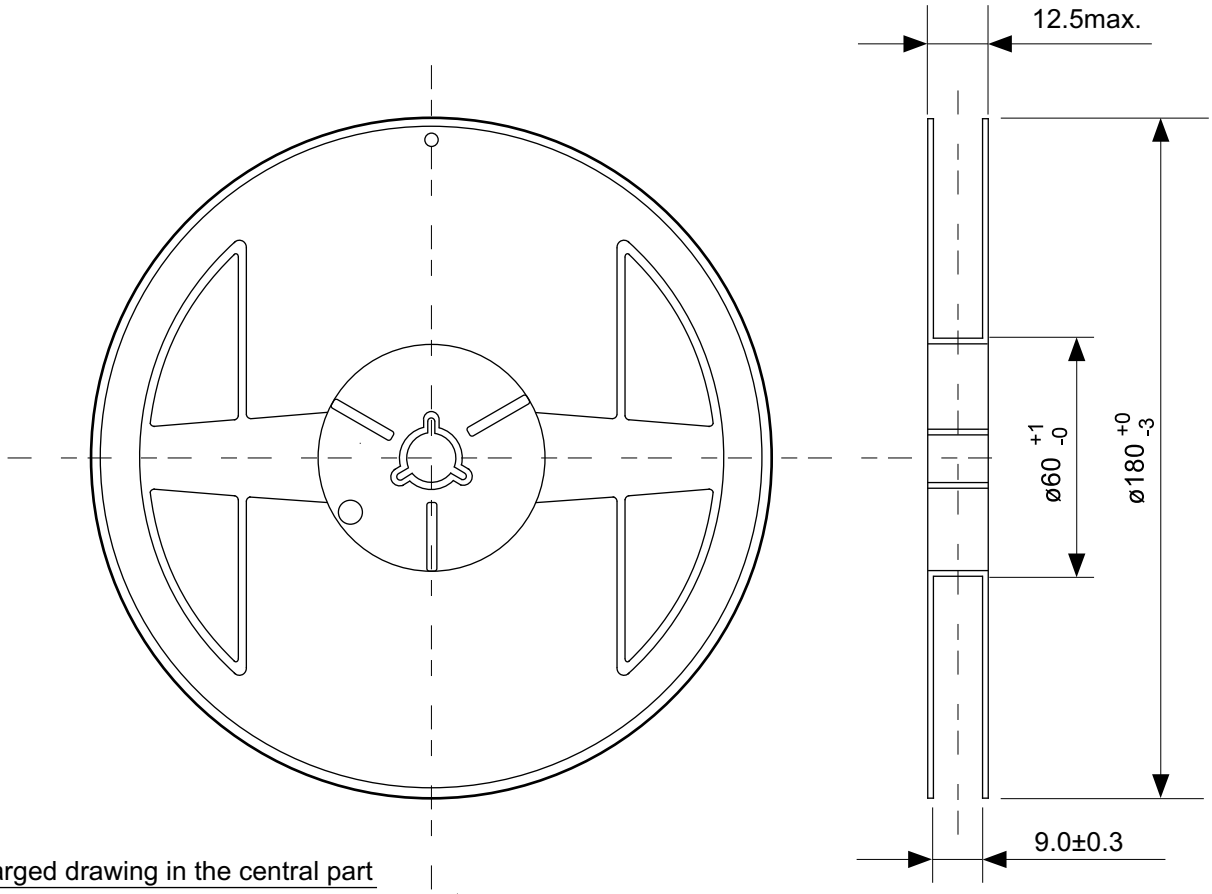
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

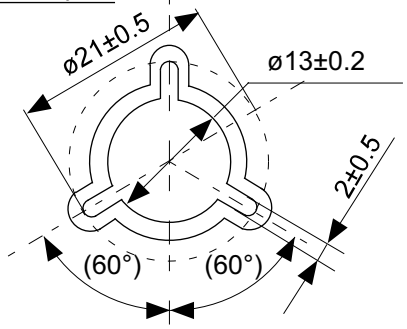


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

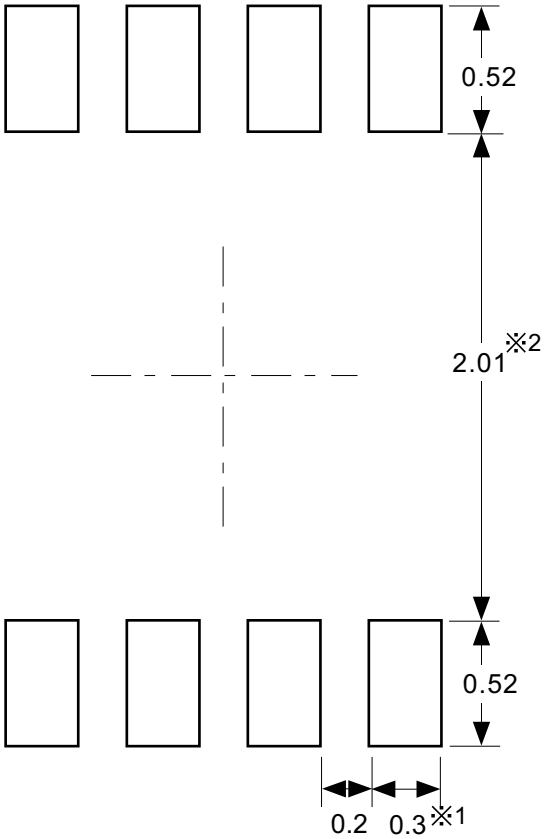


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

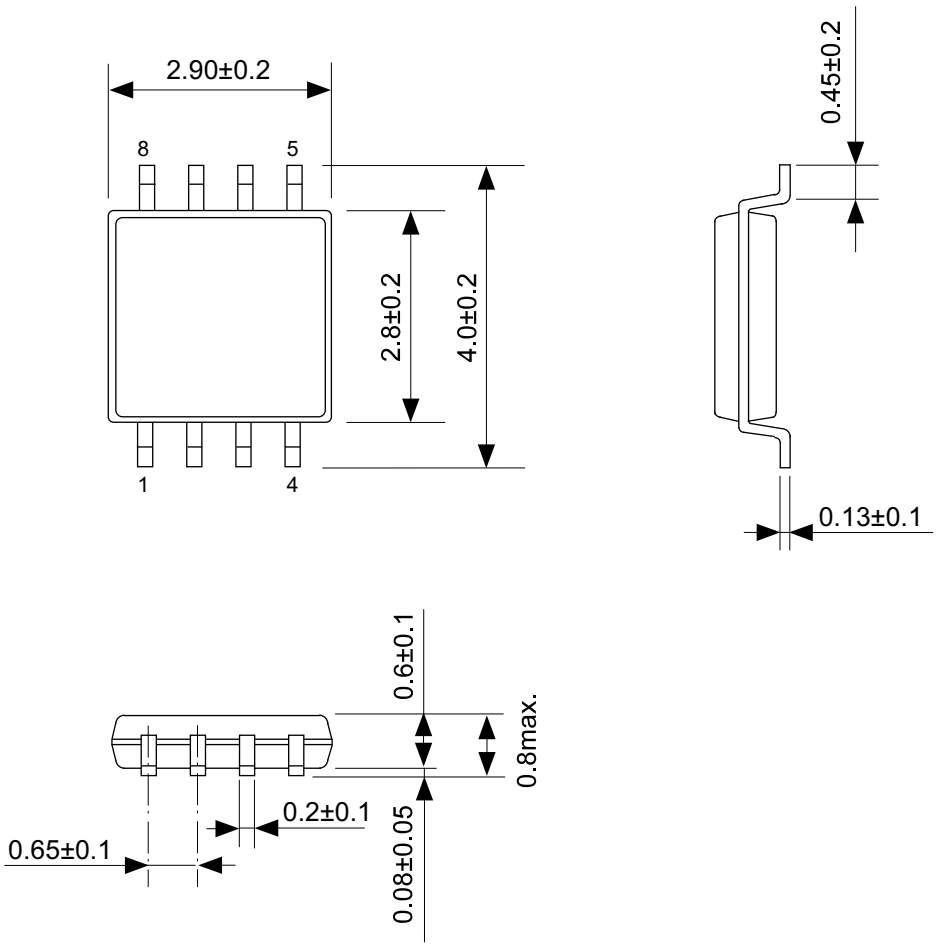
Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

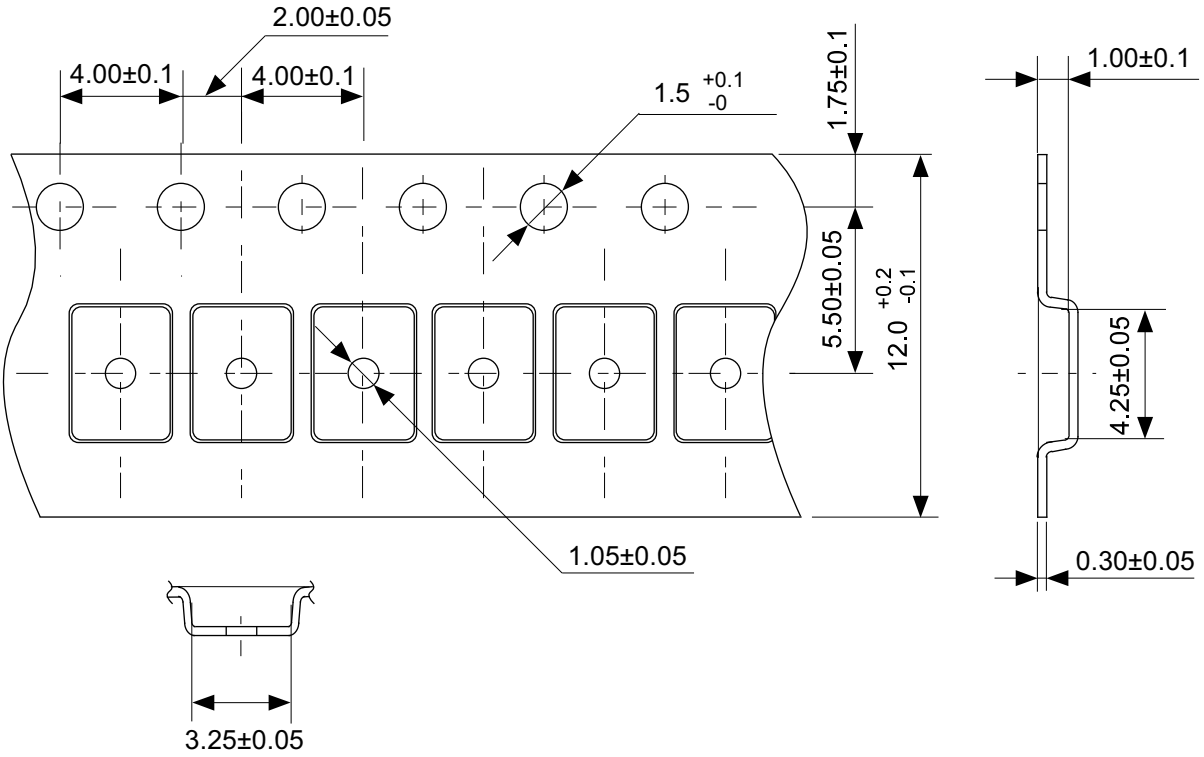
No. PH008-A-L-SD-4.1

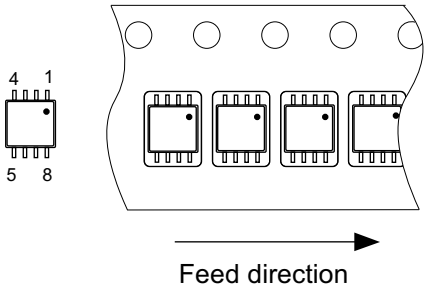
TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	



No. FM008-A-P-SD-1.2

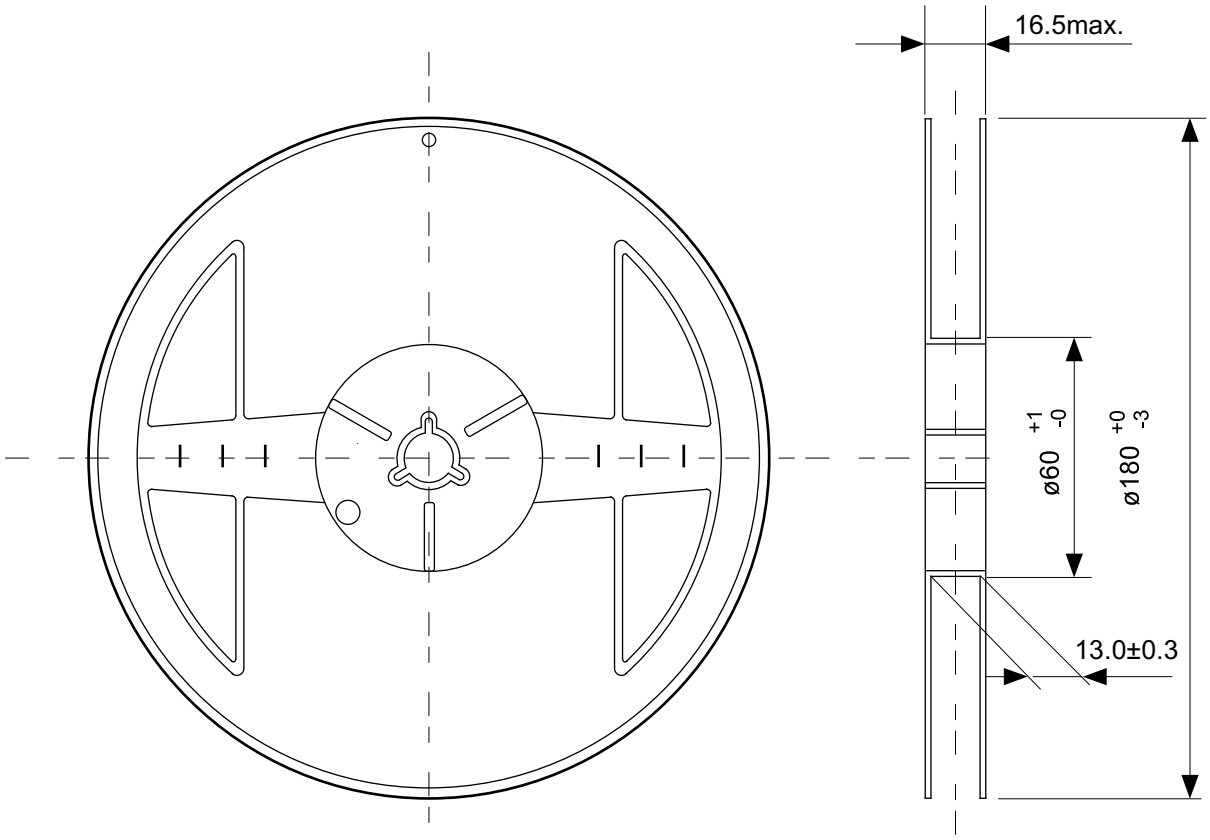
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	



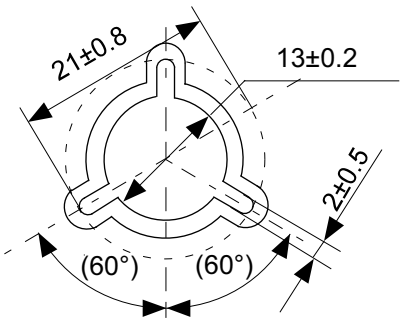


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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