



Low-*RON*, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

General Description

The MAX4901–MAX4905 switches feature negative signal capability that allows signals below ground to pass through without distortion. The MAX4901/MAX4902 are a dual SPST (single-pole/single-throw) and the MAX4903/MAX4904/MAX4905 are a single SPDT (single-pole/double-throw) configuration. These analog switches operate from a single +1.8V to +5.5V supply and have low 0.6Ω on-resistance, making them ideal for switching audio signals.

The MAX4905 includes a comparator that can be used for headphone detection or mute/send key function. The MAX4902/MAX4904/MAX4905 have internal shunt resistors to automatically discharge any capacitance at the NO₋ and NC connection points. This reduces click-and-pop sounds that occur when switching audio signals between pre-charged points. A break-before-make feature and auto-discharge also help to reduce popping.

These SPST and SPDT switches are available in space-saving 8-pin TDFN and 9-bump UCSP™ packages and operate over the -40°C to +85°C extended temperature range.

Applications

Cell Phones
PDAs and Handheld Devices

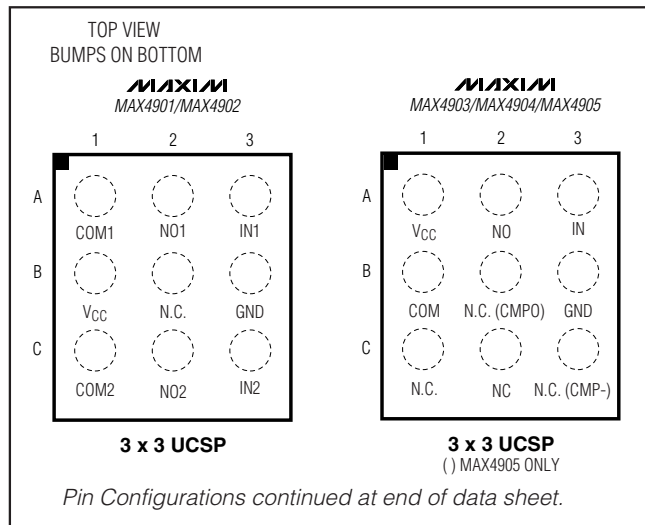
Notebook Computers
MP3 Players

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- ◆ Distortion-Free Signal Throughput Down to $V_{CC} - 5.5V$
- ◆ Comparator for Headphone or Mute Detection (MAX4905)
- ◆ Clickless Switches with Internal Shunt Resistors (MAX4902/MAX4904/MAX4905)
- ◆ 0.6Ω (typ) Low On-Resistance (R_{ON})
- ◆ 0.25Ω On-Resistance Flatness
- ◆ +1.8V to +5.5V Supply Voltage
- ◆ 0.04% THD

Pin Configurations



MAX4901–MAX4905

Ordering Information/Selector Guide

| PART | PIN-PACKAGE | TOP MARK | CONFIGURATION | COMPARATOR | SHUNT | PKG CODE |
|--------------|------------------------|----------|---------------|------------|-------|----------|
| MAX4901EBL-T | 1.5mm x 1.5mm 9 UCSP-9 | AEU | 2 x SPST | No | No | B9-1 |
| MAX4901ETA-T | 8 TDFN-8 | AOW | 2 x SPST | No | No | T833-2 |
| MAX4902EBL-T | 1.5mm x 1.5mm 9 UCSP-9 | AEV | 2 x SPST | No | Yes | B9-1 |
| MAX4902ETA-T | 8 TDFN-8 | AOX | 2 x SPST | No | Yes | T833-2 |
| MAX4903EBL-T | 1.5mm x 1.5mm 9 UCSP-9 | AEY | 1 x SPDT | No | No | B9-1 |
| MAX4903ETA-T | 8 TDFN-8 | AOY | 1 x SPDT | No | No | T833-2 |
| MAX4904EBL-T | 1.5mm x 1.5mm 9 UCSP-9 | AEW | 1 x SPDT | No | Yes | B9-1 |
| MAX4904ETA-T | 8 TDFN-8 | AOZ | 1 x SPDT | No | Yes | T833-2 |
| MAX4905EBL-T | 1.5mm x 1.5mm 9 UCSP-9 | AEX | 1 x SPDT | Yes | Yes | B9-1 |
| MAX4905ETA-T | 8 TDFN-8 | APA | 1 x SPDT | Yes | Yes | T833-2 |

Note: All devices operate over the -40°C to +85°C operating temperature range.



Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

| | |
|---|--|
| V _{CC} , I _N _, CMP- | -0.3V to +6.0V |
| COM_, NO_, NC | (V _{CC} - 6V) to (V _{CC} + 0.3V) |
| CMPO | -0.3V to (V _{CC} + 0.3V) |
| Open-Switch Continuous Current NO_, NC (MAX4902/MAX4904/MAX4905) | ±30mA |
| Closed-Switch Continuous Current COM_, NO_, NC | ±100mA |
| Peak Current COM_, NO_, NC (Pulsed at 1ms, 50% duty cycle) | ±200mA |
| Peak Current COM_, NO_, NC (Pulsed at 1ms, 10% duty cycle) | ±300mA |

Continuous Power Dissipation (T_A = +70°C)

| | |
|---|-----------------|
| 8-Pin TDFN (derate 18.2mW/°C above +70°C) | 1455mW |
| 9-Bump UCSP (derate 5.2mW/°C above +70°C) | 412mW |
| ESD Method 3015.7 | ±2kV |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Bump Temperature (soldering) | |
| Infrared (15s) | +220°C |
| Vapor Phase (60s) | +215°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|---|--|--|-------|-----------------|-------|
| POWER SUPPLY | | | | | | |
| Power-Supply Range | V _{CC} | | 1.8 | | 5.5 | V |
| Supply Current | I ₊ | V _{CC} = 5.5V, V _{INL} = 0V or V _{CC} | MAX4901– MAX4904 | 0.001 | 1 | μA |
| | | | MAX4905 | 5 | 10 | |
| ANALOG SWITCH | | | | | | |
| Analog Signal Range | V _{NO_} , V _{NC} , V _{COM_} | (Note 2) | V _{CC} - 5.5 | | V _{CC} | V |
| On-Resistance | R _{ON(NC)} , R _{ON(NO)} | V _{CC} = 2.7V, V _{NC} or V _{NO_} = V _{CC} - 5.5V, -1V, 0, 1V, 2V, V _{CC} ; I _{COM} = 100mA (Notes 3, 4) | T _A = +25°C | 0.6 | 1.0 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 1.2 | |
| On-Resistance Match Between Channels | ΔR _{ON} | V _{CC} = 2.7V, I _{NO_} or I _{NC} = 100mA or V _{NO_} (Notes 3, 4, 5) | T _A = +25°C | 0.01 | 0.25 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 0.30 | |
| On-Resistance Flatness | R _{FLAT} | V _{CC} = 2.7V, V _{NC} or V _{NO_} = V _{CC} - 5.5V, -1V, 0, 1V, 2V, V _{CC} ; I _{COM} = 100mA (Notes 4, 6) | T _A = +25°C | 0.25 | 0.5 | Ω |
| | | | T _A = T _{MIN} to T _{MAX} | | 0.5 | |

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

MAX4901-MAX4905

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.0V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------------------------|---|---------------------------------|------|-----|----------|
| Shunt Resistance | R_{SH} | $I_{NO_}$ or $I_{NC_} = 10mA$, $V_{CC} = 2.7V$ (MAX4902/MAX4904/ MAX4905) | | 30 | 50 | Ω |
| NO_, NC Off-Leakage Current | $I_{NO_}(OFF)$, $I_{NC_}(OFF)$ | $V_{CC} = 2.7V$, switch open; V_{NC} or $V_{NO_} = -2.5V, +2.5V$; $V_{COM_}$ $= +2.5V, -2.5V$ (MAX4901/ MAX4903) (Notes 3, 7) | $T_A = +25^{\circ}C$ | -6 | +6 | nA |
| | | | $T_A = T_{MIN}$ to T_{MAX} | -50 | +50 | |
| COM_ Off-Leakage Current | $I_{COM_}(OFF)$ | $V_{CC} = 2.7V$, switch open; V_{NC} or $V_{NO_} = -2.5V, +2.5V$; $V_{COM_} = -2.5V, +2.5V$ (MAX4901) (Note 3) | $T_A = +25^{\circ}C$ | -6 | +6 | nA |
| | | | $T_A = T_{MIN}$ to T_{MAX} | -50 | +50 | |
| COM_ On-Leakage Current | $I_{COM_}(ON)$ | $V_{CC} = 2.7V$, switch closed; V_{NC} or $V_{NO_} = -2.5V, +2.5V$, or unconnected; $V_{COM_} = -2.5V$, $+2.5V$ or unconnected (Note 3) | $T_A = +25^{\circ}C$ | -6 | +6 | nA |
| | | | $T_A = T_{MIN}$ to T_{MAX} | -50 | +50 | |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Turn-On Time | t_{ON} | $V_{CC} = 2.7V$, $V_{NO_} = 1.5V$, $V_{IN_} = 0V$ to V_{CC} ; $V_{NC} = 1.5V$, $V_{IN_} = V_{CC}$ to 0; $R_L = 50\Omega$, $C_L = 5pF$ (Figure 1) | | 25 | 100 | ns |
| Turn-Off Time | t_{OFF} | $V_{CC} = 2.7V$, $V_{NO_} = 1.5V$, $V_{IN_} = V_{CC}$ to 0; $V_{NC} = 1.5V$, $V_{IN_} = 0$ to V_{CC} ; $R_L = 50\Omega$, $C_L = 5pF$ (Figure 1) | | 15 | 100 | ns |
| Break-Before-Make Time Delay (MAX4903/MAX4904/MAX4905) | t_{BBM} | $V_{CC} = 2.7V$, $V_{NO_} = 1.5V$, $V_{IN_} = V_{CC}$ to 0; $V_{NC} = 1.5V$, $V_{IN_} = 0$ to V_{CC} ; $R_L = 50\Omega$, $C_L = 5pF$ (Figure 2) | $T_A = +25^{\circ}C$ | 2 | 10 | ns |
| | | | $T_A = T_{MIN}$ to T_{MAX} | 1 | | |
| Charge Injection | Q | $V_{COM_} = 0V$, $R_S = 0\Omega$, $C_L = 1.0nF$ (Figure 3) | | 125 | | pC |
| Off-Isolation (Note 8) | V_{ISO} | $f = 100kHz$, $V_{COM_} = 1V_{RMS}$, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 4) | | -70 | | dB |
| Crosstalk | V_{CT} | $f = 100kHz$, $V_{COM_} = 1V_{RMS}$, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 4) | | -75 | | dB |
| Power-Supply Rejection Ratio | PSRR | $f = 10kHz$, $V_{COM_} = 1V_{RMS}$, $R_L = 50\Omega$, $C_L = 5pF$ | | 60 | | dB |
| On-Channel -3dB Bandwidth | BW | Signal = 0dBm, $R_L = 50\Omega$, $C_L = 5pF$ (Figure 4) | | 27 | | MHz |
| Total Harmonic Distortion | THD | $f = 20Hz$ to $20kHz$, $V_{COM_} = 0.5V_{P-P}$, DC bias = 0, $R_L = 32\Omega$ | | 0.04 | | % |

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.0V$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|--------------------------------|---|------|-----------------|------|---------|
| NO_, NC Off-Capacitance | $C_{NO(OFF)}$ $C_{NC(OFF)}$ | $f = 1MHz$, $V_{COM} = 0.5V_{P-P}$, DC bias = 0 (Figure 5) | | 40 | | pF |
| COM On-Capacitance | $C_{COM(ON)}$ | $f = 1MHz$, $V_{COM} = 0.5V_{P-P}$, DC bias = 0 (Figure 5) | | 200 | | pF |
| DIGITAL I/O (IN_) | | | | | | |
| Input Logic-High Voltage | V_{IH} | $V_{CC} = 2.7V$ to $3.6V$ | 1.4 | | | V |
| | | $V_{CC} = 4.2V$ to $5.5V$ | 2.0 | | | |
| Input Logic-Low Voltage | V_{IL} | $V_{CC} = 2.7V$ to $3.6V$ | | | 0.5 | V |
| | | $V_{CC} = 4.2V$ to $5.5V$ | | | 0.8 | |
| Input Leakage Current | I_{IN} | $V_{IN-} = 0V$ or V_{CC} | -1 | | +1 | μA |
| COMPARATOR (MAX4905) | | | | | | |
| Comparator Threshold | | | | $V_{CC} / 3$ | | V |
| Comparator Output-High Voltage | | $I_{SOURCE} = 1mA$ | | $V_{CC} - 0.4V$ | | V |
| Comparator Output-Low Voltage | | $I_{SINK} = 1mA$ | | | 0.4 | V |
| Comparator Input Leakage | | $V_{CMP-} = 0$ to $2.7V$ | -100 | | +100 | nA |
| Comparator Switching Time | | $V_{CC} = 2.7V$, $V_{CMP-} = 0V$ to V_{CC} , from 50% of V_{CMP-} to 50% of V_{CMPO} | | 1 | 2 | μs |

Note 1: UCSP and TDFN parts are 100% tested at $T_A = +25^{\circ}C$ only, and guaranteed by design over the specified temperature range.

Note 2: Signals on COM_, NO_, or NC exceeding V_{CC} are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 3: Guaranteed by design.

Note 4: I_{COM} for UCSP is 10mA.

Note 5: $\Delta RON = RON(MAX) - RON(MIN)$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: The MAX4902/MAX4904/MAX4905 have an internal shunt resistor when, in off-state, will determine off-current.

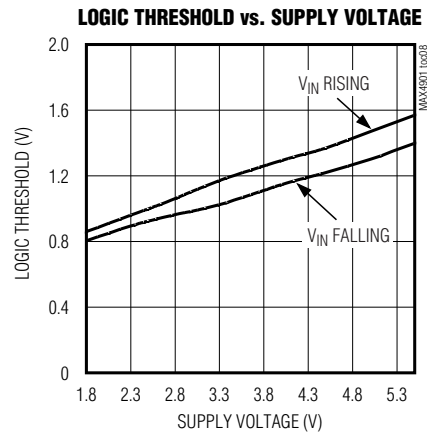
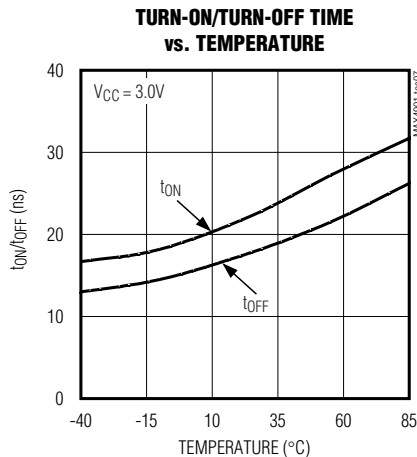
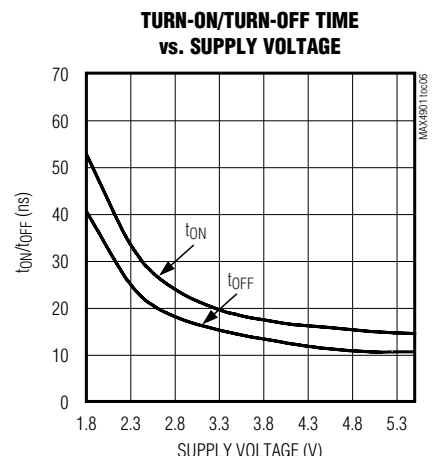
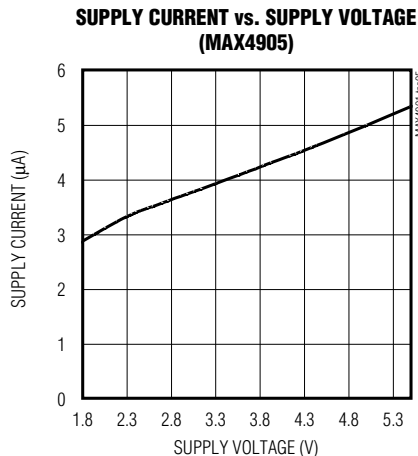
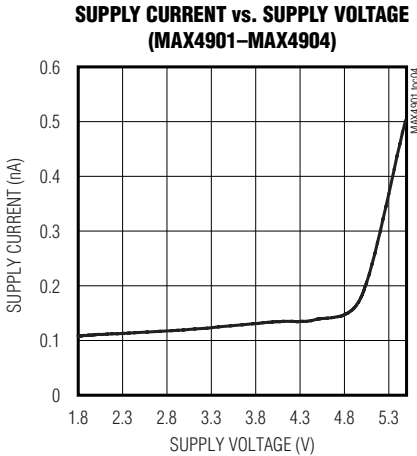
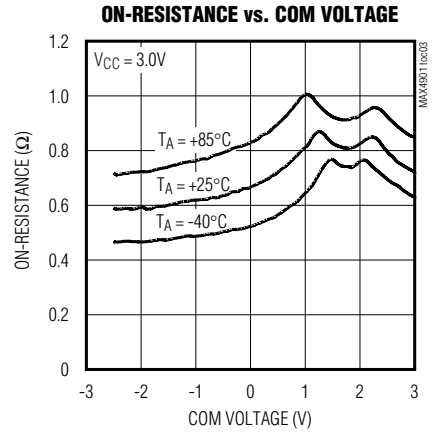
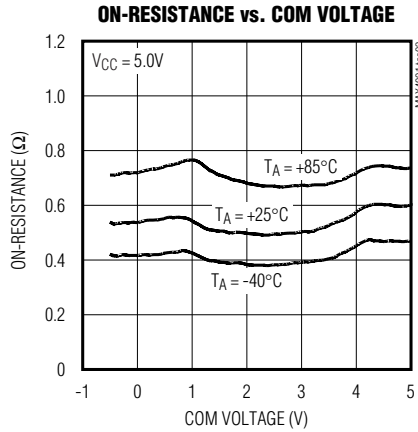
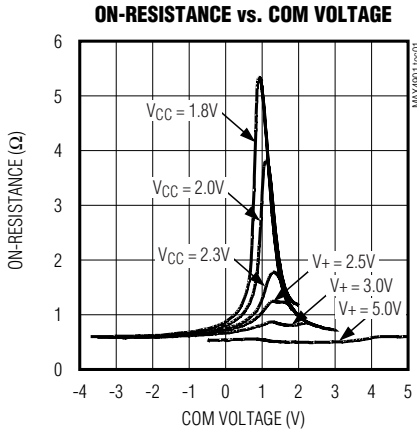
Note 8: Off-Isolation = $20\log_{10}(V_{COM} / V_{NO})$, V_{COM} = output, V_{NO} = input to off switch.

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, $V_{CC} = 3.0\text{V}$, unless otherwise noted.)

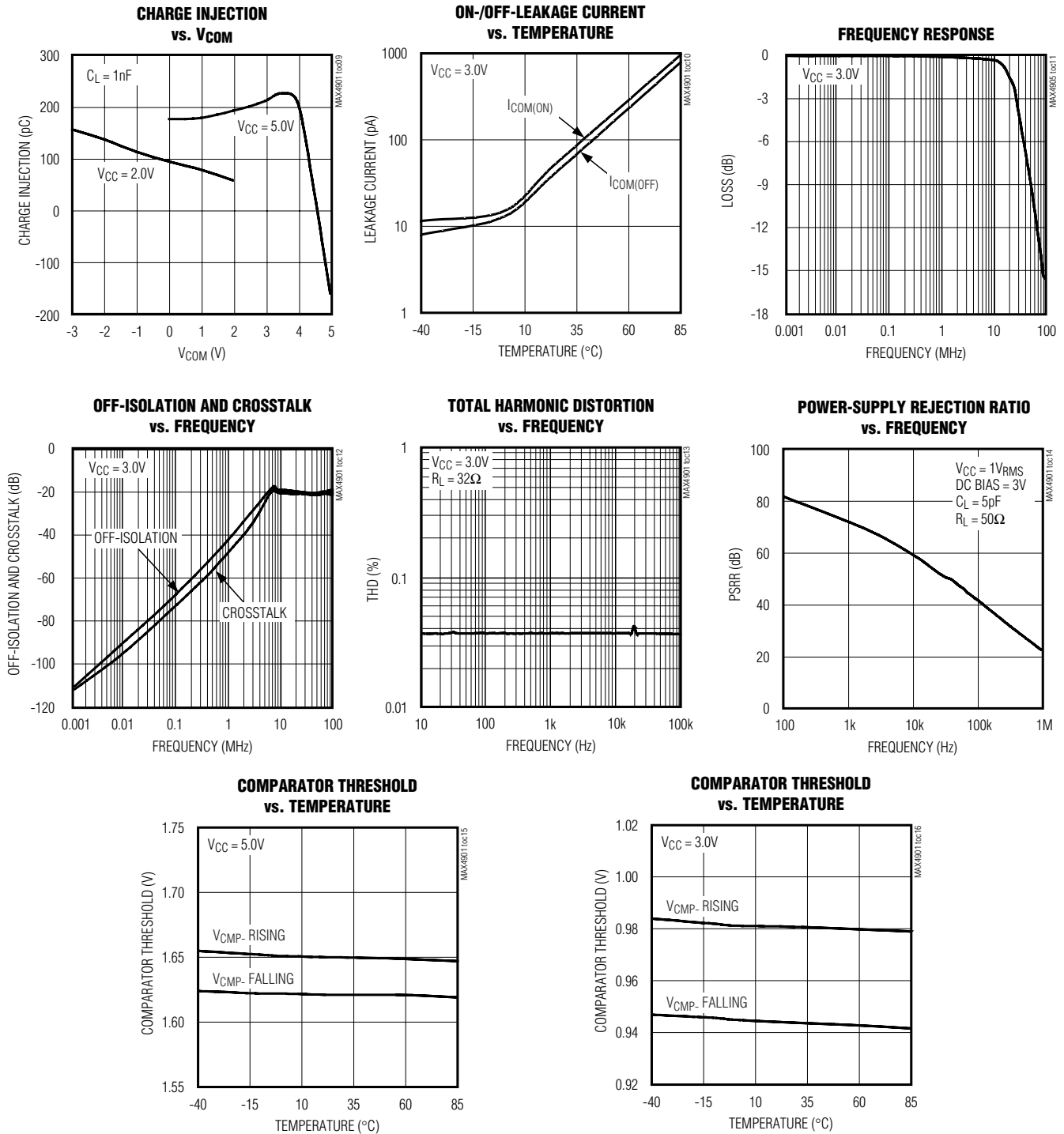
MAX4901-MAX4905



Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = 3.0\text{V}$, unless otherwise noted.)



Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Pin Description (MAX4901/MAX4902 Dual-SPST Switches)

| PIN | | NAME | FUNCTION |
|------|------|-----------------|--|
| TDFN | UCSP | | |
| 1 | B1 | V _{CC} | Positive Supply-Voltage Input. Bypass V _{CC} to GND with a 0.1µF capacitor as close to V _{CC} as possible. |
| 2 | A1 | COM1 | Analog Switch 1, Common Terminal |
| — | B2 | N.C. | No Connection. Leave N.C. unconnected. |
| 3 | A2 | NO1 | Analog Switch 1, Normally Open Terminal. NO1 (MAX4902) has a shunt resistor to GND when the switch is in open position. |
| 4 | A3 | IN1 | Digital Control Input for Analog Switch 1. A logic high on IN1 connects COM1 to NO1 and a logic low opens the switch. |
| 5 | B3 | GND | Ground |
| 6 | C3 | IN2 | Digital Control Input for Analog Switch 2. A logic high on IN2 connects COM2 to NO2 and a logic low opens the switch. |
| 7 | C2 | NO2 | Analog Switch 2, Normally Open Terminal. NO2 has a shunt resistor to GND when the switch is in open position (MAX4902). |
| 8 | C1 | COM2 | Analog Switch 2, Common Terminal |
| EP | — | EP | Exposed Pad. Connect exposed pad to GND. |

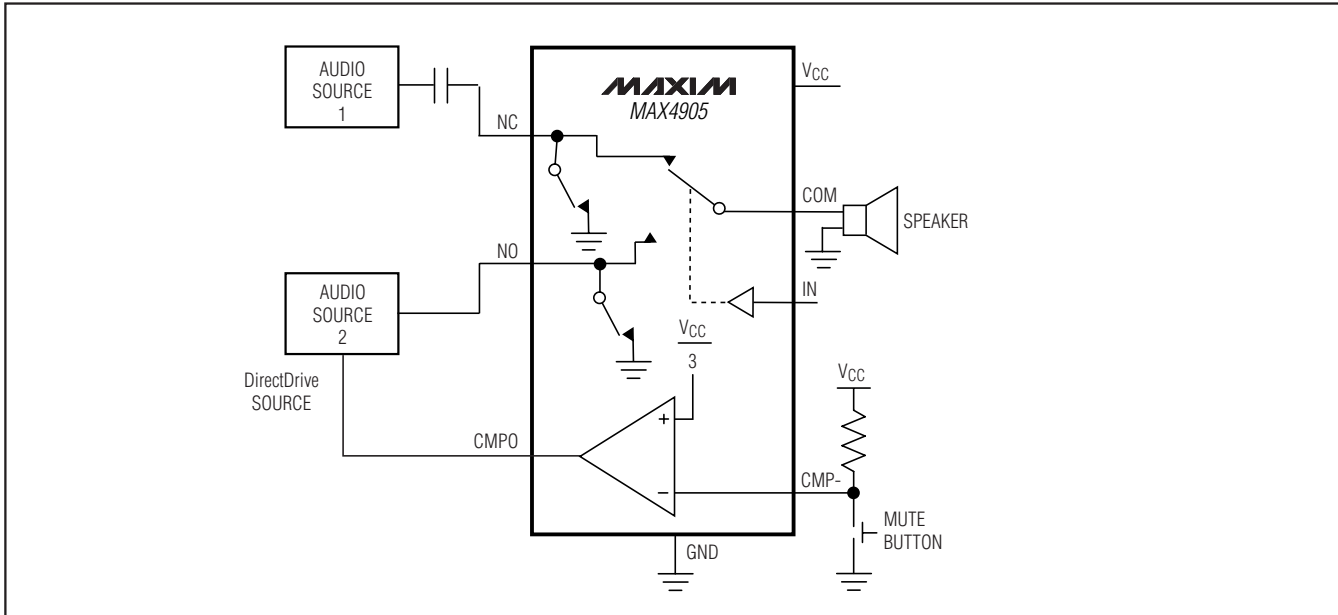
MAX4901-MAX4905

Pin Description (MAX4903/MAX4904/MAX4905 SPDT Switches)

| PIN | | NAME | FUNCTION |
|------|------|-----------------|--|
| TDFN | UCSP | | |
| 1 | A1 | V _{CC} | Positive Supply-Voltage Input. Bypass V _{CC} to GND with a 0.1µF capacitor as close to V _{CC} as possible. |
| 2 | A2 | NO | Analog Switch, Normally Open Terminal. NO has a shunt resistor to GND when the switch is in open position (MAX4904/MAX4905). |
| 3 | A3 | IN | Digital Control Input. Logic low on IN connects COM to NC and logic high connects COM to NO. |
| 4 | B2 | N.C. | No Connection. Leave N.C. unconnected (MAX4903/MAX4904). |
| | | CMPO | Comparator Output (MAX4905) |
| 5 | B3 | GND | Ground |
| 6 | C3 | N.C. | No Connection. Leave N.C. unconnected (MAX4903/MAX4904). |
| | | CMP- | Comparator Input (MAX4905) |
| 7 | C2 | NC | Analog Switch, Normally Closed Terminal. NC has a shunt resistor to GND when the switch is in open position (MAX4904/MAX4905). |
| 8 | B1 | COM | Analog Switch, Common Terminal |
| — | C1 | N.C. | No Connection. Leave N.C. unconnected (MAX4903/MAX4904/MAX4905) |
| EP | — | EP | Exposed Pad. Connect exposed pad to GND. |

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Typical Operating Circuit



Detailed Description

The MAX4901–MAX4905 are low on-resistance, low-voltage, dual-SPST and single-SPDT analog switches that operate from a +1.8V to +5.5V supply and are fully specified for nominal 3.0V applications. The devices feature a negative signal capability that allows signals below ground to pass through without distortion and have break-before-make switching (MAX4903/MAX4904/MAX4905).

The MAX4905 features a comparator that can be used for headphone or mute detection. The comparator threshold is internally generated to be approximately $1/3$ of V_{CC} . The MAX4902/MAX4904/MAX4905 feature an internal shunt resistor to discharge any capacitance at NO_+ and NC connection points. This reduces the click-and-pop sounds that occur when switching audio signals.

Applications Information

Digital Control Inputs

The MAX4901–MAX4905 logic inputs accept up to +5.5V, regardless of supply voltage. For example, with a +3.3V supply, IN_+ can be driven low to GND and high to +5.5V, allowing for mixing of logic levels in a system. Driving IN_+ rail-to-rail minimizes power consumption. For a +1.8V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high). For a +5V supply voltage, the logic thresholds are 0.8V (low) and 2.0V (high).

Analog Signal Levels

The on-resistance of the MAX4901–MAX4905 changes very little for analog input signals across the entire supply-voltage range (see the *Typical Operating Characteristics*). The switches are bidirectional.

The MAX4901–MAX4905 pass signals as low as $V_{CC} - 5.5V$, including signals below ground with minimal distortion. Note that there are shunt resistors on NO_+ and NC when they are unconnected to COM_+ for the MAX4902/MAX4904/MAX4905.

Comparator (MAX4905)

The MAX4905 includes a comparator that can be used for mute and headphone detection functions. The positive terminal of the comparator is internally set to $V_{CC} / 3$. When the negative terminal (CMP_-) is below the threshold, the comparator output ($CMPO$) is a logic high.

The comparator threshold of $V_{CC} / 3$ allows for detection of headphones because headphone audio signals are typically biased to $V_{CC} / 2$.

Shunt Resistor (MAX4902/MAX4904/MAX4905)

The 50Ω shunt resistors on the MAX4902/MAX4904/MAX4905 automatically discharge any capacitance at the NC or NO_+ terminals when they are unconnected to COM_+ . This reduces audio click-and-pop sounds that occur when switching between audio sources.

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

MAX4901-MAX4905

Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} before applying analog signals, especially if the analog signal is not current-limited.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note: *UCSP—A Water-Level Chip-Scale Package* on Maxim's web site at www.maxim-ic.com/ucsp.

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW
NOTE: N.C. IS NO CONNECTION (SEE PIN DESCRIPTION TABLE)

MAX4901/MAX4902

TDFN
*EXPOSED PAD CONNECTED TO GND

MAX4903/MAX4904

TDFN
*EXPOSED PAD CONNECTED TO GND

MAX4905

*EXPOSED PAD CONNECTED TO GND

| MAX4901-MAX4905 | | |
|-----------------|-----|-----|
| IN | NC | NO |
| 0 | ON | OFF |
| 1 | OFF | ON |

| MAX4904/ MAX4905 | |
|---------------------|------|
| NCS* | NOS* |
| OFF | ON |
| ON | OFF |

*NCS AND NOS REFER TO NORMALLY CLOSED SHUNT REGISTER

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Test Circuits/Timing Diagrams

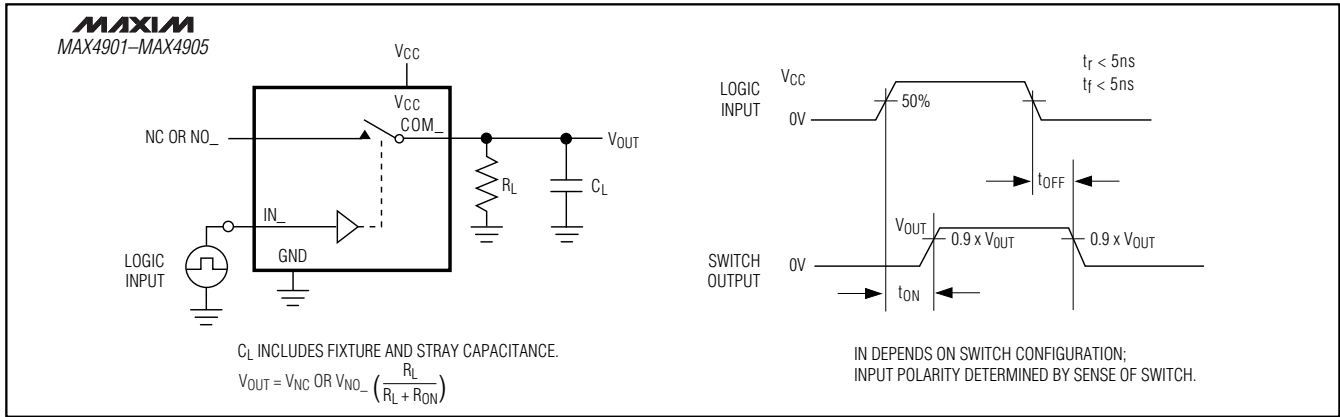


Figure 1. Switching Time

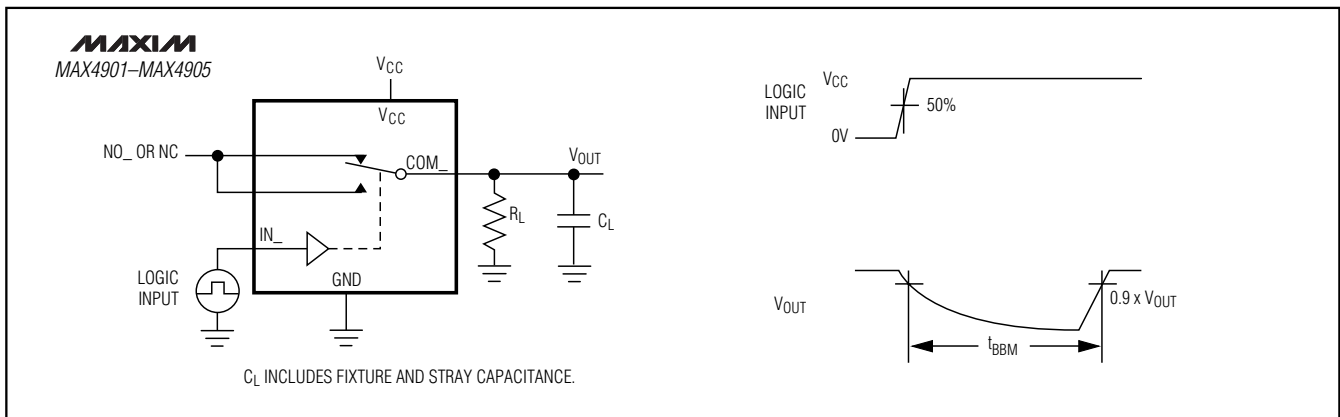


Figure 2. Break-Before-Make Interval

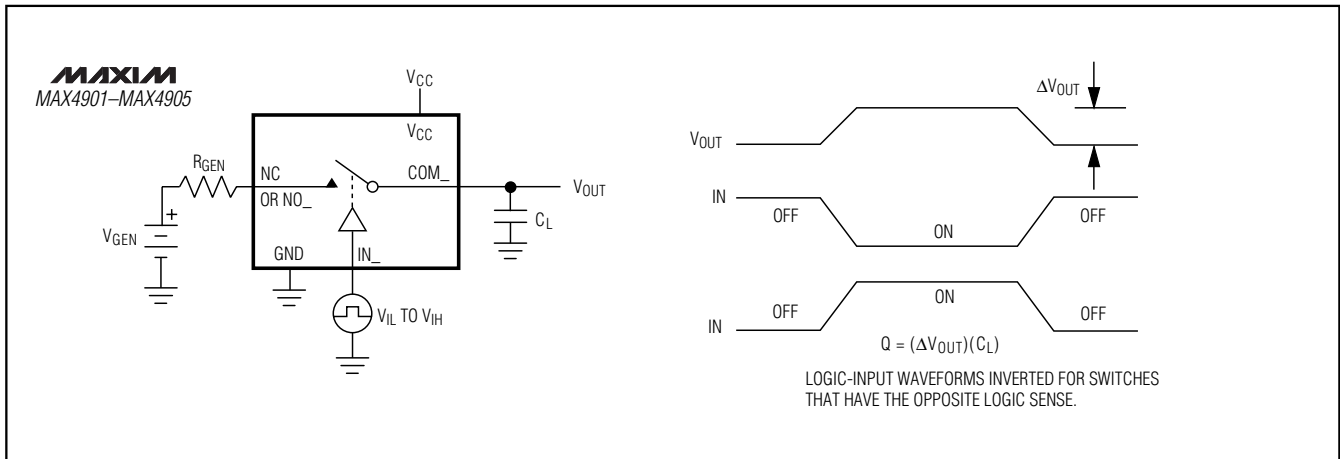


Figure 3. Charge Injection

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Test Circuits/Timing Diagrams (continued)

MAX4901-MAX4905

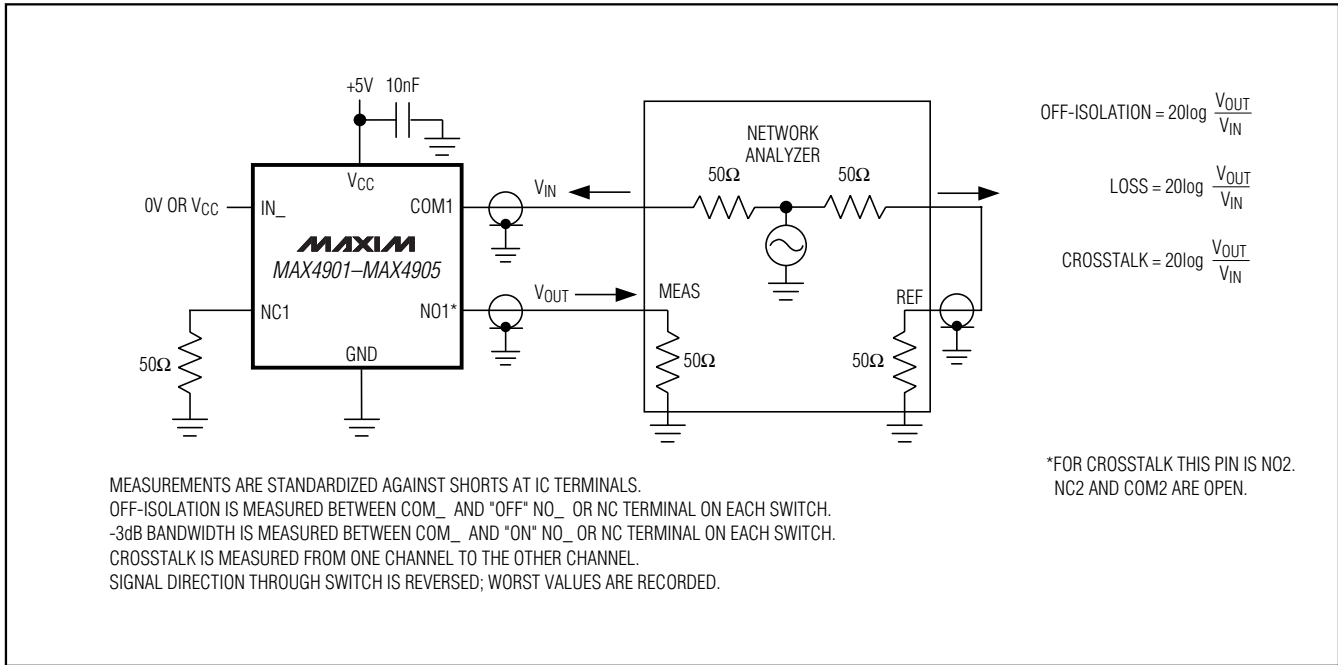


Figure 4. -3dB Bandwidth, Off-Isolation, and Crosstalk

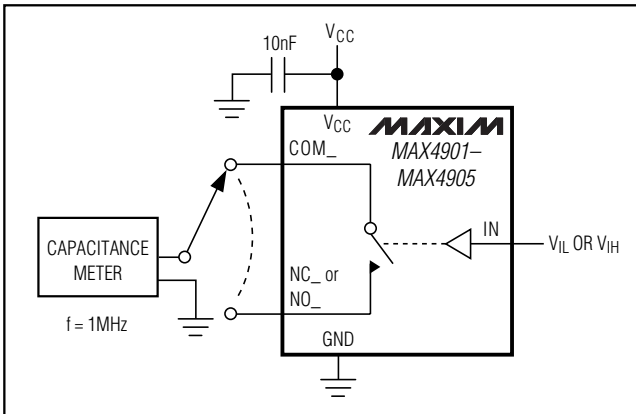


Figure 5. Channel Off-/On-Capacitance

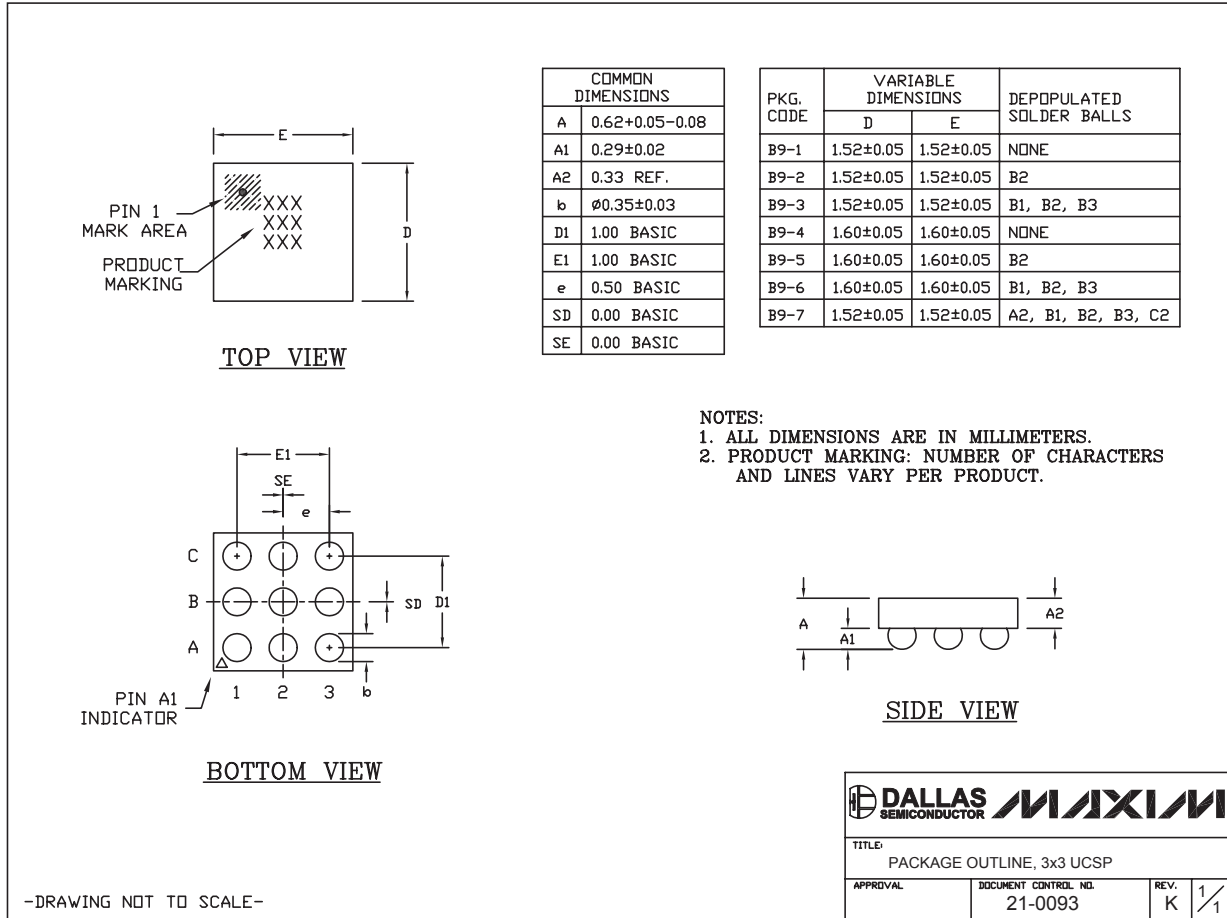
Chip Information

PROCESS: BiCMOS

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR **MAXIM**

TITLE: PACKAGE OUTLINE, 3x3 UCSP

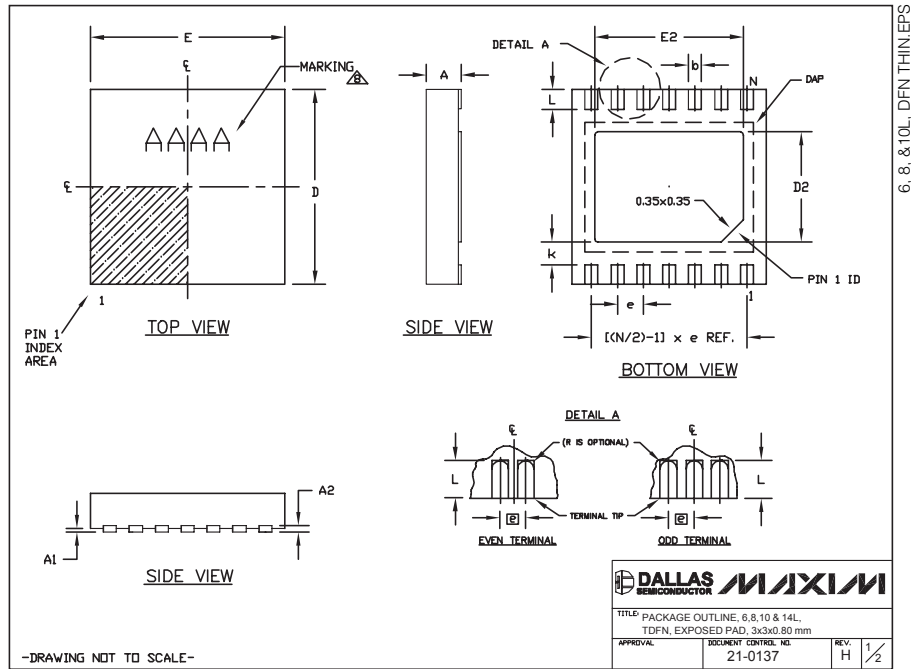
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| APPROVAL | DOCUMENT CONTROL NO. 21-0093 | REV. K | 1/1 |
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Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX4901-MAX4905



| COMMON DIMENSIONS | | | PACKAGE VARIATIONS | | | | | | | |
|-------------------|-----------|------|--------------------|----|-----------|-----------|----------|----------------|-----------|---------------|
| SYMBOL | MIN. | MAX. | PKG. CODE | N | D2 | E2 | e | JEDEC SPEC | b | [(N/2)-1] x e |
| A | 0.70 | 0.80 | T633-1 | 6 | 1.50±0.10 | 2.30±0.10 | 0.95 BSC | MO229 / WEEA | 0.40±0.05 | 1.90 REF |
| D | 2.90 | 3.10 | T633-2 | 6 | 1.50±0.10 | 2.30±0.10 | 0.95 BSC | MO229 / WEEA | 0.40±0.05 | 1.90 REF |
| E | 2.90 | 3.10 | T833-1 | 8 | 1.50±0.10 | 2.30±0.10 | 0.65 BSC | MO229 / WECC | 0.30±0.05 | 1.95 REF |
| A1 | 0.00 | 0.05 | T833-2 | 8 | 1.50±0.10 | 2.30±0.10 | 0.65 BSC | MO229 / WECC | 0.30±0.05 | 1.95 REF |
| L | 0.20 | 0.40 | T833-3 | 8 | 1.50±0.10 | 2.30±0.10 | 0.65 BSC | MO229 / WECC | 0.30±0.05 | 1.95 REF |
| k | 0.25 MIN. | | T1033-1 | 10 | 1.50±0.10 | 2.30±0.10 | 0.50 BSC | MO229 / WEED-3 | 0.25±0.05 | 2.00 REF |
| A2 | 0.20 REF. | | T1033-2 | 10 | 1.50±0.10 | 2.30±0.10 | 0.50 BSC | MO229 / WEED-3 | 0.25±0.05 | 2.00 REF |
| | | | T1433-1 | 14 | 1.70±0.10 | 2.30±0.10 | 0.40 BSC | ---- | 0.20±0.05 | 2.40 REF |
| | | | T1433-2 | 14 | 1.70±0.10 | 2.30±0.10 | 0.40 BSC | ---- | 0.20±0.05 | 2.40 REF |

NOTES:
 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
 2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
 3. WARPAGE SHALL NOT EXCEED 0.10 mm.
 4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
 5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
 6. "N" IS THE TOTAL NUMBER OF LEADS.
 7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
 8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

| | | | |
|--|----------------------|--------------|-------|
| DALLAS SEMICONDUCTOR | | MAXIM | |
| TITLE PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm | | | |
| APPROVAL | DOCUMENT CONTROL NO. | REV. | H 2/2 |
| | 21-0137 | | |

-DRAWING NOT TO SCALE-

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