

MAX2880

250MHz to 12.4GHz, High-Performance, Fractional/Integer-N PLL

General Description

The MAX2880 is a high-performance phase-locked loop (PLL) capable of operating in both integer-N and fractional-N modes. Combined with an external reference oscillator, loop filter, and VCO, the device forms an ultra-low noise and low-spur frequency synthesizer capable of accepting RF input frequencies of up to 12.4GHz.

The MAX2880 consists of a high-frequency and low-noise-phase frequency detector (PFD), precision charge pump, 10-bit programmable reference counter, 16-bit integer N counter, and 12-bit variable modulus fractional modulator.

The MAX2880 is controlled by a 3-wire serial interface and is compatible with 1.8V control logic. The device is available in a lead-free, RoHS-compliant, 4mm x 4mm, 20-pin TQFN package, and operates over an extended -40°C to +85°C temperature range.

Applications

- Microwave Point-to-Point Systems
- Wireless Infrastructure
- Satellite Communications
- Test and Measurement
- RF DAC and ADC Clocks

Benefits and Features

- Integer and Fractional-N Modes
- 250MHz to 12.4GHz Broadband RF Input
- Normalized In-Band Noise Floor
 - -229dBc/Hz in Integer Mode
 - -227dBc/Hz in Fractional Mode
- -10dBm to +5dBm Wide Input Sensitivity
- Low-Noise Phase Frequency Detector
 - 105MHz in Fractional Mode
 - 140MHz in Integer Mode
- Reference Frequency Up to 205MHz
- Operates from +3.0V to +3.6V Supply
- Cycle Slip Reduction and Fast Lock
- Software and Hardware Shutdown
- Software Lock Detect
- On-Chip Temperature Sensor
- Compatible with +1.8V Control Logic
- Phase Adjustment

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX2880.related.

Functional Diagram

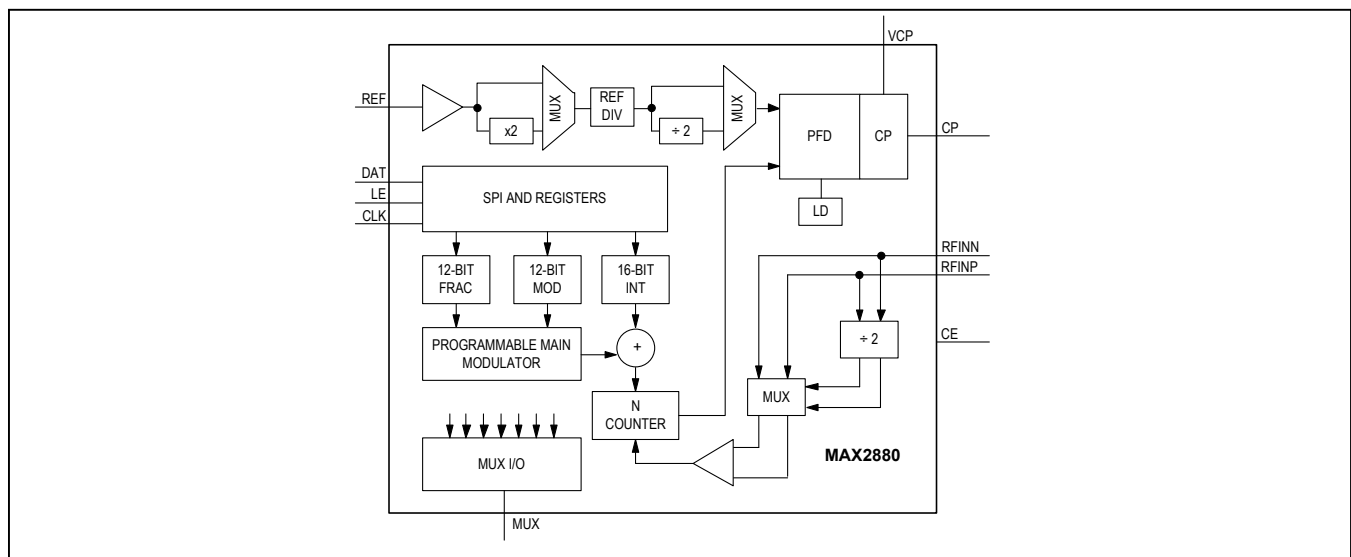


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Absolute Maximum Ratings

| | | | |
|---|------------------------------------|--|-----------------|
| V _{CC_} to GND_..... | -0.3V to +3.9V | Junction Temperature..... | +150°C |
| V _{CP} to GND_..... | -0.3V to +5.8V | Operating Temperature Range..... | -40°C to +85°C |
| CP to GND_..... | -0.3V to (V _{CP} + 0.3V) | Storage Temperature Range..... | -65°C to +150°C |
| All Other Pins to GND_..... | -0.3V to (V _{CC_} + 0.3V) | Lead Temperature (soldering, 10s)..... | +300°C |
| RFINP, RFINN..... | +10dBm | Soldering Temperature (reflow)..... | +260°C |
| Continuous Power Dissipation (T _A = +70°C) | | | |
| TQFN (derate 25.6mW/°C above +70°C)..... | 2051.3mW | | |

Package Thermal Characteristics (Note 1)

TQFN

| | | | |
|--|--------|---|-------|
| Junction-to-Ambient Thermal Resistance (θ _{JA})..... | 39°C/W | Junction-to-Case Thermal Resistance (θ _{JC})..... | 6°C/W |
|--|--------|---|-------|

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

(Measured using the MAX2880 Evaluation Kit. V_{CC_} = 3V to 3.6V, V_{CP} = V_{CC_} to 5.5V, V_{GND_} = 0V, f_{REF} = 50MHz, f_{PFD} = 50MHz, T_A = -40°C to +85°C. Typical values measured at V_{CC_} = 3.3V, V_{CP} = 5V, T_A = +25°C, no RF applied, Registers 0 through 4 settings: 303C0000, 00000009, 00008052, 00000BC3, 00000084, unless otherwise noted.) (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|------------------------|------------------|------|-----|-------|
| Supply Voltage (V _{CC_}) | | 3 | 3.3 | 3.6 | V |
| Charge-Pump Supply (V _{CP}) | | V _{CC_} | | 5.5 | V |
| V _{CC_} Supply Current | PRE = 0, RFINN = 6GHz | | 39 | 50 | mA |
| | PRE = 1, RFINN = 12GHz | | 49 | 59 | |
| | Shutdown Mode | | | 1 | |
| V _{CP} Supply Current | | | 0.65 | 2.0 | mA |

AC Electrical Characteristics

(Measured using the MAX2880 Evaluation Kit. V_{CC_} = 3V to 3.6V, V_{CP} = V_{CC_} to 5.5V, V_{GND_} = 0V, f_{REF} = 50MHz, f_{PFD} = 50MHz, f_{RFINN} = 6000MHz, T_A = -40°C to +85°C. Typical values measured at V_{CC_} = 3.3V, V_{CP} = 5V, T_A = +25°C, P_{RFINN} = 2dBm, Registers 0 through 4 settings: 303C0000, 00000009, 00008052, 00000BC3, 00000084, unless otherwise noted.) (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|---|-----|------|------------------|------------------|
| Input Frequency | | 250 | | 12,400 | MHz |
| Input Power | | -10 | | +5 | dBm |
| REF Input Frequency Range | | 10 | | 205 | MHz |
| REF Input Sensitivity | | 0.7 | | V _{CC_} | V _{P-P} |
| REF Input Capacitance | | | 2 | | pF |
| REF Input Current | | -60 | | +60 | µA |
| Phase Detector Frequency | Fractional mode | | | 105 | MHz |
| | Integer mode | | | 140 | |
| Sink/Source Current | CP[3:0] = 1111, R _{RSET} = 5.1kΩ | | 5.12 | | mA |
| | CP[3:0] = 0000, R _{RSET} = 5.1kΩ | | 0.32 | | |

AC Electrical Characteristics (continued)

(Measured using the MAX2880 Evaluation Kit. $V_{CC_} = 3V$ to $3.6V$, $V_{CP} = V_{CC_}$ to $5.5V$, $V_{GND_} = 0V$, $f_{REF} = 50MHz$, $f_{PFD} = 50MHz$, $f_{RFINN} = 6000MHz$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values measured at $V_{CC_} = 3.3V$, $V_{CP} = 5V$, $T_A = +25^{\circ}C$, $P_{RFINN} = 2dBm$, Registers 0 through 4 settings: 303C0000, 00000009, 00008052, 00000BC3, 00000084, unless otherwise noted.) (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|--|-----|----------------|-----|-------------|
| RSET Range | | 2.7 | | 10 | k Ω |
| Charge-Pump Output Voltage | | 0.5 | $V_{CP} - 0.5$ | | V |
| In-Band Noise Floor | Normalized (Note 3) | | -229 | | dBc/Hz |
| 1/f Noise | Normalized (Note 4) | | -122 | | dBc/Hz |
| In-Band Phase Noise | (Note 5) | | -101 | | dBc/Hz |
| Integrated RMS Jitter | (Note 6) | | 0.14 | | ps |
| Spurious Signals Due to PFD | | | -84 | | dBc |
| ADC Resolution | | | 7 | | Bits |
| Temperature Sensor Accuracy | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ | | ± 2.0 | | $^{\circ}C$ |

Digital I/O Characteristics

($V_{CC_} = 3V$ to $3.6V$, $V_{GND_} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values at $V_{CC_} = 3.3V$, $T_A = +25^{\circ}C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|-----------------|----------------------|------------------|-----|-----|---------|
| Input Logic-Level Low | V_{IL} | | | 0.4 | | V |
| Input Logic-Level High | V_{IH} | | | 1.5 | | V |
| Input Current | I_{IH}/I_{IL} | | -1 | | +1 | μA |
| Input Capacitance | | | | 1 | | pF |
| Output Logic-Level Low | V_{OL} | 0.3mA sink current | | | 0.4 | V |
| Output Logic-Level High | V_{OH} | 0.3mA source current | $V_{CC_} - 0.4$ | | | V |
| Output Current Level High | I_{OH} | | | 0.5 | | mA |

SPI Timing Characteristics

($V_{CC_} = 3V$ to $3.6V$, $V_{GND_} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$. Typical values at $V_{CC_} = 3.3V$, $T_A = +25^{\circ}C$.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|-----------|--|-----|-----|-----|-------|
| CLK Clock Period | t_{CP} | Guaranteed by SCL pulse-width low and high | | 50 | | ns |
| CLK Pulse-Width Low | t_{CL} | | | 25 | | ns |
| CLK Pulse-Width High | t_{CH} | | | 25 | | ns |
| LE Setup Time | t_{LES} | | | 20 | | ns |
| LE Hold Time | t_{LEH} | | | 10 | | ns |
| LE Minimum Pulse-Width High | t_{LEW} | | | 20 | | ns |
| Data Setup Time | t_{DS} | | | 25 | | ns |
| Data Hold Time | t_{DH} | | | 25 | | ns |
| MUX Setup Time | t_{MS} | | | 10 | | ns |
| MUX Hold Time | t_{MH} | | | 10 | | ns |

Note 2: Production tested at $T_A = +25^{\circ}C$. Cold and hot are guaranteed by design and characterization.

Note 3: Measured at 100kHz offset with 50MHz Bliley NV108C1954 OCVCXO with 500kHz loop bandwidth. Registers 0 through 4 settings: 303C0000, 00000009, 0F008052, 000025C3, 00000094.

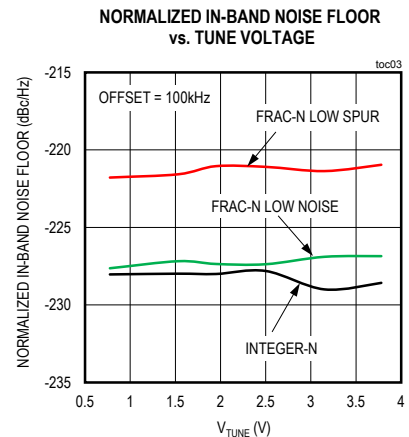
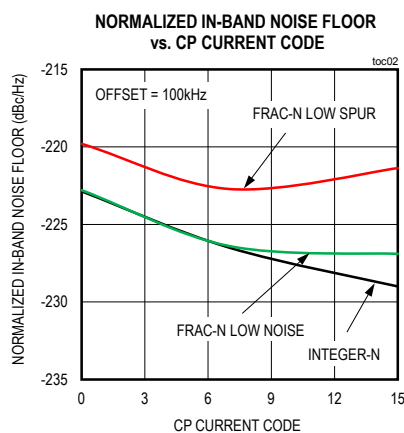
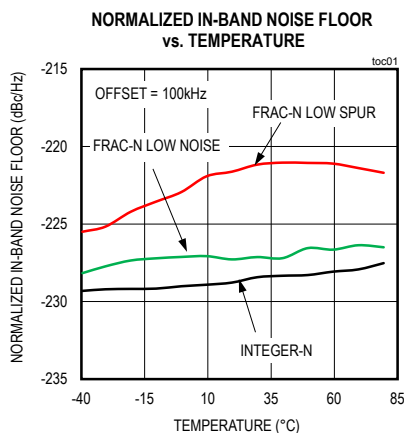
Note 4: $1/f$ noise contribution to the in-band noise is computed by using $1/f_{NOISE} = PN - 10\log(10kHz/f_{OFFSET}) - 20\log(f_{RF}/1GHz)$. Registers 0 through 4 settings: 303C0000, 00000009, 0F008052, 000025C3, 00000094.

Note 5: $f_{REF} = 50MHz$; $f_{PFD} = 50MHz$; offset frequency = 10kHz; VCO frequency = 6GHz, $N = 120$; loop BW = 100kHz, CP[3:0] = 1111; integer mode. Registers 0 through 4 settings 303C0000, 00000009, 0F008052, 000025C3, 00000094.

Note 6: $f_{REF} = 50MHz$; $f_{PFD} = 50MHz$; VCO frequency = 6GHz; $N = 120$; loop BW = 100kHz, CP[3:0] = 1111; integer mode. Registers 0 through 4 settings 303C0000, 00000009, 0F008052, 000025C3, 00000094.

Typical Operating Characteristics

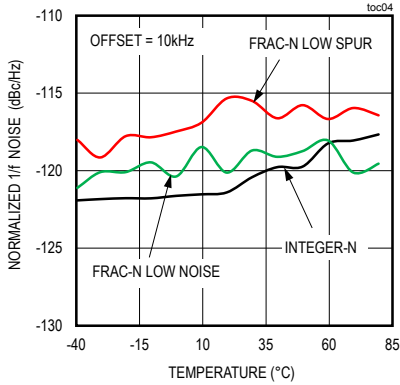
(Measured using the MAX2880 Evaluation Kit. $V_{CC_} = 3.3V$, $V_{GND_} = 0V$, $V_{CP} = 5.0V$, CP[3:0]= 1111, $f_{RFIN} = 6GHz$, $f_{REF} = 50MHz$, $f_{PFD} = 50MHz$, $T_A = +25^{\circ}C$, unless otherwise noted. See [Table 1](#) and [Table 2](#)).



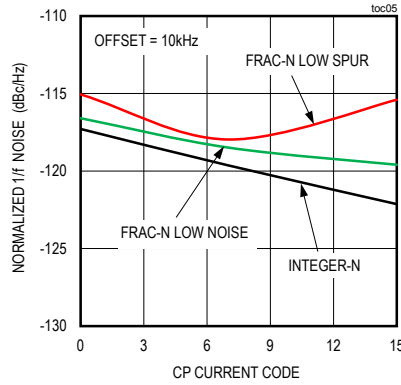
Typical Operating Characteristics (continued)

(Measured using the MAX2880 Evaluation Kit. $V_{CC-} = 3.3V$, $V_{GND-} = 0V$, $V_{CP} = 5.0V$, $CP[3:0] = 1111$, $f_{RFIN} = 6GHz$, $f_{REF} = 50MHz$, $f_{PFD} = 50MHz$, $T_A = +25^\circ C$, unless otherwise noted. See [Table 1](#) and [Table 2](#)).

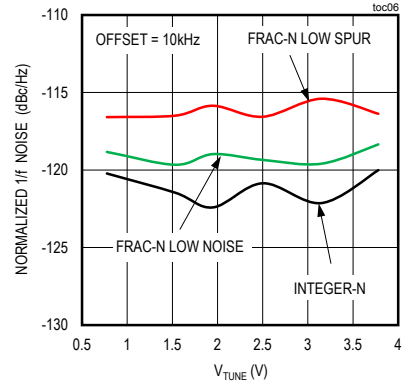
NORMALIZED 1/f NOISE vs. TEMPERATURE



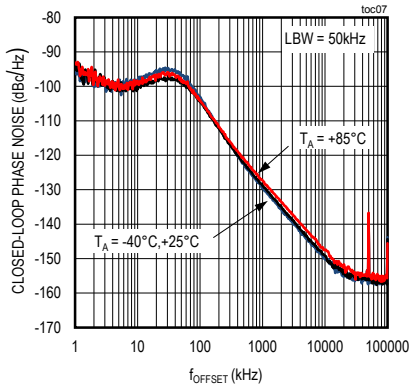
NORMALIZED 1/f NOISE vs. CP CURRENT CODE



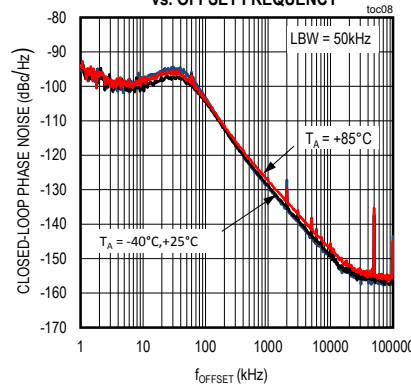
NORMALIZED 1/f NOISE vs. TUNE VOLTAGE



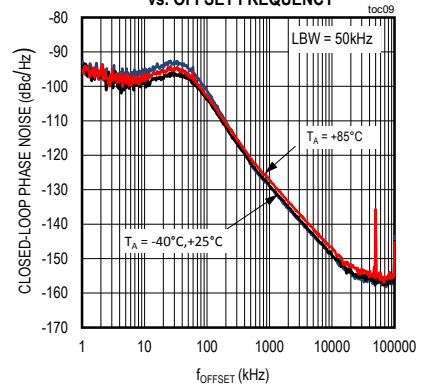
INTEGER-N CLOSED-LOOP PHASE NOISE vs. OFFSET FREQUENCY



FRAC-N LOW-NOISE MODE CLOSED-LOOP PHASE NOISE vs. OFFSET FREQUENCY



FRAC-N LOW-SPUR MODE CLOSED-LOOP PHASE NOISE vs. OFFSET FREQUENCY



RF INPUT SENSITIVITY vs. FREQUENCY

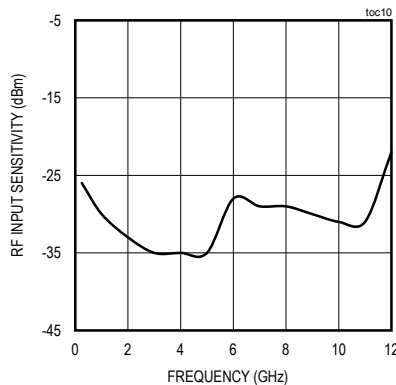


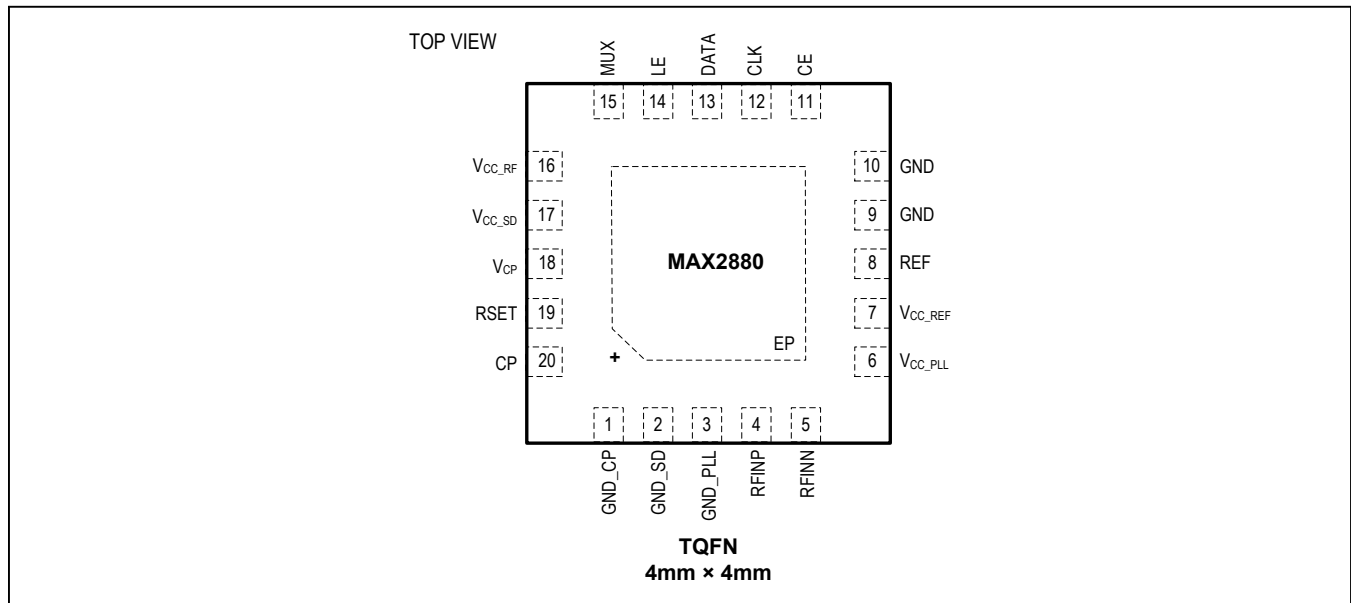
Table 1. Typical Operating Characteristics Testing Conditions

| TOC | MODE | REG 0 (hex) | REG 1 (hex) | REG 2 (hex) | REG 3 (hex) | REG 4 (hex) | COMMENTS |
|-----|------------------|-------------|-------------|-------------|-------------|-------------|-----------------------------|
| 1 | INTEGER N | 303C0000 | 04000001 | 2F00FFFA | 00000543 | 00000004 | LBW = 500kHz |
| | FRAC N LOW SPUR | 303C00A0 | 04000001 | 6F008C82 | 00000B43 | 00000004 | |
| | FRAC N LOW NOISE | 303C00A0 | 04000001 | 0F008C82 | 00000343 | 00000004 | |
| 2 | INTEGER N | 303C0000 | 04000001 | 2F00FFFA | 00000543 | 00000004 | LBW = 500kHz |
| | FRAC N LOW SPUR | 303C00A0 | 04000001 | 6F008C82 | 00000B43 | 00000004 | |
| | FRAC N LOW NOISE | 303C00A0 | 04000001 | 0F008C82 | 00000343 | 00000004 | |
| 3 | INTEGER N | 303C0000 | 04000001 | 2F00FFFA | 00000543 | 00000004 | LBW = 500kHz |
| | FRAC N LOW SPUR | 303C00A0 | 04000001 | 6F008C82 | 00000B43 | 00000004 | |
| | FRAC N LOW NOISE | 303C00A0 | 04000001 | 0F008C82 | 00000343 | 00000004 | |
| 4 | INTEGER N | 303C0000 | 04000001 | 2F00FFFA | 00000543 | 00000004 | LBW = 500kHz |
| | FRAC N LOW SPUR | 303C00A0 | 04000001 | 6F008C82 | 00000B43 | 00000004 | |
| | FRAC N LOW NOISE | 303C00A0 | 04000001 | 0F008C82 | 00000343 | 00000004 | |
| 5 | INTEGER N | 303C0000 | 04000001 | 2F00FFFA | 00000543 | 00000004 | LBW = 500kHz |
| | FRAC N LOW SPUR | 303C00A0 | 04000001 | 6F008C82 | 00000B43 | 00000004 | |
| | FRAC N LOW NOISE | 303C00A0 | 04000001 | 0F008C82 | 00000343 | 00000004 | |
| 6 | INTEGER N | 303C0000 | 04000001 | 2F00FFFA | 00000543 | 00000004 | LBW = 500kHz |
| | FRAC N LOW SPUR | 303C00A0 | 04000001 | 6F008C82 | 00000B43 | 00000004 | |
| | FRAC N LOW NOISE | 303C00A0 | 04000001 | 0F008C82 | 00000343 | 00000004 | |
| 7 | INTEGER N | 303C0000 | 04000001 | 2F00FFFA | 00000543 | 00000004 | LBW = 50kHz |
| 8 | FRAC N LOW NOISE | 303C00A0 | 04000001 | 0F008C82 | 00000343 | 00000004 | LBW = 50kHz |
| 9 | FRAC N LOW SPUR | 303C00A0 | 04000001 | 6F008C82 | 00000B43 | 00000004 | LBW = 50kHz |
| 10 | INTEGER N | 303C0000 | 04000001 | 2F00FFFA | 00000543 | 00000004 | $f_{RF} < 6.2\text{GHz}$ |
| | INTEGER N | 303C0000 | 06000001 | 2F00FFFA | 00000543 | 00000004 | $f_{RF} \geq 6.2\text{GHz}$ |

Table 2. Loop Filter Component

| LOOP BW (kHz) | K_{VCO} (MHz/V) | CP CODE | f_{REF} (MHz) | f_{PFD} (MHz) | MAX2880 EVALUATION KIT COMPONENT VALUES | | | | |
|---------------|-------------------|---------|-----------------|-----------------|---|-------------|---------------|---------------|--------|
| | | | | | C14 | C13 | R10 | R33 | C15 |
| 50 | 85 | 1111 | 50 | 50 | 10nF | 100nF | 100 Ω | 47.5 Ω | 1000pF |
| 100 | 85 | 1111 | 50 | 50 | 680pF | 0.1 μ F | 174 Ω | 100 Ω | 18pF |
| 500 | 85 | 0001 | 50 | 50 | Open | 330pF | 15k Ω | 0 Ω | Open |
| 500 | 85 | 0111 | 50 | 50 | 12pF | 2200pF | 1820 Ω | 100 Ω | 18pF |
| 500 | 85 | 1111 | 50 | 50 | 33pF | 4700pF | 910 Ω | 100 Ω | 18pF |

Pin Configuration



Pin Description

| PIN | NAME | FUNCTION |
|-------|---------|--|
| 1 | GND_CP | Charge-Pump Ground. Connect to board ground, not to the paddle. |
| 2 | GND_SD | Sigma Delta Modulator Ground. Connect to board ground, not to the paddle. |
| 3 | GND_PLL | PLL Ground. Connect to board ground, not to the paddle. |
| 4 | RFINP | Positive RF Input to Prescaler. AC ground through capacitor, if not used. |
| 5 | RFINN | Negative RF Input to Prescaler. Connect to VCO output through coupling capacitor. |
| 6 | VCC_PLL | PLL Power Supply. Place decoupling capacitors as close as possible to pin. |
| 7 | VCC_REF | REF Power Supply. Place decoupling capacitors as close as possible to pin. |
| 8 | REF | Reference Frequency Input. This is a high-impedance input with a nominal bias voltage of $V_{CC_REF}/2$. AC-couple to reference signal. |
| 9, 10 | GND | Ground. Connect to the board ground, not the paddle. |
| 11 | CE | Chip Enable. A logic-low powers the device down. |
| 12 | CLK | Serial Clock Input. The data is latched into the 32-bit shift register on the rising edge of the CLK line. |
| 13 | DATA | Serial Data Input. The serial data is loaded MSB first. The 3 LSBs identify the register address. |
| 14 | LE | Load Enable Input. When LE goes high the data stored in the shift register is loaded into the appropriate register. |
| 15 | MUX | Multiplexed I/O. See Table 5 . |
| 16 | VCC_RF | RF Power Supply. Place decoupling capacitors as close as possible to pin. |
| 17 | VCC_SD | Sigma Delta Modulator Power Supply. Place decoupling capacitors as close as possible to pin. |
| 18 | VCP | Charge-Pump Power Supply. Place decoupling capacitors as close as possible to the pin. |
| 19 | RSET | Charge-Pump Current Range Input. Connect an external resistor to ground to set the minimum CP current. $I_{CP} = 1.63/R_{SET} \times (1 + CP)$. |
| 20 | CP | Charge-Pump Output. Connect to external loop filter input. |
| — | EP | Exposed Pad. Connect to board ground. |

Detailed Description

4-Wire Serial Interface

The MAX2880 serial interface contains five read-write and one read-only 32-bit registers. The 29 most-significant bits (MSBs) are data, and the three least-significant bits (LSBs) are the register address. Register data is loaded MSB first through the 4-wire serial port interface (SPI). When latch enable (LE) is logic-low, the logic level at DATA is shifted at the rising edge of CLK. At the rising edge of LE, the 29 data bits are latched into the register selected by the address bits. Default values are not guaranteed upon power-up. Program all register values after power-up.

Register programming order should be address 0x04, 0x03, 0x02, 0x01, and 0x00. Several bits are double buffered to update the settings at the same time. See the register descriptions for double buffered settings.

Any register can be read back through the MUX pin. The user must first set MUX bits = 0111. Next, write the register to be read, but with the READ bit of that register (the MSB) = 1. If the READ bit is set, the data of bits 30:3 do not matter because they are not latched into the register on a read operation. After the address bits are clocked and the LE pin is set, the MSB of that register appears on the MUX pin after the next rising edge on CLK pin. The MUX pin will continue to change after the rising edge of the next 28 clocks. After the LSB has been read, the user can reset the MUX bits to 0000.

Shutdown Mode

The MAX2880 can be put into shutdown mode by setting SHDN = 1 (register 3, bit 5) or by setting the CE pin to logic-low.

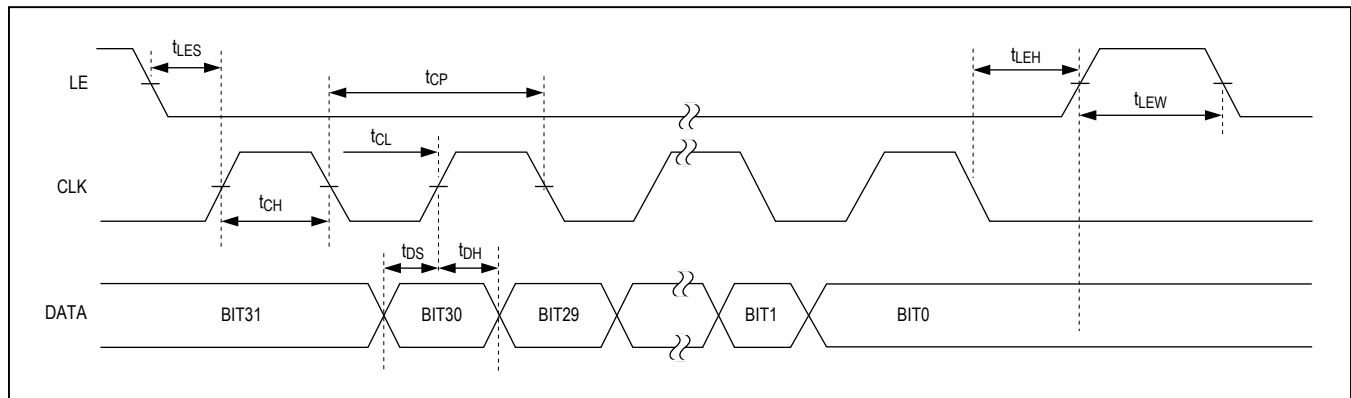


Figure 1. SPI Timing Diagram

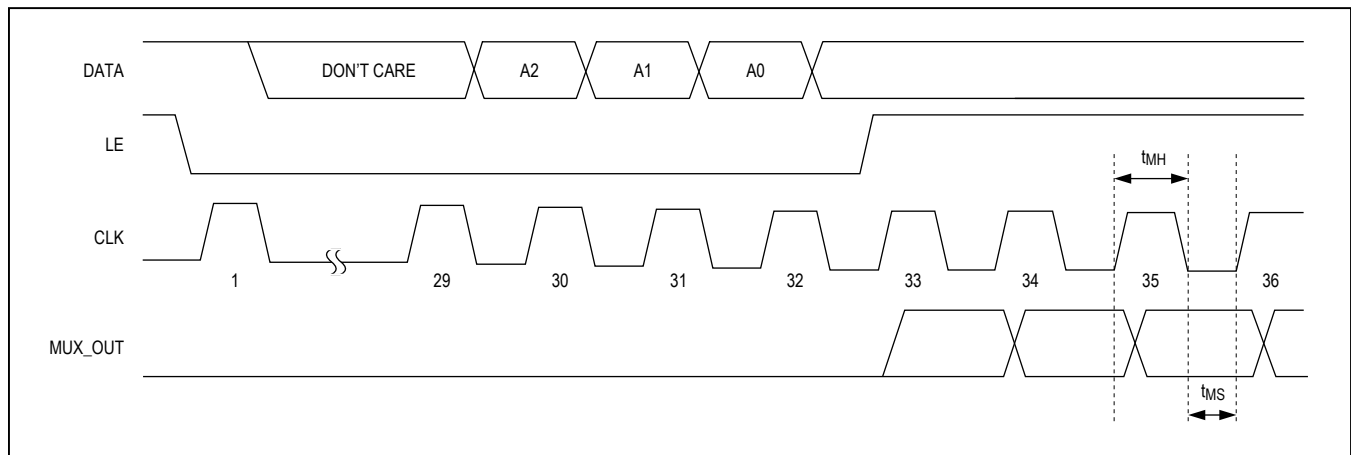


Figure 2. Initiating Readback

Reference Input

The reference input stage is configured as a CMOS inverter with shunt resistance from input to output. In shut-down mode this input is set to high impedance to prevent loading of the reference source.

The reference input signal path also includes optional x2 and ÷2 blocks. When the reference doubler is enabled (DBR = 1), the maximum reference input frequency is limited to 100MHz. When the doubler is disabled, the reference input frequency is limited to 205MHz. The minimum reference frequency is 10MHz. The minimum R counter divide ratio is 1, and the maximum divide ratio is 1023.

Int, Frac, Mod, and R Counter Relationship

The phase-detector frequency is determined as follows:

$$f_{\text{PFD}} = f_{\text{REF}} \times [(1 + \text{DBR}) / (\text{R} \times (1 + \text{RDIV2}))]$$

f_{REF} represents the external reference input frequency. DBR (register 2, bit 20) sets the f_{REF} input frequency doubler mode (0 or 1). RDIV2 (register 2, bit 21) sets the f_{REF} divide-by-2 mode (0 or 1). R (register 2, bits 19:15) is the value of the 5-bit programmable reference counter (1 to 31). The maximum f_{PFD} is 105MHz for Fractional-N and 140MHz for Integer-N. The R-divider can be held in reset when RST (register 3, bit 3) = 1.

The VCO frequency is determined as follows:

$$f_{\text{VCO}} = f_{\text{PFD}} \times (\text{N} + \text{F}/\text{M}) \times (\text{PRE} + 1)$$

N is the value of the 16-bit N counter (16 to 65535), programmable through bits 30:27 (MSBs) of register 1 and bits 26:15 of register 0 (LSBs). M is the fractional modulus value (2 to 4095), programmable through bits 14:3 of register 2. F is the fractional division value (0 to MOD - 1), programmable through bits 14:3 of register 0. In fractional-N mode, the minimum N value is 19 and maximum N value is 4091. The N counter is held in reset when RST = 1 (register 3, bit 3). PRE is RF input prescaler control where 0 = divide-by-1, and 1 = divide-by-2 (register 1, bit 25). If the RF input frequency is above 6.2GHz, then set PRE = 1.

Integer-N/Fractional-N Modes

Integer-N mode is selected by setting bit INT = 1 (register 3, bit 10). When operating in integer-N mode, it is also necessary to set bit Lock Detect Function, LDF = 1 (register 3, bit 9) to set the lock detect to integer-N mode.

The device's fractional-N mode is selected by setting bit INT = 0 (register 3, bit 10). Additionally, set bit LDF = 0 (register 3, bit 9) for fractional-N lock-detect mode.

If the device is in fractional-N mode, it will remain in fractional-N mode when fractional division value F = 0, which can result in unwanted spurs. To avoid this condition, the device can automatically switch to integer-N mode when F = 0 if the bit F01 = 1 (register 4, bit 29).

Phase Detector and Charge Pump

The device's charge-pump current is determined by the value of the resistor from pin RSET to ground and the value of bits CP (register 2, bits 27:24) as follows:

$$I_{\text{CP}} = 1.63/\text{R}_{\text{SET}} \times (1 + \text{CP})$$

When operating in the fractional-N mode, the charge-pump linearity (CPL) bits can be adjusted by the user to optimize in-band noise and spur levels. In the integer-N mode, CPL must be set to 0. If lower noise operation in integer-N mode is desired, set the charge-pump output clamp bit CPOC = 1 (register 3, bit 13) to prevent leakage current into the loop filter. In fractional-N mode, set CPOC = 0..

The charge-pump output can be put into high-impedance mode when TRI = 1 (register 3, bit 4). The output is in normal mode when TRI = 0.

The phase detector polarity can be changed if an active inverting loop filter topology is used. For noninverting loop filters, set PDP = 1 (register 3, bit 6). For inverting loop filters, set PDP = 0.

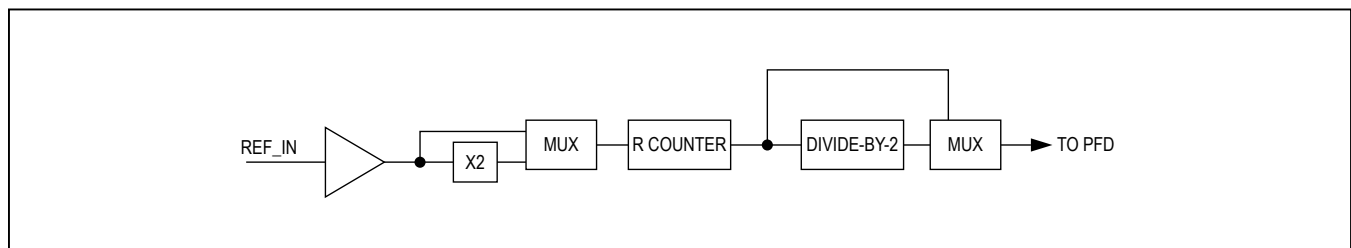


Figure 3. Reference Input

MUX and Lock Detect

MUX is a multipurpose test output for observing various internal functions of the MAX2880. MUX can also be configured as serial data output. MUX bits (register 0, bits 30:27) are used to select the desired MUX signal (see [Table 5](#)).

The digital lock detect is dependent on the mode of the synthesizer. In fractional-N mode set LDF = 0, and in integer-N mode set LDF = 1. To set the accuracy of the digital lock detect, see [Table 3](#) and [Table 4](#).

Cycle Slip Reduction

Cycle slip reduction is one of two available methods to improve lock time. It is enabled by setting CSR bit (register 2, bit 28) to 1. In this mode, the charge pump must be set for its minimum value.

Fast-Lock

Fast-lock is the other method available for improving lock time by temporarily increasing the loop bandwidth at the start of the locking cycle. It is enabled by setting the CDM bits to 01 (register 4, bits 20:19). In addition, the charge-pump current has to be set to CP = 0000 (register 2, bits 27:24), MUX bits configured to 1100 (register 0, bits 30:27), and the shunt resistive portion of the loop filter has to be segmented into two parts, where one resistor is 1/4 of the total resistance, and the other resistor is 3/4 of the total resistance. [Figure 4](#) and [Figure 5](#) illustrate the two

possible topologies. Once enabled, fast lock is activated after writing to register 0. During this process, the charge pump is automatically increased to its maximum (CP bits = 1111) and the shunt loop filter resistance is reduced to 1/4 of the total resistance when the internal switch shorts the MUX pin to ground. Bits CDIV (register 4, bits 18:7) control the time spent in the wide bandwidth mode. The time spent in the fast lock is:

$$t = \text{CDIV}/f_{\text{PFD}}$$

The time should be set long enough to allow the loop to settle before switching back to the lower loop bandwidth.

RF Inputs

The differential RF inputs are connected to a high-impedance input buffer which drives a demultiplexer for selecting between two RF input frequency ranges: 250MHz to 6.2GHz and 6.2GHz to 12.4GHz. When the RF input frequency is 250MHz to 6.2GHz, the fixed divide-by-2 prescaler is bypassed by setting bit PRE to 0. When the RF input frequency is 6.2GHz to 12.4GHz, the fixed divide-by-2 path is selected by setting PRE to 1. The supported input power range is -10dBm to +5dBm. For single-ended operation, terminate the unused RF input to GND through a 100pF capacitor.

Since the RF input of the device is high impedance, a DC isolated external shunt resistor is used to provide the 50Ω input impedance for the system (see the [Typical Application Circuit](#)).

Table 3. Fractional-N Digital Lock-Detect Settings

| PFD FREQUENCY (MHz) | LDS | LDP | LOCKED UP/DOWN TIME SKEW (ns) | NUMBER OF LOCKED CYCLES TO SET LD | TIME SKEW TO UNSET LD (ns) |
|---------------------|-----|-----|-------------------------------|-----------------------------------|----------------------------|
| ≤ 32 | 0 | 0 | 10 | 40 | 15 |
| ≤ 32 | 0 | 1 | 6 | 40 | 15 |
| > 32 | 1 | X | 4 | 40 | 4 |

Table 4. Integer-N Digital Lock-Detect Settings

| PFD FREQUENCY (MHz) | LDS | LDP | LOCKED UP/DOWN TIME SKEW (ns) | NUMBER OF LOCKED CYCLES TO SET LD | TIME SKEW TO UNSET LD (ns) |
|---------------------|-----|-----|-------------------------------|-----------------------------------|----------------------------|
| ≤ 32 | 0 | 0 | 10 | 5 | 15 |
| ≤ 32 | 0 | 1 | 6 | 5 | 15 |
| > 32 | 1 | X | 4 | 5 | 4 |

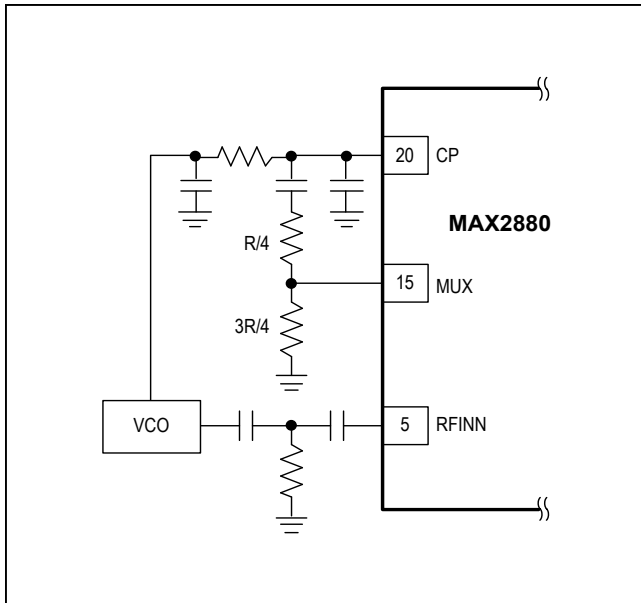


Figure 4. Fast-Lock Loop Filter Topology 1

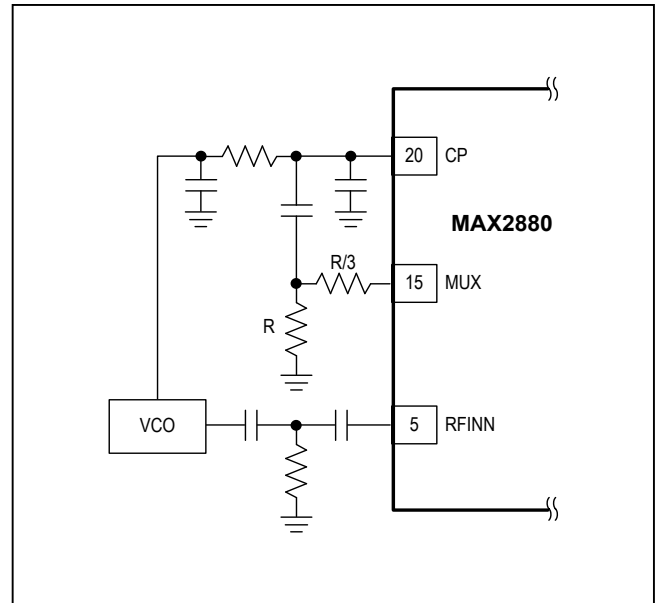


Figure 5. Fast-Lock Loop Filter Topology 2

Phase Adjustment

After achieving lock, the phase of the RF output can be changed in increments of P (register 1, bits 14:3)/ M (register 2, bits 14:3) $\times 360^\circ$.

When aligning the phase of multiple devices, connect their MUX pins together and do the following:

- 1) Force the voltage on the MUX pins to V_{IL} .
- 2) Set MUX = 1000.
- 3) Program the MAX2880s for the desired frequency and allow them to lock.
- 4) Force the voltage on the MUX pins to V_{IH} . This resets the MAX2880s so they are synchronous.
- 5) Set P (register 1, bits 14:3) for the desired amount of phase shift for each part.
- 6) Set CDM bits (register 4, bits 20:19) = 10. This enables the phase shift.
- 7) Reset CDM = 00.

Fractional Modes

The MAX2880 offers three modes for the sigma-delta modulator. Low noise mode offers lower in-band noise at the expense of spurs, and the low-spur modes offer lower spurs at the expense of noise. To operate in low noise

mode, set SDN bits to 00 (register 2, bits 30:29). In the low-spur mode, choose between two possible dithering modes (SDN = 10 or 11) for the optimal spur performance.

Temperature Sensor

The device is equipped with an on-chip temperature sensor and 7-bit ADC.

To read the digitized output of the temperature sensor:

- 1) Set CDM = 11 to enable the ADC clock.
- 2) Set $CDIV = f_{PFD}/100kHz$. If the result is not an integer, then round down to the nearest integer.
- 3) Set ADCM (register 4, bits 6:4) = 001 for temperature sensor mode.
- 4) Set ADCS (register 4, bit 3) = 1 to start the ADC.
- 5) Wait at least 100 μs for the ADC to convert the temperature.
- 6) Set MUX = 0111 to read the temperature out of the MUX pin.
- 7) Read back register 6. Bits 9:3 are the ADC digitized value.

The temperature can be converted as:

$$t = -1.8 \times ADC + 129^\circ C$$

Register and Bit Descriptions

The operating mode of the MAX2880 is controlled via 5 read/write on-chip registers and 1 read-only register.

Defaults are not guaranteed upon power-up and are provided for reference only. All reserved bits should only be written with default values. In shutdown mode, the register values are retained.

Table 5. Register 0 (Address: 000, Default: 383C0000 Hex)

| BIT LOCATION | BIT ID | NAME | DEFINITION |
|--------------|-----------|---------------------------|---|
| 31 | READ | READ | 0 = Write to register 1 = Read from register |
| 30:27 | MUX[3:0] | MUX Mode | Sets MUX Pin Configuration 0000 = High-Impedance Output 0001 = D_VDD 0010 = D_GND 0011 = R Divider Output 0100 = N Divider Output 0101 = Analog Lock Detect 0110 = Digital Lock Detect 0111 = SPI Output 1000 = SYNC input 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Fast Lock 1101 = R Divider/2 1110 = N Divider/2 1111 = Reserved |
| 26:15 | N[11:0] | Integer Division Value | Sets integer part (N divider) of the feedback divider factor. MSBs are located in register 1. All integer values from 16 to 65,535 are allowed for integer mode. Integer values from 19 to 4091 are allowed for fractional mode. |
| 14:3 | F[11:0] | Fractional Division Value | Sets Fractional Value. Allowed F values are 0 to M-1. 000000000000 = 0 (see F01 bit description) 000000000001 = 1 ---- 111111111110 = 4094 111111111111 = 4095 |
| 2:0 | ADDR[2:0] | Address Bits | Register address bits |

Table 6. Register 1 (Address: 001, Default: 00000001 Hex)

| BIT LOCATION | BIT ID | NAME | DEFINITION |
|--------------|-----------|------------------------|--|
| 31 | READ | Register Read | 0 = Write to register 1 = Read from register |
| 30:27 | N[15:12] | Integer Division Value | Sets Integer part (N divider) of the feedback divider factor. LSBs are located in register 0. All integer values from 16 to 65,535 are allowed for integer mode. Integer values from 19 to 4091 are allowed for fractional mode. |
| 26 | Unused | Unused | Set to 0 |
| 25 | PRE | RF Input Prescaler | Sets RF Input prescaler to divide-by-1 or divide-by-2 0 = Divide-by-1 (250MHz to 6.2GHz) 1 = Divide-by-2 (6.2GHz to 12.4GHz) |
| 24:20 | Unused | Unused | Set to all 0's. |
| 19:15* | R[9:5] | Reference Divider Mode | Sets Reference Divide Value (R). LSBs located in register 2. 0000000000 = 0 (Unused) 0000000001 = 1 ----- 1111111111 = 1023 |
| 14:3 | P[11:0] | Phase Value | Sets Phase Value. See the Phase Adjustment section 000000000000 = 0 000000000001 = 1 ----- 111111111111 = 4095 |
| 2:0 | ADDR[2:0] | Address Bits | Register address bits |

*Bits double buffered by Register 0.

Table 7. Register 2 (Address: 010, Default: 0000FFFA Hex)

| BIT LOCATION | BIT ID | NAME | DEFINITION |
|--------------|----------|----------------------|---|
| 31 | READ | Register Read | 0 = Write to register 1 = Read from register |
| 30:29 | SDN[1:0] | Fractional-N Modes | Sets Noise Mode (see the Fractional Modes section under the Detailed Description): 00 = Low-Noise Mode 01 = Reserved 10 = Low-Spur Mode 1 11 = Low-Spur Mode 2 |
| 28 | CSR | Cycle Slip Reduction | 0 = Cycle Slip Reduction disabled 1 = Cycle Slip Reduction enabled |

Table 7. Register 2 (Address: 010, Default: 0000FFFA Hex) (continued)

| BIT LOCATION | BIT ID | NAME | DEFINITION |
|--------------|---------|------------------------|---|
| 27:24 | CP[3:0] | Charge-Pump Current | Sets Charge-Pump Current [[ICP = 1.63/RSET x (1 + CP[3:0])]] |
| 23:22 | Unused | Unused | Factory Use Only, set to 00. |
| 21* | RDIV2 | Reference Div2 Mode | Sets Reference Divider Mode 0 = Disable reference divide by 2 1 = Enable reference divide by 2 |
| 20* | DBR | Reference Doubler Mode | Sets Reference Doubler Mode 0 = Disable reference doubler 1 = Enable reference doubler |
| 19:15* | R[4:0] | Reference Divider Mode | Sets Reference Divide Value (R). Double buffered by Register 0. MSBs located in register 1. 0000000000 = 0 (Unused) 0000000001 = 1 ----- 1111111111 = 1023 |
| 14:3* | M[11:0] | Modulus Value | Fractional Modulus value used to program f_{VCO} . See the Int, Frac, Mod, and R Counter Relationship section. Double buffered by register 0. 000000000000 = Unused 000000000001 = Unused 000000000010 = 2 ----- 111111111111 = 4095 |
| 2:0 | ADDR | Address Bits | Register address |

*Bits double buffered by Register 0.

Table 8. Register 3 (Address: 011, Default: 00000043 Hex)

| BIT LOCATION | BIT ID | NAME | DEFINITION |
|--------------|----------|-------------------|---|
| 31 | READ | Register Read | 0 = Write to register 1 = Read from register |
| 30:18 | Unused | Unused | Write to all 0's |
| 17 | F01 | F01 | Sets integer mode for F = 0. 0 = If F[11:0] = 0, then fractional-N mode is set 1 = If F[11:0] = 0, then integer-N mode is auto set |
| 16:15 | CPT[1:0] | Charge-Pump Test | Sets Charge-Pump Test Modes 00 = Normal mode 01 = Reserved 10 = Force CP into source mode 11 = Force CP into Sink mode |
| 14 | RSTSD | Sigma Delta Reset | 0 = Reset Sigma Delta Modulator to known value after each write to register 0 1 = Do not reset Sigma Delta Modulator to known value after each write to register 0 |

Table 8. Register 3 (Address: 011, Default: 0000043 Hex) (continued)

| BIT LOCATION | BIT ID | NAME | DEFINITION |
|--------------|-----------|---------------------------------|---|
| 13 | CPOC | CP Output Clamp | Sets Charge-Pump Output Clamp Mode 0 = Disables clamping of the CP output when the CP is off. 1 = Enables the clamping of the CP output when the CP is off (improved integer-N in-band phase noise). |
| 12:11 | CPL[1:0] | CP Linearity | Sets CP Linearity Mode 00 = Disables the CP linearity mode (integer-N mode). 01 = Enables the CP linearity mode (Fractional-N mode) 10 = Enables the CP linearity mode (Fractional-N mode) 11 = Enables the CP linearity mode (Fractional-N mode) |
| 10 | INT | Integer Mode | Controls Synthesizer Integer or Fractional-N Mode 0 = Fractional-N mode 1 = Integer mode |
| 9 | LDF | Lock Detect Function | Sets Lock Detect Function 0 = Fractional-N lock detect 1 = Integer-N lock detect |
| 8 | LDS | Lock Detect Speed | Lock Detect Speed Adjustment 0 = $f_{PFD} \leq 32\text{MHz}$ 1 = $f_{PFD} > 32\text{MHz}$ |
| 7 | LDP | Lock Detect Precision | Sets Lock Detect Precision 0 = 10ns 1 = 6ns |
| 6 | PDP | Phase Detector Polarity | Sets Phase Detector Polarity 0 = Negative (for use with inverting active loop filters) 1 = Positive (for use with passive loop filers and noninverting active loop filters) |
| 5 | SHDN | Shutdown Mode | Sets Power-Down Mode 0 = Normal mode 1 = Device shutdown |
| 4 | TRI | Charge-Pump High-Impedance Mode | Sets Charge-Pump High-Impedance Mode 0 = Disabled 1 = Enabled |
| 3 | RST | Counter Reset | Sets Counter Reset Mode 0 = Normal operation 1 = R and N counters reset |
| 2:0 | ADDR[2:0] | Address Bits | Register address |

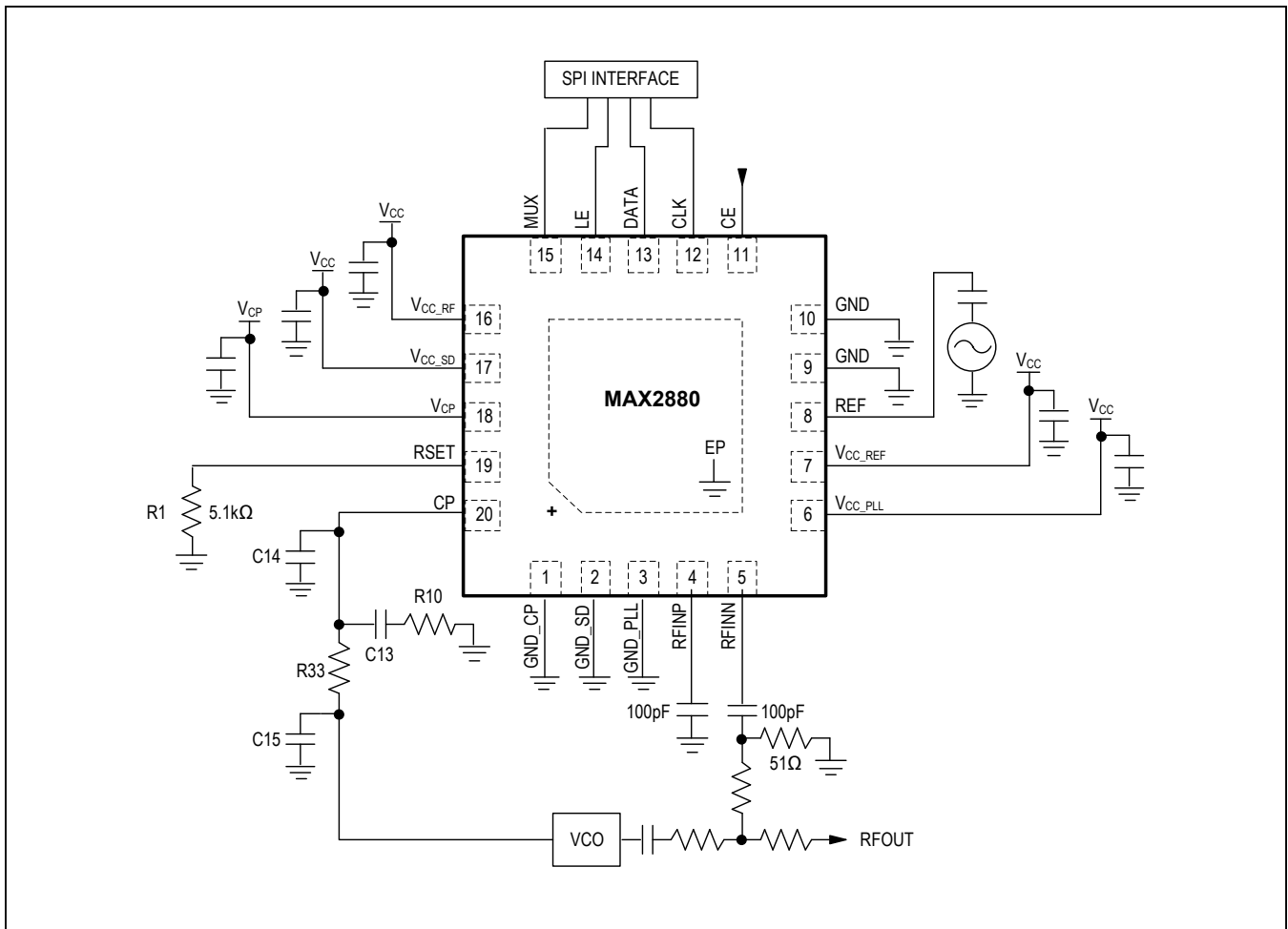
Table 9. Register 4 (Address: 100, Default: 00000004 Hex)

| BIT LOCATION | BIT ID | NAME | DEFINITION |
|--------------|------------|---------------------|--|
| 31 | READ | Register Read | 0 = Write to register 1 = Read from register |
| 30:22 | Unused | Unused | Write to all 0's |
| 21 | SDREF | Shutdown Reference | Shutdown Reference Stage 0 = Reference stage enabled 1 = Reference stage disabled |
| 20:19 | CDM[1:0] | Clock-Divider Mode | Sets Clock-Divider Mode 00 = Clock divider off 01 = Fast-lock enabled 10 = Phase adjustment 11 = ADC clock |
| 18:7 | CDIV[11:0] | Clock-Divider Value | Sets 12-Bit Clock-Divider Value 000000000000 = Unused 000000000001 = 1 000000000010 = 2 ----- 111111111111 = 4095 |

Table 10. Register 6 (Read-Only Register)

| BIT LOCATION | BIT ID | NAME | DEFINITION |
|--------------|-----------|------------------|--|
| 31 | READ | READ | 0 = N/A 1 = Read from register |
| 30:13 | Unused | Unused | |
| 11 | POR | Power on Reset | POR Readback Status 0 = POR has been read back 1 = POR has not been read back (registers at default) |
| 10 | ADCV | ADC Data Valid | ADC Data Valid 0 = ADC converting 1 = ADC data valid |
| 9:3 | ADC[6:0] | ADC output value | |
| 2:0 | ADDR[2:0] | Register Address | Register address bits |

Typical Application Circuit



Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-------------|----------------|-------------|
| MAX2880ETP+ | -40°C to +85°C | 20 TQFN-EP* |

+Denotes lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 20 TQFN-EP | T2044+2 | 21-0139 | 90-0036 |

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|-----------------|---------------|
| 0 | 12/13 | Initial release | — |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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Промышленная ул, дом № 19, литера Н,
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