

# I<sup>2</sup>C BUS

## 2kbit + 2kbit 2ports serial EEPROM

### BU99022NUX-3

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#### ●Description

BU99022NUX-3 series is 2kbit + 2kbit 2ports serial EEPROM of I<sup>2</sup>C BUS interface method.

#### ●FEATURES

- 2kbit + 2kbit 2ports serial EEPROM
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 1.7V~5.5V single power source action most suitable for battery use
- 1.7V~5.5V wide limit of action voltage, possible FAST MODE 400KHz action
- Page write mode useful for initial value write at factory shipment
- Auto erase and auto end function at data write
- Low current consumption
- Write mistake prevention function
  - Write (write protect) function added (only port2 EEPROM)
  - Write mistake prevention function at low voltage
- VSON008X2030 small package
- Data rewrite up to 1,000,000 times
- Data kept for 40 years
- Noise filter built in SCL / SDA terminal
- Shipment data all address FFh

### ● Absolute maximum rating (Ta=25°C)

Parameter	symbol	Limits	Unit
Impressed voltage	V <sub>CC</sub>	-0.3~+6.5	V
Permissible dissipation	P <sub>d</sub>	300 <sup>*1</sup>	mW
Storage temperature range	T <sub>stg</sub>	-65~+150	°C
Operation temperature range	T <sub>opr</sub>	-40~+85	°C
Terminal voltage	-	-0.3~V <sub>CC</sub> +1.0 <sup>*2</sup>	V
Junction Temperature <sup>*3</sup>	T <sub>jmax</sub>	150	°C

\*1 When using at Ta=25°C or higher, 3.0mW to be reduced per 1°C.

\*2 The Max value of Terminal Voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Terminal Voltage is not under -0.8V.

\*3 Junction temperature at the storage condition.

### ● Memory cell characteristics (Ta=25°C, V<sub>CC</sub>=1.7~5.5V)

Parameter	Limits			Unit
	Min.	Typ.	Max	
Write/Erase cycle <sup>*1</sup>	1,000,000	—	—	cycles
Data retention <sup>*1</sup>	40	—	—	Years

<sup>\*1</sup> Not 100% TESTED

### ● Recommended operating condition

Parameter	Symbol	Limits	Unit
Power source voltage	V <sub>CC</sub>	1.7~5.5	V
Input voltage	V <sub>IN</sub>	0~V <sub>CC</sub>	

### ● DC operating characteristics

(Unless otherwise specified, Ta=-40~+85°C, V<sub>CC</sub>=1.7~5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
"H" input voltage1	V <sub>IH1</sub>	0.7V <sub>CC</sub>	—	V <sub>CC</sub> +1.0	V	
"L" input voltage1	V <sub>IL1</sub>	-0.3 <sup>*1</sup>	—	0.3V <sub>CC</sub>	V	
"L" output voltage1	V <sub>OL1</sub>	—	—	0.4	V	I <sub>OL</sub> =3.0mA, 2.5V≤V <sub>CC</sub> ≤5.5V (SDA1, SDA2)
"L" output voltage2	V <sub>OL2</sub>	—	—	0.2	V	I <sub>OL</sub> =0.7mA, 1.7V≤V <sub>CC</sub> <2.5V (SDA1, SDA2)
Input leak current	I <sub>LI</sub>	-1	—	1	μA	V <sub>IN</sub> =0~V <sub>CC</sub>
Output leak current	I <sub>LO</sub>	-1	—	1	μA	V <sub>OUT</sub> =0~V <sub>CC</sub> (SDA1, SDA2)
Operating Current	I <sub>CCW1</sub>	—	—	2.0	mA	V <sub>CC</sub> 1=5.5V, f <sub>SCL</sub> =400kHz, t <sub>WR</sub> =5ms, Byte write Page write
	I <sub>CCW2</sub>	—	—	2.0		V <sub>CC</sub> 2=5.5V, f <sub>SCL</sub> =400kHz, t <sub>WR</sub> =5ms, Byte write Page write
	I <sub>CCR1</sub>	—	—	0.5	mA	V <sub>CC</sub> 1=5.5V, f <sub>SCL</sub> =400kHz Random read, current read, sequential read
	I <sub>CCR2</sub>	—	—	0.5		V <sub>CC</sub> 2=5.5V, f <sub>SCL</sub> =400kHz Random read, current read, sequential read
Standby current	I <sub>SB1</sub>	—	—	2.0	μA	V <sub>CC</sub> 1=5.5V, SDA1 · SCL1=V <sub>CC</sub>
	I <sub>SB2</sub>	—	—	2.0		V <sub>CC</sub> 2=5.5V, SDA2 · SCL2=V <sub>CC</sub> WP2=GND

○ This product is not designed for protection against radio active rays.

\*1 When the pulse width is 50ns or less, it is -0.8V.

## ●AC operating characteristic

(Unless otherwise specified, Ta=−40~+85°C, VCC=1.7~5.5V)

Parameter	Symbol	Limit			Unit
		Min.	Typ.	Max.	
SCL frequency	fSCL	—	—	400	kHz
Data clock "HIGH" time	tHIGH	0.6	—	—	μs
Data clock "LOW" time	tLOW	1.2	—	—	μs
SDA, SCL rise time <sup>*1,2</sup>	tR	—	—	1.0	μs
SDA, SCL fall time <sup>*1,2</sup>	tF	—	—	1.0	μs
Start condition hold time	tHD:STA	0.6	—	—	μs
Start condition setup time	tSU:STA	0.6	—	—	μs
Input data hold time	tHD:DAT	0	—	—	ns
Input data setup time	tSU:DAT	100	—	—	ns
Output data delay time	tPD	0.1	—	0.9	μs
Output data hold time	tDH	0.1	—	—	μs
Stop condition setup time	tSU:STO	0.6	—	—	μs
Bus release time before transfer start	tBUF	1.2	—	—	μs
Internal write cycle time	tWR	—	—	5	ms
Noise removal valid period (SDA, SCL terminal)	tI	—	—	0.1	μs
WP hold time	tHD:WP	1.0	—	—	μs
WP setup time	tSU:WP	0.1	—	—	μs
WP valid time	tHIGH:WP	1.0	—	—	μs

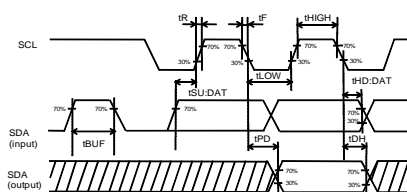
\*1 Not 100% TESTED.

\*2 It is recommended that tR/tF is less than 300ns fundamentally.

When tR/tF is more than 300ns and less than 1μs, it is possible that other device on the same bus are entered unintended start/stop condition. For prevent it, note in designing the AC timing.

Condition Input data level: VIL=0.2×VCC VIH=0.8×VCC  
Input data timing reference level: 0.3×VCC/0.7×VCC  
Output data timing reference level: 0.3×VCC/0.7×VCC  
Rise/Fall time : ≤20ns

## ●Sync data input / output timing



Input read at the rise edge of SCL  
Odata output in sync with the fall of SCL

Fig.1-(a) Sync data input / output timing

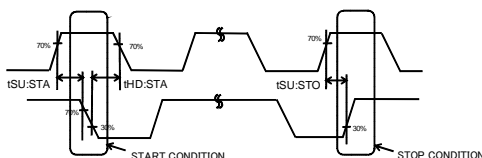


Fig.1-(b) Start-stop bit timing

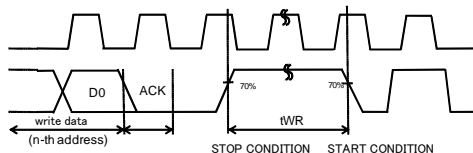


Fig.1-(c) Write cycle timing

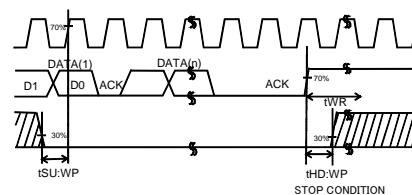


Fig.2 WP timing at write execution

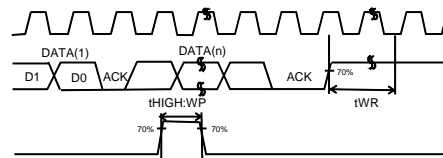


Fig.3 WP timing at write cancel

●Block diagram

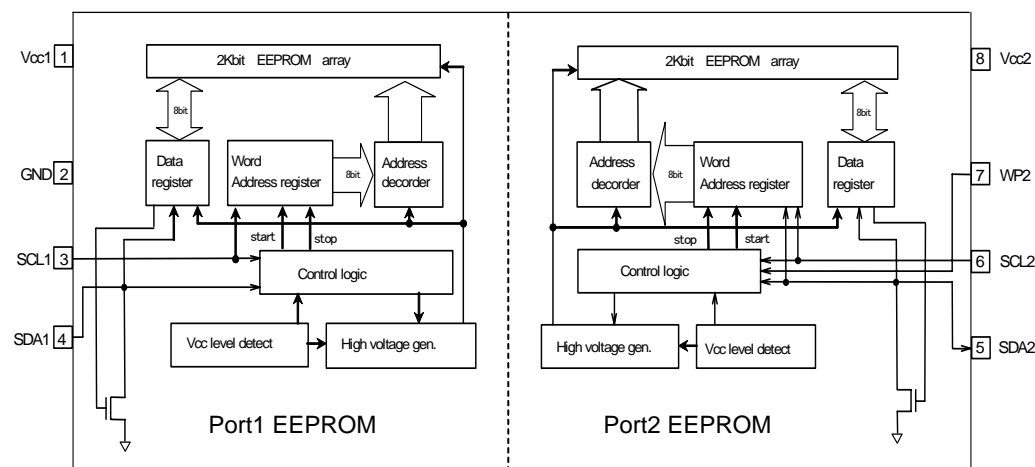


Fig.4 Block Diagram

●Pin assignment and description

Pin No.	Pin Name	Input/output	Function
1	Vcc1	—	Connect the power source
2	GND	—	Reference voltage of all input/output,0V
3	SCL1	Input	Serial clock input for port1
4	SDA1	input/output	Serial data input /serial data output for port1 EEPROM
5	SDA2	input/output	Serial data input /serial data output for port2 EEPROM
6	SCL2	input	Serial clock input for port2 EEPROM
7	WP2	input	Write protect terminal for port2 EEPROM
8	Vcc2	—	Connect the power source

●Operating condition of port1 and port2 EEPROM

Vcc1	Vcc2	port1	port2
0V	0V	×	×
0V	Vcc	×	○
0V	open	×	×
Vcc	0V	○	×
Vcc	Vcc	○	○
Vcc	open	○	×
open	0V	×	×
open	Vcc	×	○
open	open	×	×

○ : operating possible  
× : operating impossible

●Characteristic data (The following values are Typ. ones.)

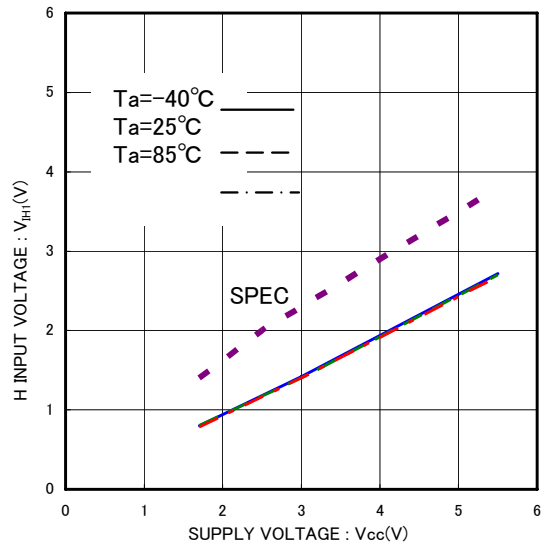


Fig.5 'H' input voltage  $V_{IH1}$   
(SCL1,SCL2,SDA1,SDA2,WP2)

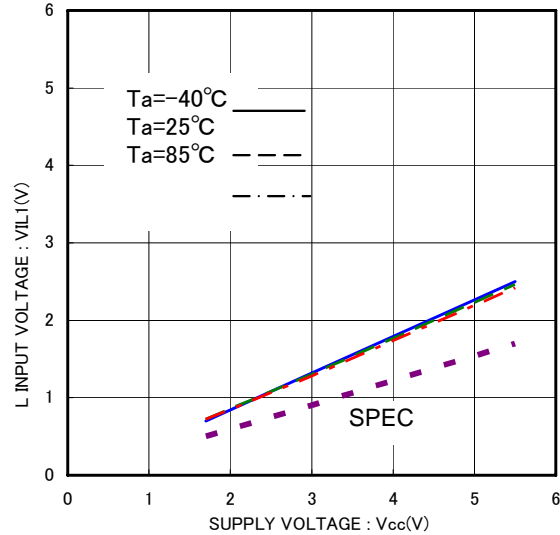


Fig.6 'L' input voltage  $V_{IL1}$   
(SCL1,SCL2,SDA1,SDA2,WP2)

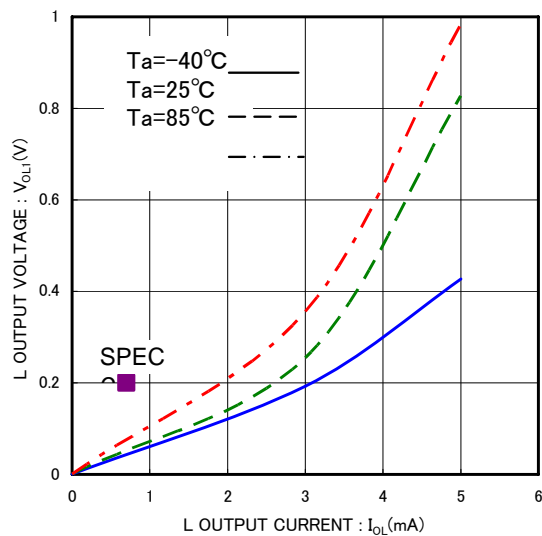


Fig.7 'L' output voltage  $V_{OL1}$ - $I_{OL}$  ( $V_{CC}=1.7\text{V}$ )

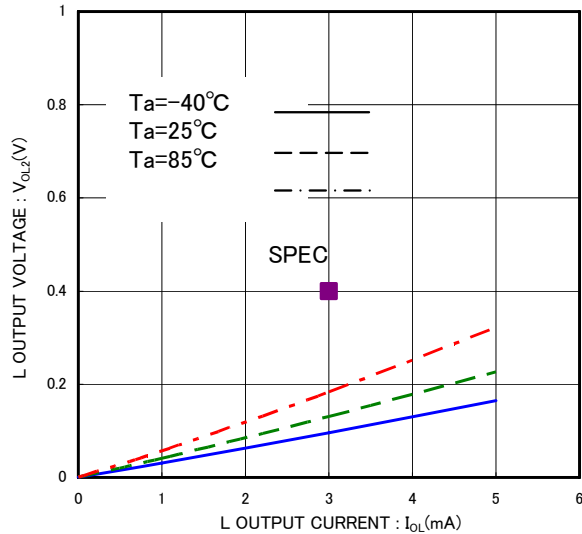


Fig.8 'L' output voltage  $V_{OL2}$ - $I_{OL}$  ( $V_{CC}=2.5\text{V}$ )

●Characteristic data (The following values are Typ. ones.)

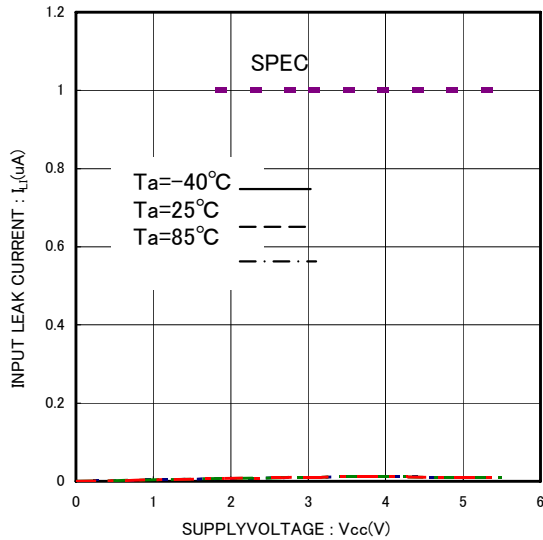


Fig.9 Input leak current  $I_{LI}$   
(SCL1,SCL2,SDA1,SDA2,WP2)

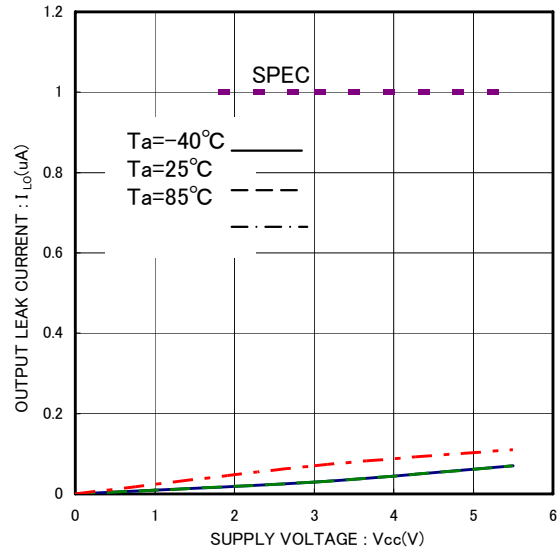


Fig.10 Output leak current  $I_{LO}$   
(SDA1,SDA2)

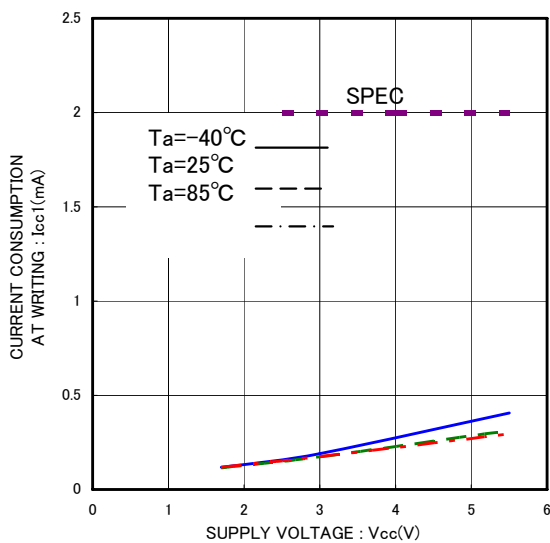


Fig.11 Current consumption at WRITE operation  $I_{CC1}$   
(f<sub>scl</sub>=400kHz)

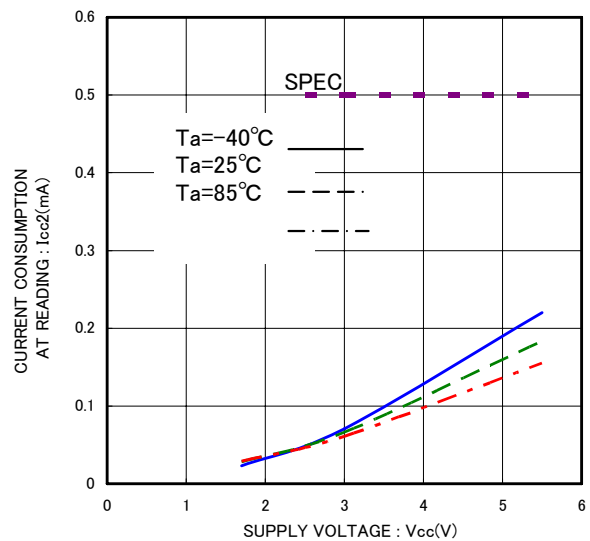


Fig.12 Current consumption at READ operation  $I_{CC2}$   
(f<sub>scl</sub>=400kHz)

●Characteristic data (The following values are Typ. ones.)

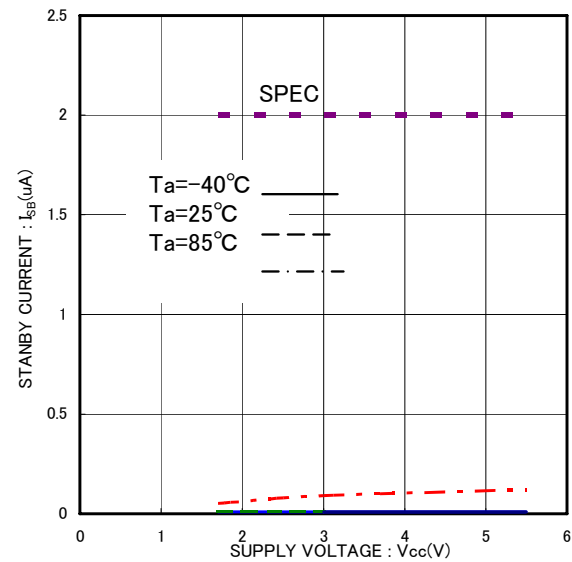


Fig.13 Standby operation  $I_{SB}$

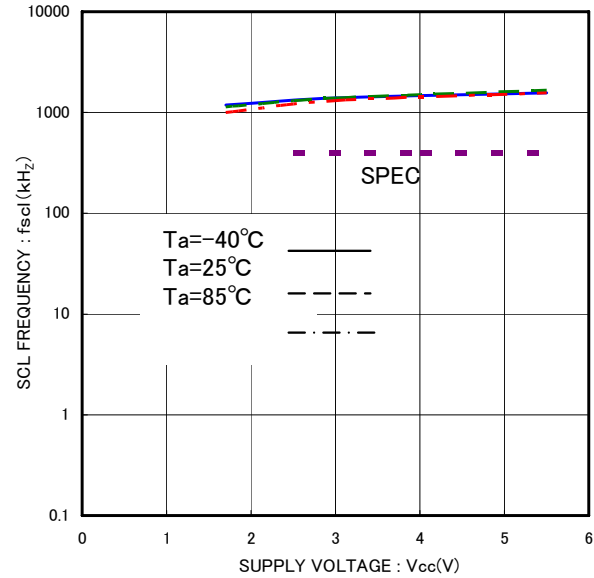


Fig.14 SCL frequency  $f_{SCL}$

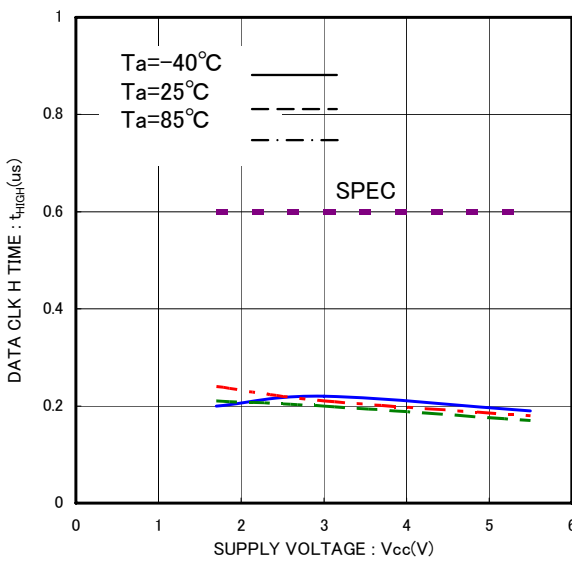


Fig.15 Data clock High Period  $t_{HIGH}$

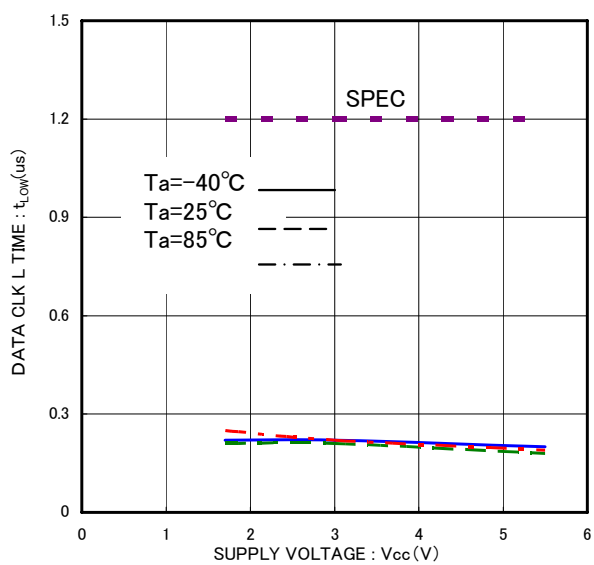


Fig.16 Data clock Low Period  $t_{LOW}$

●Characteristic data (The following values are Typ. ones.)

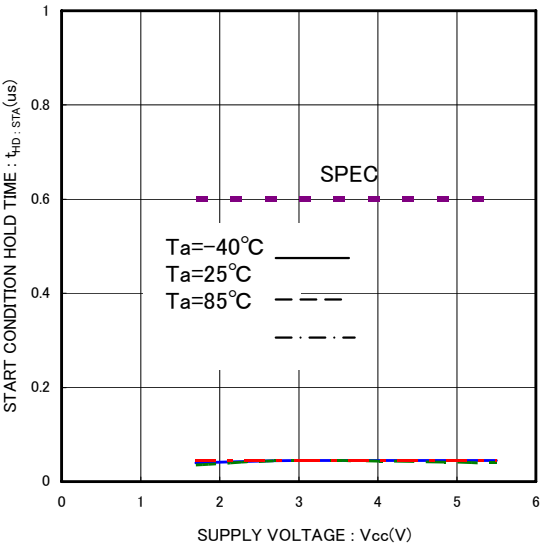


Fig.17 Start Condition Hold Time  $t_{HD:STA}$

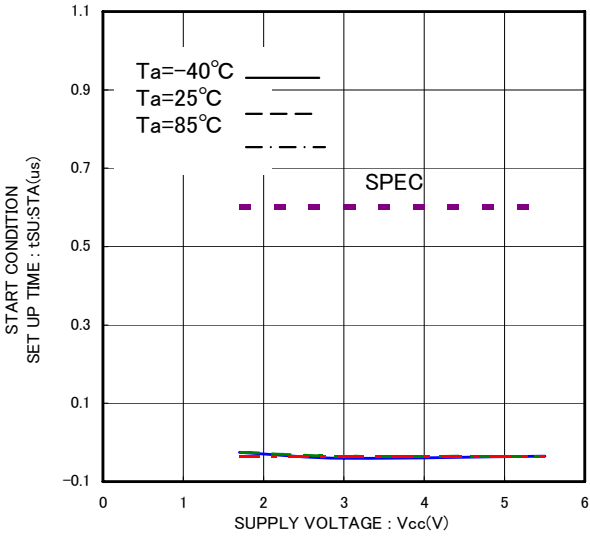


Fig.18 Start Condition Setup Time  $t_{SU:STA}$

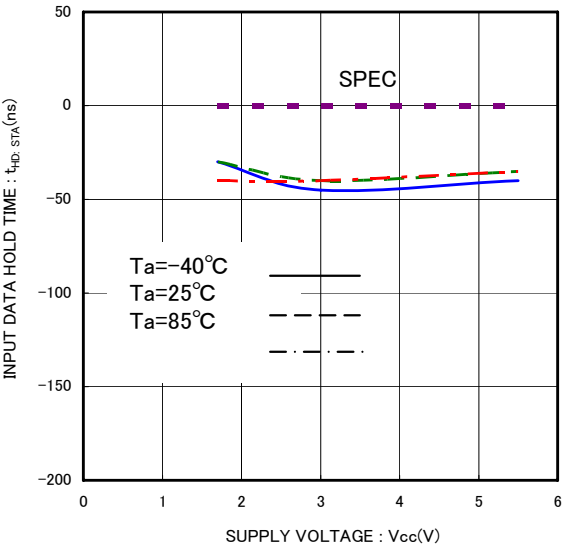


Fig.19 Input Data Hold Time  $t_{HD:DAT}$ (HIGH)

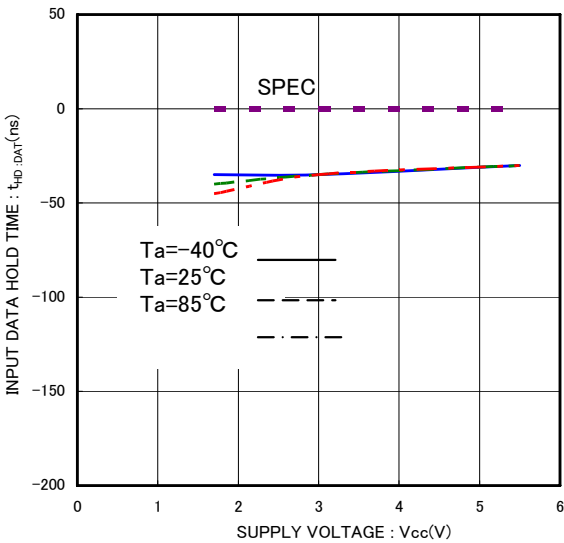


Fig.20 Input Data Hold Time  $t_{HD:DAT}$ (LOW)



●Characteristic data (The following values are Typ. ones.)

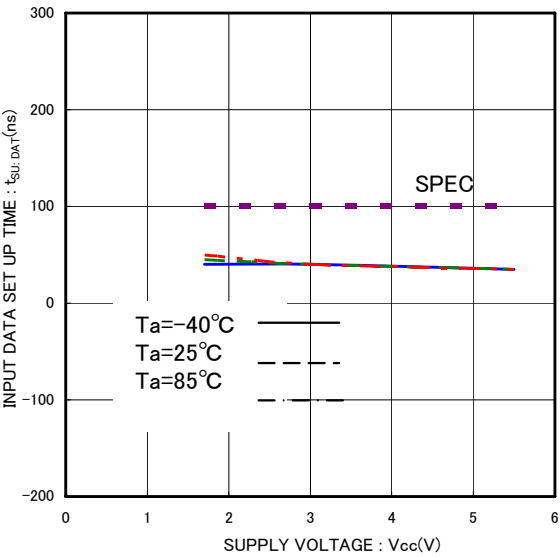


Fig.21 Input Data Setup Time  $t_{SU:DAT}$ (HIGH)

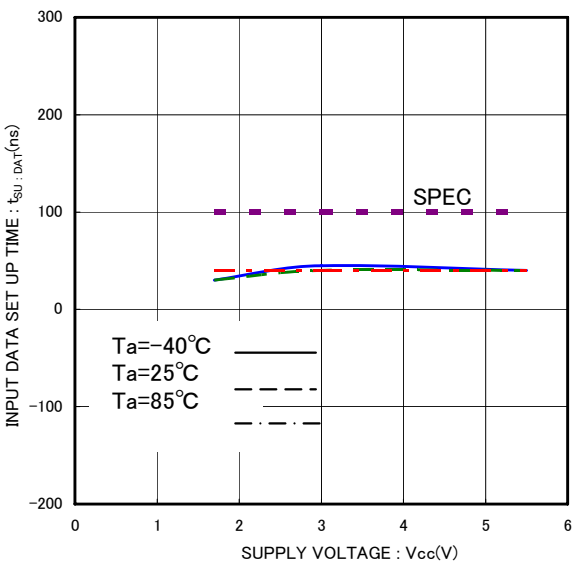


Fig.22 Input Data setup time  $t_{SU:DAT}$ (LOW)

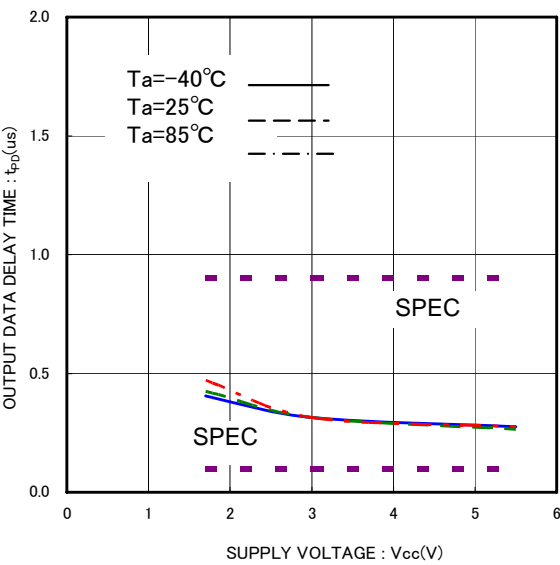


Fig..23 'L' Data output delay time  $t_{PD0}$

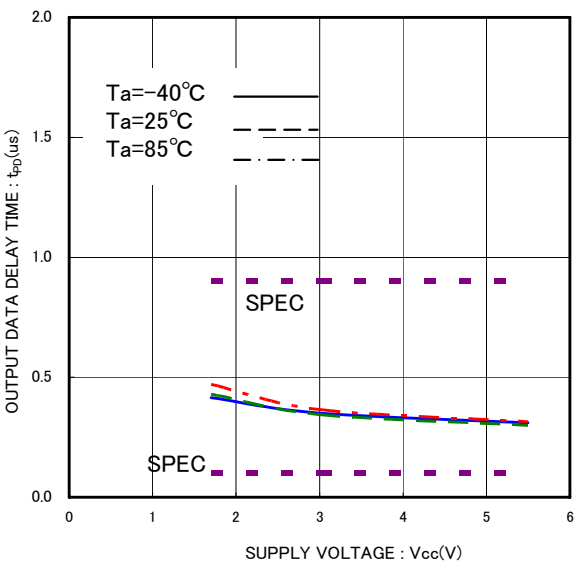


Fig.24 'H' Data output delay time  $t_{PD1}$

●Characteristic data (The following values are Typ. ones.)

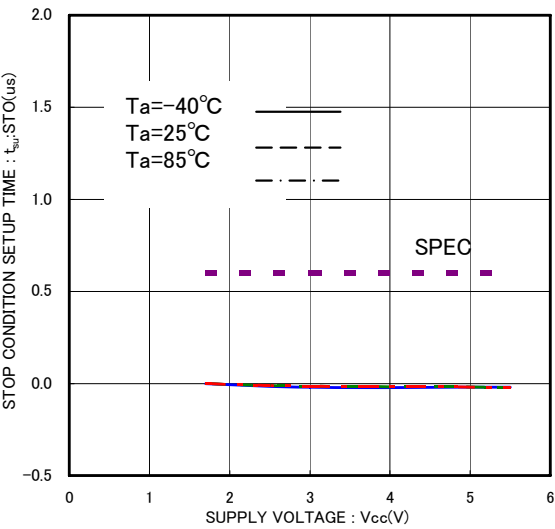


Fig.25 Stop condition setup time  $t_{SU:STO}$

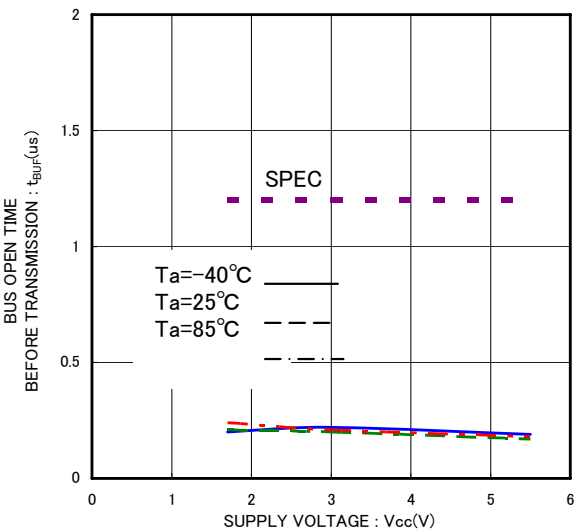


Fig.26 BUS open time before transmission  $t_{BUF}$

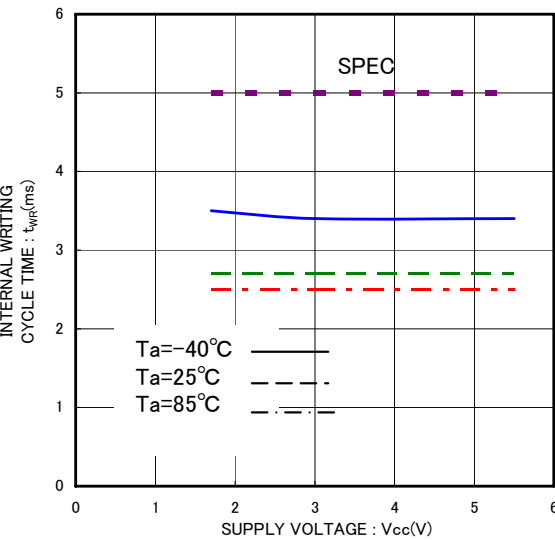


Fig.27 Internal writing cycle time  $t_{WR}$

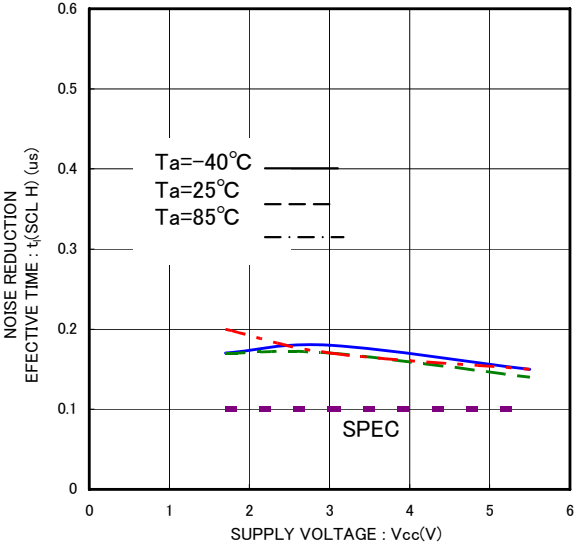


Fig.28 Noise reduction effective time  $t_i(\text{SCL H})$

●Characteristic data (The following values are Typ. ones.)

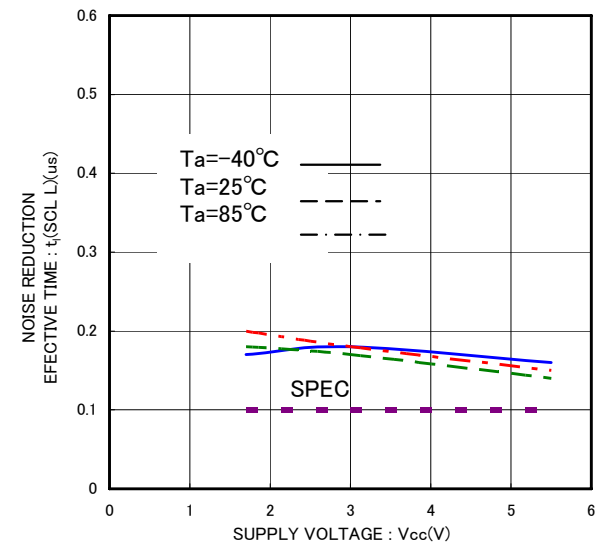


Fig.29 Noise reduction effective time  $t_i(\text{SCL L})$

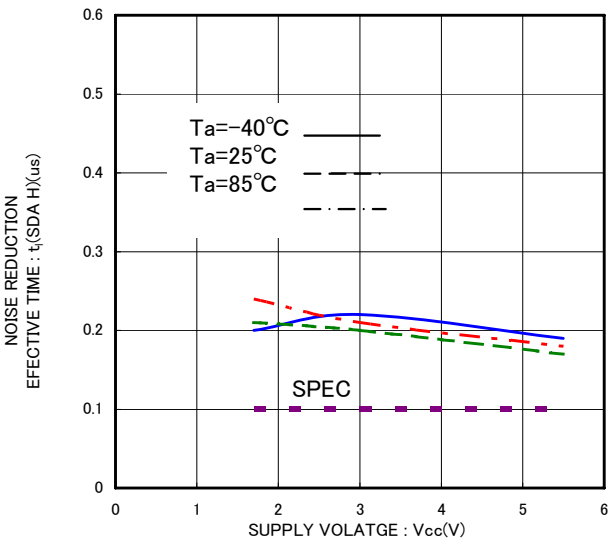


Fig.30 Noise reduction effective time  $t_i(\text{SDA H})$

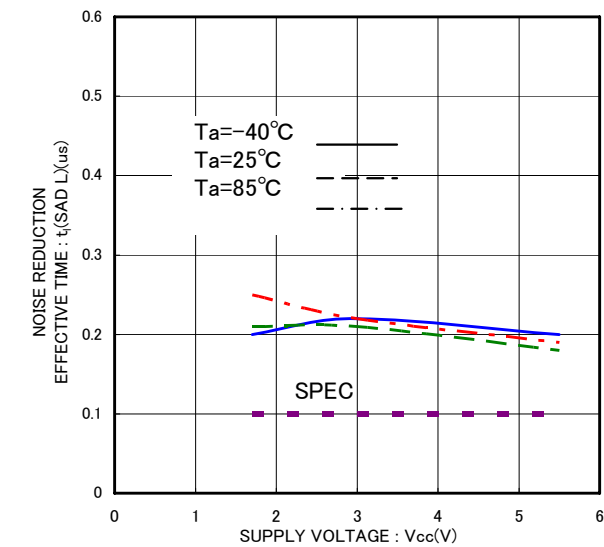


Fig.31 Noise reduction effective time  $t_i(\text{SDA L})$

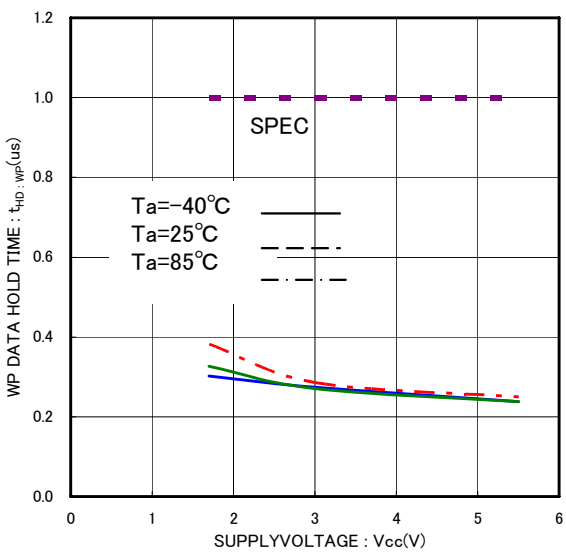


Fig.32 WP data hold time  $t_{HD:WP}$

●Characteristic data (The following values are Typ. ones.)

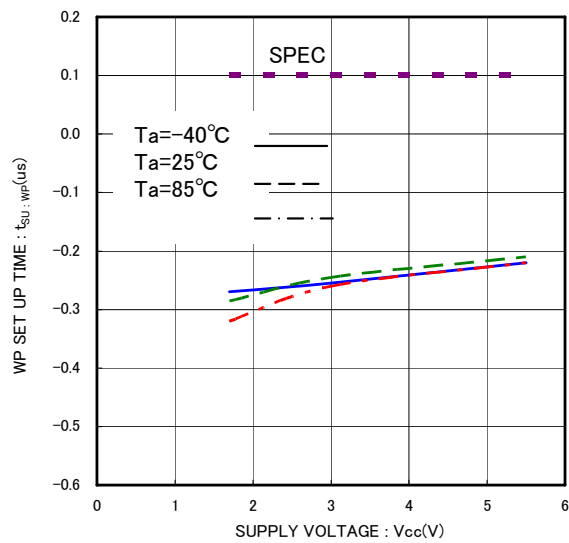


Fig.33 WP setup time  $t_{SU:WP}$

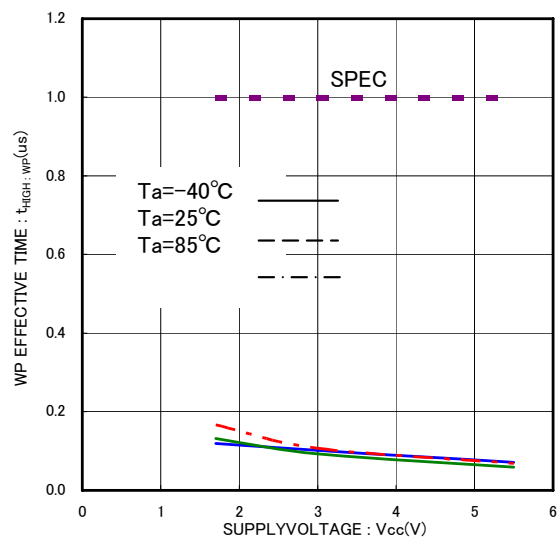


Fig.34 WP effective time  $t_{HIGH:WP}$

## ● I<sup>2</sup>C BUS communication

### ○ I<sup>2</sup>C BUS data communication

I<sup>2</sup>C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I<sup>2</sup>C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).

Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by address peculiar to devices. EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

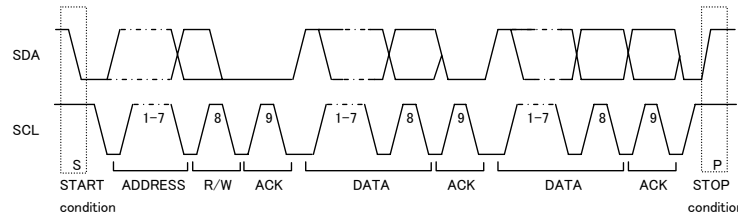


Fig.35 Data transfer timing

### ○ Start condition (Start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, any command is executed.

### ○ Stop condition (stop bit recognition)

- Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

### ○ Acknowledge (ACK) signal

- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device ( $\mu$ -COM at slave address input of write command, read command, and this IC at data output of read command) at the transmitter (sending) side releases the bus after output of 8bit data.
- The device (this IC at slave address input of write command, read command, and  $\mu$ -COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- Each write action outputs acknowledge signal (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
- Each read action outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'. When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master ( $\mu$ -COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read action. And this IC gets in status.

## ●Write Command

### ○Write cycle

- Arbitrary data is written to EEPROM. When to write only 1 byte, byte write is normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The maximum number of write bytes is up to 8.

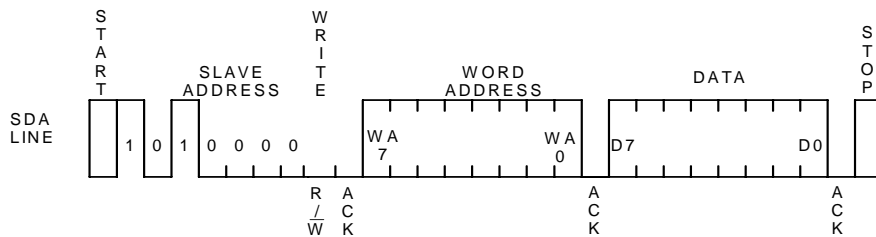


Fig.36 Byte write cycle (port1 EEPROM)

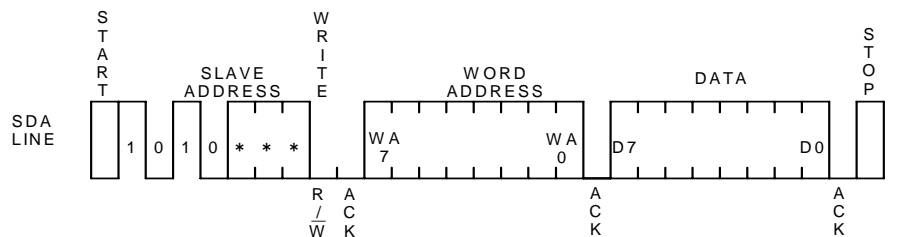


Fig.37 Byte write cycle (port2 EEPROM)

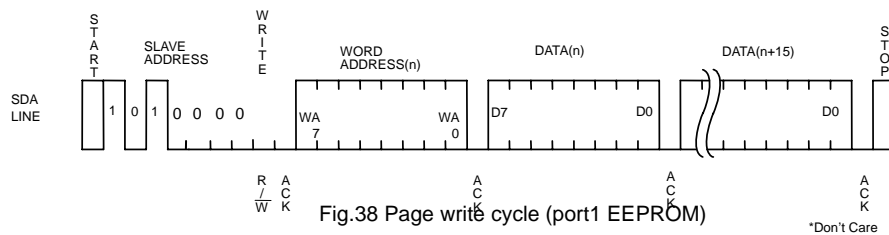


Fig.38 Page write cycle (port1 EEPROM)

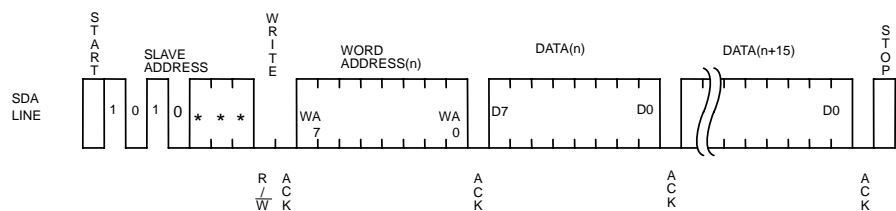


Fig.39 Page write cycle (port2 EEPROM)

- During internal write execution, all input commands are ignored, therefore ACK is not sent back.
- Data is written to the address designated by word address (n-th address).
- By issuing stop bit after 8bit data input, write to memory cell inside starts.
- When internal write is started, command is not accepted for tWR (5ms at maximum).
- By page write cycle, the following can be written in bulk :  
And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
- As for page write cycle , after the significant 5 bits of word address are designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 3 bits is incremented internally, and data up to 8 bytes can be written.

### ○Write protect (WP2) terminal

#### • Write protect (WP2) function

When WP2 terminal is set Vcc (H level), data rewrite of all addresses is prohibited (only port2 EEPROM).

When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not use it open.

In the case of use it as an ROM, it is recommended to connect it to pull up or Vcc.

At extremely low voltage at power ON / OFF, by setting the WP terminal 'H', mistake write can be prevented.

## ●Read Command

### ○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.

Random read cycle is a command to read data by designating address, and is used generally.

Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.

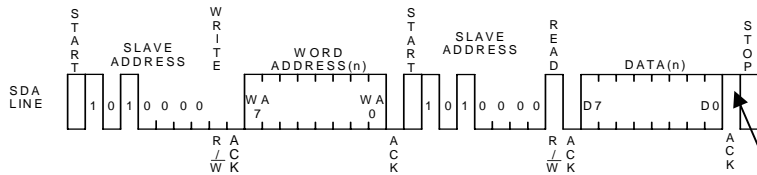


Fig.40 Random read cycle (port1 EEPROM)

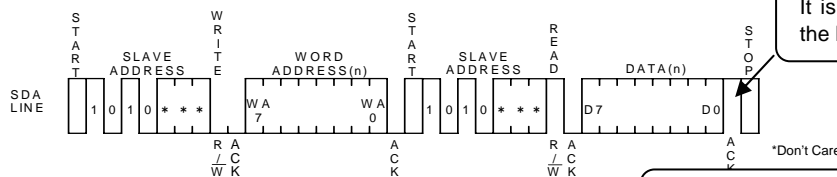


Fig.41 Random read cycle (port2 EEPROM)

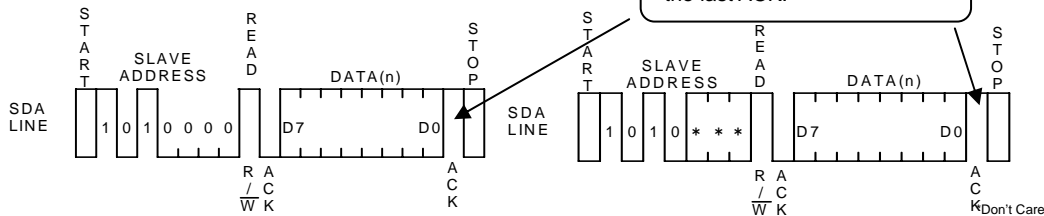


Fig.42 Current read cycle (port1 EEPROM)

Fig.43 Current read cycle (port2 EEPROM)

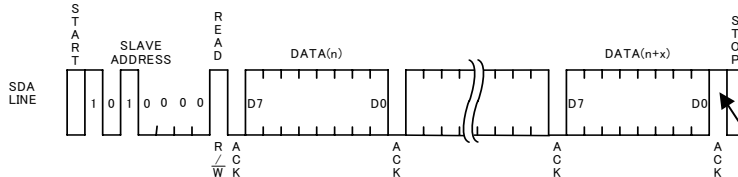


Fig.44 Sequential read cycle (port1 EEPROM)

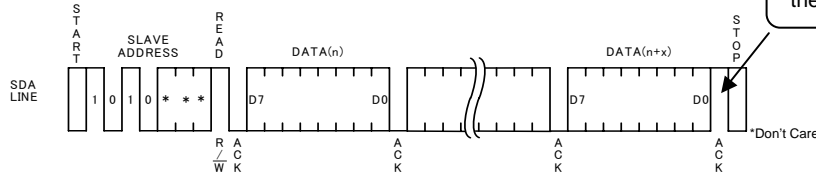


Fig.45 Sequential read cycle (port2 EEPROM)

- In random read cycle, data of designated word address can be read.
  - When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
  - When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master ( $\mu$ -COM) side, the next address data can be read in succession.
  - Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H'.
  - When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
- Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

## ● Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Fig.46, Fig.47, Fig.48.) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

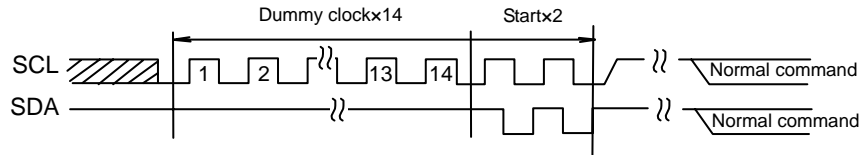


Fig.46 The case of dummy clock +START+START+ command input

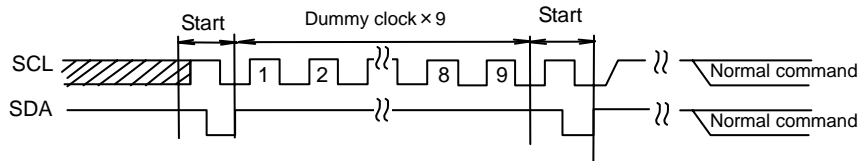


Fig.47 The case of START +9 dummy clocks +START+ command input

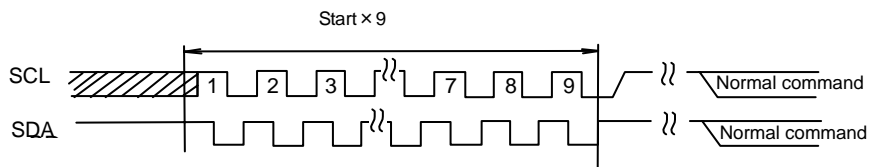


Fig.48 STARTx9+ command input

※Start command from START input.

## ● Acknowledge polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write action, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for  $t_{WR} = 5\text{ms}$ .

When to write continuously,  $R/\overline{W} = 0$ , when to carry out current read cycle after write, slave address  $R/\overline{W} = 1$  is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

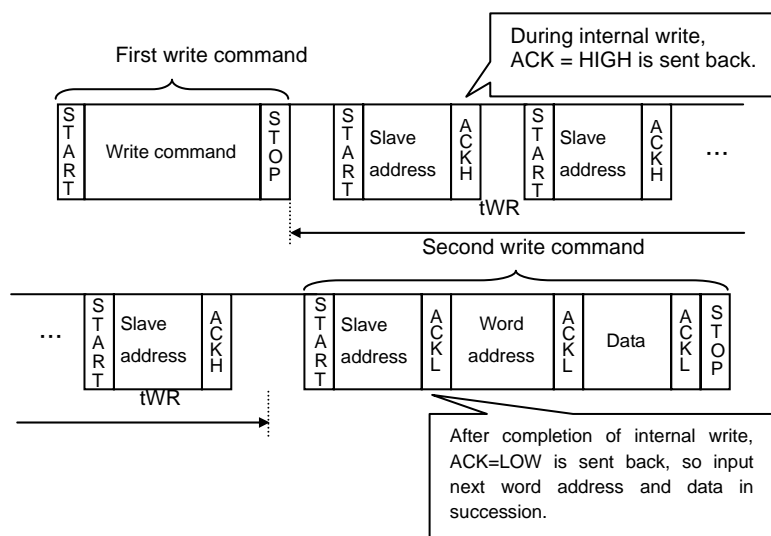


Fig.49 Case to continuously write by acknowledge polling



### ●WP valid timing (write cancel)

WP2 is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP2='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area.

WP input in this area becomes Don't care. The area from the rise of SCL to take in D0 to input the stop condition is cancel valid area. And, after execution of forced end by WP, standby status gets in.

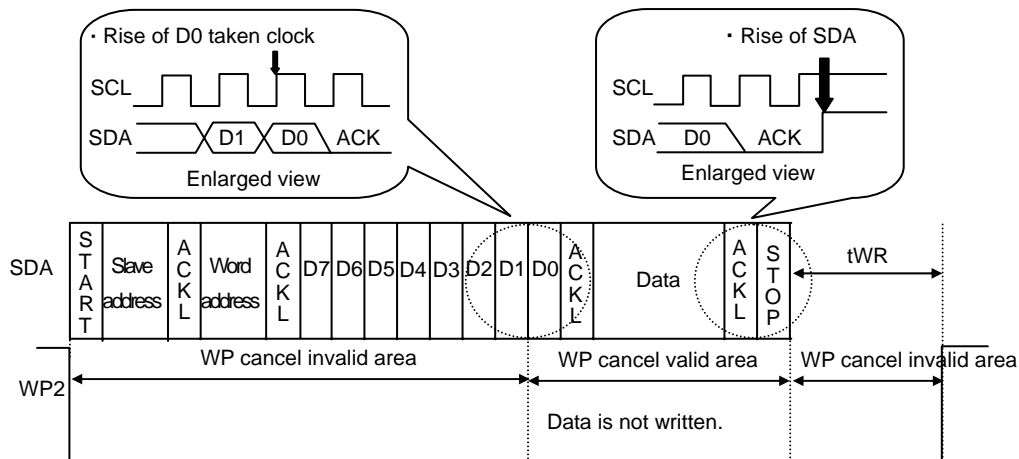


Fig.50 WP valid timing

### ●Command cancel by start condition and stop condition

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Fig.51)

However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

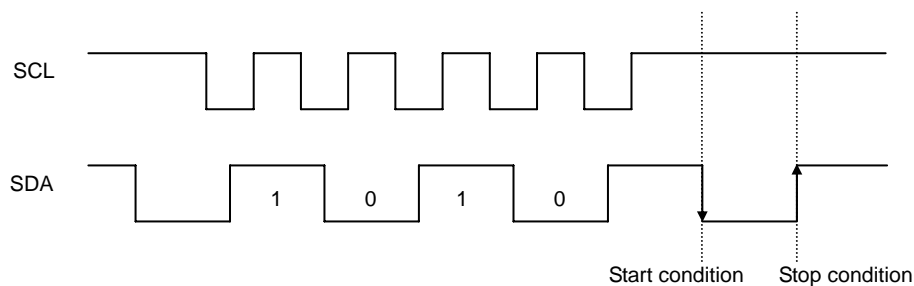


Fig.51 Case of cancel by start, stop condition during slave address input

## ● I/O peripheral circuit

### ○ Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value ( $R_{PU}$ ), select an appropriate value to this resistance value from microcontroller  $V_{IL}$ ,  $I_L$ , and  $V_{OL}-I_{OL}$  characteristics of this IC. If  $R_{PU}$  is large, action frequency is limited. The smaller the  $R_{PU}$ , the larger the consumption current at action.

### ○ Maximum value of $R_{PU}$

The maximum value of  $R_{PU}$  is determined by the following factors.

① SDA rise time to be determined by the capacitance (CBUS) of bus line of  $R_{PU}$  and SDA should be  $t_R$  or below.

And AC timing should be satisfied even when SDA rise time is late.

② The bus electric potential (A) to be determined by input leak total ( $I_L$ ) of device connected to bus at output of 'H' to SDA bus and  $R_{PU}$  should sufficiently secure the input 'H' level ( $V_{IH}$ ) of microcontroller and EEPROM including recommended noise margin  $0.2V_{CC}$ .

$$V_{CC} - I_L R_{PU} - 0.2 V_{CC} \geq V_{IH}$$

$$\therefore R_{PU} \leq \frac{0.8V_{CC} - V_{IH}}{I_L}$$

Ex.)  $V_{CC}=3V$   $I_L=10\mu A$   $V_{IH}=0.7 V_{CC}$   
from ②

$$R_{PU} \leq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leq 300 \text{ [k}\Omega\text{]}$$

### ○ Minimum value of $R_{PU}$

The minimum value of  $R_{PU}$  is determined by the following factors.

When IC outputs LOW, it should be satisfied that  $V_{OLMAX}=0.4V$  and  $I_{OLMAX}=3mA$ .

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leq I_{OL}$$

$$\therefore R_{PU} \geq \frac{V_{CC} - V_{OL}}{I_{OL}}$$

②  $V_{OLMAX}=$  should secure the input 'L' level ( $V_{IL}$ ) of microcontroller and EEPROM including recommended noise margin  $0.1V_{CC}$ .

$$V_{OLMAX} \leq V_{IL} - 0.1 V_{CC}$$

Ex.)  $V_{CC}=3V$ ,  $V_{OL}=0.4V$ ,  $I_{OL}=3mA$ , microcontroller, EEPROM  $V_{IL}=0.3V_{CC}$

$$\text{from ① } R_{PU} \geq \frac{3 - 0.4}{3 \times 10^{-3}}$$

$$\geq 867 \text{ [}\Omega\text{]}$$

$$\text{And } V_{OL}=0.4 \text{ [V]}$$

$$V_{IL}=0.3 \times 3$$

$$=0.9 \text{ [V]}$$

Therefore, the condition ② is satisfied.

### ○ Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several  $k\Omega$  ~ several ten  $k\Omega$  is recommended in consideration of drive performance of output port of microcontroller.

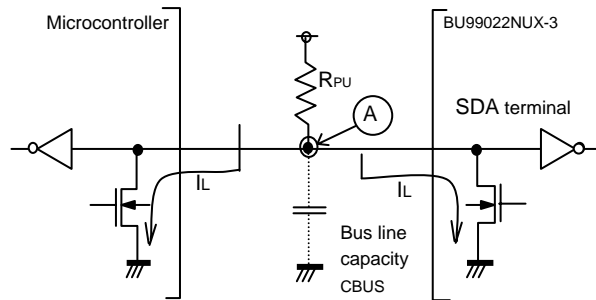


Fig.52 I/O circuit diagram

## ●Cautions on microcontroller connection

### ORs

In I<sup>2</sup>C BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance  $R_s$  between the pull up resistance  $R_{PU}$  and the SDA terminal of EEPROM. This controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously.  $R_s$  also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output,  $R_s$  can be used.

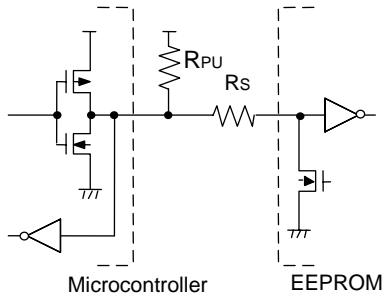


Fig.53-(a) I/O circuit diagram

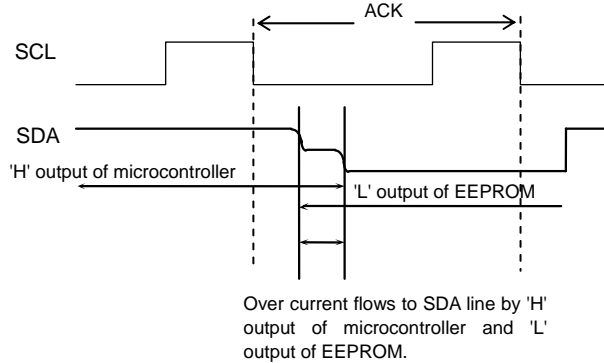


Fig.53-(b) Input / output collision timing

### OMaximum value of $R_s$

The maximum value of  $R_s$  is determined by the following relations.

①SDA rise time to be determined by the capacity (CBUS) of bus line of  $R_{PU}$  and SDA should be  $t_R$  or below.

And AC timing should be satisfied even when SDA rise time is late.

②The bus electric potential(A) to be determined by  $R_{PU}$  and  $R_s$  the moment when EEPROM outputs 'L' to SDA bus sufficiently secure the input 'L' level ( $V_{IL}$ ) of microcontroller including recommended noise margin 0.1Vcc.

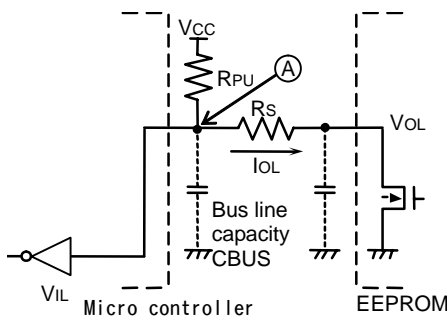


Fig.54-(a) I/O Circuit Diagram

$$\frac{(V_{CC}-V_{OL}) \times R_s}{R_{PU}+R_s} + V_{OL} + 0.1V_{CC} \leq V_{IL}$$

$$\therefore R_s \leq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

$$\text{Ex.) } V_{CC}=3V \quad V_{IL}=0.3V_{CC} \quad V_{OL}=0.4V \quad R_{PU}=20k\Omega$$

$$R_s \leq \frac{0.3 \times 3 - 0.4 - 0.1 \times 3}{1.1 \times 3 - 0.3 \times 3} \times 20 \times 10^3$$

$$\leq 1.67[k\Omega]$$

### OMinimum value of $R_s$

The minimum value of  $R_s$  is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as  $I$ , the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

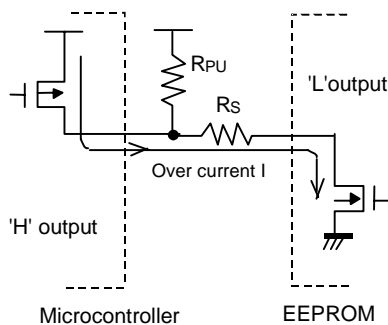


Fig.54-(b) I/O circuit diagram

$$\frac{V_{CC}}{R_s} \leq I$$

$$\therefore R_s \geq \frac{V_{CC}}{I}$$

$$\text{Ex.) } V_{CC}=3V, I=10mA$$

$$R_s \geq \frac{3}{10 \times 10^{-3}}$$

$$\geq 300[\Omega]$$

● I<sup>2</sup>C BUS input / output circuit

OInput (SCL1,SCL2,WP2)

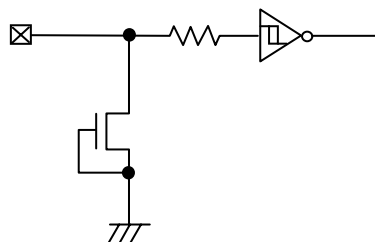


Fig.55-(a) Input pin circuit diagram

OInput / output (SDA1,SDA2)

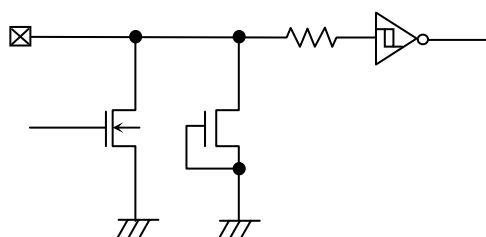


Fig.55-(b) Input / output pin circuit diagram

### ●Notes on power ON

At power on, in IC internal circuit and set, Vcc rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the action, observe the following conditions at power on.

1. Set SDA = 'H' and SCL = 'L' or 'H'
2. Start power source so as to satisfy the recommended conditions of  $t_R$ ,  $t_{OFF}$ , and  $V_{bot}$  for operating POR circuit.

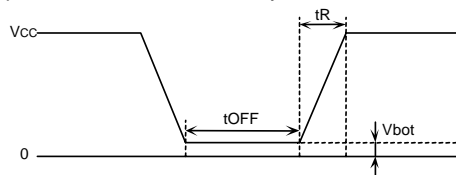


Fig.56 Rise waveform diagram

Recommended conditions of  $t_R$ ,  $t_{OFF}$ ,  $V_{bot}$

$t_R$	$t_{OFF}$	$V_{bot}$
10ms or below	10ms or larger	0.3V or below
100 or below	10ms or larger	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.

When the above conditions 1 and 2 cannot be observed, take the following countermeasures.

- a) In the case when the above condition 1 cannot be observed. When SDA becomes 'L' at power on.

→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

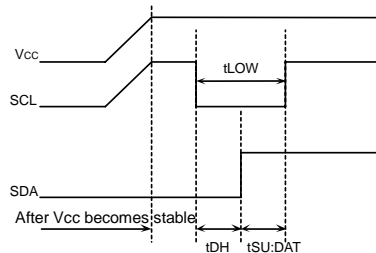


Fig.57 When SCL= 'H' and SDA= 'L'

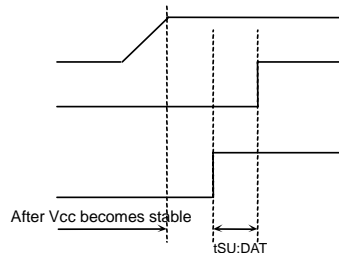


Fig.58 When SCL='L' and SDA='L'

- b) In the case when the above condition 2 cannot be observed.  
→After power source becomes stable, execute software reset(P15).
- c) In the case when the above conditions 1 and 2 cannot be observed.  
→Carry out a), and then carry out b).

### ●Low voltage malfunction prevention function

LVCC circuit prevents data rewrite action at low power, and prevents wrong write. At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

### ●Vcc noise countermeasures

#### ○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1μF) between IC Vcc and GND. At that moment, attach it as close to IC as possible.

And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

### ●Cautions on use

- (1) Described numeric values and data are design representative values, and the values are not guaranteed.
- (2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.
- (3) Absolute maximum ratings  
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.
- (4) GND electric potential  
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.
- (5) Terminal design  
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.
- (6) Terminal to terminal shortcircuit and wrong packaging  
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.
- (7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

## ● Revision history

Date	Revision	Changes
19-Dec-2011	001	Initial Document Release

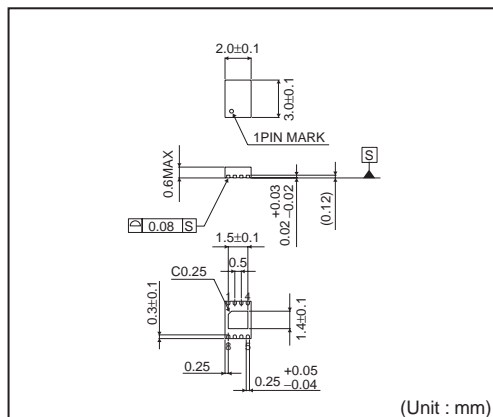
### ● Ordering information

B U 9 9 0 2 2 N U X - 3	TR
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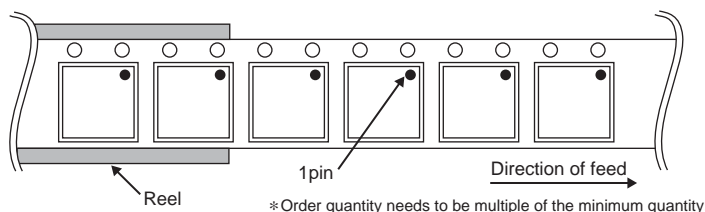
Package  
NEX : VSON008X2030

Packaging and forming specification  
TR : Embossed tape and reel

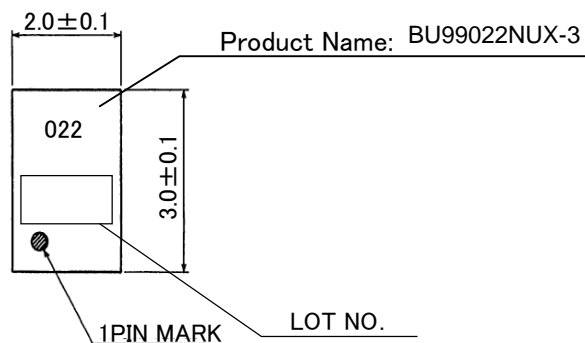
### ●Physical Dimantion. Tape abd Reel information

**VSON008X2030**

<Tape and Reel information>	
Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR ( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand )



### ● Marking Diagram



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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification



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  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
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  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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