

## 128K x 24 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

JUNE 2005

### FEATURES

- High-speed access time: 8, 10 ns
- CMOS low power operation
  - 756 mW (max.) operating @ 8 ns
  - 36 mW (max.) standby @ 8 ns
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Available in 119-pin Plastic Ball Grid Array (PBGA) and 100-pin TQFP packages.
- Industrial temperature available
- Lead-free available

### DESCRIPTION

The *ISSI* IS61LV12824 is a high-speed, static RAM organized as 131,072 words by 24 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When  $\overline{CE1}$ ,  $\overline{CE2}$  are HIGH and CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs,  $\overline{CE1}$ , CE2,  $\overline{CE2}$  and  $\overline{OE}$ . The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

The IS61LV12824 is packaged in the JEDEC standard 119-pin PBGA and 100-pin TQFP.

### FUNCTIONAL BLOCK DIAGRAM



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**PIN CONFIGURATION - 119-pin PBGA**

	1	2	3	4	5	6	7
<b>A</b>	NC	A11	A14	A15	A16	A4	NC
<b>B</b>	NC	A12	A13	$\overline{\text{CE1}}$	A5	A3	NC
<b>C</b>	I/O16	NC	CE2	NC	$\overline{\text{CE2}}$	NC	I/O0
<b>D</b>	I/O17	V <sub>ccq</sub>	GND	GND	GND	V <sub>ccq</sub>	I/O1
<b>E</b>	I/O18	GND	V <sub>cc</sub>	GND	V <sub>cc</sub>	GND	I/O2
<b>F</b>	I/O19	V <sub>ccq</sub>	GND	GND	GND	V <sub>ccq</sub>	I/O3
<b>G</b>	I/O20	GND	V <sub>cc</sub>	GND	V <sub>cc</sub>	GND	I/O4
<b>H</b>	I/O21	V <sub>ccq</sub>	GND	GND	GND	V <sub>ccq</sub>	I/O5
<b>J</b>	V <sub>ccq</sub>	GND	V <sub>cc</sub>	GND	V <sub>cc</sub>	GND	V <sub>ccq</sub>
<b>K</b>	I/O22	V <sub>ccq</sub>	GND	GND	GND	V <sub>ccq</sub>	I/O6
<b>L</b>	I/O23	GND	V <sub>cc</sub>	GND	V <sub>cc</sub>	GND	I/O7
<b>M</b>	I/O12	V <sub>ccq</sub>	GND	GND	GND	V <sub>ccq</sub>	I/O8
<b>N</b>	I/O13	GND	V <sub>cc</sub>	GND	V <sub>cc</sub>	GND	I/O9
<b>P</b>	I/O14	V <sub>ccq</sub>	GND	GND	GND	V <sub>ccq</sub>	I/O10
<b>R</b>	I/O15	NC	NC	NC	NC	NC	I/O11
<b>T</b>	NC	A10	A8	$\overline{\text{WE}}$	A0	A1	NC
<b>U</b>	NC	A9	A7	$\overline{\text{OE}}$	A6	A2	NC

**PIN DESCRIPTIONS**

A0-A16	Address Inputs
I/O0-I/O23	Data Inputs/Outputs
$\overline{\text{CE1}}, \overline{\text{CE2}}$	Chip Enable Input LOW
CE2	Chip Enable Input HIGH
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{WE}}$	Write Enable Input
NC	No Connection
V <sub>cc</sub>	Power
V <sub>ccq</sub>	I/O Power
GND	Ground

**PIN CONFIGURATION**  
**100-Pin TQFP**



**PIN DESCRIPTIONS**

A0-A16	Address Inputs
I/O0-I/O23	Data Inputs/Outputs
$\overline{CE1}, \overline{CE2}$	Chip Enable Input LOW
CE2	Chip Enable Input HIGH
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
NC	No Connection
Vcc	Power
Vccq	I/O Power
GND	Ground

## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{CE2}$	$\overline{OE}$	I/O0-I/O23	Vcc Current
Not Selected	X	H	X	X	X	High-Z	ISB1, ISB2
	X	X	L	X	X		
	X	X	X	H	X		
Output Disabled	H	L	H	L	H	High-Z	Icc
Read	H	L	H	L	L	DOUT	Icc
Write	L	L	H	L	X	DIN	Icc

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit	
VCC	Power Supply Voltage Relative to GND	-0.5 to 5.0	V	
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	V	
TSTG	Storage Temperature	-65 to + 150	°C	
TBIAS	Temperature Under Bias:	Com.	-10 to + 85	°C
		Ind.	-45 to + 90	°C
PT	Power Dissipation	2.0	W	
IOUT	DC Output Current	±20	mA	

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE

Range	Ambient Temperature	Vcc (8 ns)	Vcc (10 ns)
Commercial	0°C to +70°C	3.3V + 10%, - 5%	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V + 10%, - 5%	3.3V ± 10%

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
VOH	Output HIGH Voltage	Vcc = Min., IOH = -4.0 mA	2.4	—	V
VOL	Output LOW Voltage	Vcc = Min., IOL = 8.0 mA	—	0.4	V
VIH	Input HIGH Voltage		2.2	Vcc + 0.3	V
VIL	Input LOW Voltage <sup>(1)</sup>		-0.3	0.8	V
ILI	Input Leakage	GND ≤ VIN ≤ Vcc	-1	1	µA
ILO	Output Leakage	GND ≤ VOUT ≤ Vcc, Outputs Disabled	-1	1	µA

**Note:**

1. VIL (min.) = -0.3V DC; VIL (min.) = -2.0V AC (pulse width ≤ 2.0 ns).  
VIH (max.) = Vcc + 0.3V DC; VIH (max.) = Vcc + 2.0V AC (pulse width ≤ 2.0 ns).

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions	-8 ns		-10 ns		Unit
			Min.	Max.	Min.	Max.	
I <sub>CC</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com. Ind.	— 210 240	— 180 210	— 180 210	mA
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , f = max. CE1, CE2, ≥ V <sub>IH</sub> , CE2 ≤ V <sub>IL</sub>	Com. Ind.	— 70 80	— 50 55	— 50 55	mA
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., CE1, CE2 ≥ V <sub>CC</sub> - 0.2V, CE2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com. Ind.	— 10 20	— 10 20	— 10 20	mA

**Note:**

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**CAPACITANCE<sup>(1)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**Note:**

1. Tested initially and after any design or process changes that may affect these parameters.

**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	2 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

**AC TEST LOADS**

Figure 1



Figure 2

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	-8		-10		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	8	—	10	—	ns
t <sub>AA</sub>	Address Access Time	—	8	—	10	ns
t <sub>OH</sub>	Output Hold Time	3	—	3	—	ns
t <sub>ACE</sub> t <sub>ACE2</sub>	$\overline{CE1}$ , $\overline{CE2}$ Access Time CE2 Access Time	8	—	—	10	ns
t <sub>OE</sub>	$\overline{OE}$ Access Time	—	4	—	4	ns
t <sub>HZE</sub> <sup>(2)</sup>	$\overline{OE}$ to High-Z Output	0	3	0	3	ns
t <sub>LZE</sub> <sup>(2)</sup>	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t <sub>HZE</sub> <sup>(2)</sup> t <sub>HZE2</sub> <sup>(2)</sup>	$\overline{CE1}$ , $\overline{CE2}$ to High-Z Output CE2 to High-Z Output	0	4	0	5	ns
t <sub>LZE</sub> <sup>(2)</sup> t <sub>LZE2</sub> <sup>(2)</sup>	$\overline{CE}$ , $\overline{CE2}$ to Low-Z Output CE2 to Low-Z Output	3	—	3	—	ns

**Notes:**

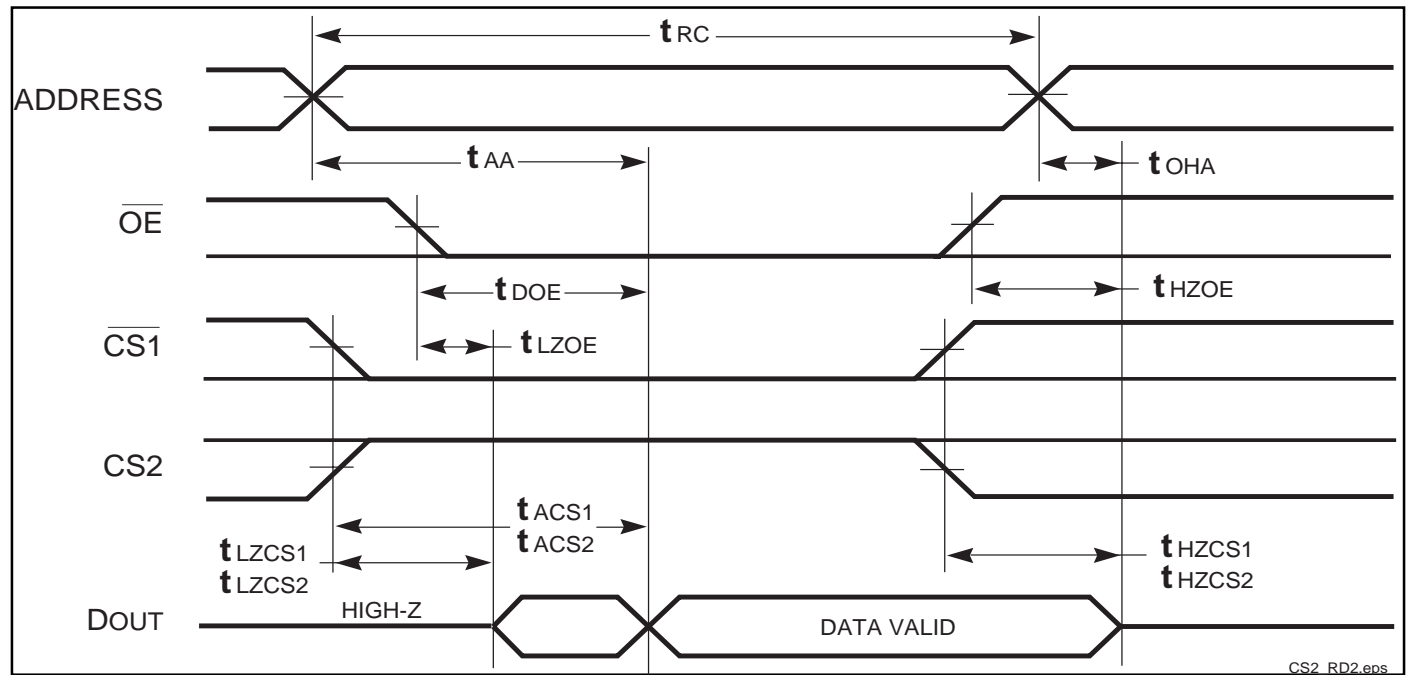
1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 200$  mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup> (Address Controlled) ( $\overline{CE1} = \overline{CE2} = \overline{OE} = V_{IL}$ ;  $CE2 = V_{IH}$ )



READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE1}$ ,  $\overline{CE2} = V_{IL}$ .  $CE2 = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CE1}$ ,  $\overline{CE2}$  LOW and CE2 HIGH transition.

WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup> (Over Operating Range)

Symbol	Parameter	-8		-10		Unit
		Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	8	—	10	—	ns
t <sub>SCE</sub>	$\overline{CE1}$ , $\overline{CE2}$ to Write End	7	—	8	—	ns
t <sub>SCE2</sub>	CE2 to Write End	7	—	8	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	7	—	8	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	ns
t <sub>PWE1</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = HIGH)	6	—	8	—	ns
t <sub>PWE2</sub>	$\overline{WE}$ Pulse Width ( $\overline{OE}$ = LOW)	6	—	9	—	ns
t <sub>SD</sub>	Data Setup to Write End	4.5	—	5	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>HZWE</sub> <sup>(2)</sup>	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	3.5	ns
t <sub>LZWE</sub> <sup>(2)</sup>	$\overline{WE}$ HIGH to Low-Z Output	3	—	3	—	ns

**Notes:**

1. Test conditions assume signal transition times of 2 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 200$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE1}$ ,  $\overline{CE2}$  LOW, CE2 HIGH and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

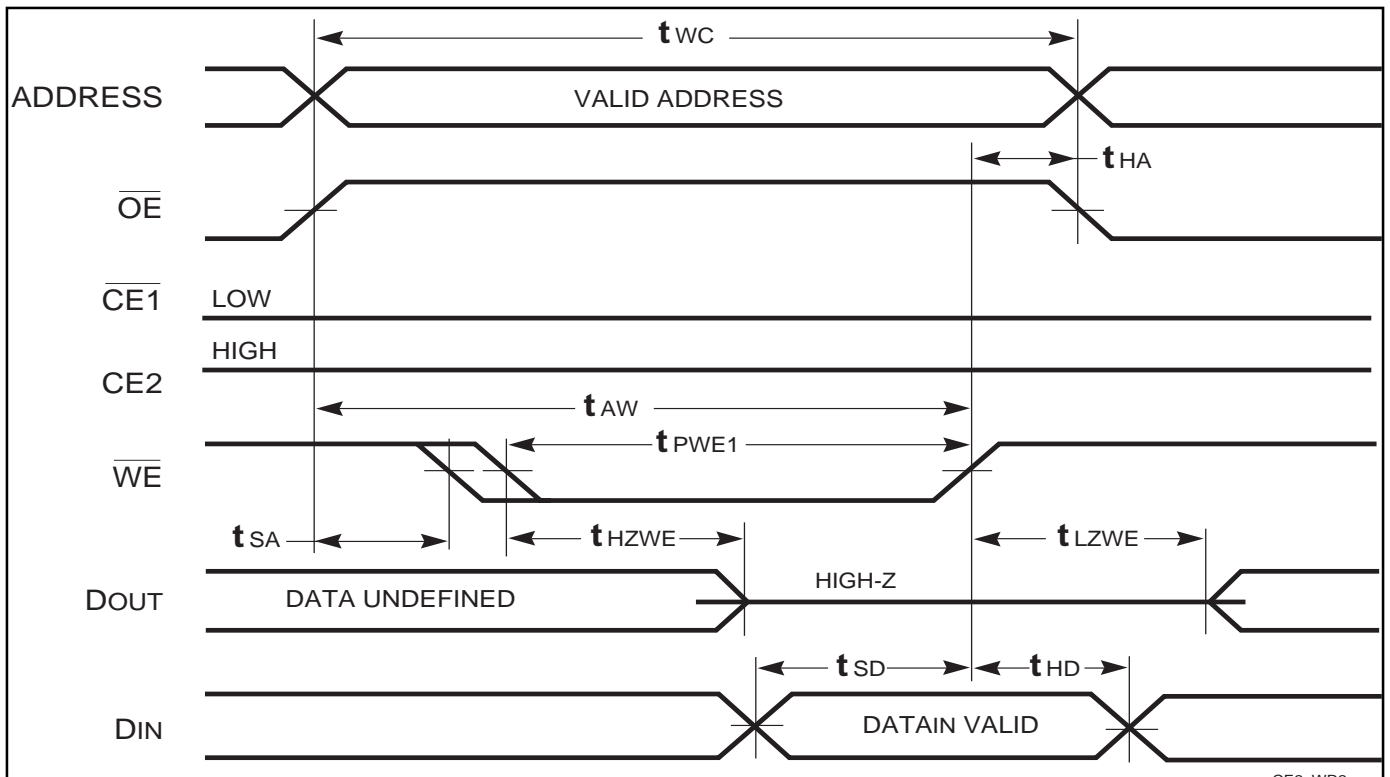


**WRITE CYCLE NO. 1** ( $\overline{CE}$  Controlled,  $\overline{OE} = \text{HIGH or LOW}$ )



CE2\_WR1.eps

**WRITE CYCLE NO. 2<sup>(1)</sup>** ( $\overline{WE}$  Controlled:  $\overline{OE} = \text{HIGH during Write Cycle}$ )



CE2\_WR2.eps

WRITE CYCLE NO. 3<sup>(1)</sup> ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW DURING WRITE CYCLE)**Note:**

1. The internal Write time is defined by the overlap of  $\overline{CE1}$  and  $\overline{CE2} = \text{LOW}$ ,  $\overline{CE2} = \text{HIGH}$  and  $\overline{WE} = \text{LOW}$ . All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Setup and Hold timing is referenced to the rising or falling edge of the signal that terminates the Write.

**ORDERING INFORMATION****Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
8	IS61LV12824-8B	Plastic Ball Grid Array
	IS61LV12824-8BL	Plastic Ball Grid Array, Lead-free
	IS61LV12824-8TQ	TQFP
10	IS61LV12824-10B	Plastic Ball Grid Array
	IS61LV12824-10BL	Plastic Ball Grid Array, Lead-free
	IS61LV12824-10TQ	TQFP

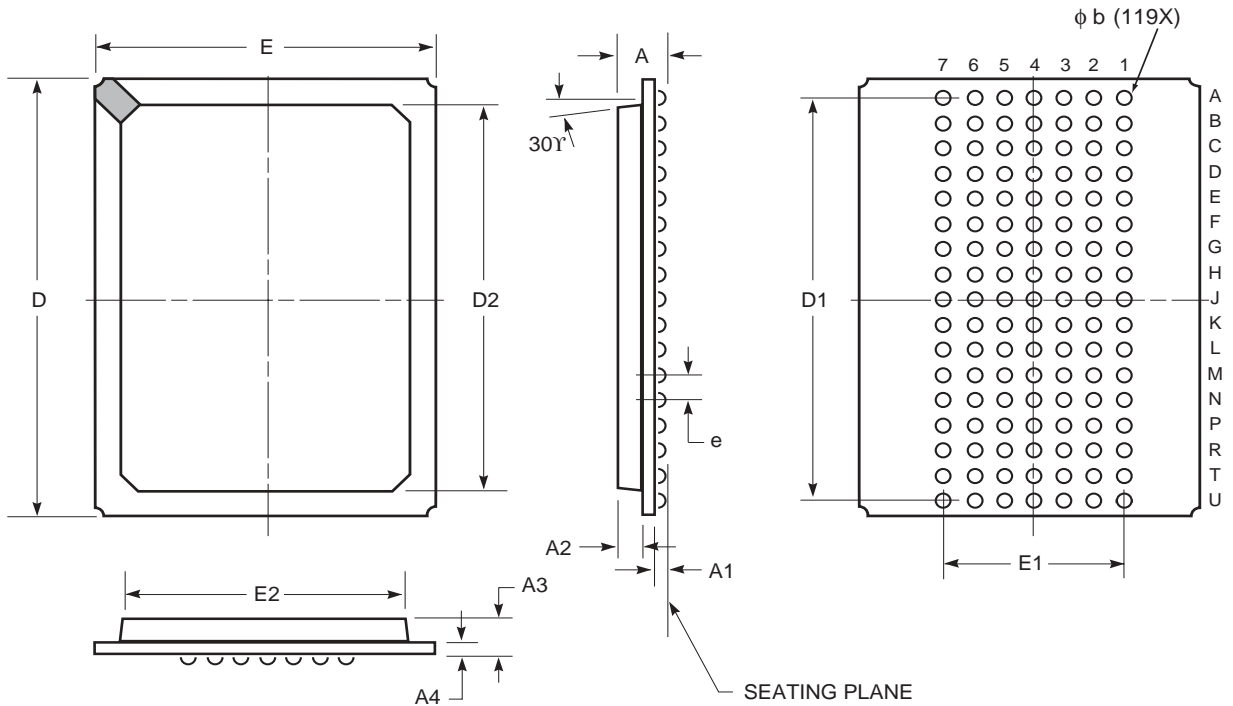
**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
8	IS61LV12824-8BI	Plastic Ball Grid Array
10	IS61LV12824-10BI	Plastic Ball Grid Array
	IS61LV12824-10TQI	TQFP
	IS61LV12824-10TQLI	TQFP, Lead-free

# PACKAGING INFORMATION



## Plastic Ball Grid Array Package Code: B (119-pin)



	MILLIMETERS		INCHES	
Sym.	Min.	Max.	Min.	Max.
N0. Leads	119			
A	—	2.41	—	0.095
A1	0.50	0.70	0.020	0.028
A2	0.80	1.00	0.032	0.039
A3	1.30	1.70	0.051	0.067
A4	0.56 BSC		0.022 BSC	
b	0.60	0.90	0.024	0.035
D	21.80	22.20	0.858	0.874
D1	20.32 BSC		0.800 BSC	
D2	19.40	19.60	0.764	0.772
E	13.80	14.20	0.543	0.559
E1	7.62 BSC		0.300 BSC	
E2	11.90	12.10	0.469	0.476
e	1.27 BSC		0.050 BSC	

### Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC=Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusion and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

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Rev. B  
02/12/03

PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)

Package Code: TQ



Thin Quad Flat Pack (TQ)									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
Ref. Std.									
No. Leads (N)	100				128				
A	—	1.60	—	0.063	—	1.60	—	0.063	
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	
A2	1.35	1.45	0.053	0.057	1.35	1.45	0.053	0.057	
b	0.22	0.38	0.009	0.015	0.17	0.27	0.007	0.011	
D	21.90	22.10	0.862	0.870	21.80	22.20	0.858	0.874	
D1	19.90	20.10	0.783	0.791	19.90	20.10	0.783	0.791	
E	15.90	16.10	0.626	0.634	15.80	16.20	0.622	0.638	
E1	13.90	14.10	0.547	0.555	13.90	14.10	0.547	0.555	
e	0.65 BSC		0.026 BSC		0.50 BSC		0.020 BSC		
L	0.45	0.75	0.018	0.030	0.45	0.75	0.018	0.030	
L1	1.00 REF.		0.039 REF.		1.00 REF.		0.039 REF.		
C	0°	7°	0°	7°	0°	7°	0°	7°	

Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.

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**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331