MCP47FEBXX

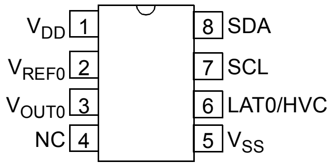
8-/10-/12-Bit Single/Dual Voltage Output Nonvolatile Digital-to-Analog Converters with I^{2}C™ Interface

Features

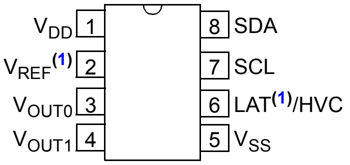
- Operating Voltage Range:
  - 2.7V to 5.5V - Full Specifications
  - 1.8V to 2.7V - Reduced Device Specifications
- Output Voltage Resolutions:
  - 8-bit: **MCP47FEB0X** (256 Steps)
  - 10-bit: **MCP47FEB1X** (1024 Steps)
  - 12-bit: **MCP47FEB2X** (4096 Steps)
- Rail-to-Rail Output
- Fast Settling Time of 6 µs (typical)
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal Band Gap (1.22V typical)
- Output Gain Options:
  - Unity (1x)
  - 2x (when not using internal V_{DD} as voltage source)
- Nonvolatile Memory (EEPROM):
  - User-programmed Power-on Reset (POR)/Brown-out Reset (BOR) output setting recall and device configuration bits
  - Auto Recall of Saved DAC register setting
  - Auto Recall of Saved Device Configuration (Voltage Reference, Gain, Power-Down)
- Power-on/Brown-out Reset Protection
- Nonvolatile Memory Write Protect ($\overline{WP}$) Bit
- Power-Down Modes:
  - Disconnects output buffer (High Impedance)
  - Selection of V_{OUT} pull-down resistors (100 kΩ or 1 kΩ)
- Low Power Consumption:
  - Normal operation: <180 µA (Single), 380 µA (Dual)
  - Power-down operation: 650 nA typical
  - EEPROM write cycle (1.9 mA maximum)
- I^{2}C™ Interface:
  - Slave address options: four predefined addresses or user programmable (all 7 bits)
  - Standard (100 kbps), Fast (400 kbps), and High-Speed (up to 3.4 Mbps) modes
- Package Types: 8-lead TSSOP
- Extended Temperature Range: -40°C to +125°C

Package Types

MCP47FEBX1
TSSOP
Single



MCP47FEBX2
TSSOP
Dual



Note 1: This pin's signal can be connected to DAC0 and/or DAC1.

General Description

The MCP47FEBXX are Single- and Dual-channel 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DAC) with nonvolatile memory and an I^{2}C serial interface.

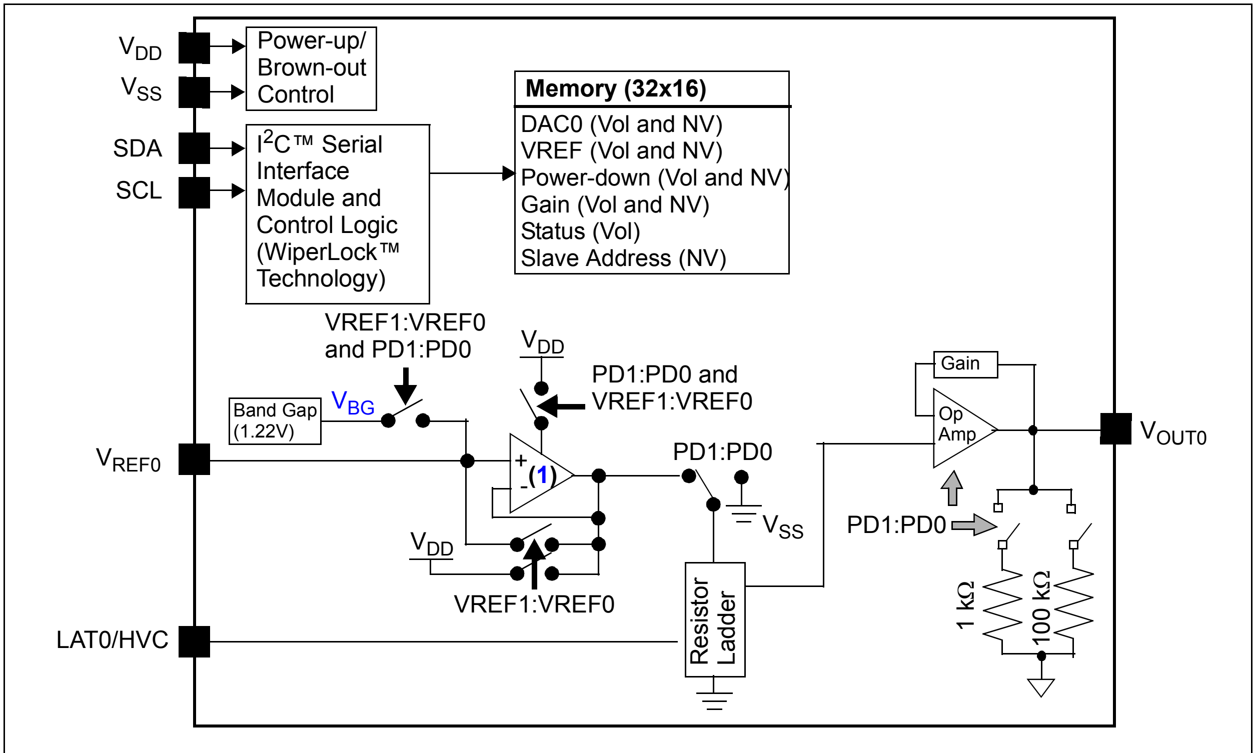
The V_{REF} pin, the device V_{DD} or the internal band gap voltage can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is connected internally to the DAC reference circuit. When the V_{REF} pin is used, the user can select the output buffer's gain to be 1 or 2. When the gain is 2, the V_{REF} pin voltage should be limited to a maximum of $V_{DD}/2$.

These devices have a two-wire I^{2}C-compatible serial interface for Standard (100 kHz), Fast (400 kHz) or High-Speed (1.7 MHz and 3.4 MHz) modes.

Applications

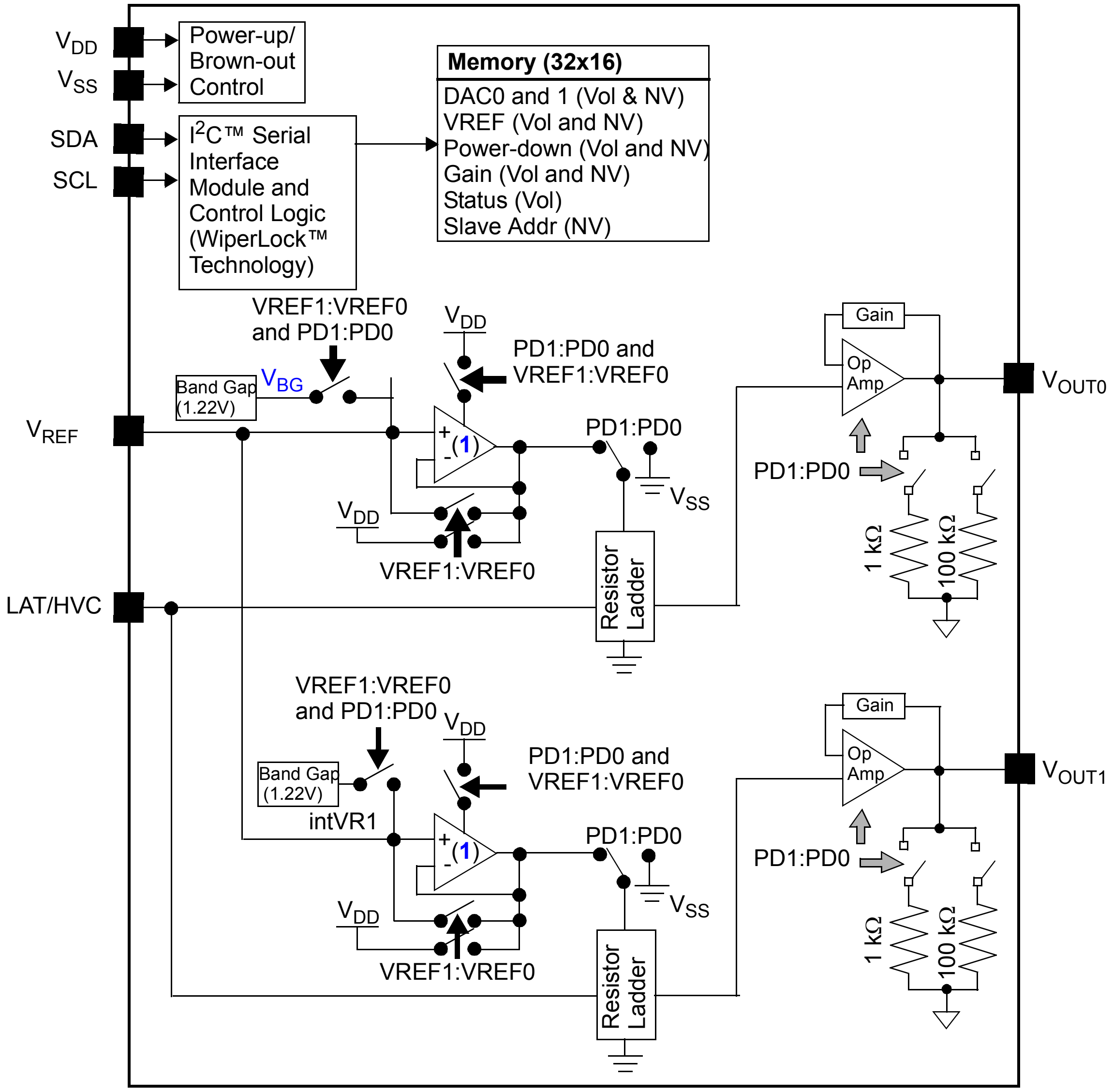
- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems
- Motor Control

MCP47FEBX1 Device Block Diagram (Single-Channel Output)



Note 1: If Internal Band Gap is selected, this buffer has a 2x gain. If the G bit = ‘1’, this is a total gain of 4.

MCP47FEBX2 Device Block Diagram (Dual-Channel Output)



Note 1: If Internal Band Gap is selected, this buffer has a 2x gain, if the G bit = ‘1’, this is a total gain of 4.

Device Features

Device	# of Channels	Resolution (bits)	Control Interface	DAC Output POR/BOR Setting (1)	# of VREF Inputs	Internal band gap ?	# of LAT Inputs	Memory	Specified Operating Range (V_{DD})
MCP47FEB01	1	8	I2C™	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB11	1	10	I2C	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB21	1	12	I2C	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB02	2	8	I2C	7Fh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB12	2	10	I2C	1FFh	1	Yes	1	EEPROM	1.8V to 5.5V
MCP47FEB22	2	12	I2C	7FFh	1	Yes	1	EEPROM	1.8V to 5.5V

Note 1: The Factory Default value. The DAC output POR/BOR value can be modified via the nonvolatile DAC output register(s).

NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Voltage on V_{DD} with respect to V_{SS}		-0.6V to +6.5V
Voltage on all pins with respect to V_{SS}		-0.6V to V_{DD}+0.3V
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ on HV pins)		±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)		±20 mA
Maximum current out of V_{SS} pin	(Single)	50 mA
	(Dual)	100 mA
Maximum current into V_{DD} pin	(Single)	50 mA
	(Dual)	100 mA
Maximum current sourced by the V_{OUT} pin		20 mA
Maximum current sunk by the V_{OUT} pin		20 mA
Maximum current sunk by the V_{REF} pin		125 µA
Maximum input current source/sunk by SDA, SCL pins		2 mA
Maximum output current sunk by SDA Output pin		25 mA
Total power dissipation (1)		400 mW
Package power dissipation (T_A = +50°C, T_J = +150°C)		
TSSOP-8		700 mW
ESD protection on all pins		≥ ±4 kV (HBM)
		≥ ±400V (MM)
		≥ ±2 kV (CDM)
Latch-Up (per JEDEC JESD78A) @ +125°C		±100 mA
Storage temperature		-65°C to +150°C
Ambient temperature with power applied		-55°C to +125°C
Soldering temperature of leads (10 seconds)		+300°C
Maximum Junction Temperature (T_J)		+150°C

> **† Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma\, I_{OH}\} + \Sigma\, \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$$

DC CHARACTERISTICS

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = ‘0’, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	DAC operation (reduced analog specifications) and Serial Interface
V_{DD} Voltage (rising) to ensure device Power-on Reset	$V_{POR/BOR}$	—	—	1.7	V	RAM retention voltage (V_{RAM}) < V_{POR} V_{DD} voltages greater than $V_{POR/BOR}$ limit ensure that device is out of reset.
V_{DD} Rise Rate to ensure Power-on Reset	V_{DDRR}	(**Note 3**)			V/ms	
High-Voltage Commands Voltage Range (HVC pin)	V_{HV}	V_{SS}	—	12.5	V	The HVC pin will be at one of three input levels (V_{IL}, V_{IH} or V_{IHH}) (1)
High-Voltage Input Entry Voltage	V_{IHHEN}	9.0	—	—	V	Threshold for Entry into WiperLock™ Technology
High-Voltage Input Exit Voltage	V_{IHHEX}	—	—	V_{DD} + 0.8V	V	**(Note 1)**
Power-on Reset to Output-Driven Delay	T_{PORD}	—	25	50	µs	V_{DD} rising, V_{DD} > V_{POR}

Note 1 This parameter is ensured by design.

Note 3 POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = ‘0’, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Supply Current	I_{DD}	—	—	500	µA	Single	Serial Interface Active (Not High-Voltage Command), VRxB:VRxA = ‘01’ (6), V_{OUT} is unloaded, V_{DD} = 5.5V volatile DAC Register = 000h I^2C™: F_{SCL} = 3.4 MHz
		—	—	700	µA	Dual	
		—	—	400	µA	Single	Serial Interface Active (2) (Not High-Voltage Command), VRxB:VRxA = ‘10’ (4), V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V volatile DAC Register = 000h I^2C: F_{SCL} = 3.4 MHz
		—	—	550	µA	Dual	
		—	—	180	µA	Single	Serial Interface Inactive (2) (Not High-Voltage Command), VRxB:VRxA = ‘00’, SCL = SDA = V_{SS}, V_{OUT} is unloaded, volatile DAC Register = 000h
		—	—	380	µA	Dual	
		—	—	180	µA	Single	Serial Interface Inactive (2) (Not High-Voltage Command), VRxB:VRxA = ‘11’, V_{REF} = V_{DD}, SCL = SDA = V_{SS}, V_{OUT} is unloaded, volatile DAC Register = 000h
		—	—	380	µA	Dual	
		—	—	1.9	mA	EE Write Current V_{REF} = V_{DD} = 5.5V (after write, Serial Interface is Inactive), write all 0’s to nonvolatile DAC 0 (address 10h), V_{OUT} pins are unloaded.	
		—	145	180	µA	Single	HVC = 12.5V (High-Voltage Command), Serial Interface Inactive V_{REF} = V_{DD} = 5.5V, LAT/HVC = V_{IHH}, DAC registers = 000h, V_{OUT} pins are unloaded.
		—	260	400	µA	Dual	
Power-Down Current	I_{DDP}	—	0.65	3.8	µA	PDxB:PDxA = ‘01’ (5), V_{OUT} not connected	

Note 2 This parameter is ensured by characterization.

Note 4 Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = ‘10’.

Note 5 The PDxB:PDxA = ‘01’, ‘10’, and ‘11’ configurations should have the same current.

Note 6 By design, this is worst-case current mode.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Resistor Ladder Resistance	R_L	100	140	180	kΩ	1.8V ≤ V_{DD} ≤ 5.5V, V_{REF} ≥ 1.0V(7)	
Resolution (# of Resistors and # of Taps) (see **C.1 "Resolution"**)	N	256			Taps	8-bit	No Missing Codes
		1024			Taps	10-bit	No Missing Codes
		4096			Taps	12-bit	No Missing Codes
Nominal V_{OUT} Match (12)	$\lvert V_{OUT} - V_{OUTMEAN}\rvert / V_{OUTMEAN}$	—	0.5	1.0	%	2.7V ≤ V_{DD} ≤ 5.5V(2)	
		—	—	1.2	%	1.8V(2)	
V_{OUT} Tempco (see **C.19 "V_{OUT} Temperature Coefficient"**)	$\Delta V_{OUT}/\Delta T$	—	15	—	ppm/°C	Code = Mid-scale (7Fh, 1FFh or 7FFh)	
V_{REF} pin Input Voltage Range	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V(1)	

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 7 Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = '10') to V_{SS} pin. For dual-channel devices (MCP47FEBX2), this is the effective resistance of the each resistor ladder. The resistance measurement is of the two resistor ladders measured in parallel.

Note 12 Variation of one output voltage to mean output voltage.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Zero-Scale Error (see **C.5 "Zero-Scale Error (EZS)"**) (Code = 000h)	E_{ZS}	—	—	0.75	LSb	8-bit	VRxB:VRxA = '11', Gx = '0', $V_{REF} = V_{DD}$, No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		VRxB:VRxA = '00', Gx = '0', V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		VRxB:VRxA = '01', Gx = '0', No Load
		—	—	3	LSb	10-bit	VRxB:VRxA = '11', Gx = '0', $V_{REF} = V_{DD}$, No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		VRxB:VRxA = '00', Gx = '0', V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		VRxB:VRxA = '01', Gx = '0', No Load
		—	—	12	LSb	12-bit	VRxB:VRxA = '11', Gx = '0', $V_{REF} = V_{DD}$, No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		VRxB:VRxA = '00', Gx = '0', V_{DD} = 5.5V, No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '10', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V VRxB:VRxA = '11', Gx = '0'. No Load
		See **Section 2.0 "Typical Performance Curves"** $^{(2)}$			LSb		VRxB:VRxA = '01', Gx = '0', No Load
Offset Error (see **C.7 "Offset Error (EOS)"**)	E_{OS}	-15	±1.5	+15	mV	VRxB:VRxA = '00', Gx = '0', No Load	
Offset Voltage Temperature Coefficient	V_{OSTC}	—	±10	—	µV/°C		

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = ‘0’, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Full-Scale Error (see **C.4 “Full-Scale Error (EFS)”**)	E_{FS}	—	—	4.5	LSb	8-bit	Code = FFh, VRxB:VRxA = ‘11’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = FFh, VRxB:VRxA = ‘10’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = FFh, VRxB:VRxA = ‘01’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = FFh, VRxB:VRxA = ‘00’, No Load
		—	—	18	LSb	10-bit	Code = 3FFh, VRxB:VRxA = ‘11’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = 3FFh, VRxB:VRxA = ‘10’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = 3FFh, VRxB:VRxA = ‘01’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = 3FFh, VRxB:VRxA = ‘00’, No Load
		—	—	70	LSb	12-bit	Code = FFFh, VRxB:VRxA = ‘11’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = FFFh, VRxB:VRxA = ‘10’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = FFFh, VRxB:VRxA = ‘01’, Gx = ‘0’, V_{REF} = 2.048V, No Load
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Code = FFFh, VRxB:VRxA = ‘00’, No Load

Note 2 This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = ‘0’, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Gain Error (see **C.9 “Gain Error (EG)”**)(9)	E_G	-1.0	±0.1	+1.0	% of FSR	8-bit	Code = 250, No Load VRxB:VRxA = ‘00’, Gx = ‘0’
		-1.0	±0.1	+1.0	% of FSR	10-bit	Code = 1000, No Load VRxB:VRxA = ‘00’, Gx = ‘0’
		-1.0	±0.1	+1.0	% of FSR	12-bit	Code = 4000, No Load VRxB:VRxA = ‘00’, Gx = ‘0’
Gain-Error Drift (see **C.10 “Gain-Error Drift (EGD)”**)	ΔG/°C	—	-3	—	ppm/°C		
Total Unadjusted Error (see **C.6 “Total Unadjusted Error (ET)”**)(2)	E_T	-2.5	—	+0.5	LSb	8-bit	VRxB:VRxA = ‘00’. No Load.
		See **Section 2.0 “Typical Performance Curves”**			LSb		V_{DD} = 1.8V, VRxB:VRxA = ‘11’, Gx = ‘0’, V_{REF} = 1.0V, No Load.
		-10.0	—	+2.0	LSb	10-bit	VRxB:VRxA = ‘00’. No Load.
		See **Section 2.0 “Typical Performance Curves”**			LSb		V_{DD} = 1.8V, VRxB:VRxA = ‘11’, Gx = ‘0’, V_{REF} = 1.0V, No Load.
		-40.0	—	+8.0	LSb	12-bit	VRxB:VRxA = ‘00’. No Load.
		See **Section 2.0 “Typical Performance Curves”**			LSb		V_{DD} = 1.8V, VRxB:VRxA = ‘11’, Gx = ‘0’, V_{REF} = 1.0V, No Load.

Note 2 This parameter is ensured by characterization.

Note 9 This gain error does not include offset error.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = ‘0’, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Integral Nonlinearity (see **C.11 “Integral Nonlinearity (INL)”**)(8, 11)	INL	-0.5	±0.1	+0.5	LSb	8-bit	VRxB:VRxA = ‘10’ (codes: 6 to 250), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘00’, ‘01’, ‘11’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘01’, V_{DD} = 5.5V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘10’, ‘11’, V_{REF} = 1.0V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V
		-1.5	±0.4	+1.5	LSb	10-bit	VRxB:VRxA = ‘10’ (codes: 25 to 1000), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘00’, ‘01’, ‘11’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘01’, V_{DD} = 5.5V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘10’, ‘11’, V_{REF} = 1.0V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V.
		-6	±1.5	+6	LSb	12-bit	VRxB:VRxA = ‘10’ (codes: 100 to 4000), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘00’, ‘01’, ‘11’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘01’, V_{DD} = 5.5V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		VRxB:VRxA = ‘10’, ‘11’, V_{REF} = 1.0V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”**(2)			LSb		V_{DD} = 1.8V, V_{REF} = 1.0V.

Note 2 This parameter is ensured by characterization.

Note 8 INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRxB:VRxA = ‘00’).

Note 11 Code Range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = ‘0’, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Differential Nonlinearity (see **C.12 “Differential Nonlinearity (DNL)”**)(8, 11)	DNL	-0.25	±0.0125	+0.25	LSb	8-bit	VRxB:VRxA = ‘10’ (codes: 6 to 250), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘00’, ‘01’, ‘11’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘01’, V_{DD} = 5.5V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘10’, ‘11’, V_{REF} = 1.0V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		V_{DD} = 1.8V
		-0.5	±0.05	+0.5	LSb	10-bit	VRxB:VRxA = ‘10’ (codes: 25 to 1000), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘00’, ‘01’, ‘11’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘01’, V_{DD} = 5.5V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘10’, ‘11’, V_{REF} = 1.0V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		V_{DD} = 1.8V
		-1.0	±0.2	+1.0	LSb	12-bit	VRxB:VRxA = ‘10’ (codes: 100 to 4000), V_{DD} = V_{REF} = 5.5V.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘00’, ‘01’, ‘11’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘01’, V_{DD} = 5.5V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		Char: VRxB:VRxA = ‘10’, ‘11’, V_{REF} = 1.0V, Gx = ‘1’.
		See **Section 2.0 “Typical Performance Curves”** (2)			LSb		V_{DD} = 1.8V

Note 2 This parameter is ensured by characterization.

Note 8 INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRxB:VRxA = ‘00’).

Note 11 Code Range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = ‘0’, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
-3 dB Bandwidth (see **C.16 “-3 dB Bandwidth”**)	BW	—	86.5	—	kHz	V_{REF} = 2.048V ± 0.1V, VRxB:VRxA = ‘10’, Gx = ‘0’
		—	67.7	—	kHz	V_{REF} = 2.048V ± 0.1V, VRxB:VRxA = ‘10’, Gx = ‘1’
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	0.01	—	V	1.8V ≤ V_{DD} < 5.5V, Output Amplifier’s minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{DD} – 0.04	—	V	1.8V ≤ V_{DD} < 5.5V, Output Amplifier’s maximum drive
Phase Margin	PM	—	66	—	Degree (°)	C_L = 400 pF, R_L = ∞
Slew Rate (10)	SR	—	0.44	—	V/µs	R_L = 5 kΩ
Short-Circuit Current	I_{SC}	3	9	14	mA	DAC code = Full Scale
Internal Band Gap						
Band Gap Voltage	V_{BG}	1.18	1.22	1.26	V	
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	15	—	ppm/°C	
Operating Range (V_{DD})		2.0	—	5.5	V	V_{REF} pin voltage stable
		2.2	—	5.5	V	V_{OUT} output linear
External Reference (V_{REF})						
Input Range (1)	V_{REF}	V_{SS}	—	V_{DD} – 0.04	V	VRxB:VRxA = ‘11’ (buffered mode)
		V_{SS}	—	V_{DD}	V	VRxB:VRxA = ‘10’ (unbuffered mode)
Input Capacitance	C_{REF}	—	1	—	pF	VRxB:VRxA = ‘10’ (unbuffered mode)
Total Harmonic Distortion (1)	THD	—	-64	—	dB	V_{REF} = 2.048V ± 0.1V, VRxB:VRxA = ‘10’, Gx = ‘0’, Frequency = 1 kHz
Dynamic Performance						
Major Code Transition Glitch (see **C.14 “Major-Code Transition Glitch”**)		—	45	—	nV-s	1 LSb change around major carry (7FFh to 800h)
Digital Feedthrough (see **C.15 “Digital Feed-through”**)		—	<10	—	nV-s	

Note 1 This parameter is ensured by design.

Note 10 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).

DC CHARACTERISTICS (CONTINUED)

DC Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature $-40°C \le T_A \le +125°C$ (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Inputs/Outputs ($\overline{\text{LAT0}}$/HVC)						
Schmitt Trigger High-Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	$2.7V \le V_{DD} \le 5.5V$ (Allows 2.7V Digital V_{DD} with 5V Analog V_{DD})
		0.5 V_{DD}	—	—	V	$1.8V \le V_{DD} \le 2.7V$
Schmitt Trigger Low-Input Threshold	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V	
Input Leakage Current	I_{IL}	-1	—	1	µA	$V_{IN} = V_{DD}$ and $V_{IN} = V_{SS}$
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 3.4 MHz
Digital Interface (SDA, SCL)						
Output Low Voltage	V_{OL}	—	—	0.4	V	$V_{DD} \ge 2.0V$, I_{OL} = 3 mA
		—	—	0.2 V_{DD}	V	$V_{DD} < 2.0V$, I_{OL} = 1 mA
Input High Voltage (SDA and SCL Pins)	V_{IH}	0.7 V_{DD}	—	—	V	$1.8V \le V_{DD} \le 5.5V$
Input Low Voltage (SDA and SCL Pins)	V_{IL}	—	—	0.3 V_{DD}	V	$1.8V \le V_{DD} \le 5.5V$
Input Leakage	I_{LI}	-1	—	1	µA	SCL = SDA = V_{SS} or SCL = SDA = V_{DD}
Pin Capacitance	C_{PIN}	—	10	—	pF	f_C = 3.4 MHz

Note 1 This parameter is ensured by design.

DC CHARACTERISTICS (CONTINUED)

DC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = '0', R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
RAM Value							
Value Range	N	0h	—	FFh	hex	8-bit	
		0h	—	3FFh	hex	10-bit	
		0h	—	FFFh	hex	12-bit	
DAC Register POR/BOR Value	N	See **Table 4-2**			hex	8-bit	
		See **Table 4-2**			hex	10-bit	
		See **Table 4-2**			hex	12-bit	
PDCON Initial Factory Setting		See **Table 4-2**			hex		
EEPROM							
Endurance	EN_{EE}	—	1M	—	Cycles	**Note 1**, **Note 2**	
Data Retention	DR_{EE}	—	200	—	Years	At +25°C(1, 2)	
EEPROM Range	N	0h	—	FFh	hex	8-bit	DACx Register(s)
		0h	—	3FFh	hex	10-bit	DACx Register(s)
		0h	—	FFFh	hex	12-bit	DACx Register(s)
Initial Factory Setting	N	See **Table 4-2**					
EEPROM Programming Write Cycle Time	t_{WC}	—	11	16	ms	V_{DD} = +1.8V to 5.5V	
Power Requirements							
Power Supply Sensitivity (**C.17 "Power-Supply Sensitivity (PSS)"**)	PSS	—	0.002	0.005	%/%	8-bit	Code = 7Fh
		—	0.002	0.005	%/%	10-bit	Code = 1FFh
		—	0.002	0.005	%/%	12-bit	Code = 7FFh

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = ‘`10`’.
5. The PDxB:PDxA = ‘`01`’, ‘`10`’, and ‘`11`’ configurations should have the same current.
6. By design, this is worst-case current mode.
7. Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = ‘`10`’) to V_{SS} pin. For dual-channel devices (MCP47FEBX2), this is the effective resistance of the each resistor ladder. The resistance measurement is of the two resistor ladders measured in parallel.
8. INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRxB:VRxA = ‘`00`’).
9. This gain error does not include offset error.
10. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).
11. Code Range dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.
12. Variation of one output voltage to mean output voltage.

1.1 Timing Waveforms and Requirements

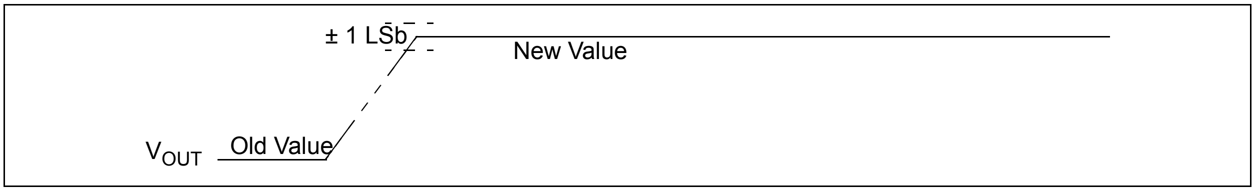


FIGURE 1-1: *V_{OUT} Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +1.8V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time (±1LSb error band, C_L = 100 pF) (see **C.13 “Settling Time”**)	t_S	—	6	—	µs	8-bit	Code = 3Fh → BFh; BFh → 3Fh(1)
		—	6	—	µs	10-bit	Code = 0FFh → 2FFh; 2FFh → 0FFh(1)
		—	6	—	µs	12-bit	Code = 3FFh → BFFh; BFFh → 3FFh(1)

Note 1 Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).

1.2 I²C Mode Timing Waveforms and Requirements

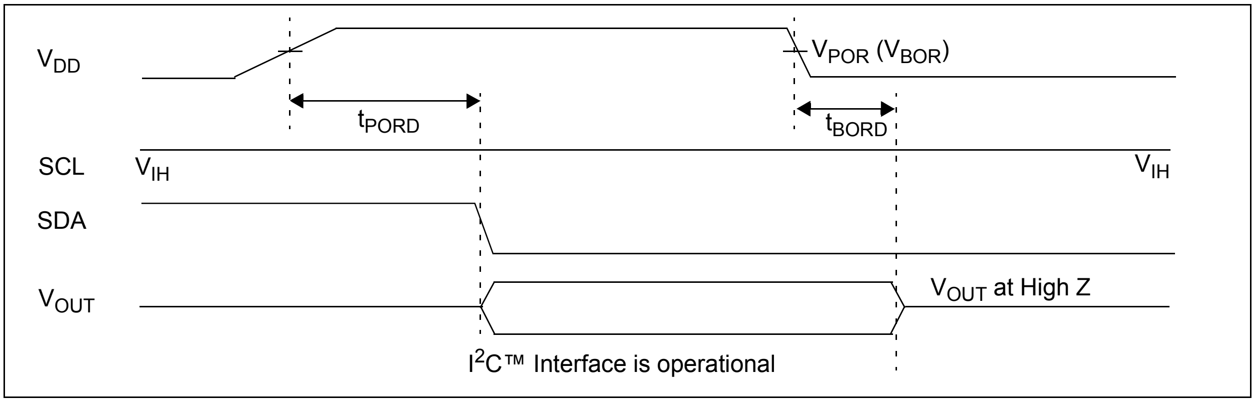


FIGURE 1-2: *Power-on and Brown-out Reset Waveforms.*

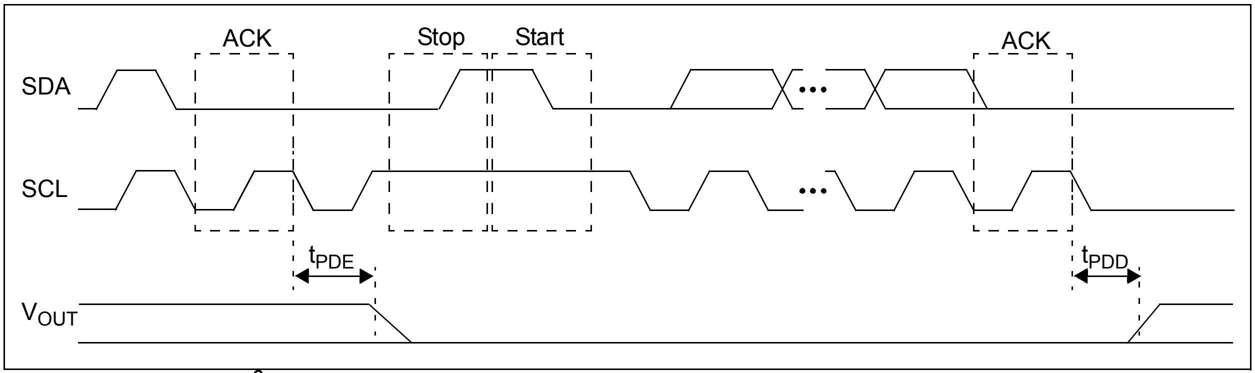


FIGURE 1-3: *I²C™ Power-Down Command Timing.*

TABLE 1-2: RESET TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +1.8V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power-on Reset Delay	t_{PORD}	—	60	—	µs	Monitor ACK bit response to ensure device responds to command.
Brown-out Reset Delay	t_{BORD}	—	45	—	µs	V_{DD} transitions from $V_{DD(MIN)}$ → > V_{POR} V_{OUT} driven to V_{OUT} disabled
Power-Down Output Disable Time Delay	T_{PDD}	—	10.5	—	µs	PDxB:PDxA = ‘`11`’, ‘`10`’, or ‘`01`’ -> “`00`” started from falling edge of the SCL at the end of the 8th clock cycle. Volatile DAC Register = FFh, V_{OUT} = 10 mV. V_{OUT} not connected.
Power-Down Output Enable Time Delay	T_{PDE}	—	1	—	µs	PDxB:PDxA = “`00`” → ‘`11`’, ‘`10`’, or ‘`01`’ started from falling edge of the SCL at the end of the 8th clock cycle. V_{OUT} = V_{OUT} - 10 mV. V_{OUT} not connected.

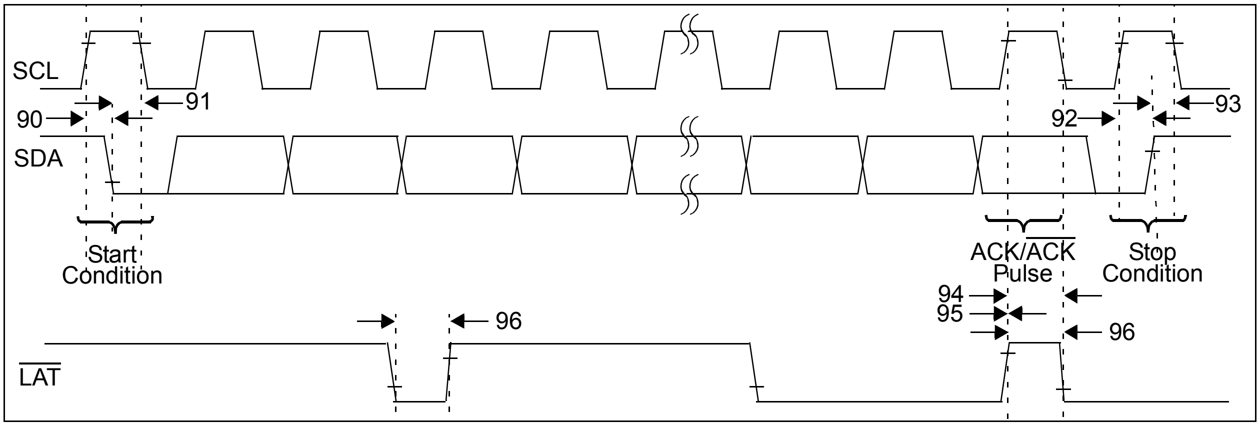


FIGURE 1-4: *I^2C™ Bus Start/Stop Bits Timing Waveforms.*

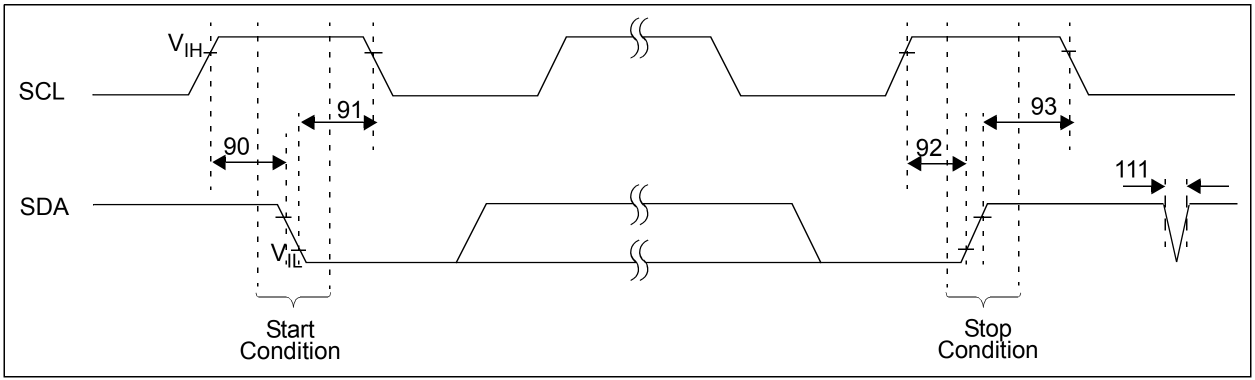


FIGURE 1-5: *I^2C™ Bus Start/Stop Bits Timing Waveforms.*

TABLE 1-3: I^2C BUS START/STOP BITS AND $\overline{\text{LAT}}$ REQUIREMENTS

I^2C™ AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) Operating Voltage range is described in **DC Characteristics**

Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
	F_{SCL}		Standard Mode	0	100	kHz	C_b = 400 pF, 1.8V - 5.5V(2)
			Fast Mode	0	400	kHz	C_b = 400 pF, 2.7V - 5.5V
			High-Speed 1.7	0	1.7	MHz	C_b = 400 pF, 4.5V - 5.5V
			High-Speed 3.4	0	3.4	MHz	C_b = 100 pF, 4.5V - 5.5V
D102	C_b	Bus Capacitive Loading	100 kHz mode	—	400	pF	
			400 kHz mode	—	400	pF	
			1.7 MHz mode	—	400	pF	
			3.4 MHz mode	—	100	pF	
90	$T_{SU:STA}$	Start Condition Setup Time (Only relevant for repeated Start condition)	100 kHz mode	4700	—	ns	**Note 2**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
91	$T_{HD:STA}$	Start Condition Hold time (After this period the first clock pulse is generated)	100 kHz mode	4000	—	ns	**Note 2**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
92	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	4000	—	ns	**Note 2**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
93	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	4000	—	ns	**Note 2**
			400 kHz mode	600	—	ns	
			1.7 MHz mode	160	—	ns	
			3.4 MHz mode	160	—	ns	
94	T_{LATSU}	$\overline{\text{LAT}}$ ↑ to SCL↑ (write data ACK bit) Setup Time		10	—	ns	Write Data delayed(3)
95	T_{LATHD}	SCL ↑ to $\overline{\text{LAT}}$↑ (write data ACK bit) Hold Time		250	—	ns	Write Data delayed(3)
96	T_{LAT}	$\overline{\text{LAT}}$ High or Low Time		50	—	ns	
97	T_{HVCSU}	HVC High to SCL High (of Start condition) - Setup Time		25	—	µs	High-Voltage Commands
98	T_{HVCHD}	SCL Low (of Stop condition) to HVC Low - Hold Time		25	—	µs	High-Voltage Commands

Note 2 Not Tested. This parameter ensured by characterization.

Note 3 The transition of the LAT signal between 10 ns before the rising edge (Spec 94) and 250 ns after the rising edge (Spec 95) of the SCL signal is indeterminate whether the change in V_{OUT} is delayed or not.

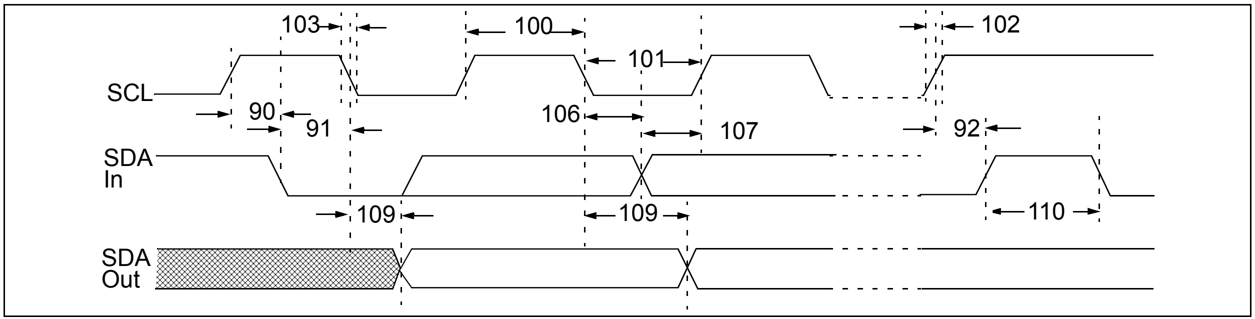


FIGURE 1-6: I^{2}C™ Bus Timing Waveforms.

TABLE 1-4: I^{2}C BUS REQUIREMENTS (SLAVE MODE)

I^{2}C™ AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C (Extended) Operating Voltage range is described in **DC Characteristics**

Param. No.	**Sym.**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
100	T_{HIGH}	Clock high time	100 kHz mode	4000	—	ns	1.8V-5.5V(2)
			400 kHz mode	600	—	ns	2.7V-5.5V
			1.7 MHz mode	120	—	ns	4.5V-5.5V
			3.4 MHz mode	60	—	ns	4.5V-5.5V
101	T_{LOW}	Clock low time	100 kHz mode	4700	—	ns	1.8V-5.5V(2)
			400 kHz mode	1300	—	ns	2.7V-5.5V
			1.7 MHz mode	320	—	ns	4.5V-5.5V
			3.4 MHz mode	160	—	ns	4.5V-5.5V
102A(2)	T_{RSCL}	SCL rise time	100 kHz mode	—	1000	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	80	ns	
			1.7 MHz mode	20	160	ns	After a Repeated Start condition or an Acknowledge bit
			3.4 MHz mode	10	40	ns	
			3.4 MHz mode	10	80	ns	After a Repeated Start condition or an Acknowledge bit
102B(2)	T_{RSDA}	SDA rise time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)
			400 kHz mode	20 + 0.1C_b	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	

Note 2 Not Tested. This parameter ensured by characterization.

TABLE 1-5: I^2C BUS REQUIREMENTS (SLAVE MODE) (CONTINUED)

I^2C™ AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ T_A ≤ +125°C (Extended) Operating Voltage range is described in **DC Characteristics**

Param. No.	Sym.	Characteristic		Min.	Max.	Units	Conditions
103A(2)	T_{FSCL}	SCL fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4)
			400 kHz mode	$20 + 0.1C_b$	300	ns	
			1.7 MHz mode	20	80	ns	
			3.4 MHz mode	10	40	ns	
103B (2)	T_{FSDA}	SDA fall time	100 kHz mode	—	300	ns	C_b is specified to be from 10 to 400 pF (100 pF maximum for 3.4 MHz mode)(4)
			400 kHz mode	$20 + 0.1C_b$	300	ns	
			1.7 MHz mode	20	160	ns	
			3.4 MHz mode	10	80	ns	
106	$T_{HD:DAT}$	Data input hold time	100 kHz mode	0	—	ns	1.8V-5.5V(2, 5)
			400 kHz mode	0	—	ns	2.7V-5.5V(5)
			1.7 MHz mode	0	—	ns	4.5V-5.5V(5)
			3.4 MHz mode	0	—	ns	4.5V-5.5V(5)
107	$T_{SU:DAT}$	Data input setup time	100 kHz mode	250	—	ns	**Note 2**, **Note 6**
			400 kHz mode	100	—	ns	**Note 6**
			1.7 MHz mode	10	—	ns	
			3.4 MHz mode	10	—	ns	
109	T_{AA}	Output valid from clock	100 kHz mode	—	3450	ns	**Note 2**, **Note 7**
			400 kHz mode	—	900	ns	**Note 7**
			1.7 MHz mode	—	150	ns	C_b = 100 pF(7, 8)
				—	310	ns	C_b = 400 pF(2, 7)
			3.4 MHz mode	—	150	ns	C_b = 100 pF(7)
110	T_{BUF}	Bus free time	100 kHz mode	4700	—	ns	Time the bus must be free before a new transmission can start(2)
			400 kHz mode	1300	—	ns	
			1.7 MHz mode	N.A.	—	ns	
			3.4 MHz mode	N.A.	—	ns	
111	T_{SP}	Input filter spike suppression (SDA and SCL)	100 kHz mode	—	50	ns	NXP Spec states N.A.(2)
			400 kHz mode	—	50	ns	
			1.7 MHz mode	—	10	ns	Spike suppression
			3.4 MHz mode	—	10	ns	Spike suppression

Note 2 Not Tested. This parameter ensured by characterization.

Note 4 Use Cb in pF for the calculations.

Note 5 A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.

Note 6 A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode (100 kHz) I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.

Note 7 As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

Note 8 Ensured by the T_{AA} 3.4 MHz specification test.

Timing Table Notes:

1. Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12- bit device).
2. Not Tested. This parameter ensured by characterization.
3. The transition of the LAT signal between 10 ns before the rising edge (Spec 94) and 250 ns after the rising edge (Spec 95) of the SCL signal is indeterminate whether the change in V_{OUT} is delayed or not.
4. Use Cb in pF for the calculations.
5. A Master Transmitter must provide a delay to ensure that difference between SDA and SCL fall times do not unintentionally create a Start or Stop condition.
6. A fast-mode (400 kHz) I^2C-bus device can be used in a standard-mode (100 kHz) I^2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the Low period of the SCL signal. If such a device does stretch the Low period of the SCL signal, it must output the next data bit to the SDA line
   T_R max.+$t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I^2C bus specification) before the SCL line is released.
7. As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
8. Ensured by the T_{AA} 3.4 MHz specification test.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	139	—	°C/W	

Note 1: The MCP47FEBXX devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of +150°C.

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The device Performance Curves are available in a separate document. This is done to keep the file size of this PDF document less than the 10 MB file attachment limit of many mail servers.
The MCP47FXBXX Performance Curves document is literature number DS20005378, and can be found on the Microchip website. Look at the MCP47FEBXX product page under “Documentation and Software”, in the Data Sheets category.

NOTES:

3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided in **Sections 3.1 "Positive Power Supply Input (V_{DD})"** through **Section 3.8 "I^2C - Serial Data Pin (SDA)"**. The descriptions of the pins for the single-DAC output device are listed in Table 3-1, and descriptions for the dual-DAC output device are listed in Table 3-2.

TABLE 3-1: MCP47FEBX1 (SINGLE-DAC) PINOUT DESCRIPTION

Pin				Standard Function
TSSOP-8L	Symbol	I/O	Buffer Type	
1	V_{DD}	—	P	Supply Voltage Pin
2	V_{REF0}	A	Analog	Voltage Reference Input Pin
3	V_{OUT0}	A	Analog	Buffered analog voltage output pin
4	NC	—	—	Not Internally Connected
5	V_{SS}	—	P	Ground reference pin for all circuitries on the device
6	LAT0/HVC	I	HV ST	DAC Register Latch/High-Voltage Command Pin. Latch Pin allows the value in the Serial Shift Register to transfer to the volatile DAC register. High-Voltage Command allows User Configuration bits to be written.
7	SCL	I	ST	I^2C™ Serial Clock Pin
8	SDA	I/O	ST	I^2C Serial Data Pin

Legend: A = Analog ST = Schmitt Trigger
I = Input O = Output I/O = Input/Output P = Power

TABLE 3-2: MCP47FEBX2 (DUAL-DAC) PINOUT DESCRIPTION

Pin				Standard Function
TSSOP-8	Symbol	I/O	Buffer Type	
1	V_{DD}	—	P	Supply Voltage Pin
2	V_{REF}	A	Analog	Voltage Reference Input Pin (for DAC0 or DAC0 and DAC1)
3	V_{OUT0}	A	Analog	Buffered analog voltage output 0 pin (DAC0 output)
4	V_{OUT1}	A	Analog	Buffered analog voltage output 1 pin (DAC1 output)
5	V_{SS}	—	P	Ground reference pin for all circuitries on the device
6	LAT/HVC	I	HV ST	DAC Register Latch/High-Voltage Command Pin. Latch Pin allows the value in the Serial Shift Register to transfer to the volatile DAC register(s) (for DAC0 or DAC0 and DAC1). High-Voltage Command allows User Configuration bits to be written.
7	SCL	I	ST	I^2C™ Serial Clock Pin
8	SDA	I/O	ST	I^2C Serial Data Pin

Legend: A = Analog ST = Schmitt Trigger
I = Input O = Output I/O = Input/Output P = Power

3.1 Positive Power Supply Input (V_{DD})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS}.

The power supply at the V_{DD} pin should be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate noise present in application boards.

3.2 Voltage Reference Pin (V_{REF})

The V_{REF} pin is either an input or an output. When the DAC's voltage reference is configured as the V_{REF} pin, the pin is an input. When the DAC's voltage reference is configured as the internal band gap, the pin is an output.

When the DAC's voltage reference is configured as the V_{REF} pin, there are two options for this voltage input: V_{REF} pin voltage buffered or unbuffered. The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop it's voltage when connected to the internal resistor ladder circuit.

When the DAC's voltage reference is configured as the device V_{DD}, the V_{REF} pin is disconnected from the internal circuit.

When the DAC's voltage reference is configured as the internal band gap, the V_{REF} pin's drive capability is minimal, so the output signal should be buffered.

See **Section 5.2 "Voltage Reference Selection"** and Register 4-2 for more details on the Configuration bits.

3.3 Analog Output Voltage Pin (V_{OUT})

V_{OUT} is the DAC analog voltage output pin. The DAC output has an output amplifier. The DAC output range is dependent on the selection of the voltage reference source (and potential Output Gain selection). These are:

- Device V_{DD} - The full-scale range of the DAC output is from V_{SS} to approximately V_{DD}.
- V_{REF} pin - The full-scale range of the DAC output is from V_{SS} to $G * V_{RL}$, where G is the gain selection option (1x or 2x).
- Internal Band Gap - The full-scale range of the DAC output is from V_{SS} to $G * (2 * V_{BG})$, where G is the gain selection option (1x or 2x).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 100 kΩ, or open. The Power-Down selection bits settings are shown Register 4-3 (Table 5-5).

3.4 No Connect (NC)

The NC pin is not connected to the device.

3.5 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.6 Latch Pin (LAT)/High-Voltage Command (HVC)

The LAT pin is used to force the transfer of the DAC register's shift register to the DAC output register. This allows DAC outputs to be updated at the same time.

The update of the VRxB:VRxA, PDxB:PDxA, Gx bits are also controlled by the LAT pin state.

The HVC pin allows the device's nonvolatile user configuration bits to be programmed when the HVC pin is greater than the V_{IHH} entry voltage.

3.7 I^2C - Serial Clock Pin (SCL)

The SCL pin is the serial clock pin of the I^2C interface. The MCP47FEBXX's I^2C interface only acts as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the V_{DD} line to the SCL pin. Refer to **Section 6.0 "I^2C Serial Interface Module"** for more details of I^2C Serial Interface communication.

3.8 I^2C - Serial Data Pin (SDA)

The SDA pin is the serial data pin of the I^2C interface. The SDA pin is used to write or read the DAC registers and Configuration bits. The SDA pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the V_{DD} line to the SDA pin. Except for Start and Stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 6.0 "I^2C Serial Interface Module"** for more details of I^2C Serial Interface communication.

4.0 GENERAL DESCRIPTION

The MCP47FEBX1 (MCP47FEB01, MCP47FEB11, and MCP47FEB21) devices are single-channel voltage output devices. MCP47FEBX2 (MCP47FEB02, MCP47FEB12, and MCP47FEB22) devices are dual-channel voltage output devices.

These devices are offered with 8-bit (MCP47FEB0X), 10-bit (MCP47FEB1X) and 12-bit (MCP47FEB2X) resolution and include nonvolatile memory (EEPROM), an I^{2}C serial interface and a write latch (LAT) pin to control the update of the written DAC value to the DAC output pin.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device's internal V_{DD}, an external V_{REF} pin voltage (buffered or unbuffered) or an internal band gap voltage source.

The DAC output is buffered with a low power and precision output amplifier (op amp). This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1x or 2x) of the output buffer is software configurable.

This device also has user-programmable nonvolatile memory (EEPROM), which allows the user to save the desired POR/BOR value of the DAC register and device configuration bits. High Voltage lock bits can be used to ensure that the devices output settings are not accidentally modified.

The devices operates from a single supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation, and from 1.8V to 5.5V for digital operation. The device operates between 1.8V and 2.7V, but some device parameters are not specified.

The main functional blocks are:

- **Power-on Reset/Brown-out Reset (POR/BOR)**
- **Device Memory**
- **Resistor Ladder**
- **Output Buffer/V_{OUT} Operation**
- **Internal Band Gap (Voltage Reference)**
- **I^{2}C Serial Interface Module**

4.1 Power-on Reset/Brown-out Reset (POR/BOR)

The internal Power-on Reset (POR)/Brown-out Reset (BOR) circuit monitors the power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events. The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

POR occurs as the voltage is rising (typically from 0V), while BOR occurs as the voltage is falling (typically from $V_{DD(MIN)}$ or higher).

The POR and BOR trip points are at the same voltage, and the condition is determined by whether the V_{DD} voltage is rising or falling (see Figure 4-1). What occurs is different depending on if the reset is a POR or BOR reset.

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its EEPROM and reading and writing to its volatile memory if the proper serial command is executed.

4.1.1 POWER-ON RESET

The Power-on Reset is the case where the device V_{DD} is having power applied to it from the V_{SS} voltage level. As the device powers-up, the V_{OUT} pin will float to an unknown value. When the device's V_{DD} is above the transistor threshold voltage of the device, the output will start being pulled low. After the V_{DD} is above the POR/BOR trip point (V_{BOR}/V_{POR}), the resistor network's wiper will be loaded with the POR value (mid-scale). The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered-up, the user can update the device memory.

When the rising V_{DD} voltage crosses the V_{POR} trip point, the following occurs:

- Nonvolatile DAC register value latched into volatile DAC register
- Nonvolatile Configuration bit values latched into volatile Configuration bits
- POR Status bit is set (`'1'`)
- The Reset Delay Timer (t_{PORD}) starts; when the reset delay timer (t_{PORD}) times out, the I^2C serial interface is operational. During this delay time, the I^2C interface will not accept commands.
- The Device Memory Address pointer is forced to 00h.

The analog output (V_{OUT}) state will be determined by the state of the volatile Configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

4.1.2 BROWN-OUT RESET

The Brown-out Reset occurs when a device had power applied to it, and that power (voltage) drops below the specified range.

When the falling V_{DD} voltage crosses the V_{POR} trip point (BOR event), the following occurs:

- Serial Interface is disabled
- EEPROM Writes are disabled
- Device is forced into a power-down state (PDxB:PDxA = `'11'`). Analog circuitry is turned off.
- Volatile DAC Register is forced to 000h
- Volatile configuration bits VRxB:VRxA and Gx are forced to `'0'`

If the V_{DD} voltage decreases below the V_{RAM} voltage, all volatile memory may become corrupted.

As the voltage recovers above the V_{POR}/V_{BOR} voltage see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a brown-out condition may cause the memory location (volatile and nonvolatile) to become corrupted.

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

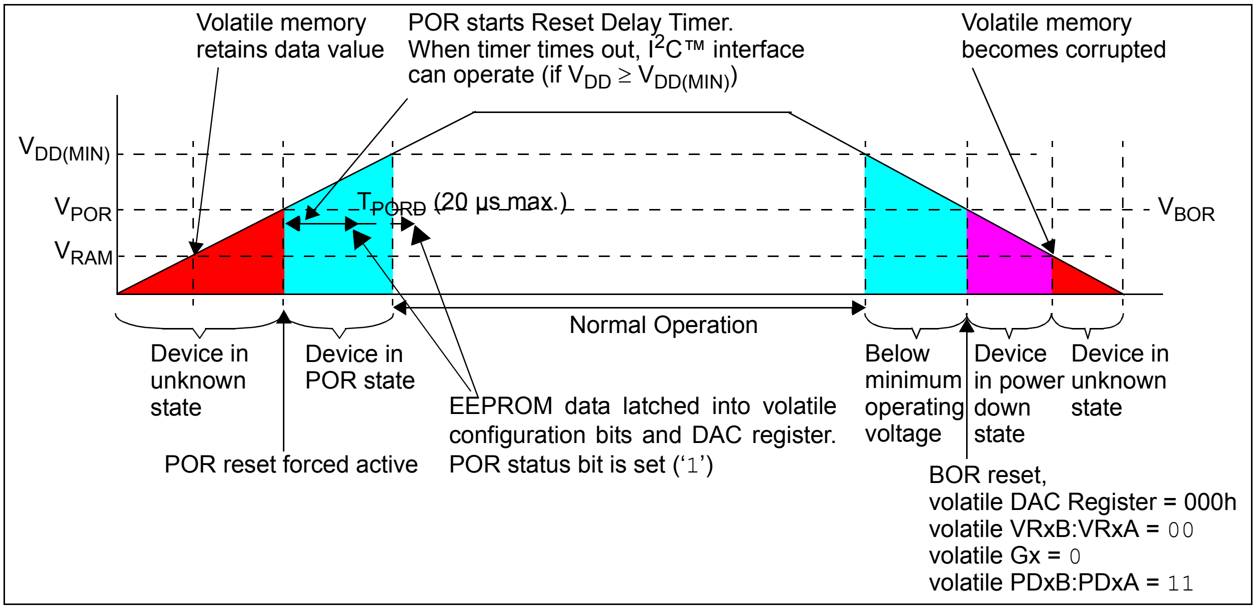


FIGURE 4-1: Power-on Reset Operation.

4.2 Device Memory

User memory includes three types of memory:

- **Volatile Register Memory (RAM)**
- **Nonvolatile Register Memory**
- **Device Configuration Memory**

Each memory address is 16 bits wide. There are five nonvolatile user-control bits that do not reside in memory mapped register space (see **Section 4.2.3 “Device Configuration Memory”**).

4.2.1 VOLATILE REGISTER MEMORY (RAM)

There are up to six Volatile Memory locations:

- DAC0 and DAC1 Output Value Registers
- VREF Select Register
- Power-Down Configuration Register
- Gain and Status Register
- WiperLock Technology Status Register

The volatile memory starts functioning when the device V_{DD} is at (or above) the RAM retention voltage (V_{RAM}). The volatile memory will be loaded with the default device values when the V_{DD} rises across the V_{POR}/V_{BOR} voltage trip point.

4.2.2 NONVOLATILE REGISTER MEMORY

This memory can be grouped into two uses of nonvolatile memory. These are the DAC Output Value and Configuration registers:

- Nonvolatile DAC0 and DAC1 Output Value Registers
- Nonvolatile VREF Select Register
- Nonvolatile Power Down Configuration Register
- Nonvolatile Gain and I^2C Slave Address

The nonvolatile memory starts functioning below the device’s V_{POR}/V_{BOR} trip point and is loaded into the corresponding volatile registers whenever the device rises above the POR/BOR voltage trip point.

The device starts writing the EEPROM memory location at the completion of the serial interface command. For the I^2C interface, this is the acknowledge pulse of the EEPROM write command.

> **Note:** When the nonvolatile memory is written, the corresponding volatile memory is **not** modified.

The nonvolatile DAC registers enables stand-alone operation of the device (without Microcontroller control) after being programmed to the desired value.

TABLE 4-1: MEMORY MAP (x16)

Address	Function	Config Bit (1)
00h	Volatile DAC0 Register	CL0
01h	Volatile DAC1 Register	CL1
02h	Reserved	—
03h	Reserved	—
04h	Reserved	—
05h	Reserved	—
06h	Reserved	—
07h	Reserved	—
08h	V_{REF} Register	—
09h	Power-Down Register	—
0Ah	Gain and Status Register	—
0Bh	WiperLock Technology Status Register	—
0Ch	Reserved	—
0Dh	Reserved	—
0Eh	Reserved	—
0Fh	Reserved	—
10h	Nonvolatile DAC0 Register	DL0
11h	Nonvolatile DAC1 Register	DL1
12h	Reserved	—
13h	Reserved	—
14h	Reserved	—
15h	Reserved	—
16h	Reserved	—
17h	Reserved	—
18h	Nonvolatile V_{REF} Register	—
19h	Nonvolatile Power-Down Register	—
1Ah	NV Gain and I^2C™ 7-bits Slave Address	SALCK
1Bh	Reserved	—
1Ch	Reserved	—
1Dh	Reserved	—
1Eh	Reserved	—
1Fh	Reserved	—

🟪 Volatile Memory address range

🟦 Nonvolatile Memory address range

Note 1: Device Configuration Memory bits requires a High-Voltage Enable or Disable Command ($\overline{\text{LAT}}/\overline{\text{LAT0}} = V_{IHH}$, or $\overline{\text{CS}} = V_{IHH}$) to modify the bit value.

4.2.3 DEVICE CONFIGURATION MEMORY

There are up to five nonvolatile user bits that are not directly mapped into the address space. These nonvolatile device configuration bits control the following functions:

- DAC Register and Configuration WiperLock Technology (2 bits per DAC)
- I^{2}C Slave Address Write Protect (Lock)

The Status register shows the states of the device WiperLock Technology configuration bits. The STATUS register is described in Register 4-6.

The operation of WiperLock Technology is discussed in **Section 4.2.6 "WiperLock Technology"** while I^{2}C Slave Address Write Protect is discussed in **Section 4.2.7 "I^{2}C Slave Address Write Protect"**.

4.2.4 UNIMPLEMENTED REGISTER BITS

Read Commands of a valid location will read unimplemented bits as '`0`'.

4.2.5 UNIMPLEMENTED (RESERVED) LOCATIONS

Normal (Voltage) Commands (Read or Write) to any unimplemented memory address (Reserved) will result in a Command Error condition (NACK). Read Commands of a reserved location will read bits as '`1`'.

High-Voltage Commands (Enable or Disable) to any unimplemented Configuration bits will result in a Command Error condition (NACK).

4.2.5.1 Default Factory POR Memory State of Nonvolatile Memory (EEPROM)

Table 4-2 shows the default factory POR initialization of the device memory map for the 8-, 10- and 12-bit devices.

Note: The Volatile memory locations will be determined by the nonvolatile memory states (registers and device configuration bits).

TABLE 4-2: FACTORY DEFAULT POR / BOR VALUES

Address	Function	POR/BOR Value		
		8-bit	10-bit	12-bit
00h	Volatile DAC0 Register	7Fh	1FFh	7FFh
01h	Volatile DAC1 Register	7Fh	1FFh	7FFh
02h	Reserved (2)	FFh	3FFh	FFFh
03h	Reserved (2)	FFh	3FFh	FFFh
04h	Reserved (2)	FFh	3FFh	FFFh
05h	Reserved (2)	FFh	3FFh	FFFh
06h	Reserved (2)	FFh	3FFh	FFFh
07h	Reserved (2)	FFh	3FFh	FFFh
08h	V_{REF} Register	0000h	0000h	0000h
09h	Power-Down Register	0000h	0000h	0000h
0Ah	Gain and Status Register	0080h	0080h	0080h
0Bh	WiperLock Technology Status Register	0000h	0000h	0000h
0Ch	Reserved (2)	FFh	3FFh	FFFh
0Dh	Reserved (2)	FFh	3FFh	FFFh
0Eh	Reserved (2)	FFh	3FFh	FFFh
0Fh	Reserved (2)	FFh	3FFh	FFFh
10h	Nonvolatile DAC0 Register	7Fh	1FFh	7FFh
11h	Nonvolatile DAC1 Register	7Fh	1FFh	7FFh
12h	Reserved (2)	FFh	3FFh	FFFh
13h	Reserved (2)	FFh	3FFh	FFFh
14h	Reserved (2)	FFh	3FFh	FFFh
15h	Reserved (2)	FFh	3FFh	FFFh
16h	Reserved (2)	FFh	3FFh	FFFh
17h	Reserved (2)	FFh	3FFh	FFFh
18h	Nonvolatile V_{REF} Register	0000h	0000h	0000h
19h	Nonvolatile Power-Down Register	0000h	0000h	0000h
1Ah	NV Gain and I^{2}C™ 7-bit Slave Address (1)	00E0h (1)	00E0h (1)	00E0h (1)
1Bh	Reserved (2)	FFh	3FFh	FFFh
1Ch	Reserved (2)	FFh	3FFh	FFFh
1Dh	Reserved (2)	FFh	3FFh	FFFh
1Eh	Reserved (2)	FFh	3FFh	FFFh
1Fh	Reserved (2)	FFh	3FFh	FFFh

🟪 Volatile Memory address range

🟦 Nonvolatile Memory address range

Note 1: A0 I^{2}C 7-bit Slave Address option is '`110 0000`' and the Slave Address Lock (SALCK) bit is enabled ('`1`').

2: Reading a reserved memory location will result in the I^{2}C command to Not ACK the command byte. The device data bits will output all '`1`'s. A Start condition will reset the I^{2}C interface.

4.2.6 WIPERLOCK TECHNOLOGY

The MCP47FEBXX device's WiperLock technology allows application-specific device settings (DAC register and configuration) to be secured without requiring the use of an additional write-protect pin. There are two configuration bits (DLx:CLx) for each DAC (DAC0 and DAC1).

Dependent on the state of the DLx:CLx configuration bits, WiperLock technology prevents the serial commands from the following actions on the DACx registers and bits:

- Writing to the specified volatile DACx Register memory location
- Writing to the specified nonvolatile DACx Register memory location
- Writing to the specified volatile DACx configuration bits
- Writing to the specified nonvolatile DACx configuration bits

Each pair of these configuration bits control one of four modes. These modes are shown in Table 4-4. The addresses for the configuration bits are shown in Table 4-1.

To modify the configuration bits, the HVC pin must be forced to the V_{IHH} state and then receive an Enable or Disable command on the desired pair of DAC Register addresses.

Note: To modify the CL0 bit, the Enable or Disable command specifies address 00h, while to modify the DL0 bit, the Enable or Disable command specifies address 10h.

Please refer to the **Section 7.5 "Enable Configuration Bit (High-Voltage)"** and **Section 7.6 "Disable Configuration Bit (High-Voltage)"** commands for operation.

Note: During device communication, if the Device Address/Command combination is invalid or an unimplemented Address is specified, then the MCP47FEBXX will NACK that byte. To reset the I^2C state machine, the I^2C communication must detect a Start bit.

4.2.6.1 POR/BOR Operation when WiperLock Technology Enabled

The WiperLock Technology state is not affected by a POR/BOR event. A POR/BOR event will load the Volatile DAC0 (DAC1) register values with the Nonvolatile DAC0 (DAC1) register values.

4.2.7 I^2C SLAVE ADDRESS WRITE PROTECT

The MCP47FEBXX device's I^2C Slave Address is stored in the EEPROM memory. This allows the address to be modified to the applications requirement. To ensure that the I^2C Slave Address is not unintentionally modified, the memory has a high voltage write protect bit. This configurations bit is shown in Table 4-3.

Note: To modify the SALCK bit, the Enable or Disable command specifies address 1Ah.

TABLE 4-3: SALCK FUNCTIONAL DESCRIPTION

SALCK	Operation
1	The nonvolatile I^2C™ Slave Address bits (ADD6:ADD0) are locked
0	The nonvolatile I^2C Slave Address bits (ADD6:ADD0) are unlocked

TABLE 4-4: WIPERLOCK TECHNOLOGY CONFIGURATION BITS FUNCTIONAL DESCRIPTION

DLx:CLx (2)	Register / Bits				Comments
	DACx		DACx Configuration (1)		
	Volatile	Nonvolatile	Volatile	Nonvolatile	
11	Locked	Locked	Locked	Locked	All DACx registers are locked
10	Locked	Locked	Unlocked	Locked	All DACx registers are locked except volatile DACx Configuration registers. This allows operation of power-down modes
01	Unlocked	Locked	Unlocked	Locked	Volatile DACx registers unlocked, nonvolatile DACx registers locked
00	Unlocked	Unlocked	Unlocked	Unlocked	All DACx registers are unlocked

Note 1: DAC Configuration bits include Voltage Reference Control bits (VRxB:VRxA), Power-Down Control bits (PDxB:PDxA), and Output Gain bits (Gx).

2: The state of these configuration bits (DLx:CLx) are reflected in WLxB:WLxA bits as shown in Register 4-6.

4.2.8 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for both the volatile memory locations and the nonvolatile memory locations. These registers will be either 8 bits, 10 bits, or 12 bits wide. The values are right justified.

REGISTER 4-1: DAC0 AND DAC1 REGISTERS (VOLATILE AND NONVOLATILE)

	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
12-bit	—	—	—	—	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
10-bit	—	—	—	—	—(1)	—(1)	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
8-bit	—	—	—	—	—(1)	—(1)	—(1)	—(1)	D07	D06	D05	D04	D03	D02	D01	D00
	bit 15															bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
🟦 = 12-bit device	🟪 = 10-bit device	☐ = 8-bit device	

12-bit	10-bit	8-bit	
bit 15-12	bit 15-10	bit 15-8	**Unimplemented:** Read as ‘0’
bit 11-0	—	—	**D11-D00:** DAC Output value - 12-bit devices FFFh = Full-Scale output value 7FFh = Mid-Scale output value 000h =Zero-Scale output value
—	bit 9-0	—	**D09-D00:** DAC Output value - 10-bit devices 3FFh = Full-Scale output value 1FFh = Mid-Scale output value 000h =Zero-Scale output value
—	—	bit 7-0	**D07-D00:** DAC Output value - 8-bit devices FFh = Full-Scale output value 7Fh = Mid-Scale output value 000h =Zero-Scale output value

Note 1: Unimplemented bit, read as ‘0’.

Register 4-2 shows the format of the Voltage Reference Control Register. Each DAC has two bits to control the source of the voltage reference of the DAC. This register is for both the volatile memory locations and the nonvolatile memory locations. The width of this register is 2 times the number of DACs for the device.

REGISTER 4-2: VOLTAGE REFERENCE (VREF) CONTROL REGISTER (VOLATILE AND NONVOLATILE) (ADDRESSES 08h AND 18h)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(1)	—(1)	VR0B	VR0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	VR1B	VR1A	VR0B	VR0A
	bit 15															bit 0

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown
▨ = Single-channel device
☐ = Dual-channel device

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as ‘`0`’
bit 1-0	bit 3-0	**VRxB-VRxA:** DAC Voltage Reference Control bits `11` = V_{REF} pin (Buffered); V_{REF} buffer enabled. `10` = V_{REF} pin (Unbuffered); V_{REF} buffer disabled. `01` = Internal Band Gap (1.22V typical); V_{REF} buffer enabled. V_{REF} voltage driven when powered-down. `00` = V_{DD} (Unbuffered); V_{REF} buffer disabled. Use this state with Power-down bits for lowest current.

Note 1: Unimplemented bit, read as ‘`0`’.

Register 4-3 shows the format of the Power-Down Control Register. Each DAC has two bits to control the Power-Down state of the DAC. This register is for both the volatile memory locations and the nonvolatile memory locations. The width of this register is 2 times the number of DACs for the device.

REGISTER 4-3: POWER-DOWN CONTROL REGISTER (VOLATILE AND NONVOLATILE) (ADDRESSES 09h, 19h)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(1)	—(1)	PB0B	PB0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	PB1B	PB1A	PB0B	PB0A
	bit 15															bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
▨ = Single-channel device		☐ = Dual-channel device	

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as '`0`'
bit 1-0	bit 3-0	**PBxB-PBxA:** DAC Power-Down Control bits(2) `11` = Powered Down - V_{OUT} is open circuit. `10` = Powered Down - V_{OUT} is loaded with a 100 kΩ resistor to ground. `01` = Powered Down - V_{OUT} is loaded with a 1 kΩ resistor to ground. `00` = Normal Operation (Not powered-down).

Note 1: Unimplemented bit, read as '`0`'.

2: See Table 5-5 and Figure 5-10 for more details.

Register 4-4 shows the format of the Gain Control and System Status Register. Each DAC has one bit to control the gain of the DAC and three Status bits. This register is for both the volatile memory locations and the nonvolatile memory locations.

REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER (VOLATILE) (ADDRESS 0Ah)

	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/C-1	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
Single	—	—	—	—	—	—	—[1]	G0	POR	EEWA	—	—	—	—	—	—
Dual	—	—	—	—	—	—	G1	G0	POR	EEWA	—	—	—	—	—	—
	bit 15															bit 0

Legend:

R = Readable bit	W = Writable bit	C = Clear-able bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
🟪 = Single-channel device		☐ = Dual-channel device	

Single	Dual	
bit 15-9	bit 15-10	**Unimplemented:** Read as ‘0’
—	bit 9	**G1:** DAC1 Output Driver Gain control bits (**Dual-Channel Device only**) 1 = 2x Gain. Not applicable when V_{DD} is used as V_{RL}. 0 = 1x Gain.
bit 8	bit 8	**G0:** DAC0 Output Driver Gain control bits 1 = 2x Gain. Not applicable when V_{DD} is used as V_{RL}. 0 = 1x Gain.
bit 7	bit 7	**POR:** Power-on Reset (Brown-out Reset) Status bit This bit indicates if a Power-on Reset (POR) or Brown-out Reset (BOR) event has occurred since the last read command of this register. Reading this register clears the state of the POR Status bit. 1 = A POR (BOR) event occurred since the last read of this register. Reading this register clears this bit. 0 = A POR (BOR) event has not occurred since the last read of this register.
bit 6	bit 6	**EEWA:** EEPROM Write Active Status bit This bit indicates if the EEPROM Write Cycle is occurring 1 = An EEPROM Write Cycle is currently occurring. Only serial commands to the volatile memory are allowed. 0 = An EEPROM Write Cycle is NOT currently occurring.
bit 5-0	bit 5-0	**Unimplemented:** Read as ‘0’

Note 1: Unimplemented bit, read as ‘0’.

Register 4-5 shows the format of the Nonvolatile Gain Control and Slave Address Register. Each DAC has one bit to control the gain of the DAC. I^{2}C devices also have eight bits that are the I^{2}C Slave Address and the status of the I^{2}C Address Lock bit.

REGISTER 4-5: GAIN CONTROL AND SLAVE ADDRESS REGISTER (NONVOLATILE) (ADDRESS 1Ah)

	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
Single	—	—	—	—	—	—(1)	G0	ADLCK	EEWA	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
Dual	—	—	—	—	—	G1	G0	ADLCK	EEWA	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
	bit 15															bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown
🟪 = Single-channel device ☐ = Dual-channel device

Single	Dual	
bit 15-9	bit 15-10	**Unimplemented:** Read as ‘`0`’
—	bit 9	**G1:** DAC1 Output Driver Gain control bits (**Dual-Channel Device only**)(2) `1` = 2x Gain. Not applicable when V_{DD} is used as V_{RL}. `0` = 1x Gain.
bit 8	bit 8	**G0:** DAC0 Output Driver Gain control bits(3) `1` = 2x Gain. Not applicable when V_{DD} is used as V_{RL}. `0` = 1x Gain.
bit 7	bit 7	**ADLCK:** I^{2}C Address Lock Status bit (Read-Only bit; reflects the state of the $\overline{\text{SALCK}}$ configuration bit). `1` = I^{2}C Slave Address is Locked (requires HV command to disable, so I^{2}C address can be changed) `0` = I^{2}C Slave Address is NOT Lock, the nonvolatile I^{2}C slave address can be changed.
bit 6-0	bit 6-0	**ADD6-ADD0:** I^{2}C 7-bit Slave Address Bits.

Note 1: Unimplemented bit, read as ‘`0`’.

2: If VR1B:VR1A = ‘`00`’; the device uses a gain of 1 only, regardless of the state of this bit (G1).

3: If VR0B:VR0A = ‘`00`’; the device uses a gain of 1 only, regardless of the state of this bit (G0).

Register 4-6 shows the format of the DAC WiperLock Technology Status Register. The width of this register is 2 times the number of DACs for the device.

REGISTER 4-6: DAC WIPERLOCK TECHNOLOGY STATUS REGISTER (VOLATILE) (ADDRESS 0BH)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0(2)	R-0(2)	R-0(2)	R-0(2)
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(1)	—(1)	WL0B	WL0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	WL1B	WL1A	WL0B	WL0A
	bit 15															bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown
▨ = Single-channel device ☐ = Dual-channel device

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as ‘0’
bit 1-0	bit 3-0	**WLxB-WLxA:** WiperLock Technology Status bits: These bits reflect the state of the DLx:CLx nonvolatile configuration bits `11` = DAC wiper and DAC Configuration (volatile and nonvolatile registers) are locked (DLx = CLx = Enabled) `10` = DAC wiper (volatile and nonvolatile) and DAC Configuration (nonvolatile registers) are locked (DLx = Enabled; CLx = Disabled). `01` = DAC wiper (nonvolatile) and DAC Configuration (nonvolatile registers) are locked (DLx = Disabled; CLx = Enabled) `00` = DAC wiper and DAC Configuration are unlocked (DLx = CLx = Disabled).

Note 1: Unimplemented bit, read as ‘0’.

2: POR Value dependent on the programmed values of the DLx:CLx configuration bits. The devices are shipped with a default DLx:CLx configuration bit state of ‘0’.

NOTES:

5.0 DAC CIRCUITRY

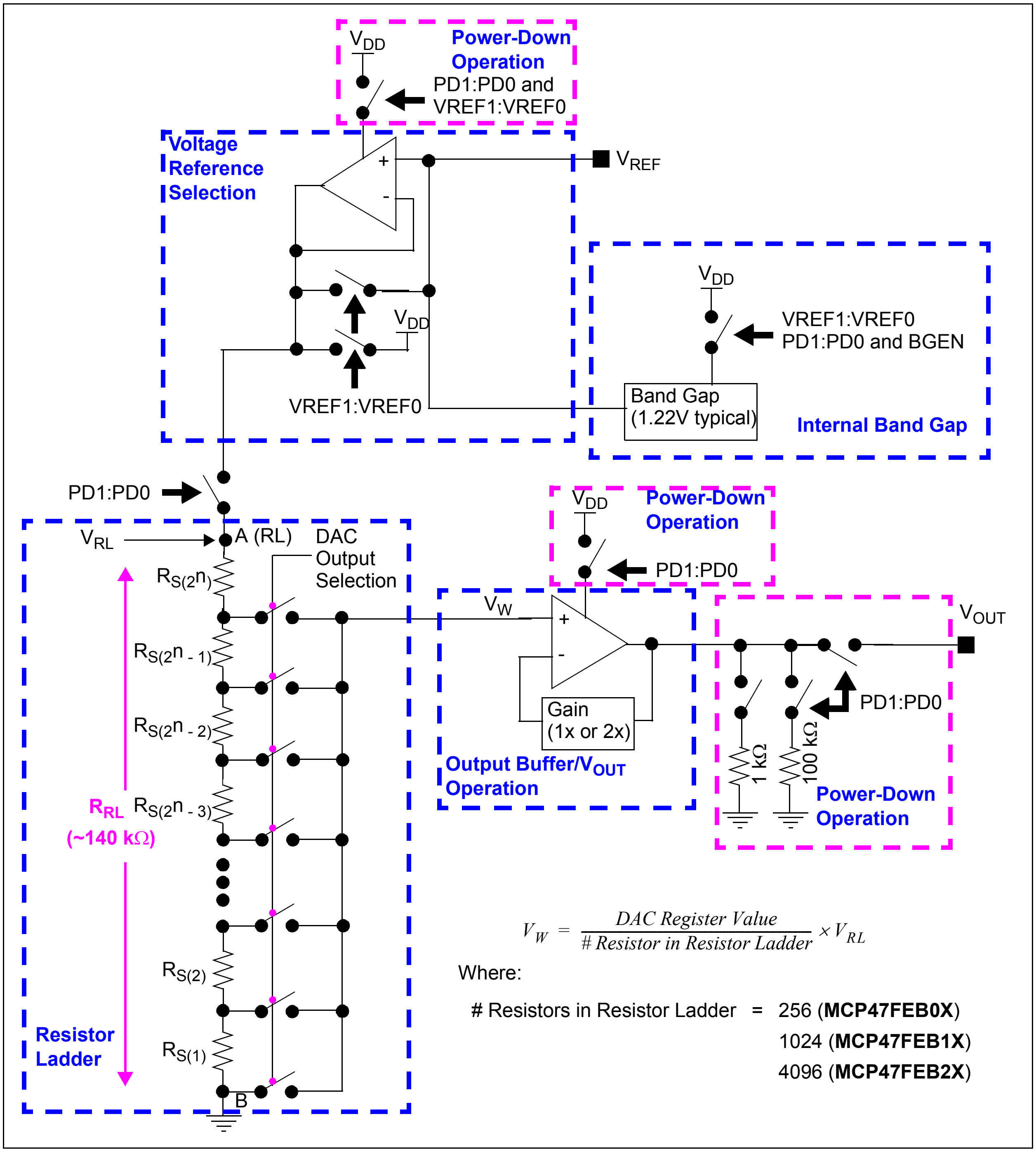
The Digital to Analog Converter circuitry converts a digital value into its analog representation. The description describes the functional operation of the device.

The DAC Circuit uses a resistor ladder implementation. Devices have up to two DACs.

Figure 5-1 shows the functional block diagram for the MCP47FEBXX DAC circuitry.

The functional blocks of the DAC include:

- **Resistor Ladder**
- **Voltage Reference Selection**
- **Output Buffer/V_{OUT} Operation**
- **Internal Band Gap** (as a voltage reference)
- **Latch Pin (LAT)**
- **Power-Down Operation**



$$V_W = \frac{DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times V_{RL}$$

Where:

Resistors in Resistor Ladder = 256 (**MCP47FEB0X**)
1024 (**MCP47FEB1X**)
4096 (**MCP47FEB2X**)

FIGURE 5-1: *MCP47FEBXX DAC Module Block Diagram.*

5.1 Resistor Ladder

The Resistor Ladder is a digital potentiometer with the B Terminal internally grounded and the A Terminal connected to the selected reference voltage (see Figure 5-2). The volatile DAC register controls the wiper position. The wiper voltage (V_W) is proportional to the DAC register value divided by the number of resistor elements (R_S) in the ladder (256, 1024 or 4096) related to the V_{RL} voltage.

The output of the resistor network will drive the input of an output buffer.

The Resistor Network is made up of these three parts:

- Resistor Ladder (string of R_S elements)
- Wiper switches
- DAC Register decode

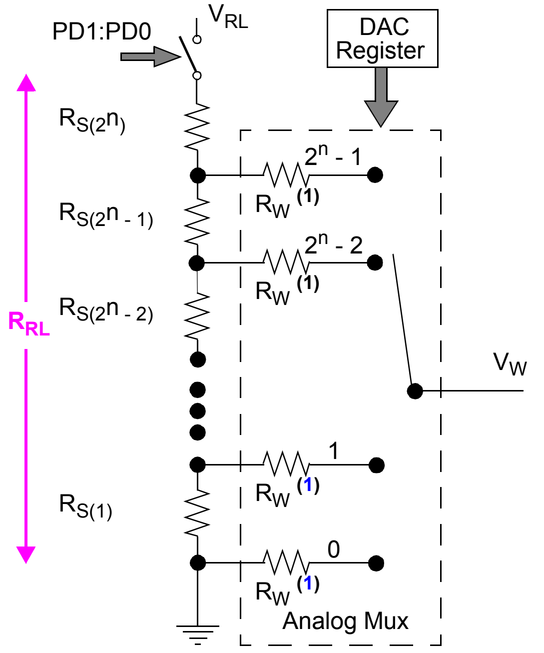
The resistor ladder (R_{RL}) has a typical impedance of approximately 140 kΩ. This resistor ladder resistance (R_{RL}) may vary from device to device up to ±20%. Since this is a voltage divider configuration, the actual R_{RL} resistance does not affect the output given a fixed voltage at V_{RL}.

Equation 5-1 shows the calculation for the step resistance.

> **Note:** The maximum wiper position is $2^n – 1$, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full scale, there is one resistor element (R_S) between the wiper and the V_{RL} voltage.

If the unbuffered V_{REF} pin is used as the V_{RL} voltage source, this voltage source should have a low output impedance.

When the DAC is powered-down, the resistor ladder is disconnected from the selected reference voltage.



$$V_W = \frac{DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times V_{RL}$$

Where:

# Resistors in R-Ladder	=	256 (**MCP47FEB0X**)
		1024 (**MCP47FEB1X**)
		4096 (**MCP47FEB2X**)

Note 1: The analog switch resistance (R_W) does not affect performance due to the voltage divider configuration.

FIGURE 5-2: *Resistor Ladder Model Block Diagram.*

EQUATION 5-1: R_S CALCULATION

$$R_S = \frac{R_{RL}}{(256)}$$

8-bit Device

$$R_S = \frac{R_{RL}}{(1024)}$$

10-bit Device

$$R_S = \frac{R_{RL}}{(4096)}$$

12-bit Device

5.2 Voltage Reference Selection

The resistor ladder has up to four sources for the reference voltage. Two user control bits (VREF1:VREF0) are used to control the selection, with the selection connected to the V_{RL} node (see Figures 5-3 and 5-4). The four voltage source options for the Resistor Ladder are:

1. V_{DD} pin voltage
2. Internal Voltage Reference (V_{BG})
3. V_{REF} pin voltage unbuffered
4. V_{REF} pin voltage internally buffered

The selection of the voltage is specified with the volatile V_{REF1}:V_{REF0} configuration bits (see Register 4-2). There are nonvolatile and volatile VREF1:VREF0 configuration bits. On a POR/BOR event, the state of the nonvolatile VREF1:VREF0 configuration bits is latched into the volatile VREF1:VREF0 configuration bits.

When the user selects the V_{DD} as reference, the V_{REF} pin voltage is not connected to the resistor ladder.

If the V_{REF} pin is selected, then one needs to select between the buffered or unbuffered mode.

5.2.1 UNBUFFERED MODE

The V_{REF} pin voltage may be from V_{SS} to V_{DD}.

Note 1: The voltage source should have a low output impedance. If the voltage source has a high output impedance, then the voltage on the V_{REF}'s pin would be lower than expected. The resistor ladder has a typical impedance of 140 kΩ and a typical capacitance of 29 pF.

2: If the V_{REF} pin is tied to the V_{DD} voltage, V_{DD} mode (VREF1:VREF0 = '00') is recommended.

5.2.2 BUFFERED MODE

The V_{REF} pin voltage may be from 0.01V to V_{DD} - 0.04V. The input buffer (amplifier) provides low offset voltage, low noise, and a very high input impedance, with only minor limitations on the input range and frequency response.

Note 1: Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

2: If the V_{REF} pin is tied to the V_{DD} voltage, V_{DD} mode (VREF1:VREF0 = '00') is recommended.

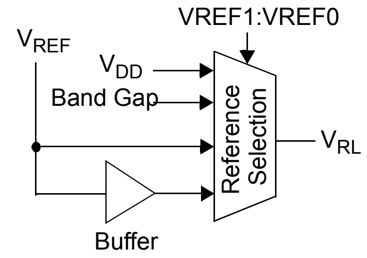
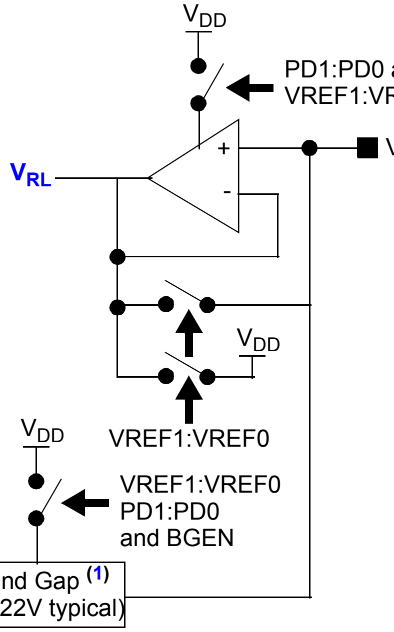


FIGURE 5-3: Resistor Ladder Reference Voltage Selection Block Diagram.



Note 1: The Band Gap voltage (V_{BG}) is 1.22V typical. The band gap output goes through the buffer with a 2x gain to create the V_{RL} voltage. See **Section 5.4 "Internal Band Gap"** for addition information on the band gap circuit.

FIGURE 5-4: Reference Voltage Selection Implementation Block Diagram.

5.2.3 BANDGAP MODE

If the Internal Band Gap is selected, then the external V_{REF} pin should not be driven and only use high-impedance loads. Decoupling capacitors are recommended for optimal operation.

The band gap output is buffered, but the internal switches limit the current that the output should source to the V_{REF} pin. The resistor ladder buffer is used to drive the Band Gap voltage for the cases of multiple DAC outputs. This ensures that the resistor ladders are always properly sourced when the band gap is selected.

5.3 Output Buffer/V_{OUT} Operation

The Output Driver buffers the wiper voltage (V_W) of the Resistor Ladder.

The DAC output is buffered with a low power and precision output amplifier (op amp). This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and high-capacitive loads without oscillation. The amplifier provides a maximum load current which is enough for most programmable voltage reference applications. Refer to **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

Note:	The load resistance must keep higher than 5 kΩ for the stable and expected analog output (to meet electrical specifications).

Figure 5-5 shows a block diagram of the output driver circuit.

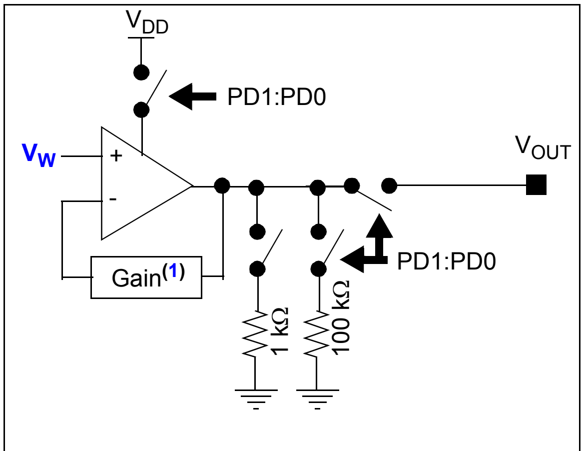
The user can select the output gain of the output amplifier. Gain options are:

a) Gain of 1, with either V_{DD} or V_{REF} pin used as reference voltage.

b) Gain of 2, only when V_{REF} pin or Internal Band Gap is used as reference voltage. The V_{REF} pin voltage should be limited to $V_{DD}/2$.

Power-down logic also controls the output buffer operation (see **Section 5.6 "Power-Down Operation"** for additional information on Power-down). In any of the three Power-Down modes, the op amp is powered-down and its output becomes a high impedance to the V_{OUT} pin.

Table 5-1 shows the gain bit operation. When the reference voltage selection (V_{RL}) is the device's V_{DD} voltage, the G bit is ignored and a gain of 1 is used.



Note 1: Gain options are 1x and 2x.

FIGURE 5-5: *Output Driver Block Diagram.*

TABLE 5-1: OUTPUT DRIVER GAIN

Gain Bit	Gain	Comment
0	1	
1	2	Limits V_{REF} pin voltages relative to device V_{DD} voltage.

5.3.1 PROGRAMMABLE GAIN

The amplifier's gain is controlled by the Gain (G) configuration bit (see Register 4-5) and the V_{RL} reference selection. When the V_{RL} reference selection is the device's V_{DD} voltage, the G bit is ignored and a gain of 1 is used.

The volatile G bit value can be modified by:

- POR event
- BOR event
- I^2C Write commands
- I^2C General Call Reset command

5.3.2 OUTPUT VOLTAGE

The volatile DAC Register values along with the device's configuration bits control the analog V_{OUT} voltage. The volatile DAC Register's value is unsigned binary. The formula for the output voltage is given in Equation 5-2. Table 5-3 shows examples of volatile DAC register values and the corresponding theoretical V_{OUT} voltage for the MCP47FEBXX devices.

EQUATION 5-2: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{V_{RL} \times DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

# Resistors in R-Ladder	=	4096 (**MCP47FEB2X**)
		1024 (**MCP47FEB1X**)
		256 (**MCP47FEB0X**)

> **Note:** When Gain = 2 ($V_{RL} = V_{REF}$), if $V_{REF} > V_{DD} / 2$, the V_{OUT} voltage will be limited to V_{DD}. So if $V_{REF} = V_{DD}$, then the V_{OUT} voltage will not change for volatile DAC Register values mid-scale and greater, since the op amp is at full-scale output.

The following events update the DAC register value and therefore the analog voltage output (V_{OUT}):

- Power-on Reset
- Brown-out Reset
- I^{2}C Write Command, Falling edge of the acknowledge pulse of the last write command byte.
- I^{2}C General Call Reset command, Output is updated with POR data (EEPROM).

Then the V_{OUT} voltage will start driving to the new value after the event has occurred.

5.3.3 STEP VOLTAGE (V_S)

The Step Voltage is dependent on the device resolution and the calculated output voltage range. One LSb is defined as the ideal voltage difference between two successive codes. The step voltage can easily be calculated by using Equation 5-3 (DAC Register Value is equal to 1). Theoretical Step Voltages are shown in Table 5-2 for several V_{REF} voltages.

EQUATION 5-3: V_S CALCULATION

$$V_S = \frac{V_{RL}}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

# Resistors in R-Ladder	=	4096 (**12-bit**)
		1024 (**10-bit**)
		256 (**8-bit**)

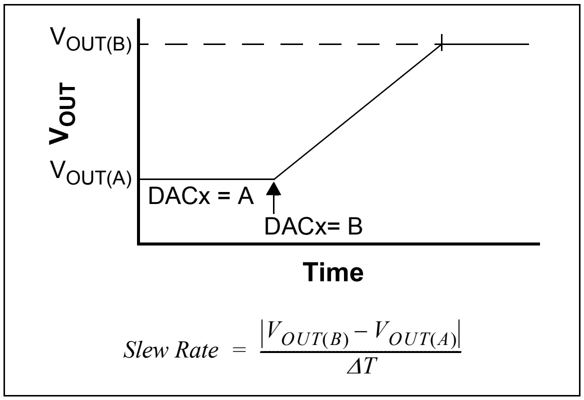
TABLE 5-2: THEORETICAL STEP VOLTAGE (V_S) (1)

	V_{REF}					
	5.0	**2.7**	**1.8**	**1.5**	**1.0**	
V_S	1.22mV	659uV	439uV	366uV	244uV	12-bit
	4.88mV	2.64mV	1.76mV	1.46mV	977uV	10-bit
	19.5mV	10.5mV	7.03mV	5.86mV	3.91mV	8-bit

Note 1: When Gain = 1x, $V_{FS} = V_{RL}$, and $V_{ZS} = 0V$.

5.3.4 OUTPUT SLEW RATE

Figure 5-6 shows an example of the slew rate of the V_{OUT} pin. The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.



$$Slew\ Rate\ =\ \frac{|V_{OUT(B)} - V_{OUT(A)}|}{\Delta T}$$

FIGURE 5-6: *V_{OUT} pin Slew Rate.*

5.3.4.1 Small Capacitive Load

With a small capacitive load, the output buffer's current is not affected by the capacitive load (C_L). But still, the V_{OUT} pin's voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer's characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer, and is referred to as the buffer slew rate (SR_{BUF}).

5.3.4.2 Large Capacitive Load

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's short-circuit current (I_{SC})
- The V_{OUT} pin's external load

I_{OUT} cannot exceed the output buffer's short-circuit current (I_{SC}), which fixes the output buffer slew rate (SR_{BUF}). The voltage on the capacitive load (C_L), V_{CL}, changes at a rate proportional to I_{OUT}, which fixes a capacitive load slew rate (SR_{CL}).

So the V_{CL} voltage slew rate is limited to the slower of the output buffer's internally set slew rate (SRBUF) and the capacitive load slew rate (SR_{CL}).

5.3.5 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications). A V_{OUT} vs. Resistive Load characterization graph can be seen in the Char Data for this device (**DS20005378**).

V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with R_L greater than 5 kΩ.

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the V_{OUT} pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V_{OUT} pin.

So, when driving large capacitive loads with the output buffer, a small series resistor (R_{ISO}) at the output (see Figure 5-7) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

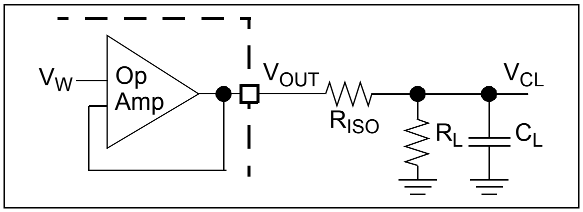


FIGURE 5-7: *Circuit to Stabilize Output Buffer for Large Capacitive Loads (C_L).*

The R_{ISO} resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R_{ISO} resistor value should be verified on the bench. Modify the R_{ISO}'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the V_{REF} pin and observe the V_{OUT} pin's characteristics.

Note: Additional insight into circuit design for driving capacitive loads can be found in AN884 – *"Driving Capacitive Loads With Op Amps"* (DS00000884).

TABLE 5-3: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT (V_{OUT}) (V_{DD} = 5.0V)

Device	Volatile DAC Register Value	V_{RL}(1)	LSb		Gain Selection (2)	V_{OUT}(3)	
			Equation	µV		Equation	V
MCP47FEB2X (12-bit)	1111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (4095/4096) ∗ 1	4.998779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (4095/4096) ∗ 1	2.499390
					2x(2)	V_{RL} ∗ (4095/4096) ∗ 2)	4.998779
	0111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (2047/4096) ∗ 1)	2.498779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (2047/4096) ∗ 1)	1.249390
					2x(2)	V_{RL} ∗ (2047/4096) ∗ 2)	2.498779
	0011 1111 1111	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (1023/4096) ∗ 1)	1.248779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (1023/4096) ∗ 1)	0.624390
					2x(2)	V_{RL} ∗ (1023/4096) ∗ 2)	1.248779
	0000 0000 0000	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (0/4096) * 1)	0
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (0/4096) * 1)	0
					2x(2)	V_{RL} ∗ (0/4096) * 2)	0
MCP47FEB1X (10-bit)	11 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (1023/1024) ∗ 1	4.995117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (1023/1024) ∗ 1	2.497559
					2x(2)	V_{RL} ∗ (1023/1024) ∗ 2	4.995117
	01 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (511/1024) ∗ 1	2.495117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (511/1024) ∗ 1	1.247559
					2x(2)	V_{RL} ∗ (511/1024) ∗ 2	2.495117
	00 1111 1111	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (255/1024) ∗ 1	1.245117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (255/1024) ∗ 1	0.622559
					2x(2)	V_{RL} ∗ (255/1024) ∗ 2	1.245117
	00 0000 0000	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (0/1024) ∗ 1	0
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (0/1024) ∗ 1	0
					2x(2)	V_{RL} ∗ (0/1024) ∗ 1	0
MCP47FEB0X (8-bit)	1111 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (255/256) ∗ 1	4.980469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (255/256) ∗ 1	2.490234
					2x(2)	V_{RL} ∗ (255/256) ∗ 2	4.980469
	0111 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (127/256) ∗ 1	2.480469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (127/256) ∗ 1	1.240234
					2x(2)	V_{RL} ∗ (127/256) ∗ 2	2.480469
	0011 1111	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (63/256) ∗ 1	1.230469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (63/256) ∗ 1	0.615234
					2x(2)	V_{RL} ∗ (63/256) ∗ 2	1.230469
	0000 0000	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (0/256) ∗ 1	0
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (0/256) ∗ 1	0
					2x(2)	V_{RL} ∗ (0/256) ∗ 2	0

Note 1: V_{RL} is the resistor ladder's reference voltage. It is independent of VREF1:VREF0 selection.

2: Gain selection of 2x (Gx = '1') requires voltage reference source to come from V_{REF} pin (VREF1:VREF0 = '10' or '11') and requires V_{REF} pin voltage (or V_{RL}) ≤ $V_{DD}/2$ or from the internal band gap (VREF1:VREF0 = '01').

3: These theoretical calculations do not take into account the Offset, Gain and nonlinearity errors.

5.4 Internal Band Gap

The internal band gap is designed to drive the Resistor Ladder Buffer.

The resistance of a resistor ladder (R_{RL}) is targeted to be 140 kΩ (±40 kΩ), which means a minimum resistance of 100 kΩ.

The band gap selection can be used across the V_{DD} voltages while maximizing the V_{OUT} voltage ranges. For V_{DD} voltages below the $2 * \text{Gain} * V_{BG}$ voltage, the output for the upper codes will be clipped to the V_{DD} voltage. Table 5-4 shows the maximum DAC register code given device VDD and Gain bit setting.

TABLE 5-4: V_{OUT} USING BAND GAP

V_{DD}	DAC Gain	Max DAC Code (1)			Comment
		12-bit	10-bit	8-bit	
5.5	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.44V(3)
	2	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 4.88V(3)
2.7	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.44V(3)
	2	8DAh	236h	8Dh	~ 0 to 55% range
2.0(4)	1	D1Dh	347h	D1h	~ 0 to 82% range
	2(2)	68Eh	1A3h	68h	~ 0 to 41% range

Note 1: Without the V_{OUT} pin voltage being clipped.
2: Recommended to use Gain = 1 setting.
3: When V_{BG} = 1.22V typical.
4: Band gap performance achieves full performance starting from a V_{DD} of 2.0V.

5.5 Latch Pin ($\overline{\text{LAT}}$)

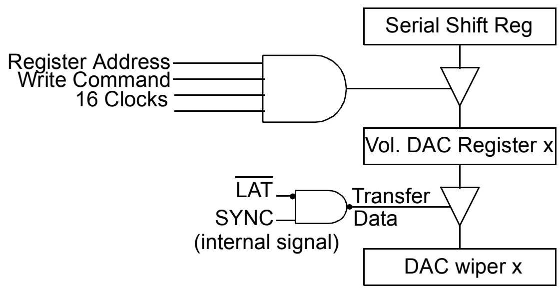
The Latch pin controls when the volatile DAC Register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero crossing or updates to the other wipers on the device. The $\overline{\text{LAT}}$ pin is asynchronous to the serial interface operation.

When the $\overline{\text{LAT}}$ pin is high, transfers from the volatile DAC register to the DAC wiper are inhibited. The volatile DAC register value(s) can be continued to be updated.

When the $\overline{\text{LAT}}$ pin is low, the volatile DAC register value is transferred to the DAC wiper.

> **Note:** This allows both the volatile DAC0 and DAC1 Registers to be updated while the $\overline{\text{LAT}}$ pin is high, and to have outputs synchronously updated as the $\overline{\text{LAT}}$ pin is driven low.

Figure 5-8 shows the interaction of the $\overline{\text{LAT}}$ pin and the loading of the DAC wiper x (from the volatile DAC Register x). The transfers are level driven. If the $\overline{\text{LAT}}$ pin is held low, the corresponding DAC wiper is updated as soon as the volatile DAC Register value is updated.



$\overline{\text{LAT}}$	SYNC	Transfer Data	Comment
1	1	0	No Transfer
1	0	0	No Transfer
0	1	1	Vol. DAC Register x → DAC wiper x
0	0	0	No Transfer

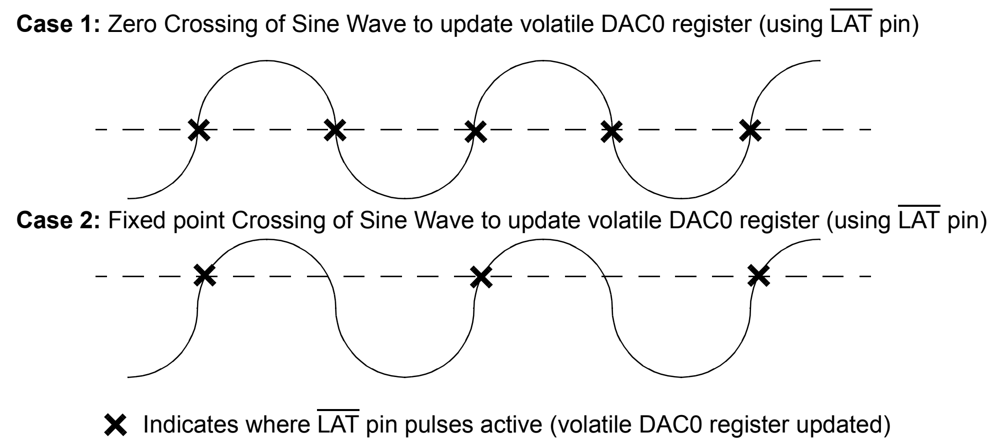
FIGURE 5-8: *$\overline{\text{LAT}}$ and DAC Interaction.*

The $\overline{\text{LAT}}$ pin allows the DAC wiper to be updated to an external event as well as have multiple DAC channels/devices update at a common event.

Since the DAC wiper x is updated from the Volatile DAC Register x, all DACs that are associated with a given $\overline{\text{LAT}}$ pin can be updated synchronously.

If the application does not require synchronization, then this signal should be tied low.

Figure 5-9 shows two cases of using the $\overline{\text{LAT}}$ pin to control when the wiper register is updated relative to the value of a sine wave signal.


Case 1: Zero Crossing of Sine Wave to update volatile DAC0 register (using $\overline{\text{LAT}}$ pin)

Case 2: Fixed point Crossing of Sine Wave to update volatile DAC0 register (using $\overline{\text{LAT}}$ pin)

✕ Indicates where $\overline{\text{LAT}}$ pin pulses active (volatile DAC0 register updated)

FIGURE 5-9: *Example use of $\overline{\text{LAT}}$ pin operation.*

5.6 Power-Down Operation

To allow the application to conserve power when the DAC operation is not required, three power-down modes are available. The Power-Down configuration bits (PD1:PD0) control the power-down operation (Figure 5-10 and Table 5-5). On devices with multiple DACs, each DACs power-down mode is individually controllable. All power-down modes do the following:

- Turn off most the DAC module's internal circuits (output op amp, resistor ladder,...)
- Op amp output becomes high-impedance to the V_{OUT} pin
- Disconnects resistor ladder from reference voltage (V_{RL})
- Retains the value of the volatile DAC register and configuration bits, and the nonvolatile (EEPROM) DAC register and configuration bits

Depending on the selected power-down mode, the following will occur:

- V_{OUT} pin is switched to one of two resistive pull-downs (See Table 5-5)
  - 100 kΩ (typical)
  - 1 kΩ (typical)
- Op amp is powered-down and the V_{OUT} pin is high-impedance.

There is a delay (T_{PDE}) between the PD1:PD0 bits changing from '`00`' to either '`01`', '`10`' or '`11`' and the op amp no longer driving the V_{OUT} output and the pull-down resistors sinking current.

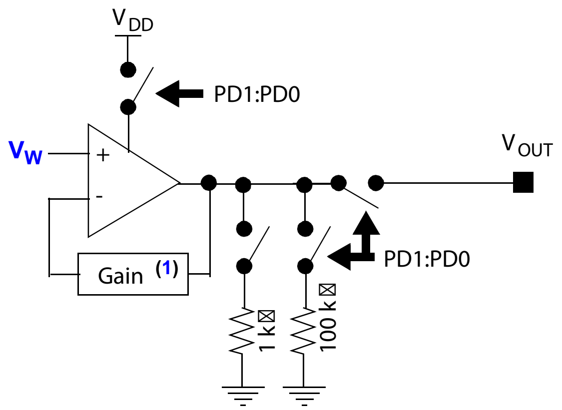
In any of the power-down modes where the V_{OUT} pin is not externally connected (sinking or sourcing current), the power-down current will typically be ~650 nA for a single-DAC device. As the number of DACs increases, the device's power-down current will also increase.

The power-down bits are modified by using a Write command to the volatile Power-Down register, or a POR event which transfers the nonvolatile Power-Down register to the volatile Power-Down register.

Section 7.0 "Device Commands" describes the I^2C commands for writing the power-down bits. The commands that can update the volatile PD1:PD0 bits are:

- Write Command (Normal and High-Voltage)
- Read Command (Normal and High-Voltage)
- Enable Configuration Bit (High-Voltage)
- Disable Configuration Bit (High-Voltage)
- General Call Reset
- General Call Wake-up

> **Note:** The I^2C serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the I^2C master device.



Note 1: Gain options are 1x and 2x.

FIGURE 5-10: V_{OUT} Power-Down Block Diagram.

TABLE 5-5: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD

PD1	PD0	Function
`0`	`0`	Normal operation
`0`	`1`	1 kΩ resistor to ground
`1`	`0`	100 kΩ resistor to ground
`1`	`1`	Open Circuit

Table 5-6 shows the current sources for the DAC based on the selected source of the DAC's reference voltage and if the device is in normal operating mode or one of the power-down modes.

TABLE 5-6: DAC CURRENT SOURCES

Device V_{DD} Current Source	PD1:0 = '`00`', VREF1:0 =				PD1:0 ≠ '`00`', VREF1:0 =			
	`00`	`01`	`10`	`11`	`00`	`01`	`10`	`11`
Output Op Amp	Y	Y	Y	Y	N	N	N	N
Resistor Ladder	Y	Y	N (1)	Y	N	N	N (1)	N
RL Op Amp	N	Y	N	Y	N	N	N	N
Band Gap	N	Y	N	N	N	Y	N	N

Note 1: Current is sourced from the V_{REF} pin, not the device V_{DD}.

5.6.1 EXITING POWER-DOWN

When the device exits the power-down mode the following occurs:

- Disabled circuits (op amp, resistor ladder, ...) are turned on
- Resistor ladder is connected to selected reference voltage (V_{RL})
- Selected pull-down resistor is disconnected
- The V_{OUT} output will be driven to the voltage represented by the volatile DAC Register's value and configuration bits

The V_{OUT} output signal will require time as these circuits are powered-up and the output voltage is driven to the specified value as determined by the volatile DAC register and configuration bits.

> **Note:** Since the op amp and resistor ladder were powered-off (0V), the op amp's input voltage (V_W) can be considered 0V. There is a delay (T_{PDD}) between the PD1:PD0 bits updating to '`00`' and the op amp driving the V_{OUT} output. The op amp's settling time (from 0V) needs to be taken into account to ensure the V_{OUT} voltage reflects the selected value.

The following events will change the PD1:PD0 bits to '`00`' and therefore exit the Power-Down mode. These are:

- Any I^2C write command where the PD1:PD0 bits are '`00`'.
- I^2C General Call Wake-up Command.
- I^2C General Call Reset Command. (if nonvolatile PD1:PD0 bits are '`00`').

5.6.2 RESET COMMANDS

When the MCP47FEBXX is in the valid operating voltage, the I^2C General Call Reset command will force a Reset event. This is similar to the Power-on Reset, except that the Reset delay timer is not started.

If the I^2C interface bus does not seem to be responsive, the technique shown in **Section 8.9 "Software I^2C Interface Reset Sequence"** can be used to force the I^2C interface to be reset.

5.7 DAC Registers, Configuration Bits, and Status Bits

The MCP47FEBXX devices have both volatile and nonvolatile (EEPROM) memory. Table 4-2 shows the volatile and nonvolatile memory and their interaction due to a POR event.

There are five configuration bits in both the volatile and nonvolatile memory, the DAC registers in both the volatile and nonvolatile memory, and two volatile status bits. The DAC registers (volatile and nonvolatile) will be either 12 bits (MCP47FEB2X), 10 bits (MCP47FEB1X), or 8 bits (MCP47FEB0X) wide.

When the device is first powered-up, it automatically uploads the EEPROM memory values to the volatile memory. The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered-up, the user can update the device memory.

The I^2C interface is how this memory is read and written. Refer to **Section 6.0 "I^2C Serial Interface Module"** and **Section 7.0 "Device Commands"** for more details on reading and writing the device's memory.

When the nonvolatile memory is written, the device starts writing the EEPROM cell at the Acknowledge pulse of the Write command.

Register 4-4 shows the operation of the device status bits, Table 4-3 and Table 4-4 show the operation of the device configuration bits, and Table 4-2 shows the factory default value of a POR/BOR event for the device configuration bits.

There are two status bits. These are only in volatile memory and give indication on the status of the device. The POR bit indicates if the device V_{DD} is above or below the POR trip point. During normal operation, this bit should be '`1`'. The RDY/$\overline{\text{BSY}}$ bit indicates if an EEPROM write cycle is in progress. While the RDY/$\overline{\text{BSY}}$ bit is low (during the EEPROM writing), all commands are ignored, except for the Read command.

6.0 I²C SERIAL INTERFACE MODULE

The MCP47FEBXX's I²C Serial Interface Module supports the I²C serial protocol specification. This I²C interface is a two-wire interface (clock and data). Figure 6-1 shows a typical I²C interface connection.

The I²C specification only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. The frame content (Commands) for the MCP47FEBXX is defined in **Section 7.0 "Device Commands"**.

An overview of the I²C protocol is available in **Section Appendix B: "I²C Serial Interface"**.

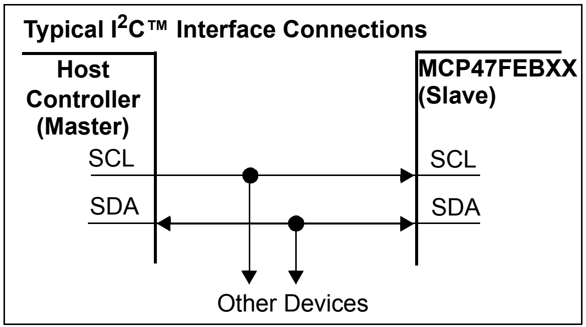


FIGURE 6-1: Typical I²C Interface.

6.1 Overview

This sections discusses some of the specific characteristics of the MCP47FEBXX's I²C Serial Interface Module. This is to assist in the development of your application.

The following sections discuss some of these device-specific characteristics.

- **Interface Pins (SCL and SDA)**
- **Communication Data Rates**
- **POR/BOR**
- **Device Memory Address**
- **General Call Commands**
- **Device I²C Slave Addressing**
- **Entering High-Speed (HS) Mode**

6.2 Interface Pins (SCL and SDA)

The MCP47FEBXX I²C's module SCL pin does not generate the serial clock since the device operates in Slave mode. Also, the MCP47FEBXX will not stretch the clock signal (SCL) since memory read access occurs fast enough.

The MCP47FEBXX I²C's module implements slope control on the SDA pin output driver.

6.3 Communication Data Rates

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High-Speed modes. The MCP47FEBXX supports these three modes. The clock rates (bit rate) of these modes are:

- Standard mode: up to 100 kHz (kbit/s)
- Fast mode: up to 400 kHz (kbit/s)
- High-Speed mode (HS mode): up to 3.4 MHz (Mbit/s)

A description on how to enter High-Speed mode is described in **Section 6.9 "Entering High-Speed (HS) Mode"**.

6.4 POR/BOR

On a POR/BOR event, the I²C Serial Interface Module state machine is reset, which includes that the Device's Memory Address pointer is forced to 00h.

6.5 Device Memory Address

The memory address is the 5-bit value that specifies the location in the device's memory that the specified command will operate on.

On a POR/BOR event, the Device's Memory Address pointer is forced to 00h.

The MCP47FEBXX retains the last "Device Memory Address" that it has received. That is, the MCP47FEBXX does not "corrupt" the "Device Memory Address" after Repeated Start or Stop conditions.

6.6 General Call Commands

The General Call commands utilize the I²C specification reserved General Call command address and command codes. The MCP47FEBXX also implements a non-standard General Call command.

The General Call commands are

- **General Call Reset**
- **General Call Wake-up** (MCP47FEBXX defined)

The General Call Wake-up command will cause all the MCP47FEBXX devices to exit their power-down state.

6.7 Multi-Master Systems

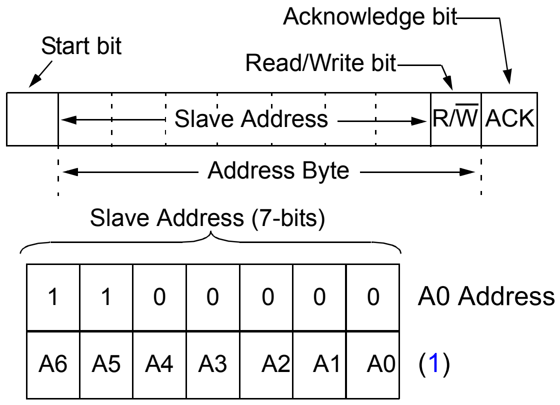
The MCP47FEBXX is not a Master device (generate the interface clock), but can be used in multi-master applications.

6.8 Device I^2C Slave Addressing

The MCP47FEBXX implements 7-bit slave addressing. The address byte is the first byte received following the Start condition from the master device (see Figure 6-2).

The slave address is implemented in a nonvolatile register (Register 4-5) which is protected from accidental register writes via the Slave Address Lock (SALCK) configuration bit. The SALCK configuration bit requires a high voltage (V_{IHH}) to be modified. The SALCK configuration bit must be disabled (see **Section 7.6 "Disable Configuration Bit (High-Voltage)"**) before a write to the nonvolatile Slave Addresses register can modify the value.

> **Note:** After modifying the nonvolatile Slave Address value (Register 4-5), it is strongly recommended that the SALCK configuration bit is enabled (see **Section 7.5 "Enable Configuration Bit (High-Voltage)"**).



Note 1: Address Bits (A6:A0) can be reprogrammed by the customer (nonvolatile device), but must unlock the Slave Address with a High-Voltage command.

FIGURE 6-2: *Slave Address Bits in the I^2C Control Byte.*

> **Note:** The I^2C 10-bit Addressing mode is not supported.

Table 6-1 shows the four standard order-able I^2C slave addresses and their respective device order code.

TABLE 6-1: I^2C ADDRESS/ORDER CODE

7-bit I^2C™ Address	Device Order Code(1)	Comment
`'1100000'` (2)	MCP47FEBXXA0-E/ST	
	MCP47FEBXXA0T-E/ST	Tape and Reel
`'1100001'` (2)	MCP47FEBXXA1-E/ST	
	MCP47FEBXXA1T-E/ST	Tape and Reel
`'1100010'` (2)	MCP47FEBXXA2-E/ST	
	MCP47FEBXXA2T-E/ST	Tape and Reel
`'1100011'` (2)	MCP47FEBXXA3-E/ST	
	MCP47FEBXXA3T-E/ST	Tape and Reel

Note 1: `'xx'` in the order code indicates the resolution and number of output channels for the device.

2: The devices I^2C Slave Address can be reprogrammed by the end user.

6.8.0.1 Custom I^2C Slave Address Options

Custom I^2C Slave Address options can be requested. Customers can request the custom I^2C Slave Address via the Non-Standard Customer Authorization Request (NSCAR) process.

> **Note 1:** Non-Recurring Engineering (NRE) charges and minimum ordering requirements for custom orders. Please contact Microchip sales for additional information.
>
> **2:** A custom device will be assigned custom device marking.

6.9 Entering High-Speed (HS) Mode

The I^2C specification requires that a High-Speed mode device must be ‘activated’ to operate in High-Speed (3.4 Mbit/s) mode. This is done by the master sending a special address byte following the Start bit. This byte is referred to as the High-Speed Master Mode Code (HSMMC).

The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next Stop condition.

The master code is sent as follows:

1. Start condition (S)
2. High-Speed Master Mode Code (`0000 1XXX`), The `XXX` bits are unique to the High-Speed (HS) mode master.
3. No Acknowledge ($\overline{A}$)

After switching to the High-Speed mode, the next transferred byte is the I^2C control byte, which specifies the device to communicate with, and any number of data bytes plus acknowledgments. The master device can then either issue a Repeated Start bit to address a different device (at High-Speed) or a Stop bit to return to Fast/Standard bus speed. After the Stop bit, any other master device (in a multi-master system) can arbitrate for the I^2C bus.

The MCP47FEBXX device does not acknowledge the HS Select byte. However, upon receiving this command, the device switches to HS mode.

See Figure 6-3 for illustration of HS mode command sequence.

For more information on the HS mode, or other I^2C modes, please refer to the NXP I^2C specification.

6.9.1 SLOPE CONTROL

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed clock modes of the interface.

6.9.2 PULSE GOBBLER

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes <10 ns during HS mode.

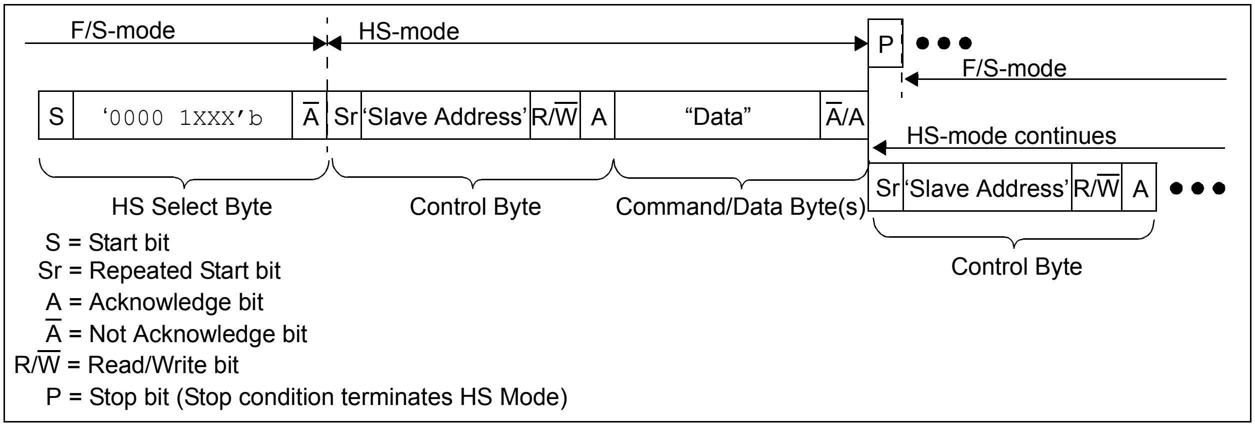


FIGURE 6-3: *HS Mode Sequence.*

7.0 DEVICE COMMANDS

This section documents the commands that the device supports.

The commands can be grouped into the following categories:

- Write Command (Normal and High-Voltage) (C1:C0 = ‘`00`’)
- Read Command (Normal and High-Voltage) (C1:C0 = ‘`11`’)
- General Call Commands
- Modify Device Configuration Bit Commands (HVC = V_{IHH})
  - Enable Configuration bit (C1:C0 = ‘`10`’)
  - Disable Configuration bit (C1:C0 = ‘`01`’)

The supported commands are shown in Table 7-1. These commands allow for both a single data or continuous data operation. Continuous data operation means that the I^2C Master does not generate a Stop bit but repeats the required data/clocks. This allows faster updates since the overhead of the I^2C control byte is removed. Table 7-1 also shows the required number of bit clocks for each command’s different mode of operation.

7.0.1 ABORTING A TRANSMISSION

A Restart or Stop condition in an expected data bit position will abort the current command sequence and if the command was a write, that data word will not be written to the MCP47FEBXX. Also the I^2C state machine will be reset.

If the condition was a Restart (Start), then the following byte will be expected to be the Slave Address byte.

If the condition was a Stop, the device will monitor for the Start Condition.

TABLE 7-1: DEVICE COMMANDS - NUMBER OF CLOCKS

Command					# of Bit Clocks (1)	Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)			Comments
Operation	Code		HV	Mode (6)					
	C1	C0				100kHz	400kHz	3.4MHz (5)	
Write Command (Normal and High-Voltage)	0	0	(3)	Single	38	2,632	10,526	89,474	
	0	0	(3)	Continuous	27n + 11	3,559	14,235	120,996	For 10 data words
Read Command (Normal and High-Voltage) (2)	1	1	(3)	Random	48	2,083	8,333	70,833	
	1	1	(3)	Continuous	18n + 11	4,762	19,048	161,905	For 10 data words
	1	1	(3)	Last Address	29	3,448	13,793	117,241	
General Call Reset Command	—	—	(3)	Single	20	5,000	20,000	170,000	**Note 4**
General Call Wake-up Command	—	—	(3)	Single	20	5,000	20,000	170,000	**Note 4**
Enable Configuration Bit (High-Voltage) Command	1	0	Yes	Single	20	5,000	20,000	170,000	
	1	0	Yes	Continuous	9n + 11	9,901	39,604	336,634	For 10 data words
Disable Configuration Bit (High-Voltage) Command	0	1	Yes	Single	20	5,000	20,000	170,000	
	0	1	Yes	Continuous	9n + 11	9,901	39,604	336,634	For 10 data words

Note 1: “n” indicates the number of times the command operation is to be repeated.
2: This command is useful to determine when an EEPROM programming cycle has completed.
3: This command can be either normal voltage or high voltage.
4: Determined by General Call command byte after the I^2C General Call address.
5: There is a minimal overhead to enter into 3.4 MHz mode.
6: Nonvolatile Registers can only use the “Single” mode.

7.1 Write Command (Normal and High-Voltage)

`Write` commands are used to transfer data to the desired memory location (from the Host controller). The `Write` command can be issued to both the Volatile and Nonvolatile memory locations.

`Write` commands can be structured as either Single or Continuous. The continuous format allows the fastest data update rate for the devices memory locations, but is not supported for nonvolatile memory locations.

The format of the command is shown in Figure 7-1 (Single) and Figure 7-3 (Continuous). For example ACK/NACK behavior see Figure 7-2.

A `Write` command to a Volatile memory location changes that location after a properly formatted Write Command and the A/$\overline{\text{A}}$ clock has been received.

A `Write` command to a nonvolatile memory location will start an EEPROM write cycle only after a properly formatted Write Command has been received and the Stop condition has occurred.

Note 1: Writes to certain memory locations will be dependent on the state of the WiperLock Technology status bits.

2: During device communication, if the Device Address/Command combination is invalid or an unimplemented Device Address is specified, then the MCP47FEBXX will NACK that byte. To reset the I^{2}C state machine, the I^{2}C communication must detect a Start bit.

7.1.1 SINGLE WRITE TO VOLATILE MEMORY

For volatile memory locations, data is written to the MCP47FEBXX after every data word transfer (during the Acknowledge). If a Stop or Restart condition is generated during a data transfer (before the A), the data will not be written to the MCP47FEBXX. After the A bit, the master can initiate the next sequence with a Stop or Restart condition.

Refer to Figure 7-1 for the byte write sequence.

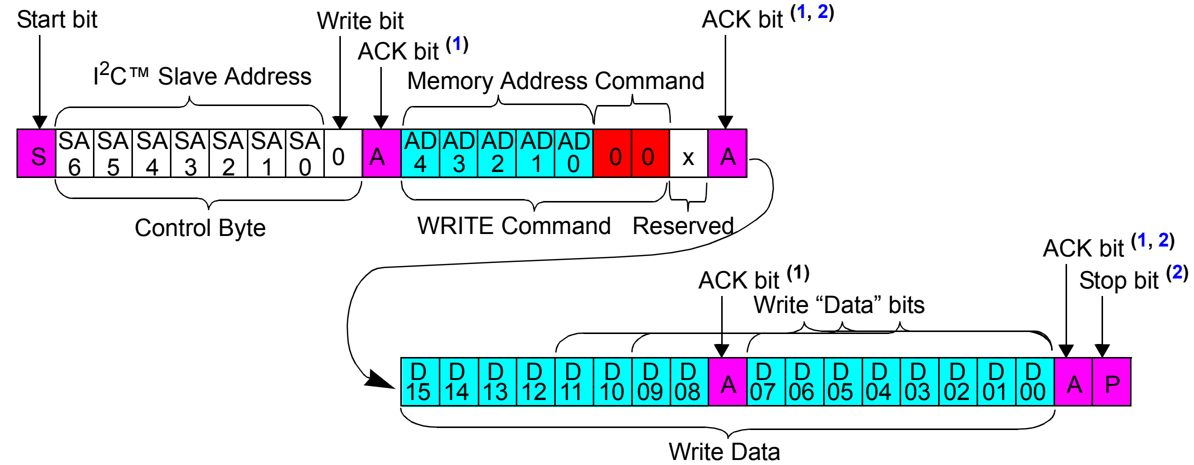
7.1.2 SINGLE WRITE TO NONVOLATILE MEMORY

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory with the exception that the EEPROM write cycle (t_{WC}) is started after a properly formatted command, including the Stop bit, is received. After the Stop condition occurs, the serial interface may immediately be re-enabled by initiating a Start condition.

During an EEPROM write cycle, access to the volatile memory is allowed when using the appropriate command sequence. Commands that address nonvolatile memory are ignored until the EEPROM write cycle (t_{WC}) completes. This allows the Host Controller to operate on the Volatile DAC registers.

Note: The EEWA status bit indicates if an EEPROM write cycle is active (see Register 4-4).

Figure 7-1 shows the waveform for a single write.



Note 1: The Acknowledge bit is generated by the MCP47FEBXX.

2: At the falling edge of the SCL pin for the Write command ACK bit, the MCP47FEBXX device updates the value of the specified device Register.

3: This command sequence does not need to terminate (using the Stop bit), and the `Write` command can be repeated (see continuous write format, **Section 7.1.3 "Continuous Writes to Volatile Memory"**).

FIGURE 7-1: *Write Random Address Command (Volatile and Nonvolatile Memory).*

7.1.3 CONTINUOUS WRITES TO VOLATILE MEMORY

A Continuous Write mode of operation is possible when writing to the device's volatile memory registers (see Table 7-1). This Continuous Write mode allows writes without a Stop or Restart condition or repeated transmissions of the I^2C Control Byte. Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address. The sequence ends with the master sending a Stop or Restart condition.

TABLE 7-1: VOLATILE MEMORY ADDRESSES

Address	Single-Channel	Dual-Channel
00h	Yes	Yes
01h	**No**	Yes
08h	Yes	Yes
09h	Yes	Yes
0Ah	Yes	Yes

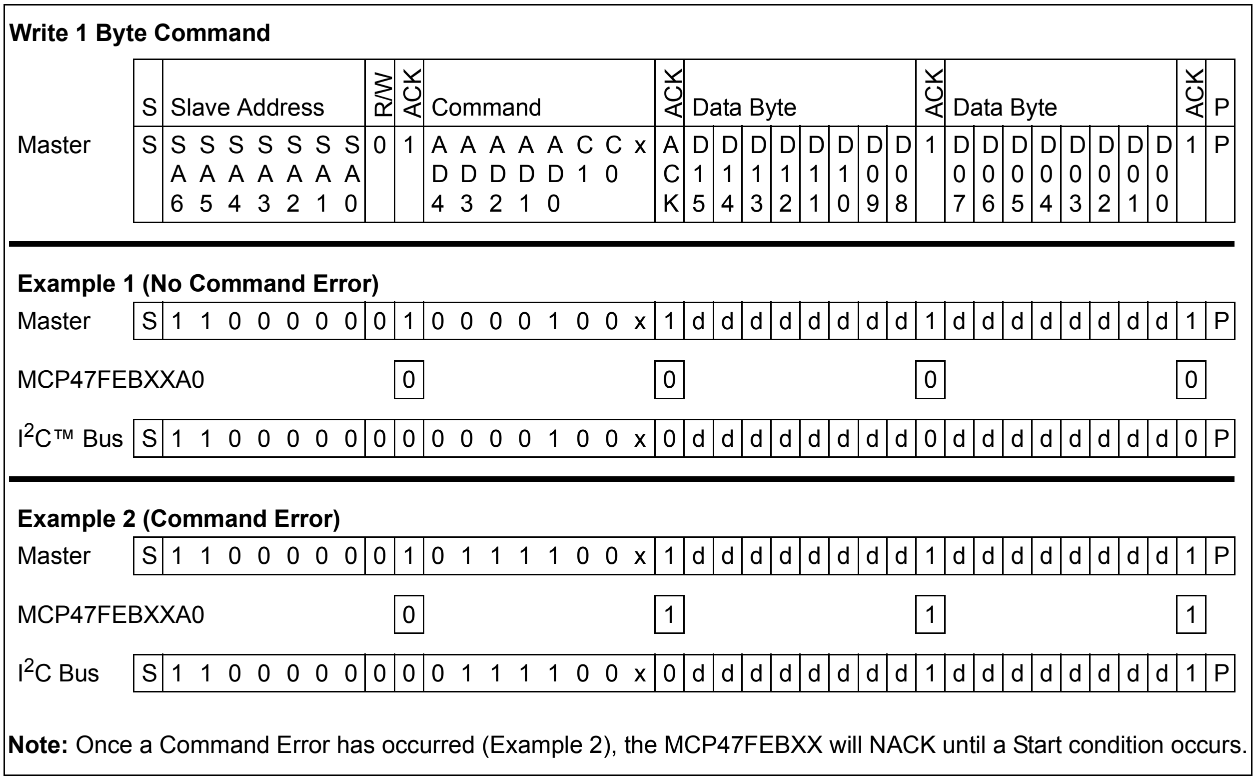
7.1.4 CONTINUOUS WRITES TO NONVOLATILE MEMORY

If a Continuous Write is attempted on nonvolatile memory, the missing Stop condition will cause the command to be an error condition ($\overline{A}$). A Start bit is required to reset the command state machine.

7.1.5 THE HIGH VOLTAGE COMMAND (HVC) SIGNAL

The `High Voltage` Command (HVC) signal is used to indicate that the command, or sequence of commands, are in the High Voltage operational state. `High Voltage` commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

Note: Writes to a volatile DAC register will not transfer to the output register until the LAT (HVC) pin is transitioned from the V_{IHHEN} voltage to a V_{IL} voltage.



Write 1 Byte Command

S | Slave Address | R/W | ACK | Command | ACK | Data Byte | ACK | Data Byte | ACK | P

Master: S | SA6 SA5 SA4 SA3 SA2 SA1 SA0 | 0 | 1 | AD4 AD3 AD2 AD1 AD0 C1 C0 x | ACK | D15 D14 D13 D12 D11 D10 D09 D08 | 1 | D07 D06 D05 D04 D03 D02 D01 D00 | 1 | P

Example 1 (No Command Error)

Master: S 1 1 0 0 0 0 0 0 1 0 0 0 0 1 0 0 x 1 d d d d d d d d 1 d d d d d d d d 1 P

MCP47FEBXXA0: 0 0 0 0

I^2C™ Bus: S 1 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 x 0 d d d d d d d d 0 d d d d d d d d 0 P

Example 2 (Command Error)

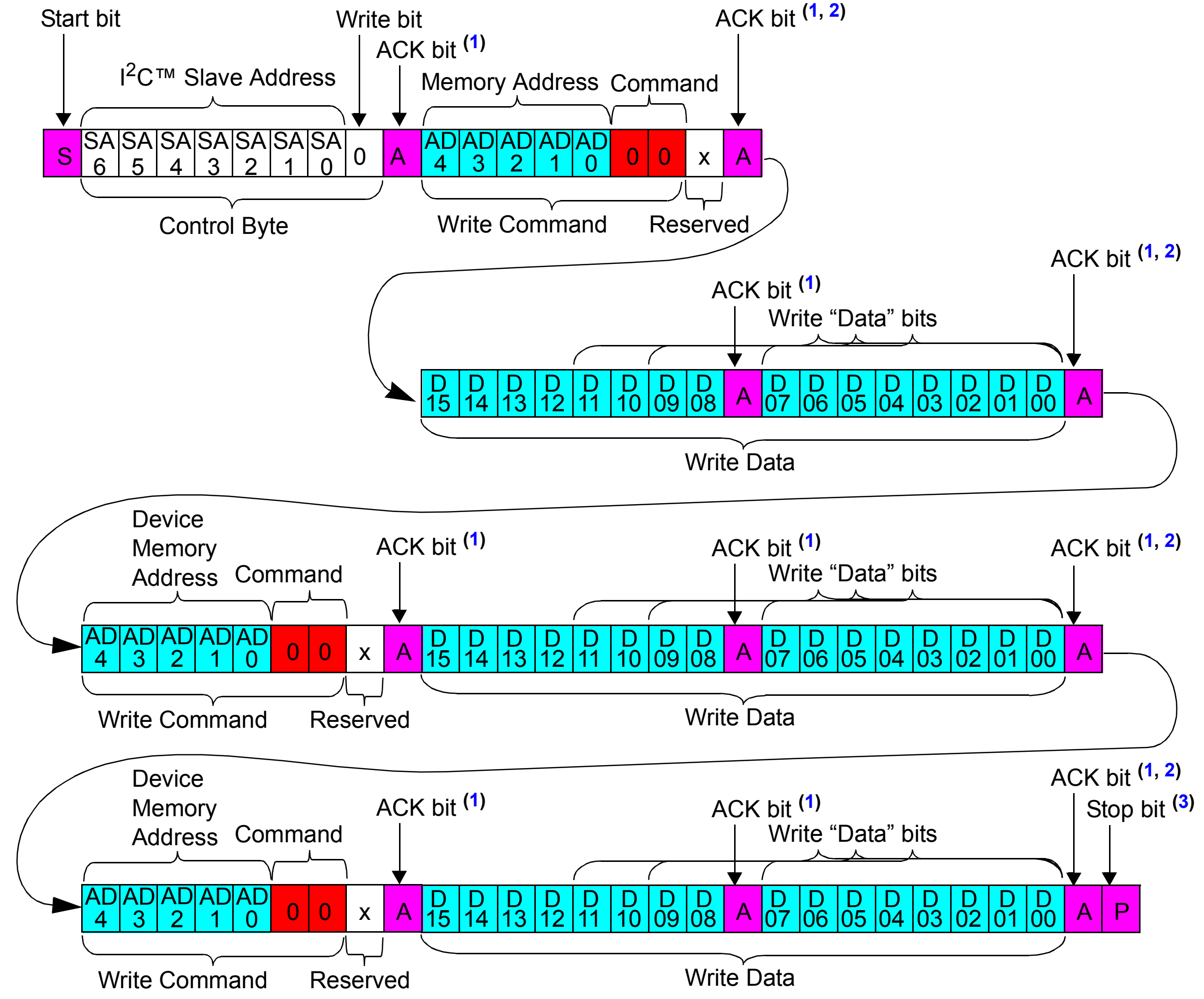
Master: S 1 1 0 0 0 0 0 0 1 0 1 1 1 1 0 0 x 1 d d d d d d d d 1 d d d d d d d d 1 P

MCP47FEBXXA0: 0 1 1 1

I^2C Bus: S 1 1 0 0 0 0 0 0 0 0 1 1 1 1 0 0 x 0 d d d d d d d d 1 d d d d d d d d 1 P

Note: Once a Command Error has occurred (Example 2), the MCP47FEBXX will NACK until a Start condition occurs.

FIGURE 7-2: *I^2C ACK / NACK Behavior (Write Command Example).*



Note 1: The Acknowledge bit is generated by the MCP47FEBXX.

2: At the falling edge of the SCL pin for the Write command ACK bit, the MCP47FEBXX device updates the value of the specified device Register.

3: This command sequence does not need to terminate (using the Stop bit), and the Write command can be repeated (see continuous write format, **Section 7.1.3 "Continuous Writes to Volatile Memory"**).

4: Only functions when writing to volatile registers (AD4:AD0 = 00h through 0Ah).

FIGURE 7-3: *Continuous Write Commands (Volatile Memory Only).*

7.2 Read Command (Normal and High-Voltage)

`Read` commands are used to transfer data from the specified memory location (to the Host controller). The `Read` command can be issued to both the Volatile and Nonvolatile memory locations.

During an EEPROM write cycle (Write to nonvolatile memory location or `Enable/Disable Configuration Bit` command) the `Read` command can only read the volatile memory locations. By reading the Status Register (0Ah), the Host Controller can determine when the write cycle has completed (via the state of the EEWA bit).

The `Read` command formats include:

- **Single Read**
  - **Single Memory Address**
  - **Last Memory Address Accessed**
- **Continuous Reads**

The MCP47FEBXX retains the last Device Memory Address that it has received. That is the MCP47FEBXX does not corrupt the Device Memory Address after Repeated Start or Stop conditions.

If the address pointer is for a nonvolatile memory location and it is during a Nonvolatile Write Cycle (t_{WC}) the MCP47FEBXX will respond with an $\overline{A}$ bit.

Note 1: During device communication, if the Device Address/Command combination is invalid or an unimplemented Address is specified, then the MCP47FEBXX will NACK that byte. To reset the I^2C state machine, the I^2C communication must detect a Start bit.

2: If the LAT pin is High (V_{IH}), reads of the volatile DAC Register read the output value, not the internal register.

3: The `Read` commands operate the same regardless of the state of the High-Voltage Command (HVC) signal.

7.2.1 SINGLE READ

The `Read` command format writes two bytes, the Control byte and the `Read` command byte (desired memory address and the `Read` command), and then has a Restart condition. Then a 2nd Control byte is transmitted, but this control byte indicates a I^2C read operation (R/W bit = ‘`1`’).

7.2.1.1 Single Memory Address

Figure 7-4 shows the sequence for reading a specified memory address.

7.2.1.2 Last Memory Address Accessed

Figure 7-5 shows the waveforms for a single read of the last memory location accessed.

This command allows faster communication when checking the status of the EEPROM Write Active (EEWA) bit (see Register 4-4), as long as the Register Address of this device’s last command was 0Ah.

7.2.2 CONTINUOUS READS

`Continuous reads` allows the device’s memory to be read quickly. `Continuous reads` are possible to all memory locations. If a nonvolatile memory write cycle is occurring, then `Read` commands may only access the volatile memory locations.

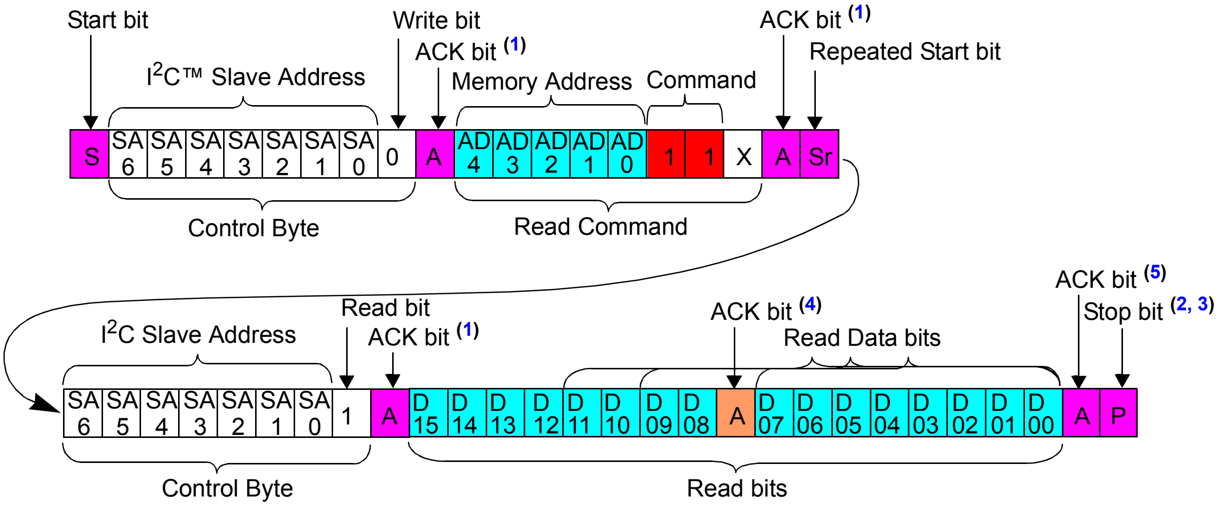
Figure 7-7 shows the sequence for three continuous reads.

For continuous reads, instead of transmitting a Stop or Restart condition after the data transfer, the master continually reads the data byte. The sequence ends with the master Not Acknowledging and then sending a Stop or Restart.

This is useful in reading the System Status register (0Ah) to determine if an EEPROM write cycle has completed (EEWA bit).

7.2.3 IGNORING AN I^2C TRANSMISSION AND “FALLING OFF” THE BUS

The MCP47FEBXX expects to receive complete, valid I^2C commands and will assume any command not defined as a valid command is due to a bus corruption, thus entering a passive high condition on the SDA signal. All signals will be ignored until the next valid Start condition and Control Byte are received.



Note 1: The Acknowledge bit is generated by the MCP47FEBXX.

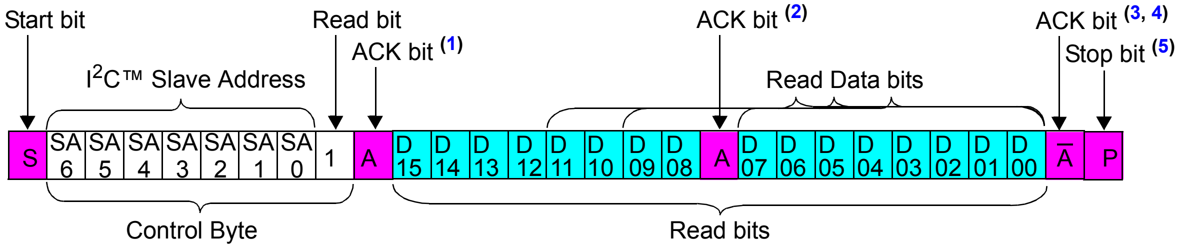
2: At the falling edge of the SCL pin for the Read command ACK bit, the MCP47FEBXX device updates the value of the specified device Register.

3: This command sequence does not need to terminate (using the Stop bit), and the Read command can be repeated (see continuous read format, **Section 7.2.2 "Continuous Reads"**).

4: Master Device is responsible for A/$\overline{\text{A}}$ signal. If an $\overline{\text{A}}$ signal occurs, the MCP47FEBXX will abort this transfer and release the bus.

5: The Master Device will Not Acknowledge, and the MCP47FEBXX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

FIGURE 7-4: *Read Command - Single Memory Address.*



Note 1: The Acknowledge bit is generated by the MCP47FEBXX.

2: Master Device is responsible for A/$\overline{\text{A}}$ signal. If a $\overline{\text{A}}$ signal occurs, the MCP47FEBXX will abort this transfer and release the bus.

3: The Master Device will Not Acknowledge, and the MCP47FEBXX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

4: At the falling edge of the SCL pin for the Read command ACK bit, the MCP47FEBXX device updates the value of the specified device Register.

5: This command sequence does not need to terminate (using the Stop bit), and the Read command can be repeated (see continuous read format, **Section 7.2.2 "Continuous Reads"**).

FIGURE 7-5: *Read Command - Last Memory Address Accessed.*

Write 1 Byte Command

	S	Slave Address	R/W	ACK	Command	ACK
Master	S	SA6 SA5 SA4 SA3 SA2 SA1 SA0	0	1	AD4 AD3 AD2 AD1 AD0 C1 C0 x	1

	Sr	Slave Address	R/W	ACK	Data Byte	ACK	Data Byte	ACK	P
Master (Continued)	Sr	SA6 SA5 SA4 SA3 SA2 SA1 SA0	1	1	D15 D14 D13 D12 D11 D10 D09 D08	1	D07 D06 D05 D04 D03 D02 D01 D00	1	P

Ex.1 (No Command Error)

	S	Slave Address	R/W	ACK	Command	ACK
Master	S	1 1 0 0 0 0 0	0	1	0 0 0 0 1 1 1 x	1
MCP47FEBXXA0				0		0
I^{2}C™ Bus	S	1 1 0 0 0 0 0	0	0	0 0 0 0 0 1 1 x	0

	Sr	Slave Address	R/W	ACK	Data Byte	ACK	Data Byte	ACK	P
Master (Continued)	S	0 0 0 0 1 0 0	1	1		1		1	P
MCP47FEBXXA0 (Continued)				0	d d d d d d d d	0	d d d d d d d d	0	
I^{2}C Bus (Continued)	S	0 0 0 0 0 0 0	1	0	d d d d d d d d	0	d d d d d d d d	0	P

Ex.2 (With Command Error)

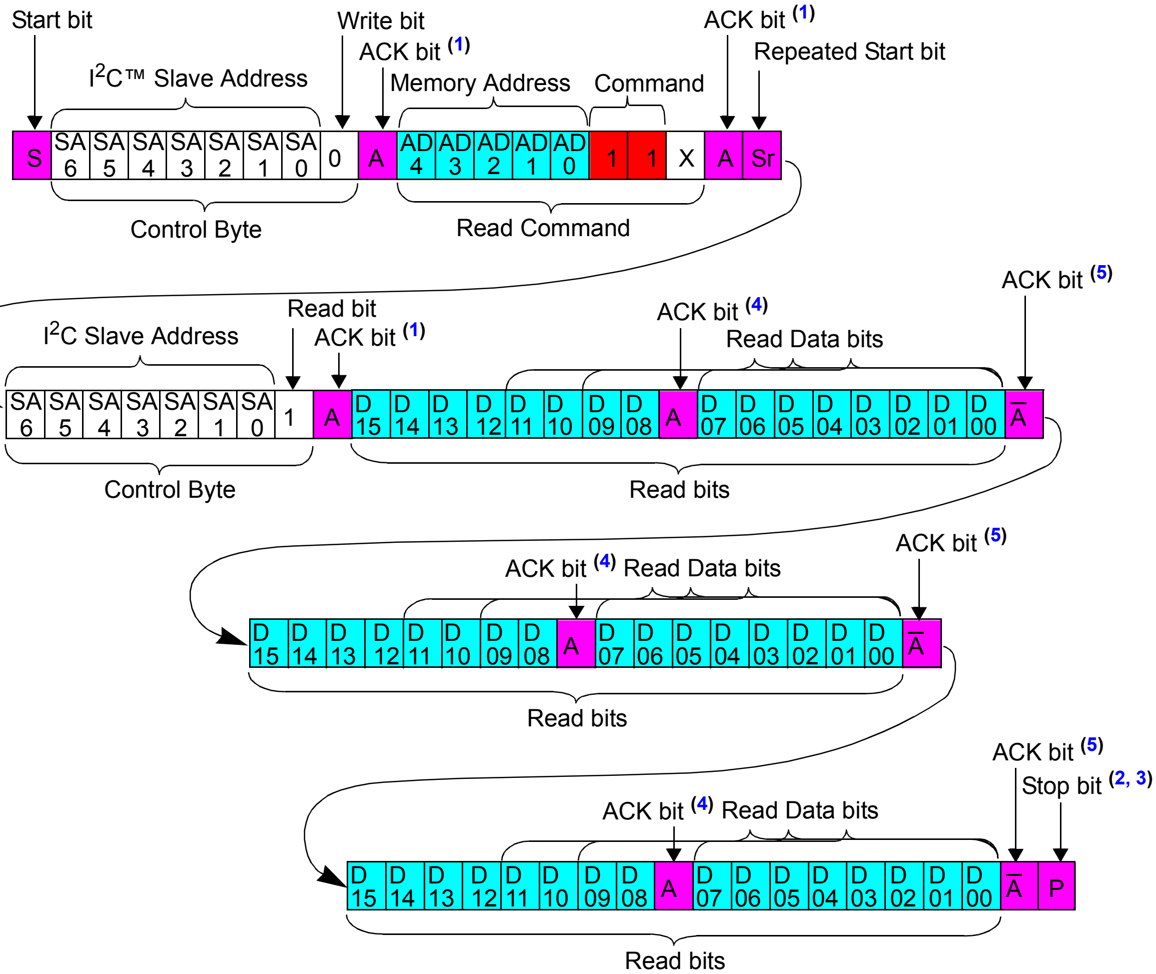
	S	Slave Address	R/W	ACK	Command	ACK
Master	S	1 1 0 0 0 0 0	0	1	0 1 1 1 1 0 0 x	1
MCP47FEBXXA0				0		1
I^{2}C Bus	S	1 1 0 0 0 0 0	0	0	0 1 1 1 1 0 0 x	1

	Sr	Slave Address	R/W	ACK	Data Byte	ACK	Data Byte	ACK	P
Master (Continued)	S	1 1 0 0 0 0 0	1	1		1		1	P
MCP47FEBXXA0 (Continued)				0	? ? ? ? ? ? ? ?	0	? ? ? ? ? ? ? ?	1	
I^{2}C Bus (Continued)	S	1 1 0 0 0 0 0	1	0	? ? ? ? ? ? ? ?	0	? ? ? ? ? ? ? ?	1	P

Note 1: Once a Command Error has occurred (Example 2), the MCP47FEBXX will NACK until a Start condition occurs.

2: For Command Error case (Example 2), the data read is from the register of the last valid address loaded into the device.

FIGURE 7-6: I^{2}C ACK/NACK Behavior (Read Command Example).



Note 1: The Acknowledge bit is generated by the MCP47FEBXX.

2: At the falling edge of the SCL pin for the Read command ACK bit, the MCP47FEBXX device updates the value of the specified device register.

3: This command sequence does not need to terminate (using the Stop bit), and the Read command can be repeated (see continuous read format, **Section 7.2.2 "Continuous Reads"**).

4: Master Device is responsible for A / $\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MCP47FEBXX will abort this transfer and release the bus.

5: The Master Device will Not Acknowledge, and the MCP47FEBXX will release the bus so the Master Device can generate a Stop or Repeated Start condition.

FIGURE 7-7: *Continuous Read Command Of Specified Address.*

7.3 General Call Commands

The MCP47FEBXX acknowledges the General Call Address command (00h in the first byte). General Call commands can be used to communicate to all devices on the I^{2}C bus (at the same time) that understand the General Call command. The meaning of the general call address is always specified in the second byte (see Figure 7-8).

If the second byte has a '1' in the LSb, the specification intends this to indicate a "Hardware General Call". The MCP47FEBXX will ignore this byte and all following bytes (and $\overline{A}$), until a Stop bit (P) is encountered.

The MCP47FEBXX devices support the following I^{2}C General Call commands:

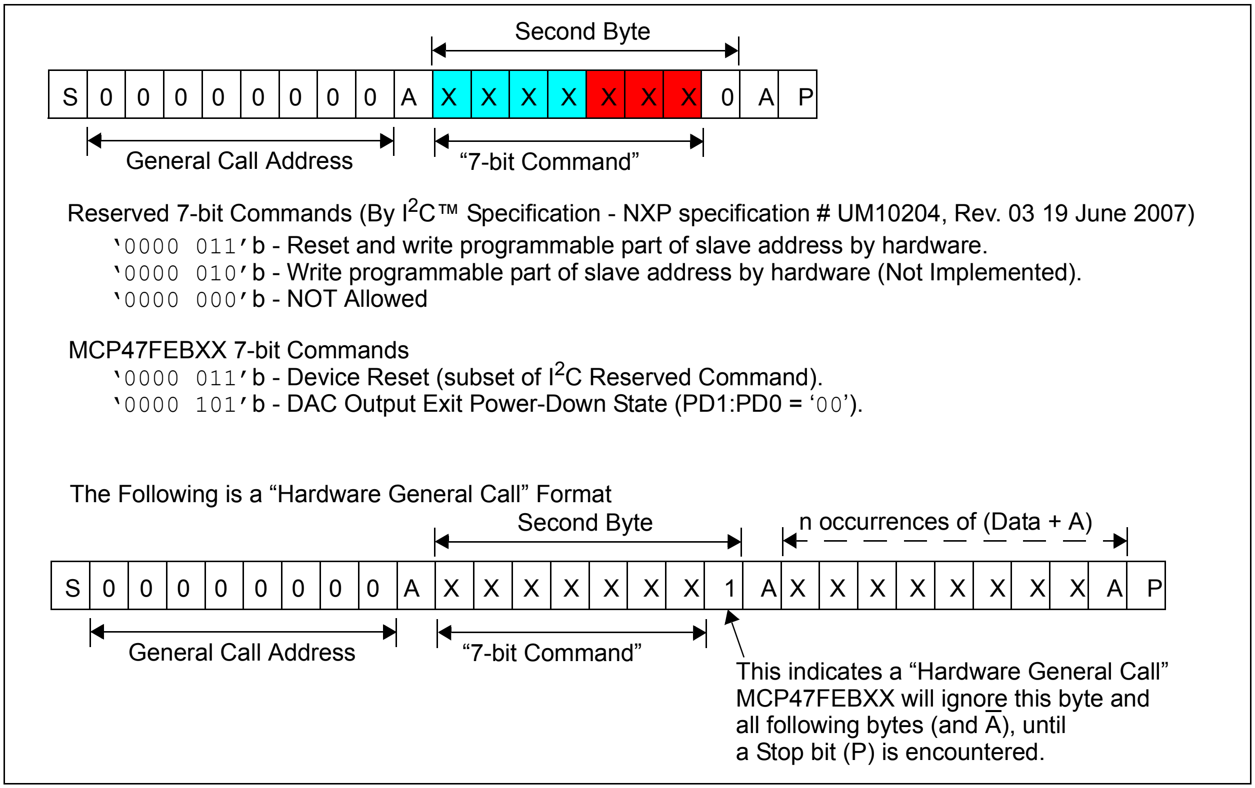
- **General Call Reset** (06h)
- **General Call Wake-up** (0Ah)

The General Call Reset command format is specified by the I^{2}C Specification. The General Call Wake-Up command is a Microchip-defined format. The General Call Wake-Up command will have all devices wake-up (that is, exit the Power-Down mode).

The other two I^{2}C Specification command codes (04h and 00h) are not supported, and therefore those commands are Not Acknowledged.

If these 7-bit commands conflict with other I^{2}C devices on the bus, then the customer will need two I^{2}C buses and ensure that the devices are on the correct bus for their desired application functionality.

> **Note:** Refer to the NXP specification #UM10204, Rev. 03 19 June 2007 document for more details on the General Call specifications. The I^{2}C specification does not allow '00000000' (00h) in the second byte.



Reserved 7-bit Commands (By I^{2}C™ Specification - NXP specification # UM10204, Rev. 03 19 June 2007)

'0000 011'b - Reset and write programmable part of slave address by hardware.
'0000 010'b - Write programmable part of slave address by hardware (Not Implemented).
'0000 000'b - NOT Allowed

MCP47FEBXX 7-bit Commands

'0000 011'b - Device Reset (subset of I^{2}C Reserved Command).
'0000 101'b - DAC Output Exit Power-Down State (PD1:PD0 = '00').

The Following is a "Hardware General Call" Format

This indicates a "Hardware General Call"
MCP47FEBXX will ignore this byte and all following bytes (and $\overline{A}$), until a Stop bit (P) is encountered.

FIGURE 7-8: General Call Formats.

7.3.1 GENERAL CALL RESET

The I^2C `General Call Reset` command forces a reset event. This is similar to the Power-on Reset, except that the reset delay timer is not started. This command allows multiple MCP47FEBXX devices to be reset synchronously.

The device performs `General Call Reset` if the second byte is “`00000110`” (06h). At the acknowledgment of this byte, the device will abort the current conversion and perform the following tasks:

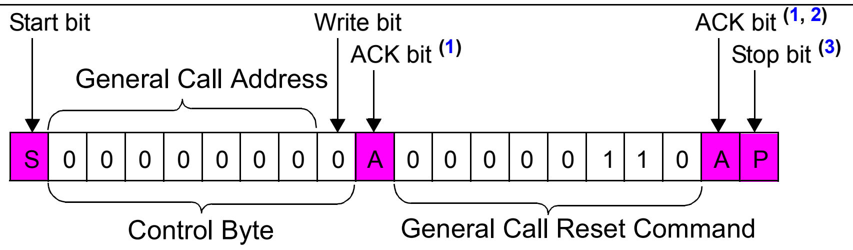
- Internal Reset similar to a Power-on Reset (POR). The contents of the EEPROM are loaded into the DAC registers and analog output is available immediately (following the Acknowledgment pulse).
- The V_{OUT} will be available immediately, but after a short time delay following the Acknowledgment pulse. The V_{OUT} value is determined by the EEPROM contents.

7.3.2 GENERAL CALL WAKE-UP

The I^2C `General Call Wake-up` command forces the device to exit from it’s Power-Down state (forces the PDxB:PDxA bits to ‘`00`’). This command allows multiple MCP47FEBXX devices to wake-up synchronously.

The device performs `General Call Wake-up` if the second byte (after the General Call Address) is “`00001010`” (0Ah). At the acknowledgment of this byte, the device will perform the following task:

- The device’s volatile power-down bits (PDxB:PDxA) are forced to ‘`00`’. The nonvolatile (EEPROM) power-down bit values are not affected by this command.

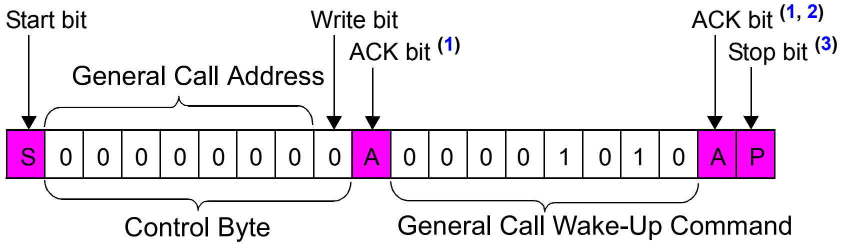


Note 1: The Acknowledge bit is generated by the MCP47FEBXX.

2: At the falling edge of the SCL pin for the `General Call Wake-Up` command ACK bit, the MCP47FEBXX device is reset.

3: This command sequence does not need to terminate (using the Stop bit), and the `General Call Wake-Up` command can be repeated, or the `General Call Reset` command can be sent.

FIGURE 7-9: *General Call Reset Command.*



Note 1: The Acknowledge bit is generated by the MCP47FEBXX.

2: At the falling edge of the SCL pin for the `General Call Wake-Up` command ACK bit, the volatile power-down bits (PDxB:PDxA) are forced to ‘`00`’.

3: This command sequence does not need to terminate (using the Stop bit), and the `General Call Wake-Up` command can be repeated, or the `General Call Reset` command can be sent.

FIGURE 7-10: *General Call Wake-Up Command.*

7.4 Modify Device Configuration Bit Commands

These commands are used to program the Device Configuration bits. These commands require a high voltage (V_{IHH}) on the HVC pin.

The MCP47FEBXX devices support the `Modify Device Configuration Bit` commands:

- **Enable Configuration Bit (High-Voltage)**
- **Disable Configuration Bit (High-Voltage)**

These Configuration bits are used to inhibit the DAC values from inadvertent modification. High voltage is required to change the state of these bits if/when the DAC values need to be modified.

7.5 Enable Configuration Bit (High-Voltage)

Figure 7-11 (Enable) shows the formats for a single `Modify Write Protect` or `Wiper-Lock Technology` command.

A `Modify Write Protect` or `Wiper-Lock Technology` command will only start an EEPROM write cycle (t_{WC}) after a properly formatted command has been received and the Stop condition occurs.

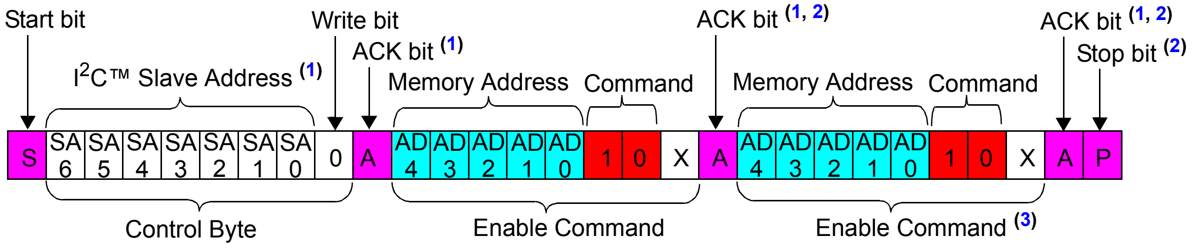
During an EEPROM write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes. This allows the Host Controller to operate on the volatile DAC, the volatile V_{REF}, Power-down, Gain and Status, and WiperLock Technology Status registers. The EEWA bit in the Status register indicates the status of an EEPROM Write Cycle.

7.5.1 THE HIGH-VOLTAGE COMMAND (HVC) SIGNAL

The High-Voltage Command (HVC) signal is used to indicate that the command, or sequence of commands, are in the High-Voltage mode. Signals >V_{IHH} (~9.0V) on the HVC pin puts the device into High-Voltage mode. `High Voltage` commands allow the device's WiperLock Technology and write-protect features to be enabled and disabled.

Note 1: There is a required delay after the HVC pin is driven to the V_{IHH} level to the 1st edge of the SCL pin.

2: The command sequence can go from an increment to any other valid command for the specified address. Issuing an increment or decrement to a nonvolatile location will cause an error condition ($\overline{A}$ will be generated).



Note 1: The Slave address is determined by the NV Gain and I²C 7-bit Slave Address Register. The default factory address is '`110 0000b`' (C0h for Control byte with write, C1h for Control byte with read).

2: This command sequence does not need to terminate (using the Stop bit) and can change to any other desired command sequence (`Disable`, `Read` or `Write`).

3: This command byte is not required and the Stop bit may occur immediately after the 2nd ACK bit in this sequence.

FIGURE 7-11: *I²C Enable Command Sequence.*

7.6 Disable Configuration Bit (High-Voltage)

Figure 7-12 (Disable) shows the formats for a single `Modify Write Protect` or `Wiper-Lock Technology` command.

A `Modify Write Protect` or `Wiper-Lock Technology` command will only start an EEPROM write cycle (t_{WC}) after a properly formatted command has been received and the Stop condition occurs.

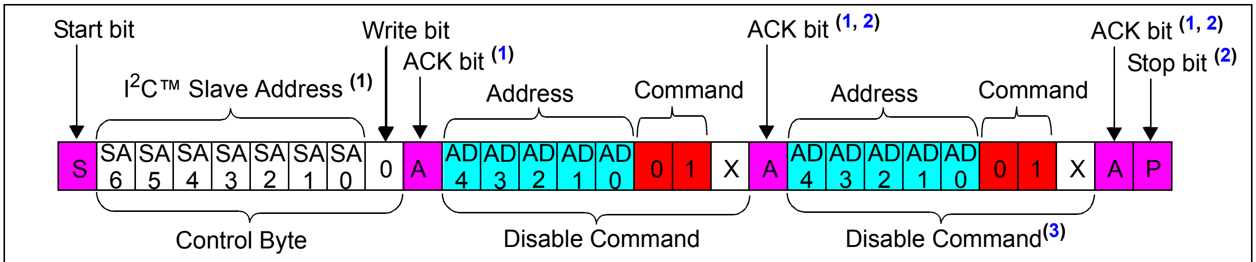
During an EEPROM write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the EEPROM write cycle (t_{WC}) completes. This allows the Host Controller to operate on the volatile DAC, the volatile V_{REF}, Power-down, Gain and Status, and WiperLock Technology Status registers. The EEWA bit in the Status register indicates the status of an EEPROM Write Cycle.

7.6.1 THE HIGH-VOLTAGE COMMAND (HVC) SIGNAL

The `High Voltage Command` (HVC) signal is used to indicate that the command, or sequence of commands, are in the High-Voltage mode. Signals >V_{IHH} (~9.0V) on the HVC pin puts MCP47FEBXX devices into High-Voltage mode. `High Voltage` commands allow the device's WiperLock Technology and write protect features to be enabled and disabled.

Note 1: There is a required delay after the HVC pin is driven to the V_{IHH} level to the 1st edge of the SCL pin.

2: The command sequence can go from an increment to any other valid command for the specified address. Issuing an increment or decrement to a nonvolatile location will cause an error condition ($\overline{A}$ will be generated).

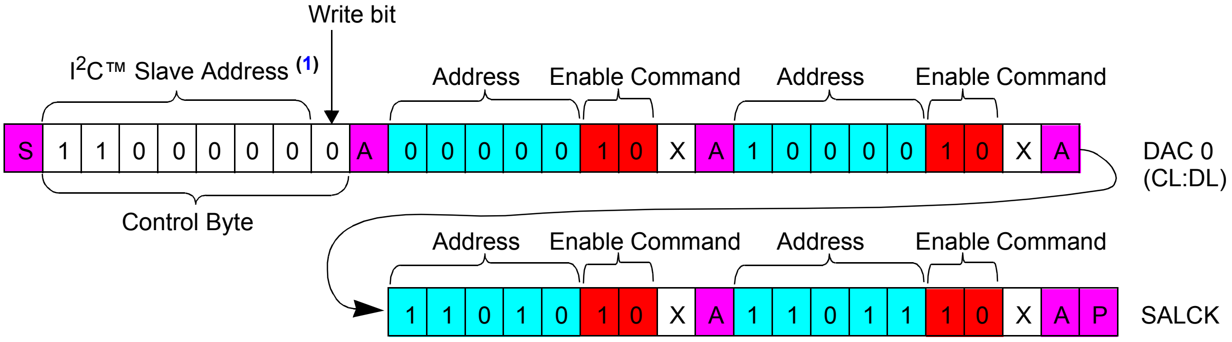


Note 1: The Slave address is determined by the NV Gain and I^2C 7-bits Slave Address Register. The default factory address is '`110 0000b`' (C0h for Control byte with write, C1h for Control byte with read).

2: This command sequence does not need to terminate (using the Stop bit) and can change to any other desired command sequence (`Enable`, `Read` or `Write`).

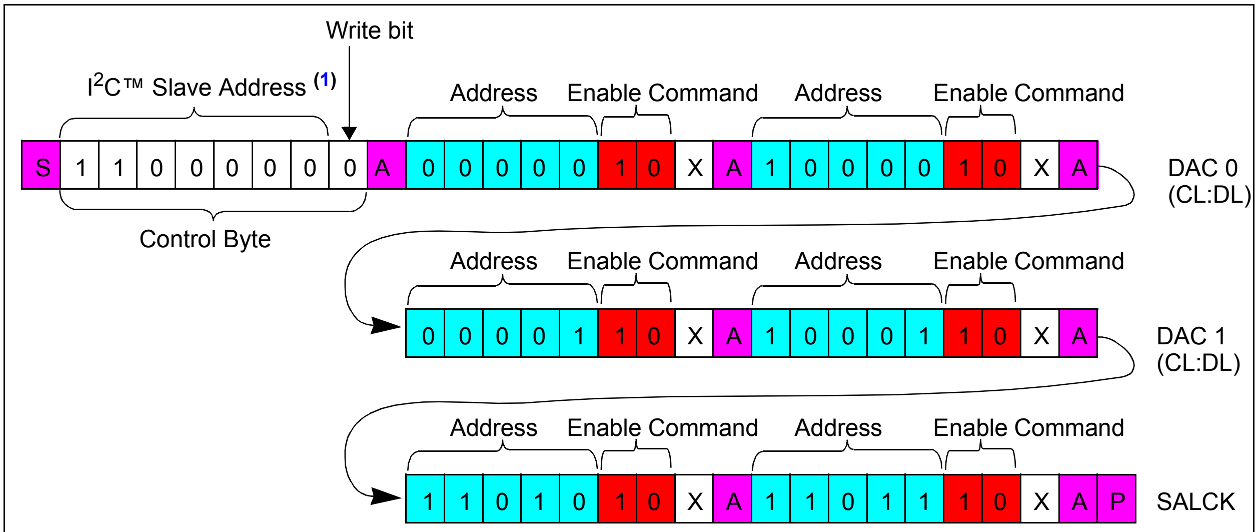
3: This command byte is not required and the Stop bit may occur immediately after the 2nd ACK bit in this sequence.

FIGURE 7-12: *I^2C Disable Command Sequence.*



Note 1: The two command bits may either specify the `Enable` Command or the `Disable` Command.

FIGURE 7-13: Configuring All User Configuration Bits Command Sequence (MCP47FEBX1).



Note 1: The two command bits may either specify the `Enable` command or the `Disable` command.

FIGURE 7-14: Configuring All User Configuration Bits Command Sequence (MCP47FEBX2).

NOTES:

8.0 TYPICAL APPLICATIONS

The MCP47FEBXX family of devices are general purpose, single/dual-channel voltage output DACs for various applications where a precision operation with low-power and nonvolatile EEPROM memory is needed.

Since the devices include a nonvolatile EEPROM memory, the user can utilize these devices for applications that require the output to return to the previous set-up value on subsequent power-ups.

Applications generally suited for the devices are:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery-Powered)
- Motor Control

8.1 Connecting to I^{2}C BUS using Pull-Up Resistors

The SCL and SDA pins of the MCP47FEBXX devices are open-drain configurations. These pins require a pull-up resistor, as shown in Figure 8-2.

The pull-up resistor values (R_1 and R_2) for SCL and SDA pins depend on the operating speed (standard, fast and high-speed) and loading capacitance of the I^{2}C bus line. A higher value of the pull-up resistor consumes less power, but increases the signal transition time (higher RC time constant) on the bus line. Therefore, it can limit the bus operating speed. The lower resistor value, on the other hand, consumes higher power, but allows higher operating speed. If the bus line has higher capacitance due to long metal traces or multiple device connections to the bus line, a smaller pull-up resistor is needed to compensate the long RC time constant. The pull-up resistor is typically chosen between 1 kΩ and 10 kΩ ranges for Standard and Fast modes, and less than 1 kΩ for High-Speed mode.

8.1.1 DEVICE CONNECTION TEST

The user can test the presence of the device on the I^{2}C bus line using a simple I^{2}C command. This test can be achieved by checking an acknowledge response from the device after sending a `Read` or `Write` command. Figure 8-1 shows an example with a `Read` command. The steps are:

1. Set the R/$\overline{\text{W}}$ bit “High” in the device’s address byte.
2. Check the ACK bit of the address byte.
   If the device acknowledges (ACK = `0`) the command, then the device is connected. Otherwise, it is not connected.
3. Send Stop bit.

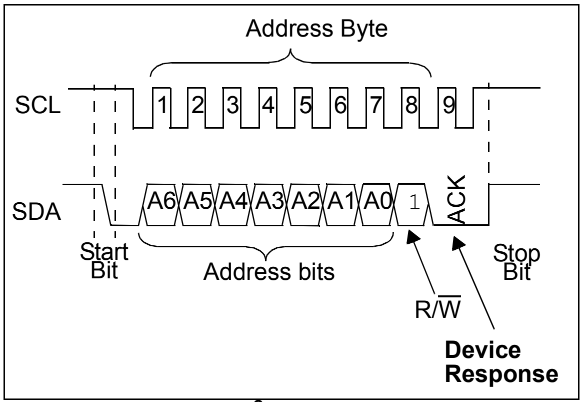
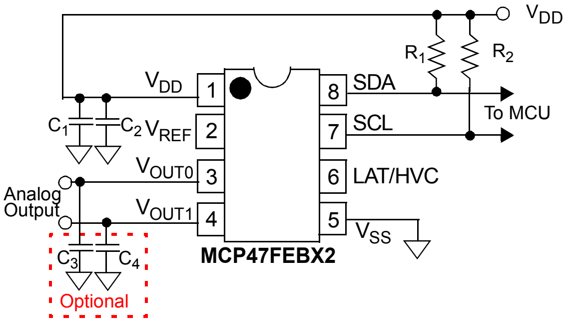


FIGURE 8-1: I^{2}C Bus Connection Test.

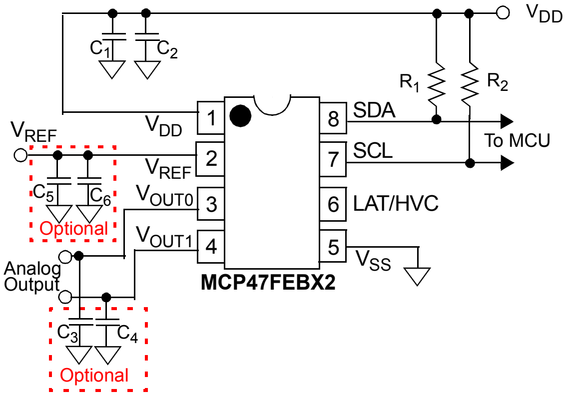
8.2 Power Supply Considerations

The power source should be as clean as possible. The power supply to the device is also used for the DAC voltage reference internally if the internal V_{DD} is selected as the resistor ladder's reference voltage (VRxB:VRxA = '`00`').

Any noise induced on the V_{DD} line can affect the DAC performance. Typical applications will require a bypass capacitor in order to filter out high-frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-2 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device should reside on the analog plane.



(a) Circuit when V_{DD} is selected as reference
(**Note:** V_{DD} is connected to the reference circuit internally.)



(b) Circuit when external reference is used.

R_1 and R_2 are I^{2}C™ pull-up resistors:

R_1 and R_2:

5 kΩ - 10 kΩ for f_{SCL} = 100 kHz to 400 kHz

~700Ω for f_{SCL} = 3.4 MHz

C_1:	0.1 µF capacitor	Ceramic
C_2:	10 µF capacitor	Tantalum
C_3:	~ 0.1 µF	Optional to reduce noise in V_{OUT} pin.
C_4:	0.1 µF capacitor	Ceramic
C_5:	10 µF capacitor	Tantalum
C_6:	0.1 µF capacitor	Ceramic

FIGURE 8-2: *Example Circuit.*

8.3 Application Examples

The MCP47FEBXX devices are rail-to-rail output DACs designed to operate with a V_{DD} range of 2.7V to 5.5V. The internal output op amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of external buffers for most applications. The user can use gain of 1 or 2 of the output op amplifier by setting the Configuration register bits. Also, the user can use internal V_{DD} as the reference or use external reference. Various user options and easy-to-use features make the devices suitable for various modern DAC applications.

Application examples include:

- Decreasing Output Step Size
- Building a “Window” DAC
- Bipolar Operation
- Selectable Gain and Offset Bipolar Voltage Output
- Designing a Double-Precision DAC
- Building Programmable Current Source
- Serial Interface Communication Times
- Software I^{2}C Interface Reset Sequence
- Power Supply Considerations
- Layout Considerations

8.3.1 DC SET POINT OR CALIBRATION

A common application for the devices is a digitally-controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP47FEB2X provides 4096 output steps. If voltage reference is 4.096V (where Gx = ‘`0`’), the LSb size is 1 mV. If a smaller output step size is desired, a lower external voltage reference is needed.

8.3.1.1 Decreasing Output Step Size

If the application is calibrating the bias voltage of a diode or transistor, a bias voltage range of 0.8V may be desired with about 200 µV resolution per step. Two common methods to achieve small step size are using lower V_{REF} pin voltage or using a voltage divider on the DAC’s output.

Using an external voltage reference (V_{REF}) is an option if the external reference is available with the desired output voltage range. However, occasionally, when using a low-voltage reference voltage, the noise floor causes a SNR error that is intolerable. Using a voltage divider method is another option, and provides some advantages when external voltage reference needs to be very low, or when the desired output voltage is not available. In this case, a larger value reference voltage is used, while two resistors scale the output range down to the precise desired level.

Figure 8-3 illustrates this concept. A bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

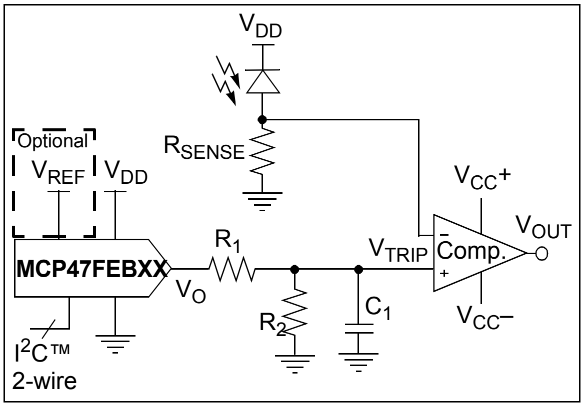


FIGURE 8-3: *Example Circuit Of Set Point or Threshold Calibration.*

EQUATION 8-1: V_{OUT} AND V_{TRIP} CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{trip} = V_{OUT}\left(\frac{R_2}{R_1 + R_2}\right)$$

8.3.1.2 Building a “Window” DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application’s accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near V_{REF}, 2 • V_{REF}, or V_{SS}, then creating a “window” around the threshold has several advantages. One simple method to create this “window” is to use a voltage divider network with a pull-up and pull-down resistor. Figure 8-4 and Figure 8-6 illustrate this concept.

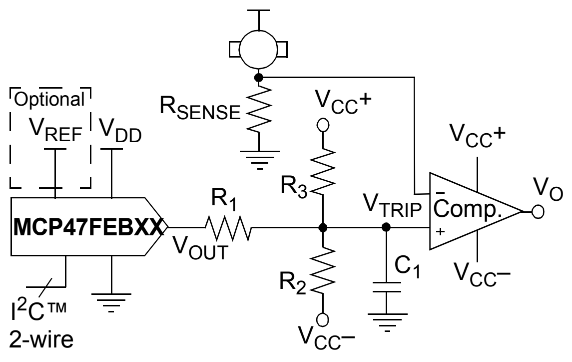


FIGURE 8-4: *Single-Supply “Window” DAC.*

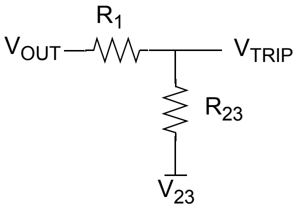
EQUATION 8-2: V_{OUT} AND V_{TRIP} CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{TRIP} = \frac{V_{OUT}R_{23} + V_{23}R_1}{R_1 + R_{23}}$$

Thevenin Equivalent

$$\begin{cases} R_{23} = \dfrac{R_2R_3}{R_2 + R_3} \\ V_{23} = \dfrac{(V_{CC+}R_2) + (V_{CC-}R_3)}{R_2 + R_3} \end{cases}$$



8.4 Bipolar Operation

Bipolar operation is achievable by utilizing an external operational amplifier. This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Figure 8-5 illustrates a simple bipolar voltage source configuration. R_1 and R_2 allow the gain to be selected, while R_3 and R_4 shift the DAC's output to a selected offset. Note that R4 can be tied to V_{DD} instead of V_{SS} if a higher offset is desired.

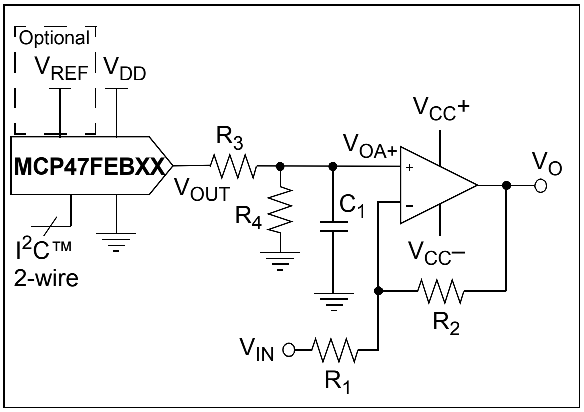


FIGURE 8-5: *Digitally-Controlled Bipolar Voltage Source Example Circuit.*

EQUATION 8-3: V_{OUT}, V_{OA+}, AND V_O CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4}{R_3 + R_4}$$

$$V_O = V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right) - V_{DD} \bullet \left(\frac{R_2}{R_1}\right)$$

8.5 Selectable Gain and Offset Bipolar Voltage Output

In some applications, precision digital control of the output range is desirable. Figure 8-6 illustrates how to use the DAC devices to achieve this in a bipolar or single-supply application.

This circuit is typically used for linearizing a sensor whose slope and offset varies.

The equation to design a bipolar “window” DAC would be utilized if R_3, R_4 and R_5 are populated.

8.5.1 BIPOLAR DAC EXAMPLE

An output step size of 1 mV, with an output range of ±2.05V, is desired for a particular application.

Step 1: Calculate the range: +2.05V – (-2.05V) = 4.1V.

Step 2: Calculate the resolution needed:

4.1V/1 mV = 4100

Since 2^{12} = 4096, 12-bit resolution is desired.

Step 3: The amplifier gain (R_2/R_1), multiplied by full-scale V_{OUT} (4.096V), must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values ($R_1 + R_2$), the V_{REF} value must be selected first. If a V_{REF} of 4.096V is used, solve for the amplifier's gain by setting the DAC to 0, knowing that the output needs to be -2.05V.

The equation can be simplified to:

EQUATION 8-4:

$$\frac{-R_2}{R_1} = \frac{-2.05}{4.096V} \qquad \frac{R_2}{R_1} = \frac{1}{2}$$

If R_1 = 20 kΩ and R_2 = 10 kΩ, the gain will be 0.5.

Step 4: Next, solve for R_3 and R_4 by setting the DAC to 4096, knowing that the output needs to be +2.05V.

EQUATION 8-5:

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot 4.096V)}{1.5 \cdot 4.096V} = \frac{2}{3}$$

If R_4 = 20 kΩ, then R_3 = 10 kΩ

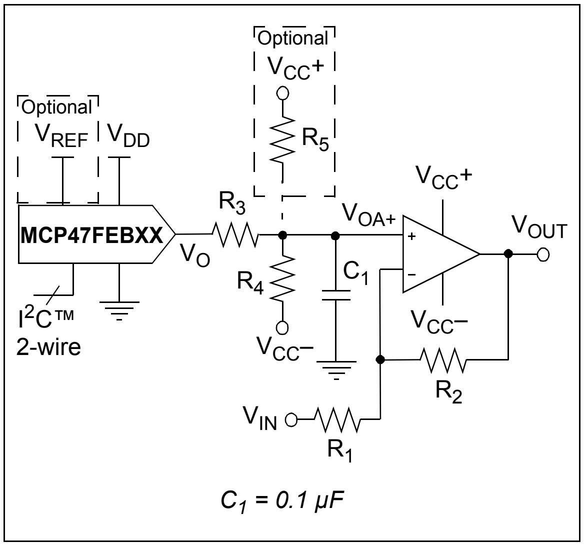


FIGURE 8-6: Bipolar Voltage Source with Selectable Gain and Offset.

EQUATION 8-6: V_{OUT}, V_{OA+}, AND V_O CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4 + V_{CC-} \bullet R_5}{R_3 + R_4}$$

$$V_O = \underbrace{V_{OA+} \bullet (1 + \frac{R_2}{R_1})}_{\text{Offset Adjust}} - \underbrace{V_{IN} \bullet (\frac{R_2}{R_1})}_{\text{Gain Adjust}}$$

EQUATION 8-7: BIPOLAR “WINDOW” DAC USING R_4 AND R_5

$$\text{Thevenin Equivalent} \left\{ V_{45} = \frac{V_{CC+}R_4 + V_{CC-}R_5}{R_4 + R_5} \right.$$

$$V_{IN+} = \frac{V_{OUT}R_{45} + V_{45}R_3}{R_3 + R_{45}}$$

$$R_{45} = \frac{R_4R_5}{R_4 + R_5}$$

$$V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_A\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

8.6 Designing a Double-Precision DAC

Figure 8-7 shows an example design of a single-supply voltage output capable of up to 24-bit resolution. This requires two 12-bit DACs. This design is simply a voltage divider with a buffered output.

As an example, if a similar application to the one developed in **Section 8.5.1 “Bipolar DAC Example”** required a resolution of 1 µV instead of 1 mV, and a range of 0V to 4.1V, then 12-bit resolution would not be adequate.

Step 1: Calculate the resolution needed:
4.1V/1 µV = 4.1×10^6.
Since $2^{22} = 4.2 \times 10^6$, 22-bit resolution is desired. Since DNL = ±1.0 LSb, this design can be attempted with the 12-bit DAC.

Step 2: Since DAC1’s V_{OUT1} has a resolution of 1 mV, its output only needs to be “pulled” 1/1000 to meet the 1 µV target. Dividing V_{OUT0} by 1000 would allow the application to compensate for DAC1’s DNL error.

Step 3: If R_2 is 100Ω, then R_1 needs to be 100 kΩ.

Step 4: The resulting transfer function is shown in the equation of Example 8-8.

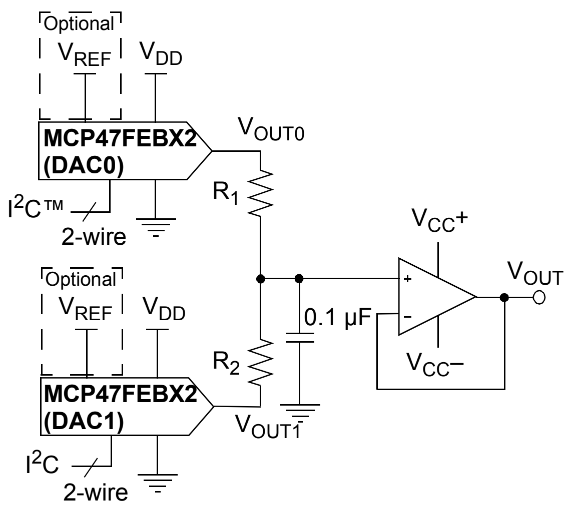


FIGURE 8-7: Simple Double Precision DAC using MCP47FEBX2.

EQUATION 8-8: V_{OUT} CALCULATION

$$V_{OUT} = \frac{V_{OUT0} * R_2 + V_{OUT1} * R_1}{R_1 + R_2}$$

Where:

V_{OUT0} = (V_{REF} ∗ G ∗ DAC0 Register Value)/4096

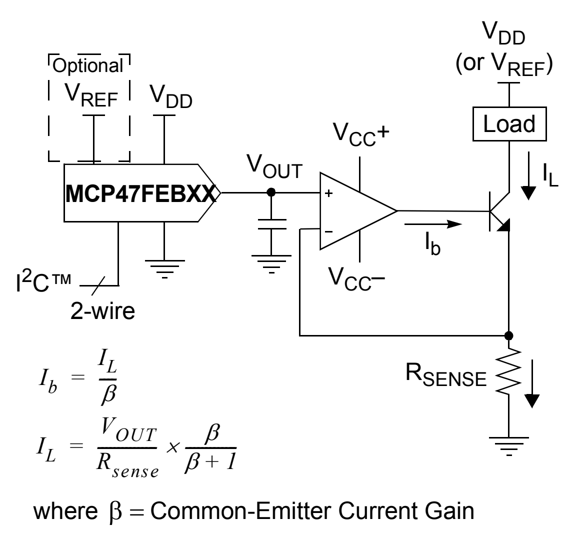
V_{OUT1} = (V_{REF} ∗ G ∗ DAC1 Register Value)/4096

Gx = Selected Op Amp Gain

8.7 Building Programmable Current Source

Figure 8-8 shows an example of building a programmable current source using a voltage follower. The current sensor resistor is used to convert the DAC voltage output into a digitally-selectable current source.

The smaller R_{SENSE} is, the less power dissipated across it. However, this also reduces the resolution that the current can be controlled.



$$I_b = \frac{I_L}{\beta}$$

$$I_L = \frac{V_{OUT}}{R_{sense}} \times \frac{\beta}{\beta + 1}$$

where β = Common-Emitter Current Gain

FIGURE 8-8: Digitally-Controlled Current Source.

8.8 Serial Interface Communication Times

Table 8-1 shows time/frequency of the supported operations of the I^2C serial interface for the different serial interface operational frequencies. This, along with the V_{OUT} output performance (such as slew rate), would be used to determine your application's volatile DAC register update rate.

TABLE 8-1: SERIAL INTERFACE TIMES / FREQUENCIES

Command					# of Bit Clocks (1)	Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)			Comments
Operation	Code		HV	Mode(6)		100 kHz	400 kHz	3.4 MHz(5)	
	C1	C0							
Write Command (Normal and High-Voltage)	0	0	(3)	Single	38	2,632	10,526	89,474	
	0	0	(3)	Continuous	27n + 11	3,559	14,235	120,996	For 10 data words
Read Command (Normal and High-Voltage) (2)	1	1	(3)	Random	48	2,083	8,333	70,833	
	1	1	(3)	Continuous	18n + 11	4,762	19,048	161,905	For 10 data words
	1	1	(3)	Last Address	29	3,448	13,793	117,241	
General Call Reset Command	—	—	(3)	Single	20	5,000	20,000	170,000	**Note 4**
General Call Wake-up Command	—	—	(3)	Single	20	5,000	20,000	170,000	**Note 4**
Enable Configuration Bit (High-Voltage) Command	1	0	Yes	Single	20	5,000	20,000	170,000	
	1	0	Yes	Continuous	9n + 11	9,901	39,604	336,634	For 10 data words
Disable Configuration Bit (High-Voltage) Command	0	1	Yes	Single	20	5,000	20,000	170,000	
	0	1	Yes	Continuous	9n + 11	9,901	39,604	336,634	For 10 data words

Note 1: "n" indicates the number of times the command operation is to be repeated.

2: This command is useful to determine when an EEPROM programming cycle has completed.

3: This command can be either normal voltage or high voltage.

4: Determined by `General Call` command byte after the I^2C General Call address.

5: There is a minimal overhead to enter into 3.4 MHz mode.

6: Nonvolatile Registers can only use the "Single" mode.

8.9 Software I^2C Interface Reset Sequence

> **Note:** This technique is documented in AN1028.

At times, it may become necessary to perform a Software Reset Sequence to ensure the MCP47FEBXX device is in a correct and known I^2C interface state. This technique only resets the I^2C state machine.

This is useful if the MCP47FEBXX device powers-up in an incorrect state (due to excessive bus noise, etc), or if the master device is reset during communication. Figure 8-9 shows the communication sequence to software reset the device.

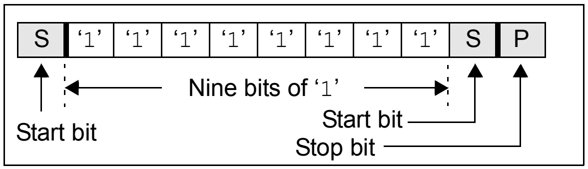


FIGURE 8-9: Software Reset Sequence Format.

The 1st Start bit will cause the device to reset from a state in which it is expecting to receive data from the master device. In this mode, the device is monitoring the data bus in Receive mode and can detect if the Start bit forces an internal Reset.

The nine bits of '`1`' are used to force a Reset of those devices that could not be reset by the previous Start bit. This occurs only if the MCP47FEBXX is driving an A bit on the I^2C bus, or is in Output mode (from a `Read` command) and is driving a data bit of '`0`' onto the I^2C bus. In both of these cases, the previous Start bit could not be generated due to the MCP47FEBXX holding the bus low. By sending out nine '`1`' bits, it is ensured that the device will see an $\overline{A}$ bit (the master device does not drive the I^2C bus low to acknowledge the data sent by the MCP47FEBXX), which also forces the MCP47FEBXX to reset.

The 2nd Start bit is sent to address the rare possibility of an erroneous write. This could occur if the master device was reset while sending a `Write` command to the MCP47FEBXX, AND then as the master device returns to normal operation and issues a Start condition, while the MCP47FEBXX is issuing an acknowledge. In this case, if the 2nd Start bit is not sent (and the Stop bit was sent) the MCP47FEBXX could initiate a write cycle.

> **Note:** The potential for this erroneous write ONLY occurs if the master device is reset while sending a Write command to the MCP47FEBxx.

The Stop bit terminates the current I^2C bus activity. The MCP47FEBXX waits to detect the next Start condition.

This sequence does not affect any other I^2C devices which may be on the bus, as they should disregard this as an invalid command.

8.10 Design Considerations

In the design of a system with the MCP47FEBXX devices, the following considerations should be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

8.10.1 POWER SUPPLY CONSIDERATIONS

The typical application will require a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-10 illustrates an appropriate bypass strategy.

In this example, the recommended bypass capacitor value is 0.1 µF. This capacitor should be placed as close (within 4 mm) to the device power pin (V_{DD}) as possible.

The power source supplying these devices should be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} should reside on the analog plane.

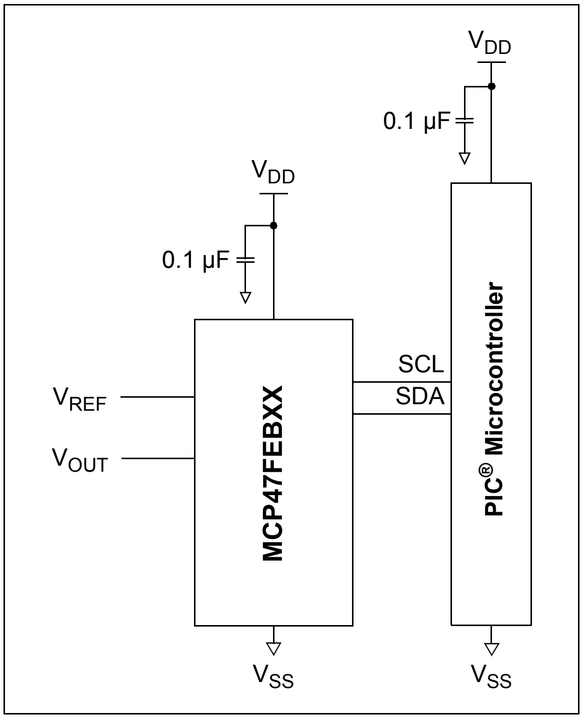


FIGURE 8-10: Typical Microcontroller Connections.

8.10.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

8.10.2.1 Noise

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP47FEBXX's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors should be terminated to the analog ground plane.

Note: Breadboards and wire-wrapped boards are not recommended.

8.10.2.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-2 shows the typical package dimensions and area for the different package options.

TABLE 8-2: PACKAGE FOOTPRINT(1)

Package			Package Footprint		
Pins	Type	Code	Dimensions (mm)		Area (mm^2)
			Length	Width	
8	TSSOP	ST	3.00	4.40	13.20

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.

NOTES:

9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups. These are:

- Development Tools
- Technical Documentation

9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP47FEBXX devices. The currently available tools are shown in Table 9-1.

Figure 9-1 shows how the TSSOP20EV bond-out PCB can be populated to easily evaluate the MCP47FEBXX devices. The 8-pin and 20-pin TSSOP packages have the same pin pitch (0.65 mm BSC) and package width (4.40 mm typ.), and the 8-pin TSSOP package can be placed on the 20-pin TSSOP footprint. Device evaluation can use the PICkit™ Serial Analyzer to control the DAC output registers and state of the configuration, control and status register.

The TSSOP20EV boards may be purchased directly from the Microchip web site at www.microchip.com.

9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-2 shows some of these documents.

TABLE 9-1: DEVELOPMENT TOOLS (Note 1)

Board Name	Part #	Comment
20-Pin TSSOP and SSOP Evaluation Board	TSSOP20EV	Most Flexible option - Recommended Bond-out PCB
14-pin SOIC/TSSOP/DIP Evaluation Board	SOIC14EV	
SOIC-8 Evaluation Board	SOIC8EV	

Note 1: Supports the PICkit™ Serial Analyzer. See the User's Guide for additional information and requirements.

TABLE 9-2: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
AN1326	Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

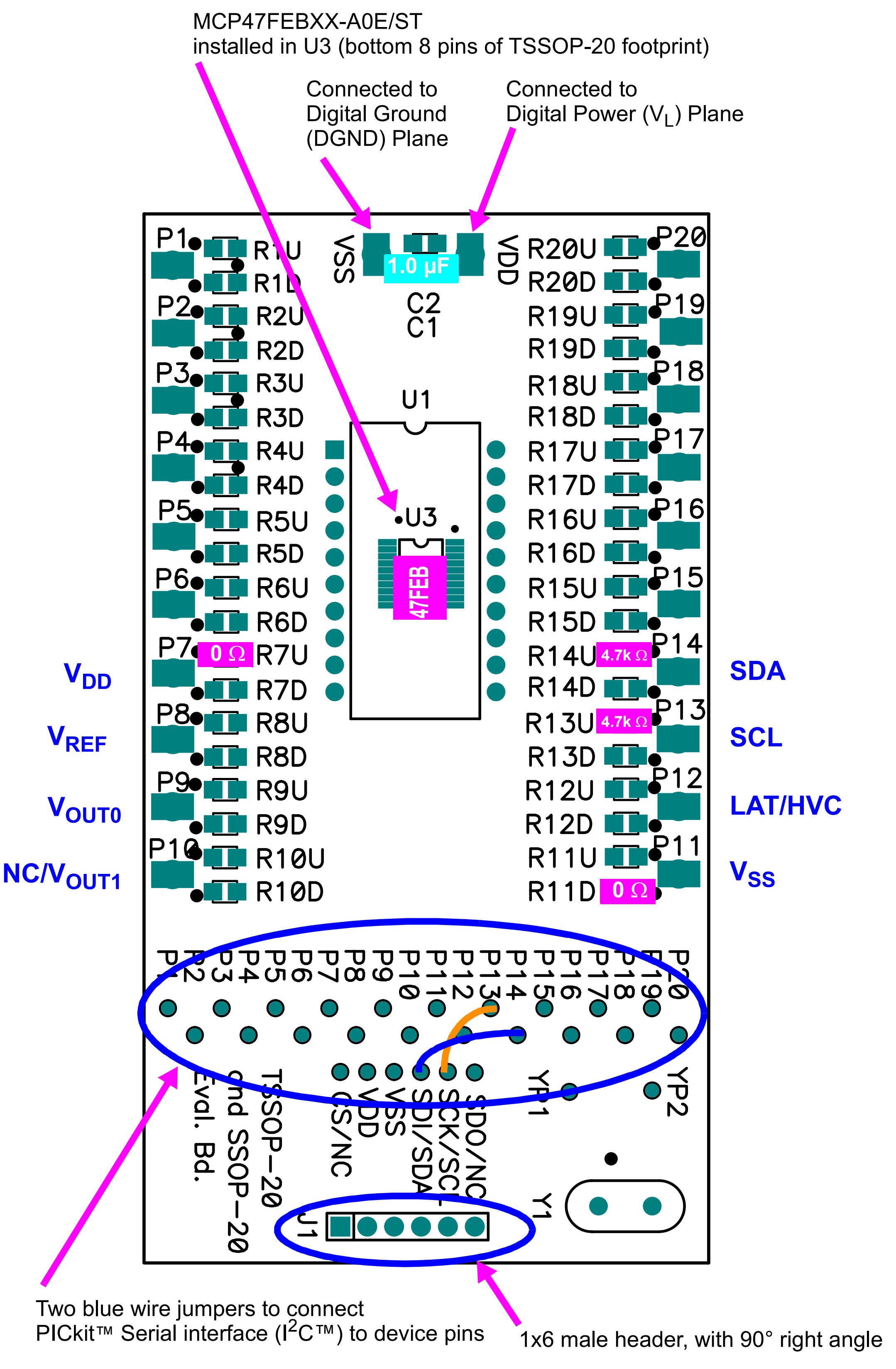
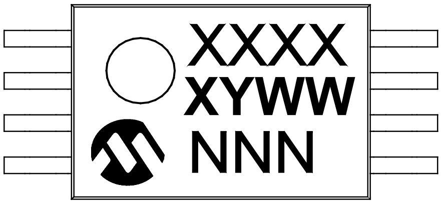


FIGURE 9-1: *MCP47FEBXX Evaluation Board Circuit Using TSSOP20EV.*

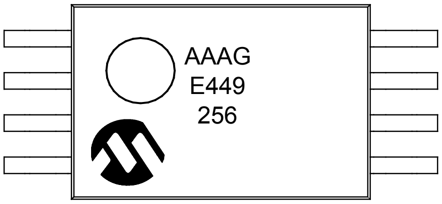
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

8-Lead TSSOP (4.4 mm)



Example



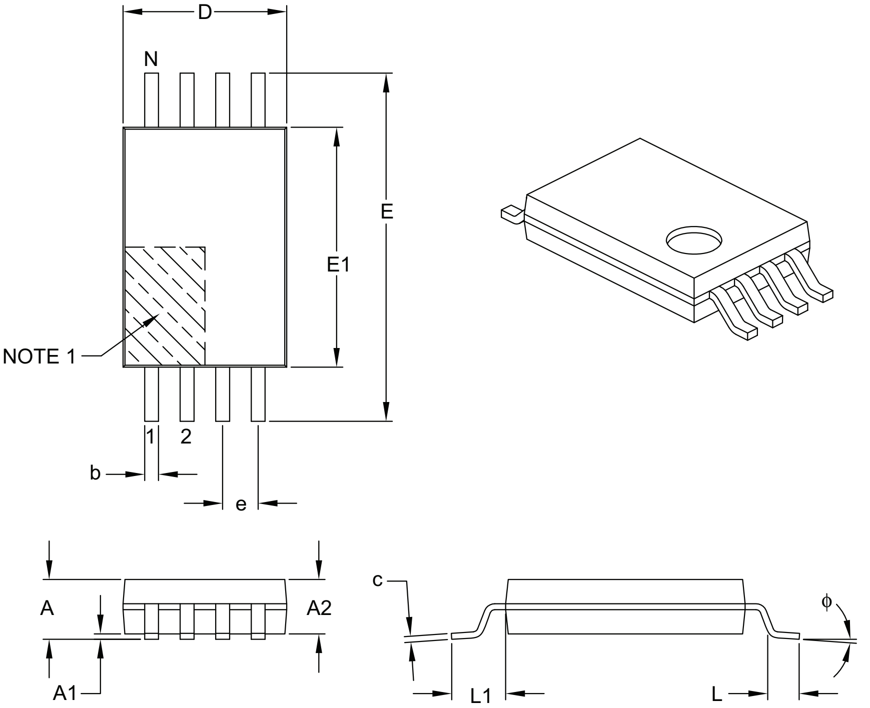
Device Number	Code	Device Number	Code
MCP47FEB01A0-E/ST	AAAG	MCP47FEB12A0-E/ST	AAAL
MCP47FEB01A0T-E/ST	AAAG	MCP47FEB12A0T-E/ST	AAAL
MCP47FEB01A1-E/ST	AAAU	MCP47FEB12A1-E/ST	AABG
MCP47FEB01A1T-E/ST	AAAU	MCP47FEB12A1T-E/ST	AABG
MCP47FEB01A2-E/ST	AAAV	MCP47FEB12A2-E/ST	AABH
MCP47FEB01A2T-E/ST	AAAV	MCP47FEB12A2T-E/ST	AABH
MCP47FEB01A3-E/ST	AAAW	MCP47FEB12A3-E/ST	AABJ
MCP47FEB01A3T-E/ST	AAAW	MCP47FEB12A3T-E/ST	AABJ
MCP47FEB02A0-E/ST	AAAK	MCP47FEB21A0-E/ST	AAAJ
MCP47FEB02A0T-E/ST	AAAK	MCP47FEB21A0T-E/ST	AAAJ
MCP47FEB02A1-E/ST	AABD	MCP47FEB21A1-E/ST	AABA
MCP47FEB02A1T-E/ST	AABD	MCP47FEB21A1T-E/ST	AABA
MCP47FEB02A2-E/ST	AABE	MCP47FEB21A2-E/ST	AABB
MCP47FEB02A2T-E/ST	AABE	MCP47FEB21A2T-E/ST	AABB
MCP47FEB02A3-E/ST	AABF	MCP47FEB21A3-E/ST	AABC
MCP47FEB02A3T-E/ST	AABF	MCP47FEB21A3T-E/ST	AABC
MCP47FEB11A0-E/ST	AAAH	MCP47FEB22A0-E/ST	AAAM
MCP47FEB11A0T-E/ST	AAAH	MCP47FEB22A0T-E/ST	AAAM
MCP47FEB11A1-E/ST	AAAX	MCP47FEB22A1-E/ST	AABK
MCP47FEB11A1T-E/ST	AAAX	MCP47FEB22A1T-E/ST	AABK
MCP47FEB11A2-E/ST	AAAY	MCP47FEB22A2-E/ST	AABL
MCP47FEB11A2T-E/ST	AAAY	MCP47FEB22A2T-E/ST	AABL
MCP47FEB11A3-E/ST	AAAZ	MCP47FEB22A3-E/ST	AABM
MCP47FEB11A3T-E/ST	AAAZ	MCP47FEB22A3T-E/ST	AABM

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

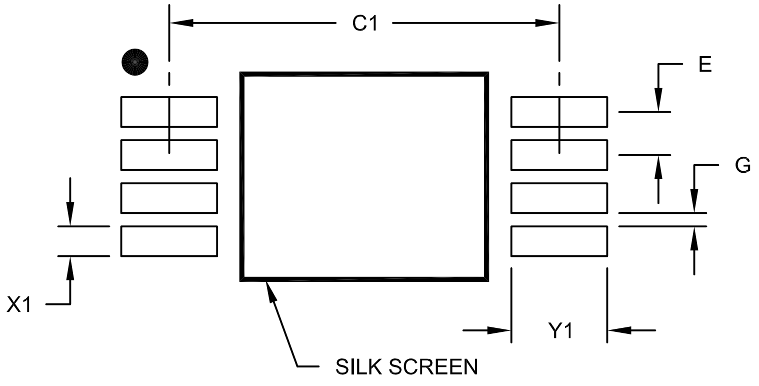
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2015)

- Original release of this document.

APPENDIX B: I²C SERIAL INTERFACE

This I²C interface is a two-wire interface that allows multiple devices to be connected to this two-wire bus. Figure B-1 shows a typical I²C interface connection.

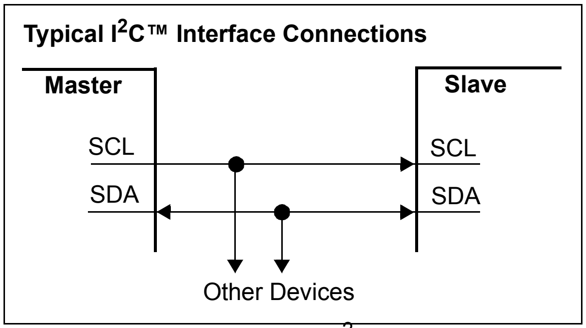


FIGURE B-1: *Typical I²C Interface.*

B.1 Overview

A device that sends data onto the bus is defined as transmitter, and a device receiving data is defined as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions. Devices that do not generate a serial clock work as slave devices. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Communication is initiated by the master (microcontroller), which sends the Start bit followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits and the $R/\overline{W}$ bit.

The I²C interface specifies different communication bit rates. These are referred to as standard, fast or high-speed modes. The MCP47FEBXX supports these three modes. The clock rates (bit rate) of these modes are:

- Standard mode: up to 100 kHz (kbit/s)
- Fast mode: up to 400 kHz (kbit/s)
- High-Speed mode (HS mode): up to 3.4 MHz (Mbit/s)

The I²C protocol supports two addressing modes:

- 7-bit slave addressing
- 10-bit slave addressing (allows more devices on I²C bus)

Only 7-bit slave addressing will be discussed in this section.

The I²C serial protocol allows multiple master devices on the I²C bus. This is referred to as “Multi-Master”. For this, all Master devices must support Multi-Master operation. In this configuration, all master devices monitor their communication. If they detect that they wish to transmit a bit that is a logic high but is detected as a logic low (some other master device driving), they “get off” the bus. That is, they stop their communication and continue to listen to determine if the communication is directed towards them.

The I²C serial protocol only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. For details on the frame content (commands/data), refer to **Section 7.0 “Device Commands”**.

The I²C serial protocol does define some commands called “General Call Addressing”, which allows the master device to communicate to all slave devices on the I²C bus.

Note: Refer to the NXP specification #UM10204, Rev. 03 19 June 2007 document for more details on the I²C specifications.

B.2 Signal Descriptions

The I^2C interface uses two pins (signals). These are:

- SDA (Serial Data)
- SCL (Serial Clock)

B.2.1 SERIAL DATA (SDA)

The Serial Data (SDA) signal is the data signal of the device. The value on this pin is latched on the rising edge of the SCL signal when the signal is an input.

With the exception of the Start (Restart) and Stop conditions, the high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. During the high period of the clock, the SDA pin's value (high or low) must be stable. Changes in the SDA pin's value while the SCL pin is high will be interpreted as a Start or a Stop condition.

B.2.2 SERIAL CLOCK (SCL)

The Serial Clock (SCL) signal is the clock signal of the device. The rising edge of the SCL signal latches the value on the SDA pin.

Depending on the clock rate mode, the interface will display different characteristics.

B.3 I^2C Operation

B.3.1 I^2C BIT STATES AND SEQUENCE

Figure B-8 shows the I^2C transfer sequence, while Figure B-7 shows the bit definitions. The serial clock is generated by the master. The following definitions are used for the bit states:

- Start Bit (S)
- Data Bit
- Acknowledge (A) Bit (driven low) /
  No Acknowledge ($\overline{A}$) bit (not driven low)
- Repeated Start Bit (Sr)
- Stop Bit (P)

B.3.1.1 Start Bit

The Start bit (see Figure B-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is "high".

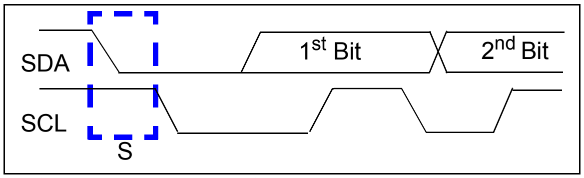


FIGURE B-2: *Start Bit.*

B.3.1.2 Data Bit

The SDA signal may change state while the SCL signal is low. While the SCL signal is high, the SDA signal MUST be stable (see Figure B-3).

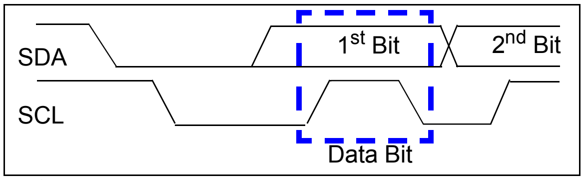


FIGURE B-3: *Data Bit.*

B.3.1.3 Acknowledge (A) Bit

The A bit (see Figure B-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically, the slave device will supply an A response after the Start bit and 8 "data" bits have been received. An A bit has the SDA signal low, while the $\overline{A}$ bit has the SDA signal high.

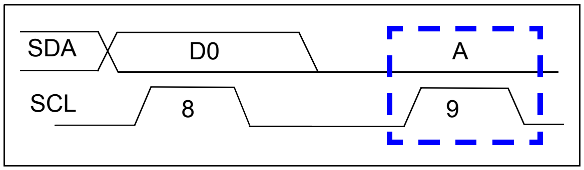


FIGURE B-4: *Acknowledge Waveform.*

Table B-1 shows some of the conditions where the slave device issues the A or Not A ($\overline{A}$).

If an error condition occurs (such as an $\overline{A}$ instead of A), then a Start bit must be issued to reset the command state machine.

TABLE B-1: MCP47FEBXX A/$\overline{A}$ RESPONSES

Event	Acknowledge Bit Response	Comment
General Call	A	
Slave Address valid	A	
Slave Address not valid	$\overline{A}$	
Communication during EEPROM write cycle	A	After device has received address and command, and valid conditions for EEPROM write
Bus Collision	N/A	I^2C™ module Resets, or a "Don't Care" if the collision occurs on the Master's "Start bit"

B.3.1.4 Repeated Start Bit

The Repeated Start bit (see Figure B-5) indicates the current master device wishes to continue communicating with the current slave device without releasing the I^{2}C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the Data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is "high".

> **Note 1:** A bus collision during the Repeated Start condition occurs if:
>
> - SDA is sampled low when SCL goes from low to high.
> - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '`1`'.

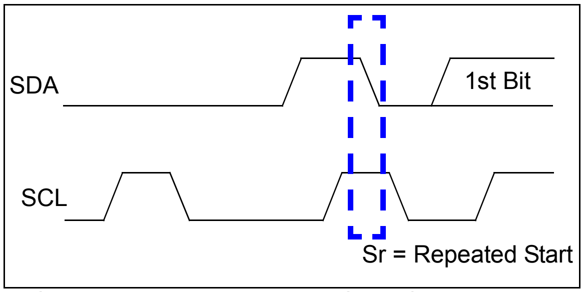


FIGURE B-5: *Repeat Start Condition Waveform.*

B.3.1.5 Stop Bit

The Stop bit (see Figure B-6) Indicates the end of the I^{2}C Data Transfer Sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is "high".

A Stop bit should reset the I^{2}C interface of the slave device.

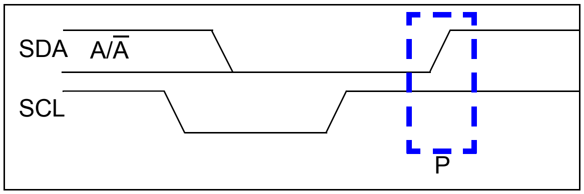


FIGURE B-6: *Stop Condition Receive or Transmit Mode.*

B.3.2 CLOCK STRETCHING

"Clock Stretching" is something that the receiving Device can do, to allow additional time to "respond" to the "data" that has been received.

B.3.3 ABORTING A TRANSMISSION

If any part of the I^{2}C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a Start or Stop condition. This is done so that noisy transmissions (usually an extra Start or Stop condition) are aborted before they corrupt the device.

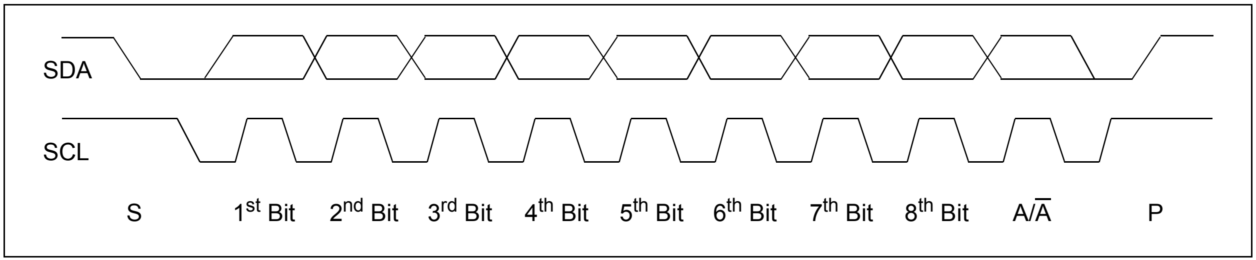


FIGURE B-7: *Typical 8-Bit I^{2}C Waveform Format.*

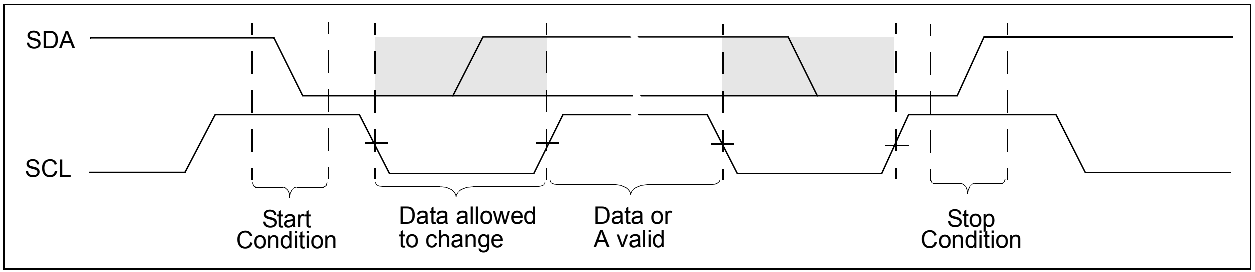


FIGURE B-8: *I^{2}C Data States and Bit Sequence.*

B.3.4 SLOPE CONTROL

As the device transitions from HS mode to FS mode, the slope control parameter will change from the HS specification to the FS specification.

For Fast (FS) and High-Speed (HS) modes, the device has a spike suppression and a Schmitt Trigger at SDA and SCL inputs.

B.3.5 DEVICE ADDRESSING

The I^2C Slave Address control byte is the first byte received following the Start condition from the master device. This byte has 7-bits to specify the Slave Address and the Read/Write control bit.

Figure B-9 shows the I^2C slave address byte format, which contains the seven address bits and a read/write (R/$\overline{\text{W}}$) bit.

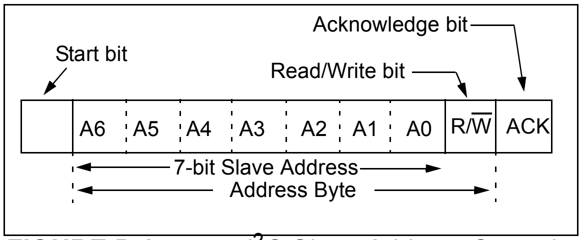


FIGURE B-9: *I^2C Slave Address Control Byte.*

B.3.6 HS MODE

The I^2C specification requires that a High-Speed mode device must be 'activated' to operate in High-Speed (3.4 Mbit/s) mode. This is done by the master sending a special address byte following the Start bit. This byte is referred to as the High-Speed Master Mode Code (HSMMC).

The device can now communicate at up to 3.4 Mbit/s on SDA and SCL lines. The device will switch out of the HS mode on the next Stop condition.

The master code is sent as follows:

1. Start condition (S)
2. High-Speed Master Mode Code (`0000 1XXX`), The `XXX` bits are unique to the High-Speed (HS) mode master.
3. No Acknowledge ($\overline{\text{A}}$)

After switching to the High-Speed mode, the next transferred byte is the I^2C control byte, which specifies the device to communicate with, and any number of data bytes plus acknowledgments. The master device can then either issue a Repeated Start bit to address a different device (at High-Speed) or a Stop bit to return to Fast/Standard bus speed. After the Stop bit, any other master device (in a multi-master system) can arbitrate for the I^2C bus.

See Figure B-10 for illustration of HS mode command sequence.

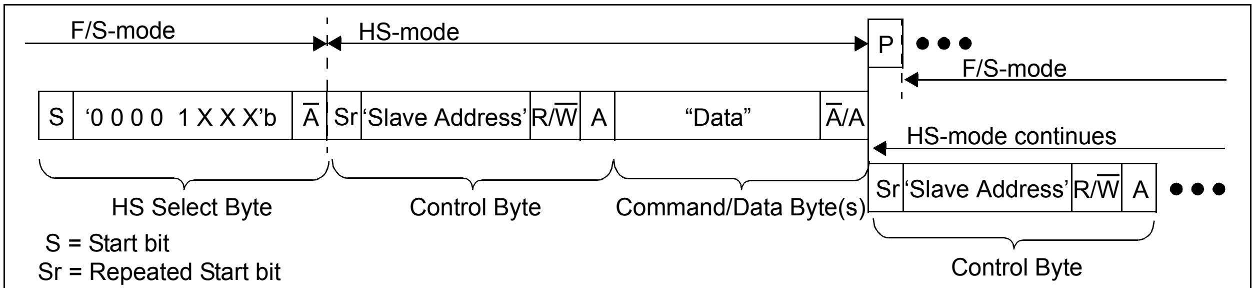
For more information on the HS mode, or other I^2C modes, please refer to the NXP I^2C specification.

B.3.6.1 Slope Control

The slope control on the SDA output is different between the Fast/Standard Speed and the High-Speed clock modes of the interface.

B.3.6.2 Pulse Gobbler

The pulse gobbler on the SCL pin is automatically adjusted to suppress spikes < 10 ns during HS mode.



S = Start bit
Sr = Repeated Start bit
A = Acknowledge bit
$\overline{\text{A}}$ = Not Acknowledge bit
R/$\overline{\text{W}}$ = Read/Write bit
P = Stop bit (Stop condition terminates HS Mode)

FIGURE B-10: *HS Mode Sequence.*

B.3.7 GENERAL CALL

The General Call is a method that the “Master” device can communicate with all other “Slave” devices. In a Multi-Master application, the other Master devices are operating in Slave mode. The General Call address has two documented formats. These are shown in Figure B-11.

The I^2C specification documents three 7-bit command bytes.

The I^2C specification does not allow ‘`00000000`’ (00h) in the second byte. Also ‘`00000100`’ and ‘`00000110`’ functionality is defined by the specification. Lastly a data byte with a ‘`1`’ in the LSb indicates a “Hardware General Call”.

For details on the operation of the MCP47FEBXX’s `General Call` commands, see **Section 7.3 “General Call Commands”**.

> **Note:** Only one `General Call` command per issue of the General Call control byte. Any additional `General Call` commands are ignored and Not Acknowledged.

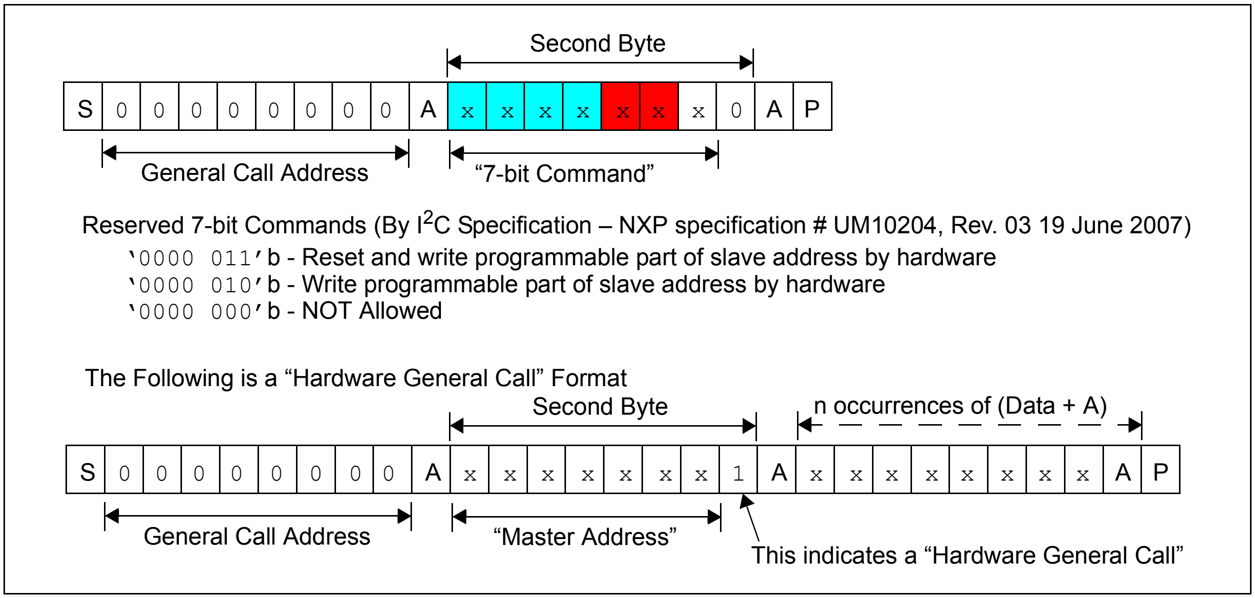


FIGURE B-11: General Call Formats.

APPENDIX C: TERMINOLOGY

C.1 Resolution

The resolution is the number of DAC output states that divide the full-scale range. For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

Note: When there are 2^N resistors in the resistor ladder and 2^N tap points, the full scale DAC register code is resistor element (1 LSb) from the source reference voltage (V_{DD} or V_{REF}).

C.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device (Equation C-1). The range may be V_{DD} (or V_{REF}) to V_{SS} (ideal), the DAC register codes across the linear range of the output driver (Measured 1), or full-scale to zero-scale (Measured 2).

EQUATION C-1: LSb VOLTAGE CALCULATION

Ideal

$$V_{LSb(IDEAL)} = \frac{V_{DD}}{2^N} \quad or \quad \frac{V_{REF}}{2^N}$$

Measured 1

$$V_{LSb(Measured)} = \frac{V_{OUT(@4000)} - V_{OUT(@100)}}{(4000 - 100)}$$

Measured 2

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

2^N = 4096 (MCP47FEB2x)
= 1024 (MCP47FEB1x)
= 256 (MCP47FEB0x)

C.3 Monotonic Operation

Monotonic operation means that the device's output voltage (V_{OUT}) increases with every 1 code step (LSb) increment (from V_{SS} to the DAC's reference voltage (V_{DD} or V_{REF})).

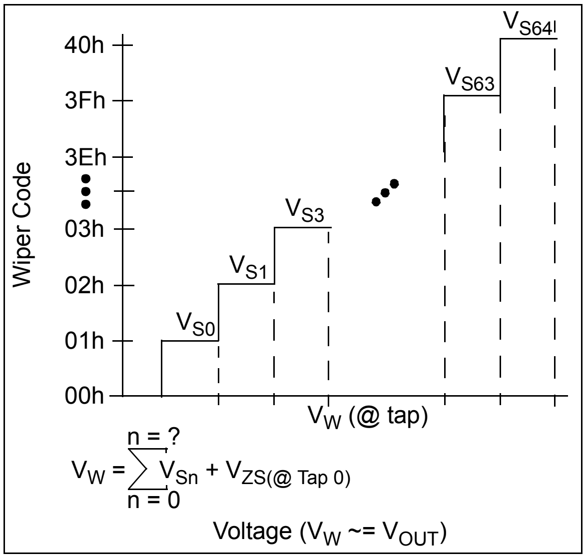


FIGURE C-1: V_W (V_{OUT}).

C.4 Full-Scale Error (E_{FS})

The Full-Scale Error (see Figure C-3) is the error on the V_{OUT} pin relative to the expected V_{OUT} voltage (theoretical) for the maximum device DAC register code (code FFFh for 12-bit, code 3FFh for 10-bit, and code FFh for 8-bit) (see Equation C-2). The error is dependent on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{SS}) greater than specified, the full-scale error will be greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION C-2: FULL SCALE ERROR

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} is expressed in LSb

$V_{OUT(@FS)}$ is the V_{OUT} voltage when the DAC register code is at Full scale.

$V_{IDEAL(@FS)}$ is the ideal output voltage when the DAC register code is at Full scale.

$V_{LSb(IDEAL)}$ is the theoretical voltage step size.

C.5 Zero-Scale Error (E_{ZS})

The Zero-Scale Error (see Figure C-2) is the difference between the ideal and measured V_{OUT} voltage with the DAC register code equal to 000h (Equation C-3). The error is dependent on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{DD}) greater than specified, the zero scale error will be greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION C-3: ZERO SCALE ERROR

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} is expressed in LSb

$V_{OUT(@ZS)}$ is the V_{OUT} voltage when the DAC register code is at Zero-scale.

$V_{LSb(IDEAL)}$ is the theoretical voltage step size.

C.6 Total Unadjusted Error (E_T)

The Total Unadjusted Error (E_T) is the difference between the ideal and measured V_{OUT} voltage. Typically, calibration of the output voltage is implemented to improve system performance.

The error in bits is determined by the theortical voltage step size to give an error in LSb.

Equation C-4 shows the Total Unadjusted Error calculation

EQUATION C-4: TOTAL UNADJUSTED ERROR CALCULATION

$$E_T = \frac{(V_{OUT\_Actual(@code)} - V_{OUT\_Ideal(@Code)})}{V_{LSb(Ideal)}}$$

Where:

E_T is expressed in LSb.

$V_{OUT\_Actual(@code)}$ = The measured DAC output voltage at the specified code.

$V_{OUT\_Ideal(@code)}$ = The calculated DAC output voltage at the specified code. (code * $V_{LSb(Ideal)}$)

$V_{LSb(Ideal)}$ = V_{REF}/# Steps
12-bit = V_{REF}/4096
10-bit = V_{REF}/1024
8-bit = V_{REF}/256

C.7 Offset Error (E_{OS})

The offset error is the delta voltage of the V_{OUT} voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP47FEBXX we specify code 100 (decimal). Offset error does not include gain error. Figure C-2 illustrates this.

This error is expressed in mV. Offset error can be negative or positive. The offset error can be calibrated by software in application circuits.

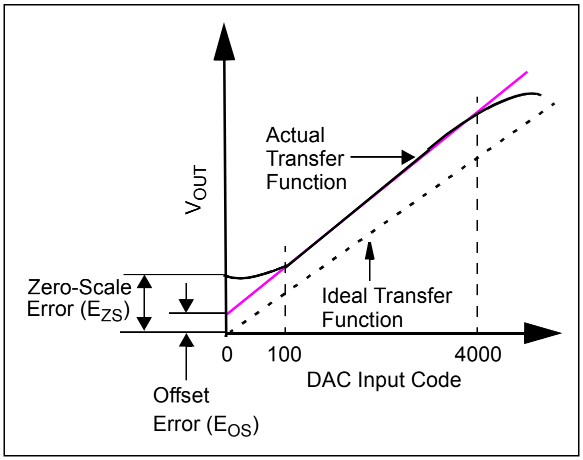


FIGURE C-2: Offset Error (Zero Gain Error).

C.8 Offset Error Drift (E_{OSD})

The Offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/°C or µV/°C.

C.9 Gain Error (E_G)

Gain error is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (ex code 100 and code 4000) (see Figure C-3). The Gain error calculation nullifies the device's offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as percent of full-scale range (% of FSR) or in LSb. FSR is the ideal Full Scale voltage of the DAC (see Equation C-5).

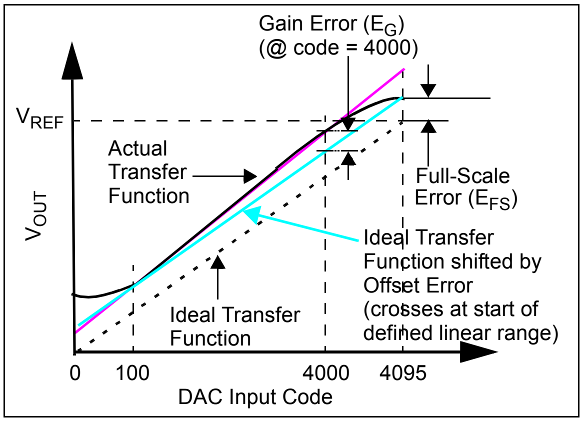


FIGURE C-3: Gain Error and Full-Scale Error Example.

EQUATION C-5: EXAMPLE GAIN ERROR

$$E_G = \frac{(V_{OUT(@4000)} - V_{OS} - V_{OUT\_Ideal(@4000)})}{V_{Full\text{-}Scale\ Range}} * 100$$

Where:

E_G is expressed in %of Full-Scale Range (FSR)

$V_{OUT(@4000)}$ = The measured DAC output voltage at the specified code.

$V_{OUT\_Ideal(@4000)}$ = The calculated DAC output voltage at the specified code. (4000 * $V_{LSb(Ideal)}$)

V_{OS} = Measured offset voltage.

$V_{Full\ Scale\ Range}$ = Expected Full-Scale output value (such as the V_{REF} voltage).

C.10 Gain-Error Drift (E_{GD})

The Gain-error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C (of full scale range).

C.11 Integral Nonlinearity (INL)

The Integral Nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line) passing through the defined end-points of the DAC transfer function (after offset and gain errors have been removed).

In the MCP47FEBXX, INL is calculated using the defined end points, DAC code 100 and code 4000. INL can be expressed as a percentage of Full-Scale Range (FSR) or in LSb. INL is also called relative accuracy. Equation C-6 shows how to calculate the INL error in LSb and Figure C-4 shows an example of INL accuracy.

Positive INL means higher V_{OUT} voltage than ideal. Negative INL means lower V_{OUT} voltage than ideal.

EQUATION C-6: INL ERROR

$$E_{INL} = \frac{(V_{OUT} - V_{Calc\_Ideal})}{V_{LSb(Measured)}}$$

Where:

INL is expressed in LSb.

V_{Calc_Ideal} = Code * $V_{LSb(Measured)}$ + V_{OS}

$V_{OUT(Code = n)}$ = The measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4000)} - V_{OUT(100)})/3900$

V_{OS} = Measured offset voltage.

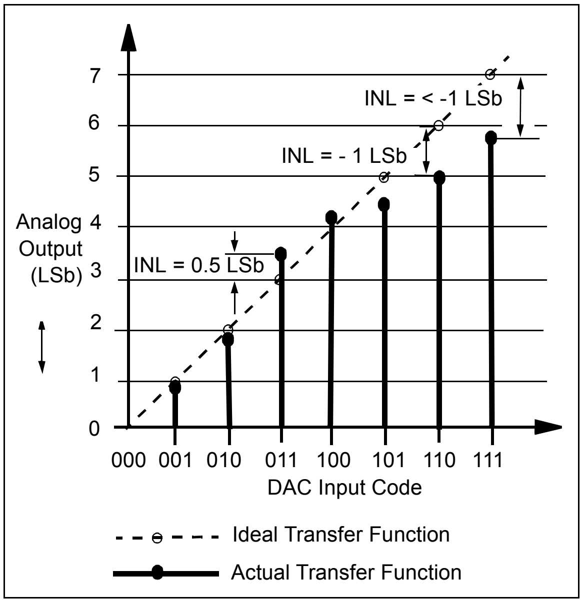


FIGURE C-4: *INL Accuracy.*

C.12 Differential Nonlinearity (DNL)

The Differential Nonlinearity (DNL) error (see Figure C-5) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC guarantees monotonic output and no missing codes. Equation C-7 shows how to calculate the DNL error between any two adjacent codes in LSb.

EQUATION C-7: DNL ERROR

$$E_{DNL} = \frac{(V_{OUT(code = n+1)} - V_{OUT(code = n)})}{V_{LSb(Measured)}} - 1$$

Where:

DNL is expressed in LSb.

$V_{OUT(Code = n)}$ = The measured DAC output voltage with a given DAC register code.

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4000)} - V_{OUT(100)})/3900$

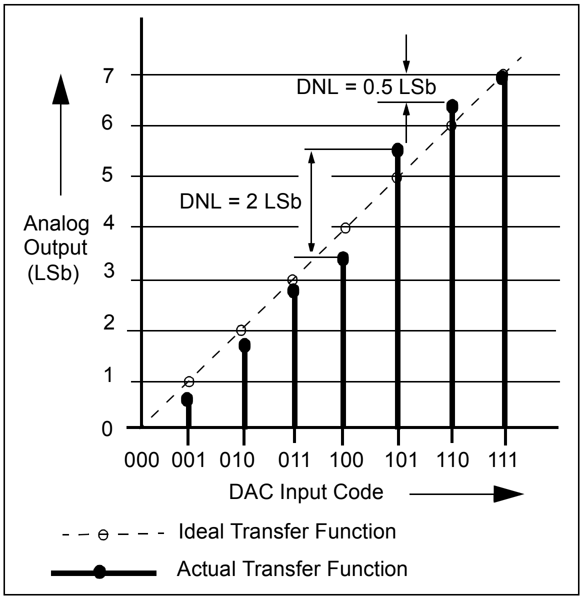


FIGURE C-5: *DNL Accuracy.*

C.13 Settling Time

The Settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of code transition, to when the V_{OUT} voltage is within the specified accuracy.

In the MCP47FEBXX, the settling time is a measure of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC Register changes from 1/4 to 3/4 of the full-scale range (12-bit device: 400h to C00h).

C.14 Major-Code Transition Glitch

Major-code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-Sec, and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: `011...111` to `100...000`, or `100... 000` to `011 ... 111`).

C.15 Digital Feed-through

The digital feed-through is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec and is measured with a full-scale change (Example: all `0`s to all `1`s and vice versa) on the digital input pins. The digital feed-through is measured when the DAC is not being written to the output register.

C.16 -3 dB Bandwidth

This is the frequency of the signal at the V_{REF} pin that causes the voltage at the V_{OUT} pin to fall -3 dB value from a static value on the V_{REF} pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

C.17 Power-Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in V_{OUT} to a change in V_{DD} for mid-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied from 5.5V to 2.7V as a step (V_{REF} voltage held constant), and expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the V_{DD} voltage.

EQUATION C-8: PSS CALCULATION

$$PSS = \frac{(\ V_{OUT(@5.5V)} - V_{OUT(@2.7V)}\ )\ /\ V_{OUT(@5.5V)}\ )}{(5.5V - 2.7V)\ /\ 5.5V}$$

Where:

PSS is expressed in % / %.

$V_{OUT(@5.5V)}$ = The measured DAC output voltage with V_{DD} = 5.5V.

$V_{OUT(@2.7V)}$ = The measured DAC output voltage with V_{DD} = 2.7V.

C.18 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied +/- 10% (V_{REF} voltage held constant), and expressed in dB or µV/V.

C.19 V_{OUT} Temperature Coefficient

The V_{OUT} temperature coefficient quantifies the error in the resistor ladder’s resistance ratio (DAC Register code value) and Output Buffer due to temperature drift.

C.20 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (Nominal output voltage V_{OUT}) due to temperature drift. For a DAC this error is typically not an issue due to the ratiometric aspect of the output.

C.21 Noise Spectral Density

Noise Spectral Density is a measurement of the device’s internally generated random noise, and is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to the mid-scale value and measuring the noise at the V_{OUT} pin. It is measured in nV/√Hz.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	**XX**	**X**	**— X**	**/XX**
Device	**Address Options**	**Tape and Reel**	**Temperature Range**	**Package**

Device:

MCP47FEB01: Single-Channel 8-Bit NV DAC with External + Internal References
MCP47FEB02: Dual-Channel 8-Bit NV DAC with External + Internal References
MCP47FEB11: Single-Channel 10-Bit NV DAC with External + Internal References
MCP47FEB12: Dual-Channel 10-Bit NV DAC with External + Internal References
MCP47FEB21: Single-Channel 12-Bit NV DAC with External + Internal References
MCP47FEB22: Dual-Channel 12-Bit NV DAC with External + Internal References

Address Options:

A0 = “`1100000`” I^2C Address.
A1 = “`1100001`” I^2C Address.
A2 = “`1100010`” I^2C Address.
A3 = “`1100011`” I^2C Address.

Tape and Reel:

T = Tape and Reel
Blank = Tube

Temperature Range:

E = -40°C to +125°C

Package:

ST = Plastic Thin Shrink Small Outline Package (TSSOP), 8-lead

Examples:

a) MCP47FEB01A0T-E/ST: 8-bit V_{OUT} resolution, I^2C Address “`1100000`”, Tape and Reel, Extended Temp., 8LD TSSOP pkg.
b) MCP47FEB01A3T-E/ST: 8-bit V_{OUT} resolution, I^2C Address “`1100011`”, Tape and Reel, Extended Temp., 8LD TSSOP pkg.

a) MCP47FEB11A0-E/ST: 10-bit V_{OUT} resolution, I^2C Address “`1100000`”, Tube, Extended Temp., 8LD TSSOP pkg.
b) MCP47FEB11A3T-E/ST: 10-bit V_{OUT} resolution, I^2C Address “`1100011`”, Tape and Reel, Extended Temp., 8LD TSSOP pkg.

a) MCP47FEB21A0T-E/ST: 12-bit V_{OUT} resolution, I^2C Address “`1100000`”, Tape and Reel, Extended Temp., 8LD TSSOP pkg.
b) MCP47FEB21A3T-E/ST: 12-bit V_{OUT} resolution, I^2C Address “`1100011`”, Tape and Reel, Extended Temp., 8LD TSSOP pkg.

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