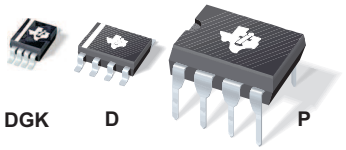


Low-Power RS-485 Transceivers, Available in a Small MSOP-8 Package

FEATURES

- **Available in a Small MSOP-8 Package**
- **Meets or Exceeds the Requirements of the TIA/EIA−485A Standard**
- **Low Quiescent Power**
  - **0.3 mA Active Mode**
  - **1 nA Shutdown Mode**
- **1/8 Unit Load—Up to 256 Nodes on a Bus**
- **Bus-Pin ESD Protection Up to 15 kV**
- **Industry-Standard SN75176 Footprint**
- **Failsafe Receiver (Bus Open, Bus Shorted, Bus Idle)**
- **Glitch–Free Power–Up/Down Bus Inputs and Outputs**

APPLICATIONS

- **Energy Meter Networks**
- **Motor Control**
- **Power Inverters**
- **Industrial Automation**
- **Building Automation Networks**
- **Battery-Powered Applications**
- **Telecommunications Equipment**

DESCRIPTION

These devices are half-duplex transceivers designed for RS–485 data bus networks. Powered by a 5–V supply, they are fully compliant with TIA/EIA-485A standard. With controlled transition times, these devices are suitable for transmitting data over long twisted-pair cables. SN65HVD3082E and SN75HVD3082E devices are optimized for signaling rates up to 200 kbps. SN65HVD3085E is suitable for data transmission up to 1 Mbps, whereas SN65HVD3088E is suitable for applications requiring signaling rates up to 20 Mbps. These devices are designed to operate with very low supply current, typically 0.3 mA, exclusive of the load. When in the inactive shutdown mode, the supply current drops to a few nanoamps, making these devices ideal for power-sensitive applications.

The wide common-mode range and high ESD protection levels of these devices make them suitable for demanding applications such as energy meter networks, electrical inverters, status/command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. These devices match the industry-standard footprint of SN75176. Power-on reset circuits keep the outputs in a high impedance state until the supply voltage has stabilized. A thermal shutdown function protects the device from damage due to system fault conditions. The SN75HVD3082E is characterized for operation from 0°C to 70°C and SN65HVD308xE are characterized for operation from –40°C to 85°C air temperature.

ORDERING INFORMATION:

T_A	SIGNALING RATE (Mbps)	PACKAGE TYPE		
		P	D(1)	DGK(2)
0°C to 70°C	0.2	SN75HVD3082EP Marked as 75HVD3082	SN75HVD3082ED Marked as VN3082	SN75HVD3082EDGK Marked as NWM
–40°C to 85°C	0.2	SN65HVD3082EP Marked as 65HVD3082	SN65HVD3082ED Marked as VP3082	SN65HVD3082EDGK Marked as NWN
	1		SN65HVD3085ED Marked as VP3085	SN65HVD3085EDGK Marked as NWK
	20		SN65HVD3088ED Marked as VP3088	SN65HVD3088EDGK Marked as NWH

(1) The D package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD3082EDR).
(2) The DGK package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD3082EDGKR).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

	UNIT
Supply voltage range, V_{CC}	–0.5 V to 7 V
Voltage range at A or B	–9 V to 14 V
Voltage range at any logic pin	–0.3 V to V_{CC} + 0.3 V
Receiver output current	–24 mA to 24 mA
Voltage input, transient pulse, A and B, through 100 Ω. See Figure 13	–50 to 50 V
Junction Temperature, T_J	170°C
Continuous total power dissipation	See the Package Dissipation Table

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE	JEDEC BOARD MODEL	T_A < 25°C POWER RATING	DERATING FACTOR (1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	Low k(2)	507 mW	4.82 mW/°C	289 mW	217 mW
	High k(3)	824 mW	7.85 mW/°C	471 mW	353 mW
P	Low k(2)	686 mW	6.53 mW/°C	392 mW	294 mW
DGK	Low k(2)	394 mW	3.76 mW/°C	255 mW	169 mW
	High k(3)	583 mW	5.55 mW/°C	333 mW	250 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the low-k thermal metric definitions of EIA/JESD51-3
(3) In accordance with the high-k thermal metric definitions of EIA/JESD51-7

RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range unless otherwise noted

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) , V_I		–7		12	V
High-level input voltage (D, DE, or $\overline{RE}$ inputs), V_{IH}		2		V_{CC}	V
Low-level input voltage (D, DE, or $\overline{RE}$ inputs), V_{IL}		0		0.8	V
Differential input voltage, V_{ID}		–12		12	V
Output current, I_O	Driver	–60		60	mA
	Receiver	–8		8	
Differential load resistance, R_L		54	60		Ω
Signaling rate, $1/t_{UI}$	SN65HVD3082E, SN75HVD3082E			0.2	Mbps
	SN65HVD3085E			1	
	SN65HVD3088E			20	
Operating free–air temperature, T_A	SN65HVD3082E, SN65HVD3085E, SN65HVD3088E	–40		85	°C
	SN75HVD3082E	0		70	
Junction temperature, T_J (2)		–40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) See thermal characteristics table for information on maintenance of this specification for the DGK package.

SUPPLY CURRENT

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open, DE at V_{CC}, $\overline{RE}$ at 0 V, No load		425	900	µA
	Driver enabled, receiver disabled	D at V_{CC} or open, DE at V_{CC}, $\overline{RE}$ at V_{CC}, No load		330	600	µA
	Receiver enabled, driver disabled	D at V_{CC} or open, DE at 0 V, $\overline{RE}$ at 0 V, No load		300	600	µA
	Driver and receiver disabled	D at V_{CC} or open, DE at 0 V, $\overline{RE}$ at V_{CC}		0.001	2	µA

(1) All typical values are at 25°C and with a 5–V supply.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Human body model	Bus terminals and GND		±15		kV
Human body model(2)	All pins		±4		kV
Charged-device-model(3)	All pins		±1		kV
Electrical Fast Transient/Burst(4)	A, B, and GND		±4		kV

(1) All typical values at 25°C.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114–A and IEC 60749–26.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.
(4) Tested in accordance with IEC 61000–4–4.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	I_O = 0, No Load	3	4.3		V
		R_L = 54 Ω, See Figure 1	1.5	2.3		
		R_L = 100 Ω	2			
		V_{TEST} = –7 V to 12 V, See Figure 2	1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	See Figure 1 and Figure 2	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		–0.1	0	0.1	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 3		500		mV
I_{OZ}	High-impedance output current	See receiver input currents				
I_I	Input current	D, DE	–100		100	µA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V, See Figure 7	–250		250	mA

(1) All typical values are at 25°C and with a 5–V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 4	HVD3082E		700	1300	ns
			HVD3085E		150	500	
			HVD3088E		12	20	
t_r t_f	Differential output signal rise time Differential output signal fall time	R_L = 54 Ω, C_L = 50 pF, See Figure 4	HVD3082E	500	900	1500	ns
			HVD3085E		200	300	
			HVD3088E		7	15	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	R_L = 54 Ω, C_L = 50 pF, See Figure 4	HVD3082E		20	200	ns
			HVD3085E		5	50	
			HVD3088E		1.4	2	
t_{PZH} t_{PZL}	Propagation delay time, high-impedance-to-high-level output Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 5 and Figure 6	HVD3082E		2500	7000	ns
			HVD3085E		1000	2500	
			HVD3088E		13	30	
t_{PHZ} t_{PLZ}	Propagation delay time, high-level-to-high-impedance output Propagation delay time, low-level-to-high-impedance output	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 5 and Figure 6	HVD3082E		80	200	ns
			HVD3085E		60	100	
			HVD3088E		12	30	
$t_{PZH(SHDN)}$ $t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-high-level output Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at V_{CC}, See Figure 5	HVD3082E		3500	7000	ns
			HVD3085E		2500	4500	
			HVD3088E		1600	2600	

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage	I_O = –8 mA		–85	–10	mV
V_{IT-}	Negative-going differential input threshold voltage	I_O = 8 mA	–200	–115		mV
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See Figure 8	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_O = 8 mA, See Figure 8		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 or V_{CC}, $\overline{RE}$ = V_{CC}	–1		1	µA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V		0.04	0.1	mA
		V_{IH} = 12 V, V_{CC} = 0 V		0.06	0.125	
		V_{IH} = –7 V, V_{CC} = 5 V	–0.1	–0.04		
		V_{IH} = –7 V, V_{CC} = 0 V	–0.05	–0.03		
I_{IH}	High-level input current, ($\overline{RE}$)	V_{IH} = 2 V	–60	–30		µA
I_{IL}	Low-level Input current, ($\overline{RE}$)	V_{IL} = 0.8 V	–60	–30		µA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 9	HVD3082E HVD3085E		75	200	ns
			HVD3086E			100	
t_{PHL}	Propagation delay time, high-to-low-level output		HVD3082E HVD3085E		79	200	ns
			HVD3088E			100	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)		HVD3082E HVD3085E		4	30	ns
			HVD3088E			10	
t_r	Output signal rise time	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 9			1.5	3	ns
t_f	Output signal fall time				1.8	3	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V See Figure 10 and Figure 11	HVD3082E HVD3085E		5	50	ns
			HVD3088E			30	
t_{PZL}	Output enable time to low level		HVD3082E HVD3085E		10	50	ns
			HVD3088E			30	
t_{PHZ}	Output enable time from high level		HVD3082E HVD3085E		5	50	ns
			HVD3088E			30	
t_{PLZ}	Output disable time from low level		HVD3082E HVD3085E		8	50	ns
			HVD3088E			30	
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, See Figure 12			1600	3500	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output				1700	3500	ns

PARAMETER MEASUREMENT INFORMATION

NOTE: Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

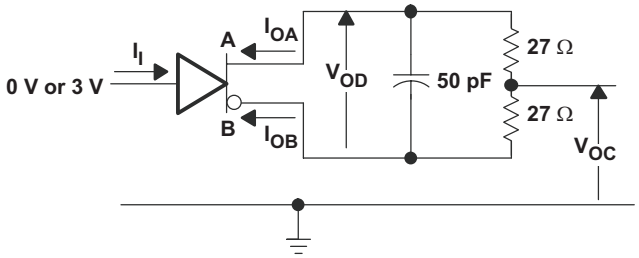


Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

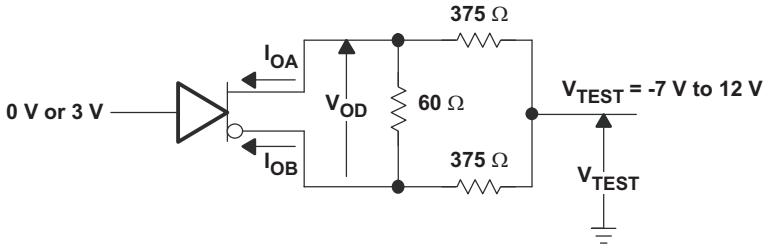


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

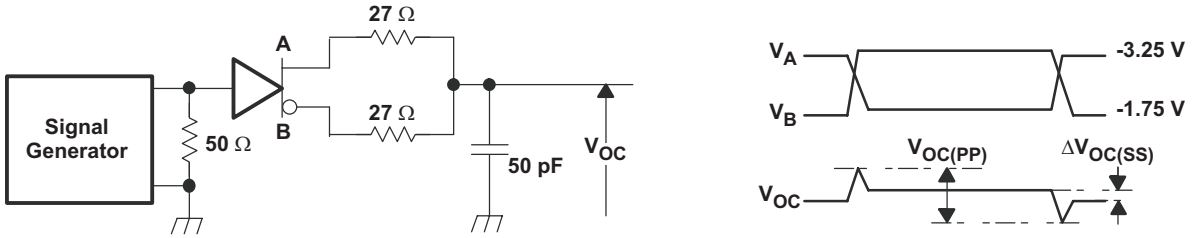


Figure 3. Driver V_{OC} Test Circuit and Waveforms

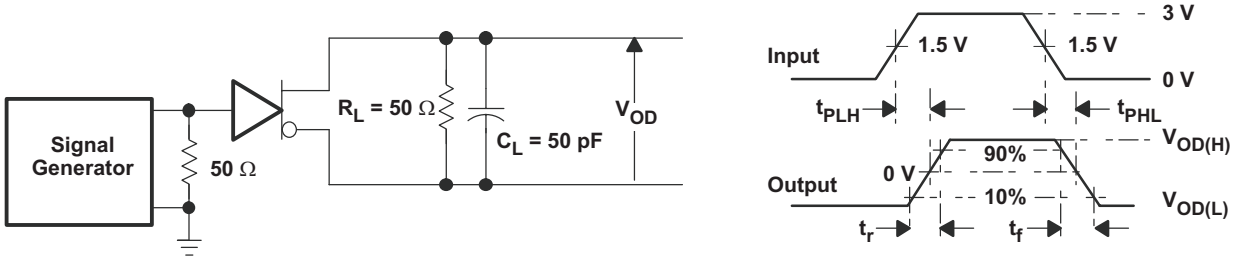


Figure 4. Driver Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

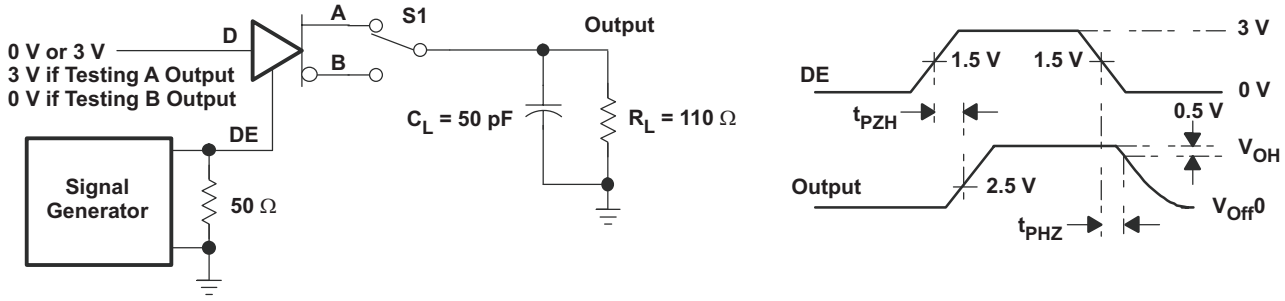


Figure 5. Driver Enable/Disable Test Circuit and Waveforms, High Output

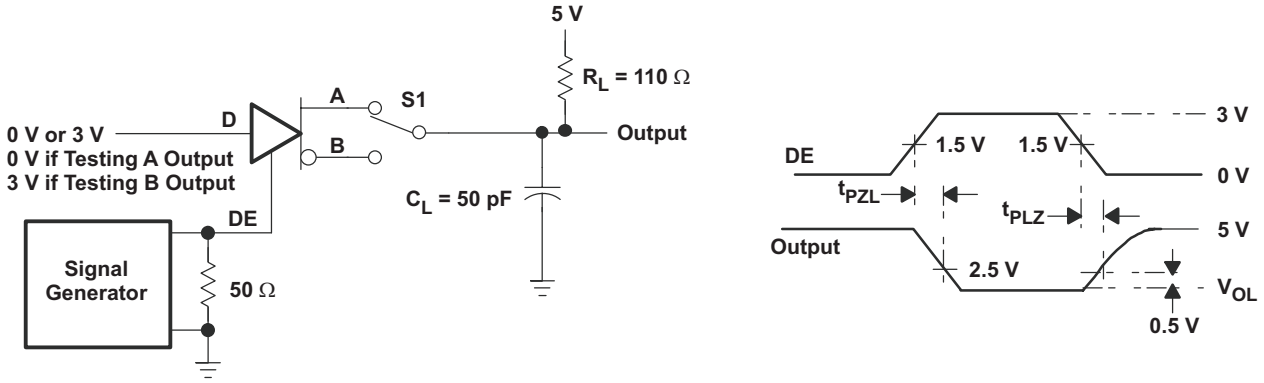


Figure 6. Driver Enable/Disable Test Circuit and Waveforms, Low Output

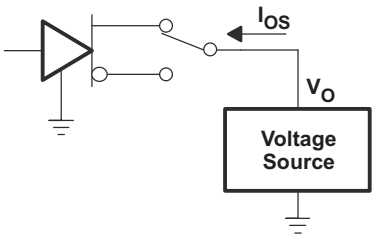


Figure 7. Driver Short-Circuit

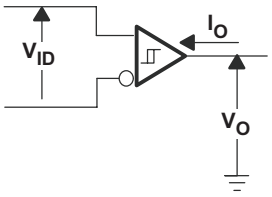
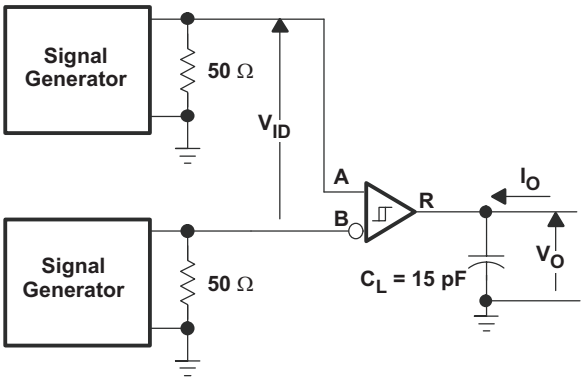


Figure 8. Receiver Switching Test Circuit and Waveforms



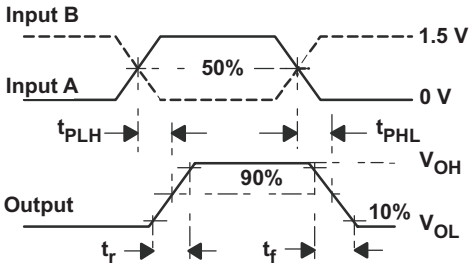


Figure 9. Receiver Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

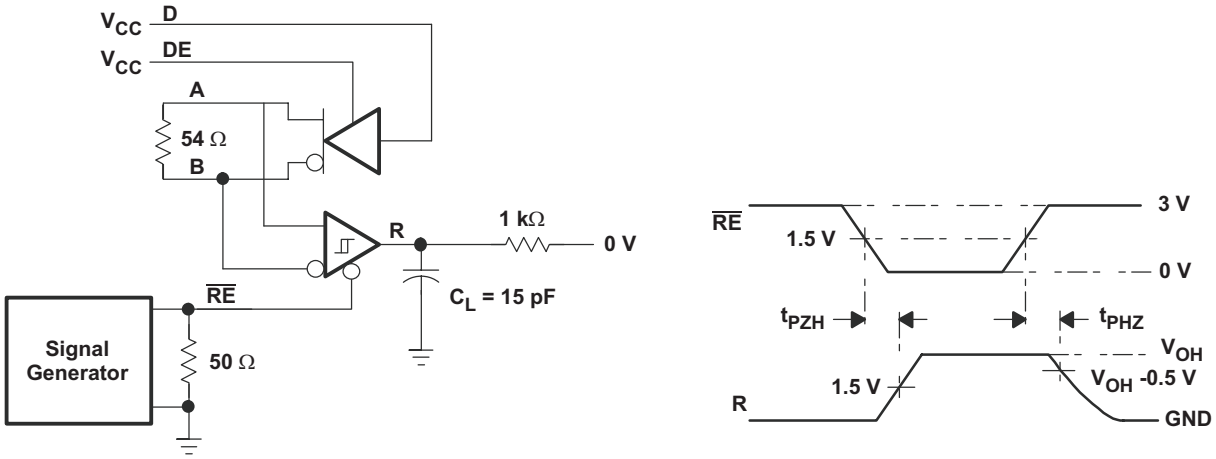


Figure 10. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

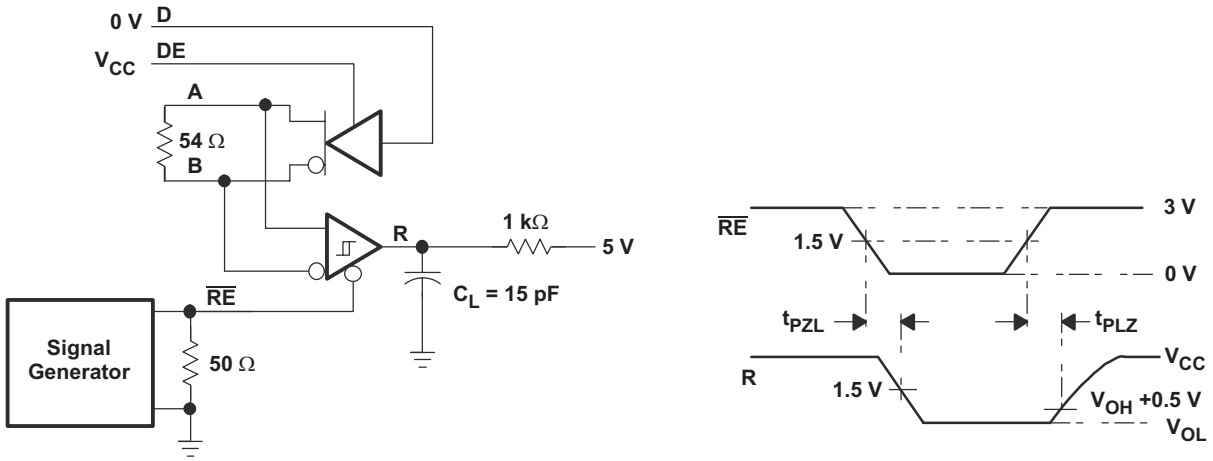


Figure 11. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

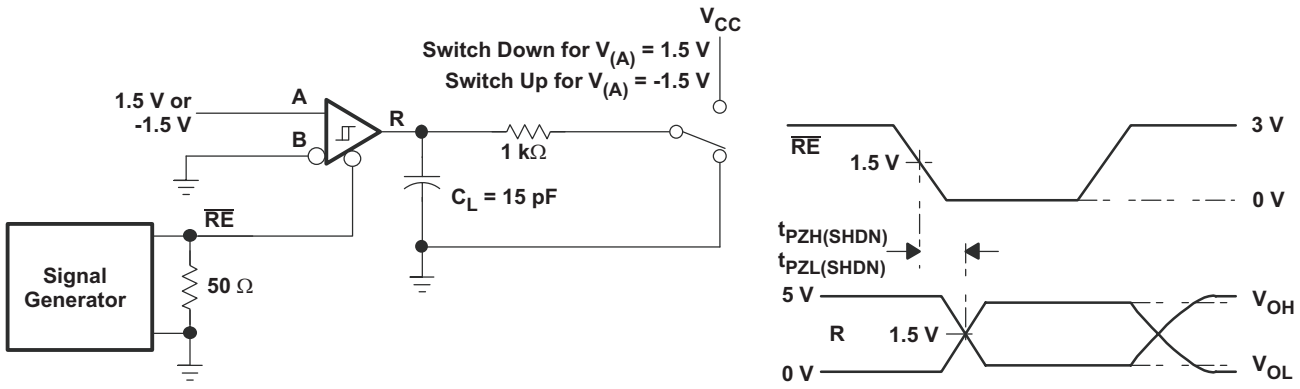


Figure 12. Receiver Enable From Shutdown Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

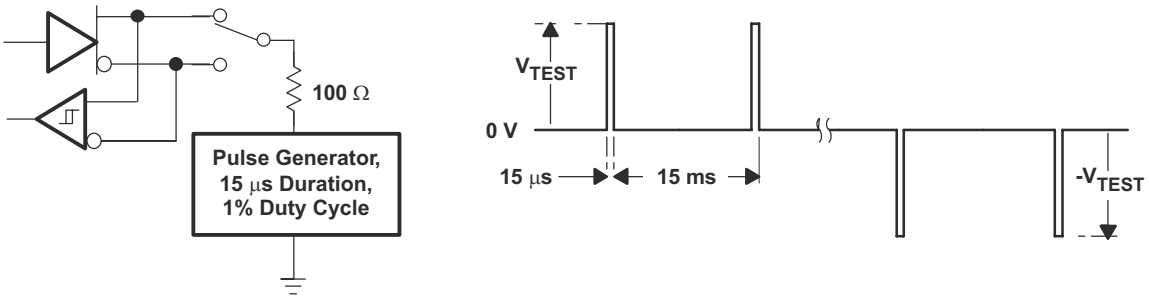
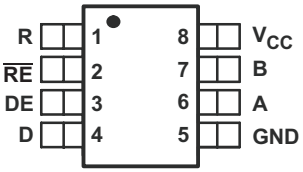


Figure 13. Test Circuit and Waveforms, Transient Overvoltage Test

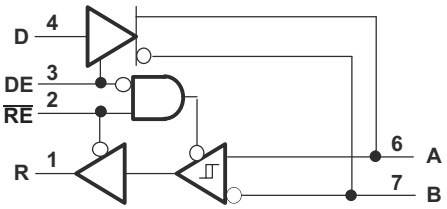
DEVICE INFORMATION

PIN ASSIGNMENT

D, P OR DGK PACKAGE
(TOP VIEW)



LOGIC DIAGRAM (POSITIVE LOGIC)



FUNCTION TABLE

DRIVER				RECEIVER		
INPUT D	INPUT DE	OUTPUTS		DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
		A	B			
H	H	H	L	$V_{ID} \le -0.2$ V	L	L
L	H	L	H	-0.2 V $< V_{ID} < -0.01$ V	L	?
X	L	Z	Z	-0.01 V $\le V_{ID}$	L	H
Open	H	H	L	X	H	Z
X	Open	Z	Z	Open circuit	L	H
				Short circuit	L	H
				IDLE Bus	L	H
				X	Open	Z

Receiver Failsafe

The differential receiver is “failsafe” to invalid bus states caused by:

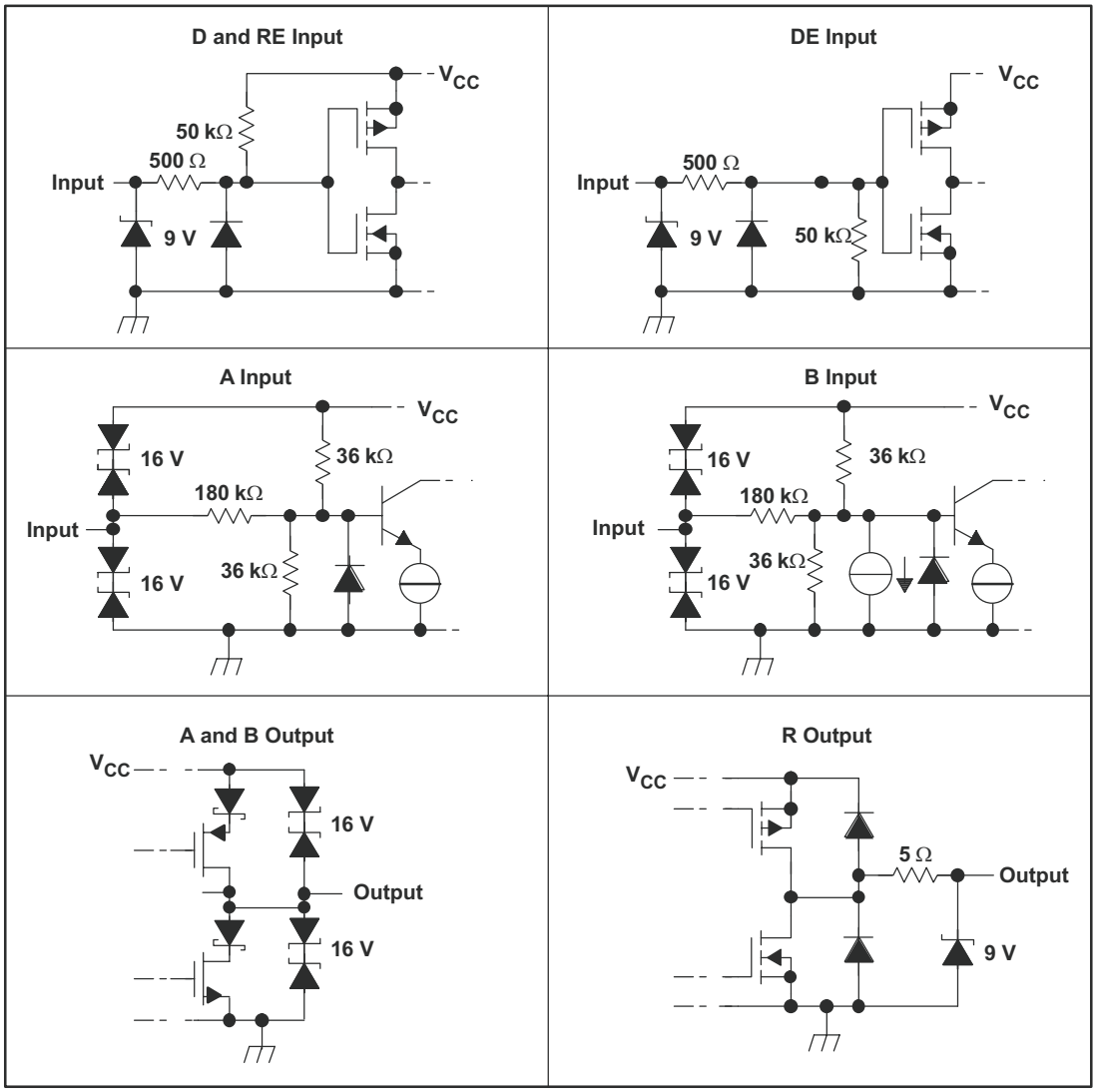
- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the “input indeterminate” range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when the V_{ID} is more negative than -200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and $V_{IT-}$and V_{HYS}. As seen in the RECEIVER ELECTRICAL CHARACTERISTICS table, differential signals more negative than -200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more negative than V_{IT-}will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and V_{IT-}) as well as the value of V_{IT+}.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



PACKAGE THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	PACKAGE	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	Low-k board, no air flow	MOSP (DGK)		266		°C/W
			SOIC (D)		210		
			PDIP (P)		155		
		High-k board, no air flow	MOSP (DGK)		180		°C/W
			SOIC (D)		130		
			PDIP (P)		70		
θ_{JB}	Junction-to-board thermal resistance	Low-k board, no air flow	MOSP (DGK)		110		°C/W
			SOIC (D)		55		
			PDIP (P)		40		
θ_{JC}	Junction-to-case thermal resistance		MOSP (DGK)		66		°C/W
			SOIC (D)		80		
			PDIP (P)		80		
$P_{(AVG)}$	Average power dissipation	Input to D is a 50% duty cycle square wave at max rec'd signal rate R_L = 54 Ω V_{CC} = 5.5 V, T_J = 130°C	ALL HVD3082E			203	mW
			ALL HVD3085E			205	
			ALL HVD3088E			276	
T_{SD}	Thermal shut-down junction temperature		ALL		165		°C

TYPICAL CHARACTERISTICS

BUS INPUT CURRENT vs BUS INPUT VOLTAGE

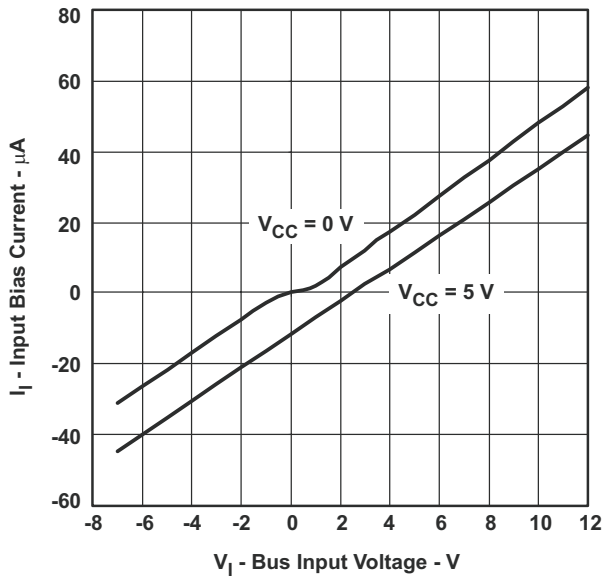


Figure 14.

SN65HVD3082E RMS SUPPLY CURRENT vs SIGNALING RATE

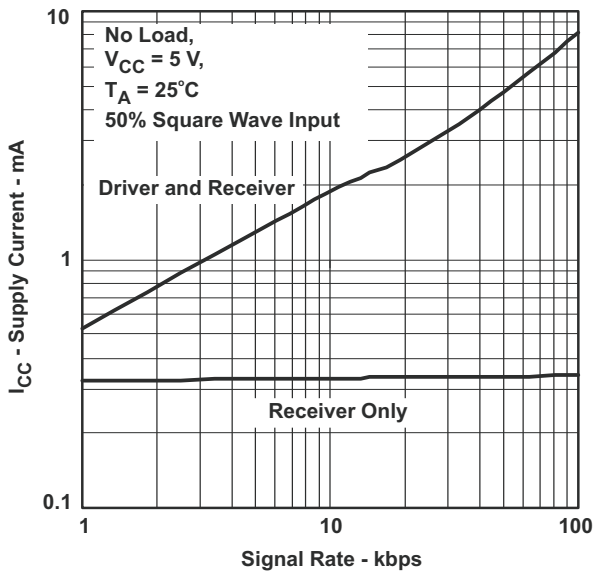


Figure 15.

TYPICAL CHARACTERISTICS (continued)

SN65HVD3085E
RMS SUPPLY CURRENT
vs
SIGNALING RATE

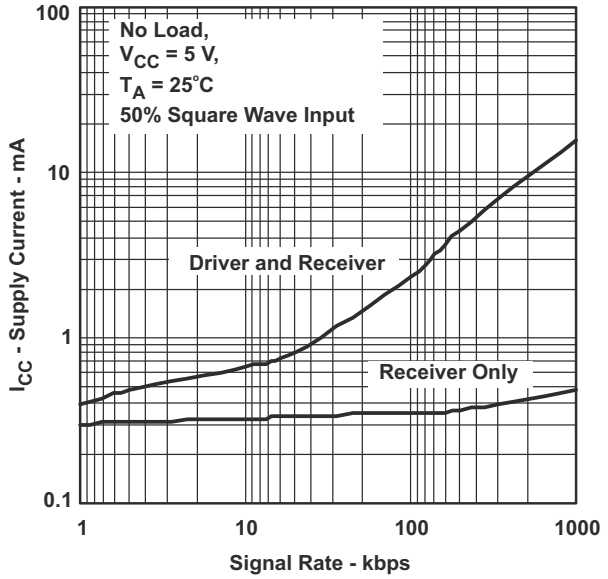


Figure 16.

SN65HVD3088E
RMS SUPPLY CURRENT
vs
SIGNAL RATE

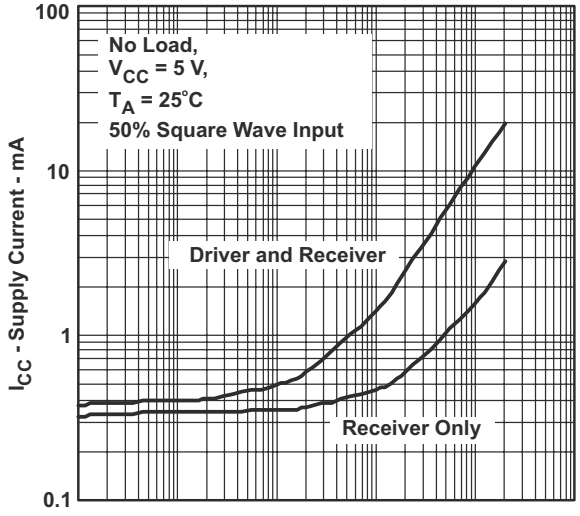


Figure 17.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DRIVER OUTPUT CURRENT

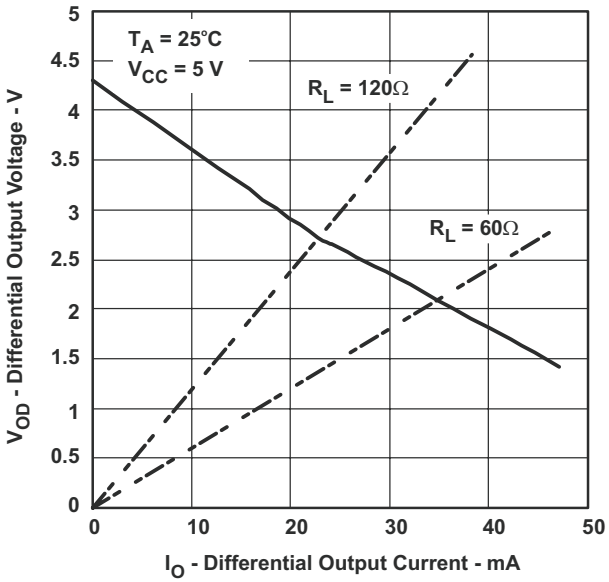


Figure 18.

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

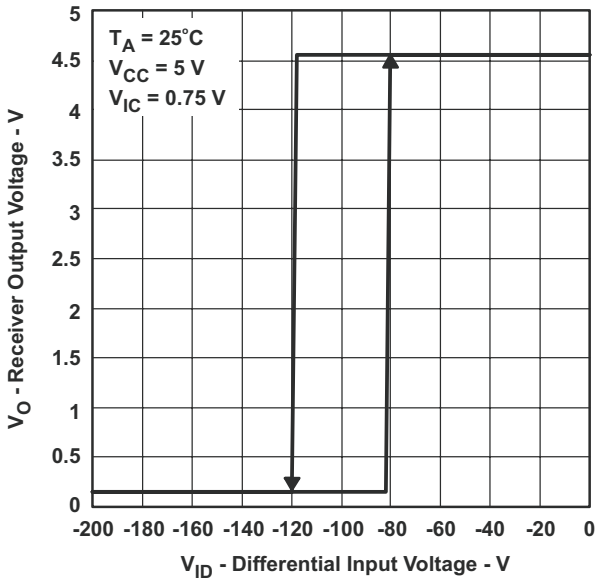


Figure 19.

TYPICAL CHARACTERISTICS (continued)

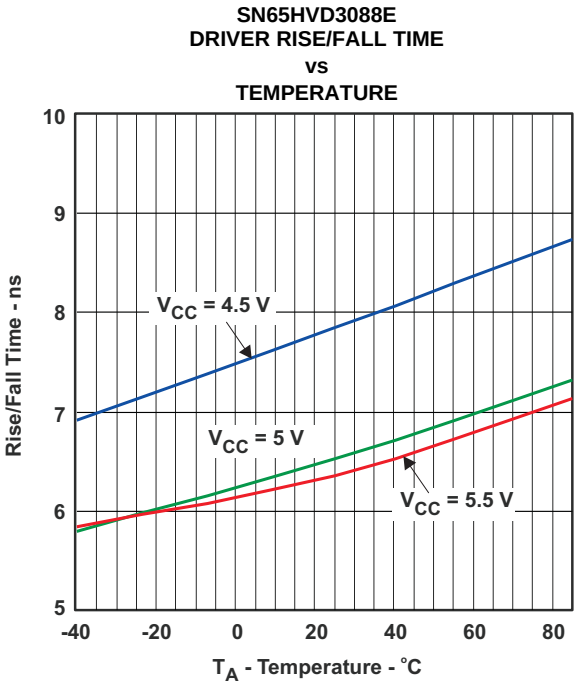
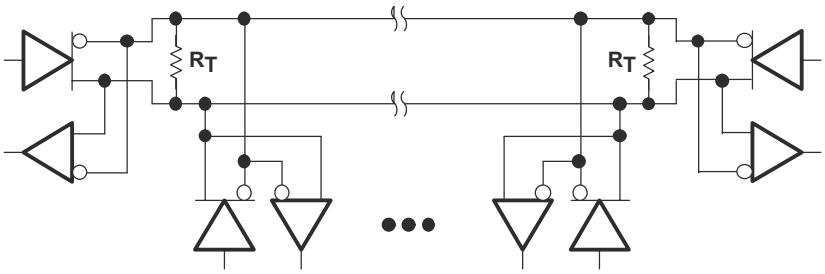


Figure 20.

APPLICATION INFORMATION



Note: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$).
Stub lengths off the main line should be kept as short as possible.

Figure 21. Typical Application Circuit

POWER USAGE IN AN RS-485 TRANSCEIVER

Power consumption is a concern in many applications. Power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS–485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes, plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The HVD308xE is rated as a 1/8 unit load device. As shown in , the bus input current is less than 1/8 mA, allowing up to 256 nodes on a single bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25 mA differential output current whenever the bus is active. Typically the HVD308xE can drive more than 25 mA to a 60 Ω load, resulting in a differential output voltage higher than the minimum required by the standard. (See Figure 16.)

Overall, the total load current can be 60 mA to a loaded RS-485 bus. This is in addition to the current required by the transceiver itself; the HVD308xE circuitry requires only about 0.4 mA with both driver and receiver enabled, and only 0.3 mA with either the driver enabled or with the receiver enabled. In low-power shutdown mode, neither the driver nor receiver is active, and the supply current is low.

Supply current increases with signaling rate primarily due to the totum pole outputs of the driver (see Figure 15). When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting and this creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

LOW-POWER SHUTDOWN MODE

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in shutdown mode. If the enable inputs are in this state for less than 60 ns, the device does not enter shutdown mode. This guards against inadvertently entering shutdown mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in shutdown mode. In this low-power shutdown mode, most internal circuitry is powered down, and the supply current is typically 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by $t_{PZH(SHDN)}$ and $t_{PZL(SHDN)}$ in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled (RE transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by $t_{PZH(SHDN)}$ and $t_{PZL(SHDN)}$ in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

THERMAL CHARACTERISTICS OF IC PACKAGES

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is NOT a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives best case in–use condition and consists of two 1–oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 22).

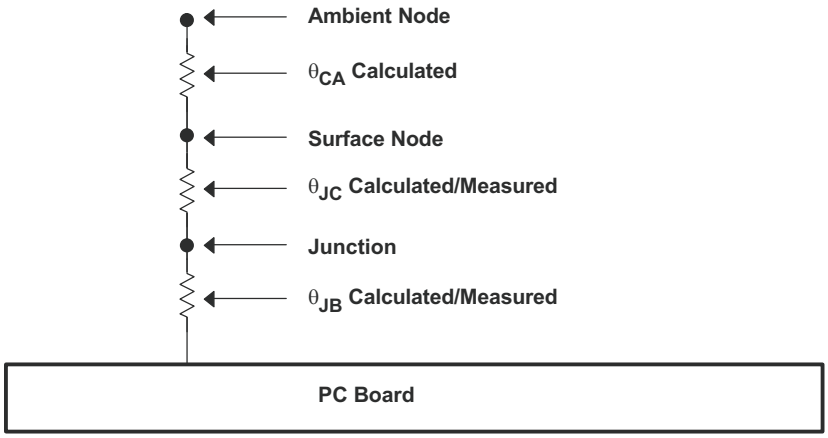


Figure 22. Thermal Resistance

REVISION HISTORY

Changes from Revision F (March 2009) to Revision G **Page**

- Added IDLE Bus to the Function Table 9
- Added Receiver Failsafe section 9
- Added Graph - DRIVER RISE/FALL TIME vs TEMPERATURE 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD3082ED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3082EDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3082EDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3082EDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3082EDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3082EDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3082EP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN65HVD3082EPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN65HVD3085ED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3085EDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3085EDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3085EDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3085EDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3085EDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3085EDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3085EDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3088ED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3088EDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD3088EDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3088EDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3088EDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3088EDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3088EDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65HVD3088EDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082ED	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082EDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082EDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082EDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082EDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082EDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082EDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082EDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN75HVD3082EP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN75HVD3082EPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SNHVD3082EDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNHVD3082EDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

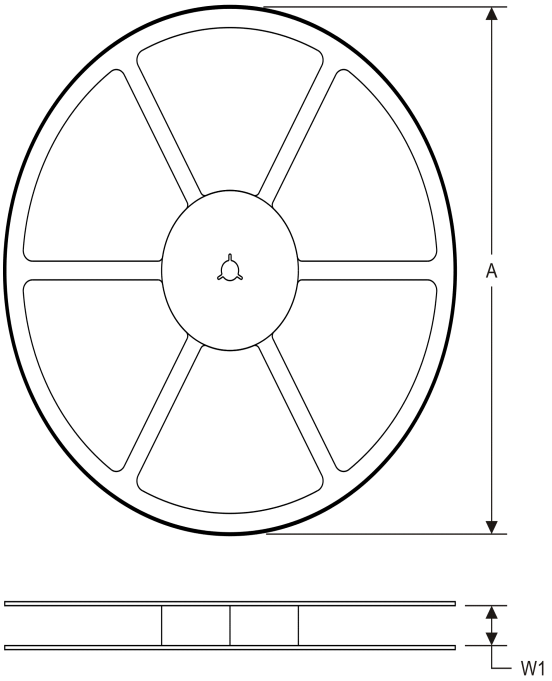
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

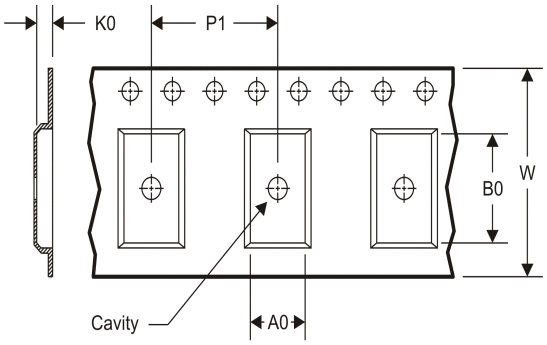
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



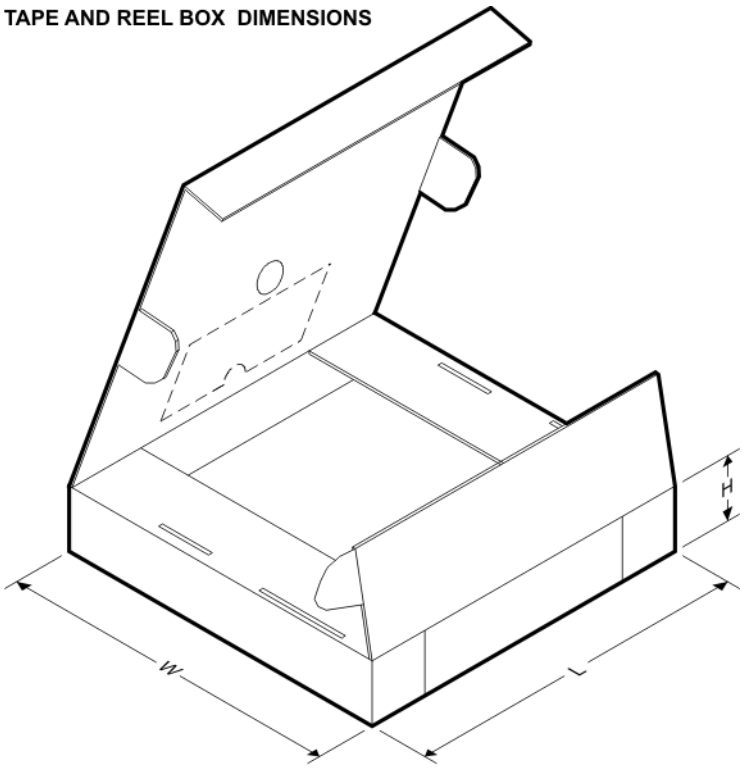
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD3082EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3082EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD3085EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3085EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD3088EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3088EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD3082EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN75HVD3082EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

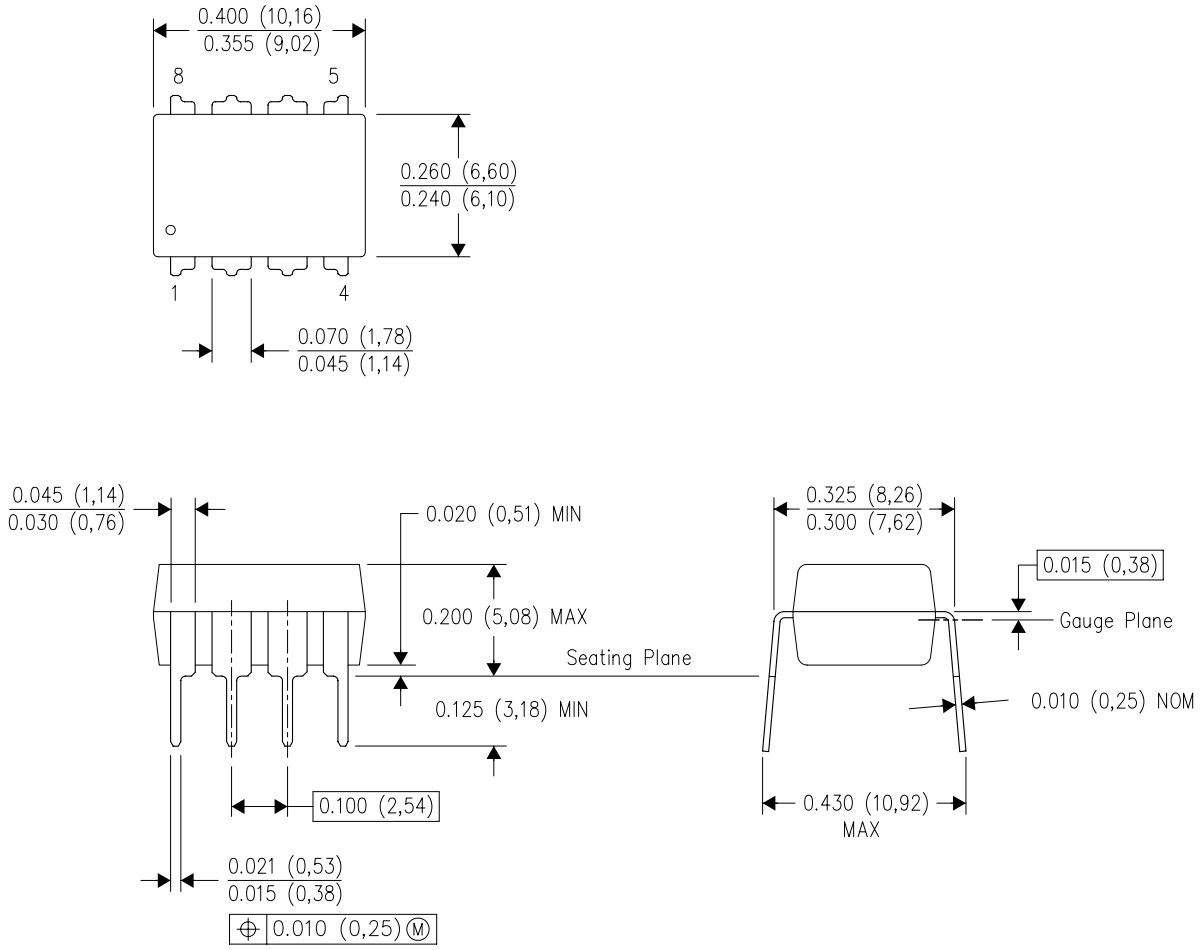
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

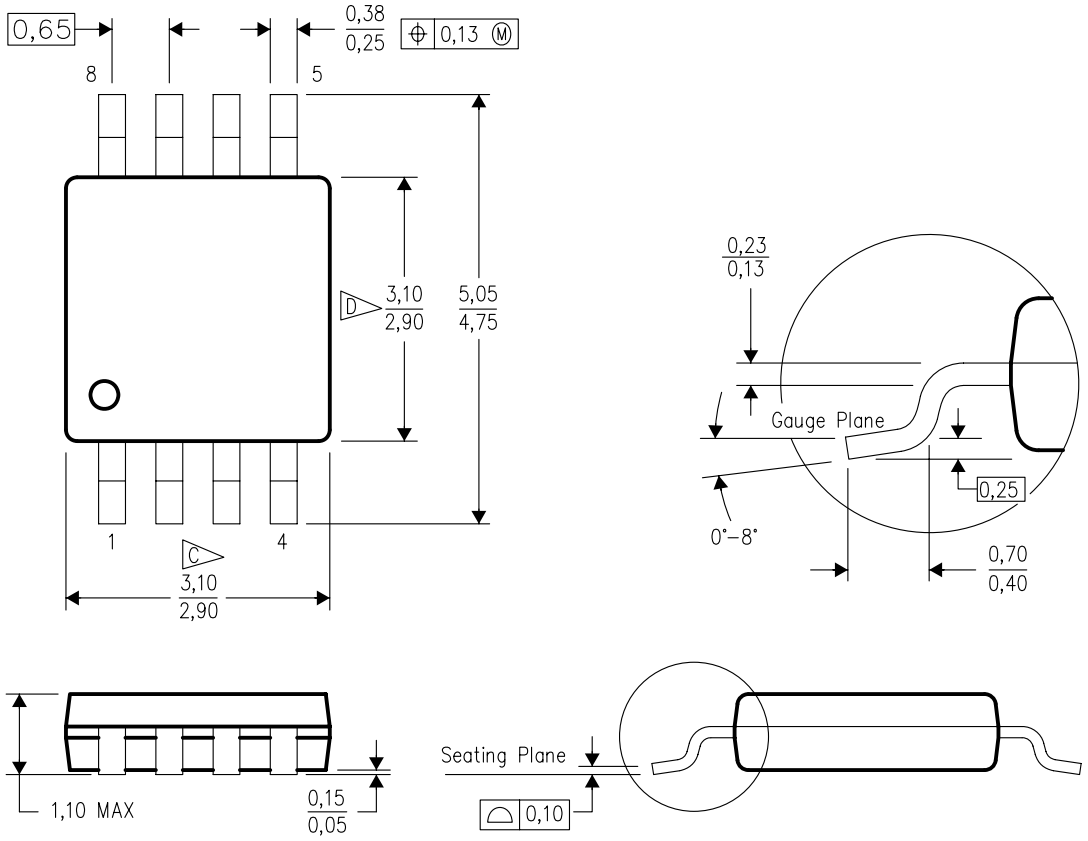
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD3082EDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65HVD3082EDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD3085EDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65HVD3085EDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD3088EDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN65HVD3088EDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75HVD3082EDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
SN75HVD3082EDR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

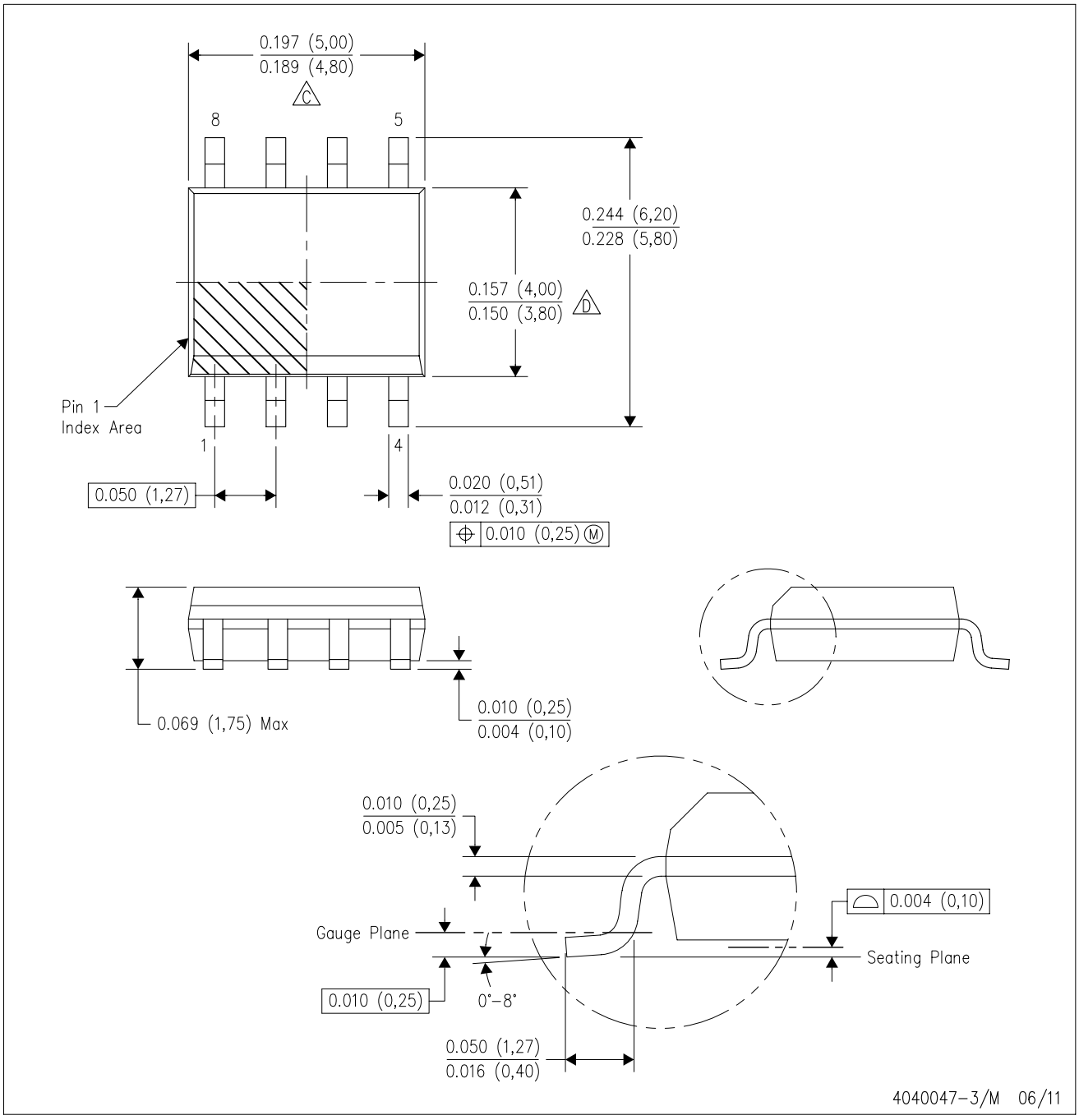
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

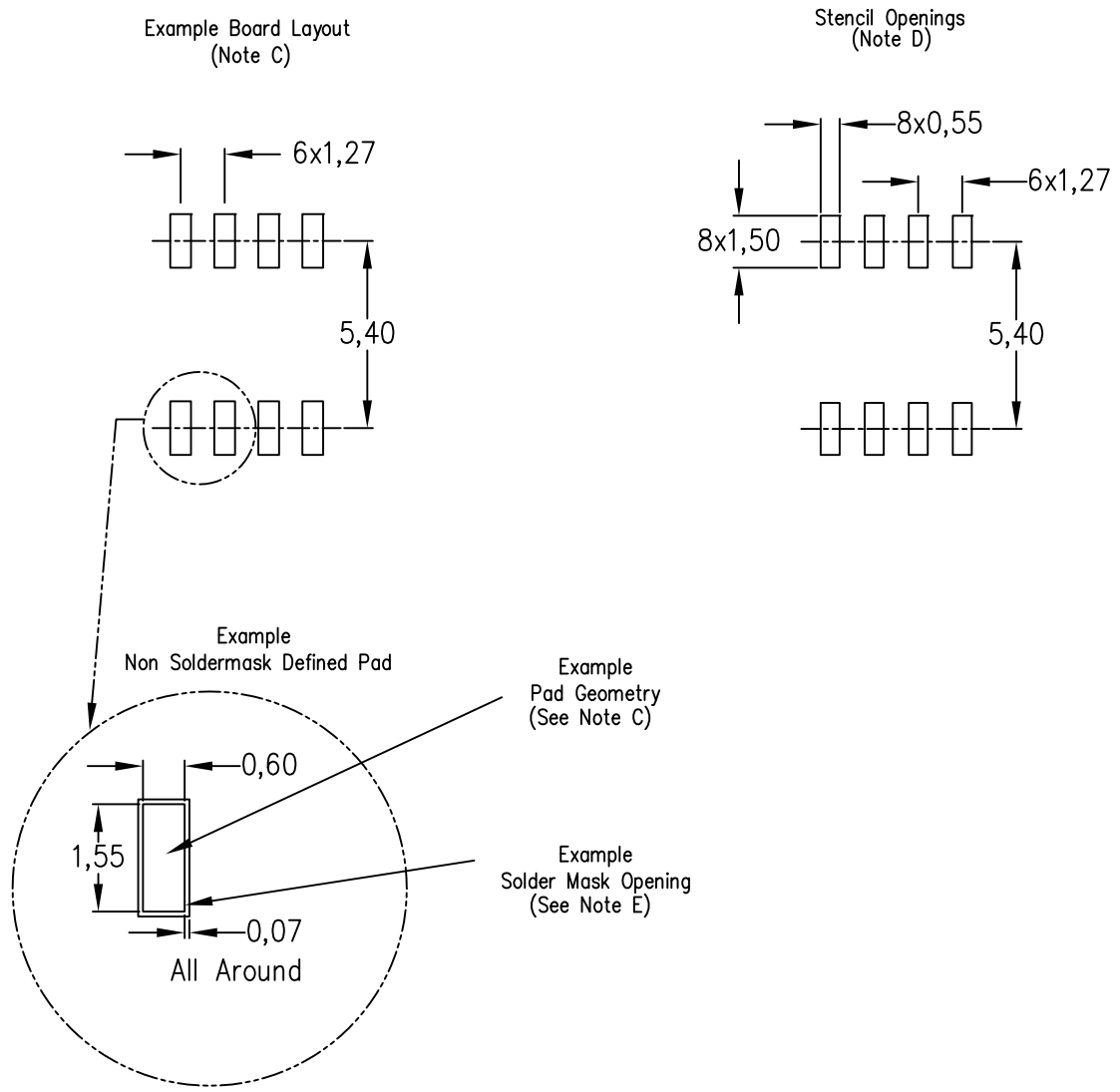
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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