

General Description

EZ-PD™ CCG2 is a USB Type-C controller that complies with the latest USB Type-C and PD standards. EZ-PD CCG2 provides a complete USB Type-C and USB Power Delivery port control solution for passive cables, active cables, and powered accessories. It can also be used in many upstream and downstream facing port applications. EZ-PD CCG2 uses Cypress's proprietary MOS8 technology with a 32-bit, 48-MHz ARM® Cortex®-M0 processor with 32-KB flash and integrates a complete Type-C Transceiver including the Type-C termination resistors R_P , R_D and R_A .

Applications

- USB Type-C EMCA cables
- USB Type-C powered accessories
- USB Type-C upstream facing ports
- USB Type-C downstream facing ports

Features

32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU
- 32-KB Flash
- 4-KB SRAM
- In-system reprogrammable

Integrated Digital Blocks

- Integrated timers and counters to meet response times required by the USB-PD protocol
- Run-time reconfigurable serial communication block (SCB) with reconfigurable I²C, SPI, or UART functionality

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Type-C Support

- Integrated transceiver (baseband PHY)
- Integrated UFP (R_D), EMCA (R_A) termination resistors, and current sources for DFP (R_P)
- Supports one USB Type-C port

Low-Power Operation

- 2.7-V to 5.5-V operation
- Two independent VCONN rails with integrated isolation between the two
- Independent supply voltage pin for GPIO that allows 1.71-V to 5.5-V signaling on the I/Os
- Reset: 1.0 μ A, Deep Sleep: 2.5 μ A, Sleep: 2.0 mA

System-Level ESD on CC and VCONN Pins

- ± 8 -kV Contact Discharge and ± 15 -kV Air Gap Discharge based on IEC61000-4-2 level 4C

Packages

- 1.63 mm \times 2.03 mm, 20-ball wafer-level CSP (WL CSP) with 0.4-mm ball pitch
- 2.5 mm \times 3.5 mm \times 0.6 mm 14-pin DFN
- 4.0 mm \times 4.0 mm, 0.55 mm 24-pin QFN
- Supports industrial (-40 °C to $+85$ °C) and extended industrial (-40 °C to $+105$ °C) temperature ranges

Logic Block Diagram

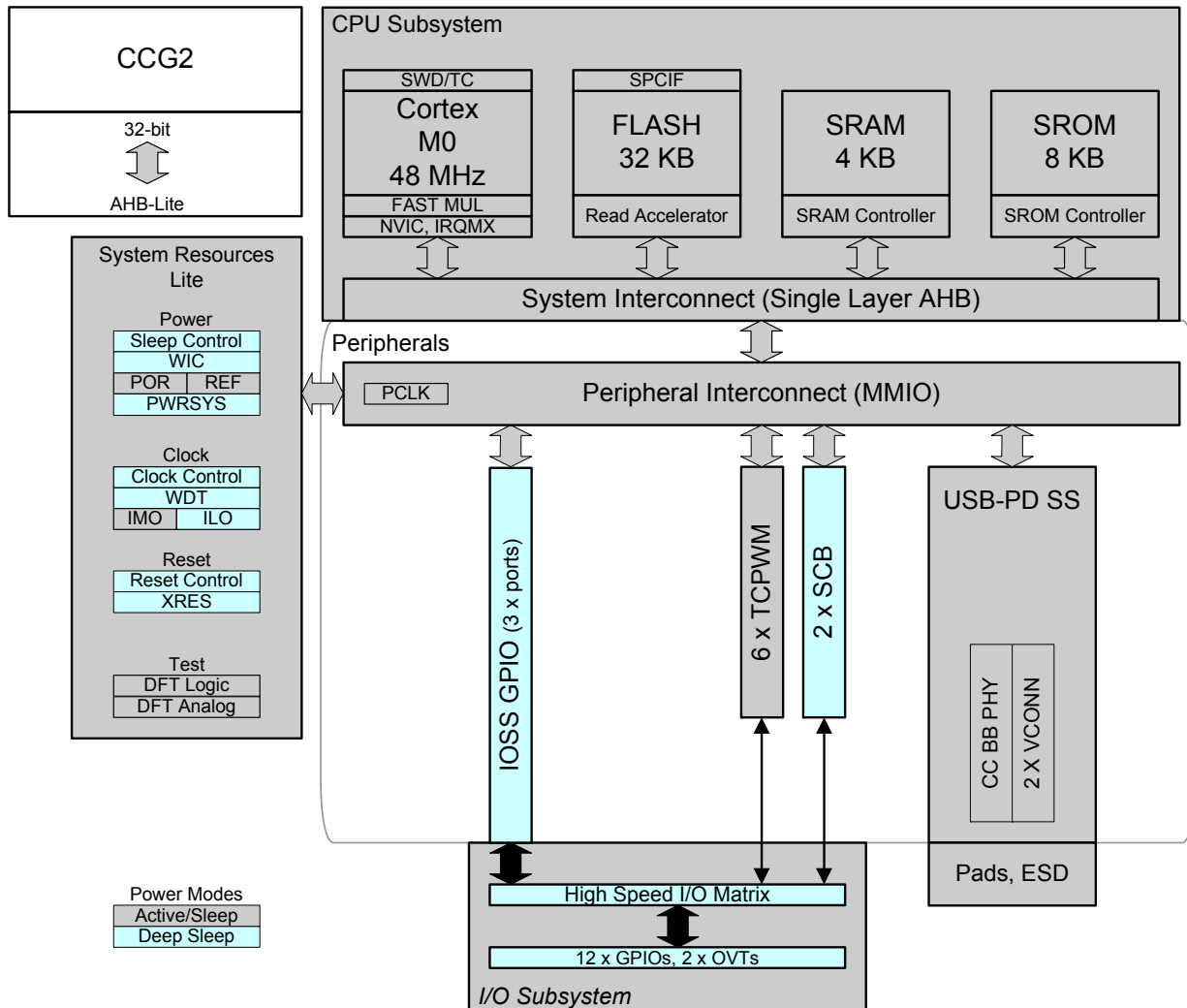


¹ Timer, counter, pulse-width modulation block
² Serial communication block configurable as UART, SPI, or I²C
³ Termination resistor denoting a UFP
⁴ Termination resistor denoting an EMCA
⁵ Configuration Channel
⁶ General-purpose input/output
⁷ Current Sources to indicate a DFP

Contents

| | | | |
|--|-----------|--|-----------|
| Functional Overview | 3 | System Resources | 22 |
| CPU and Memory Subsystem | 3 | Ordering Information | 25 |
| USB-PD Subsystem (SS) | 4 | Ordering Code Definitions | 25 |
| System Resources | 4 | Packaging | 26 |
| Peripherals | 5 | Acronyms | 28 |
| GPIO | 5 | Document Conventions | 29 |
| Pinouts | 6 | Units of Measure | 29 |
| Power | 8 | Document History Page | 30 |
| Application Diagrams | 9 | Sales, Solutions, and Legal Information | 31 |
| Electrical Specifications | 16 | Worldwide Sales and Design Support | 31 |
| Absolute Maximum Ratings | 16 | Products | 31 |
| Device Level Specifications | 17 | PSoC® Solutions | 31 |
| Digital Peripherals | 19 | Cypress Developer Community | 31 |
| Memory | 21 | Technical Support | 31 |

Figure 1. EZ-PD CCG2 Block Diagram



Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG2 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG2 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

EZ-PD CCG2 has a USB-PD subsystem consisting of a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as the 1.2-V front end. This subsystem integrates the required termination resistors to identify the role of the EZ-PD CCG2 solution. R_A is used to identify EZ-PD CCG2 as an accessory or an electronically marked cable. R_D is used to identify EZ-PD CCG2 as a UFP in a hybrid cable or a dongle. When configured as a DFP, integrated current sources perform the role of R_P or pull-up resistors. These current sources can be programmed to indicate the complete range of current capacity on VBUS defined in the Type-C spec. EZ-PD CCG2 responds to all USB-PD communication. The

EZ-PD CCG2 USB-PD sub-system can be configured to respond to SOP, SOP', or SOP'' messaging.

The USB-PD sub-system contains a 8-bit SAR (Successive Approximation Register) ADC for analog to digital conversions. The ADC includes a 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplexers an internal bandgap voltage and an internal voltage proportional to the absolute temperature. All GPIO inputs can be connected to the global Analog Multiplex Buses through a switch at each GPIO that can enable that GPIO to be connected to the mux bus for ADC use. The CC1, CC2 and RD1 pins are not available to connect to the mux busses.

Figure 2. USB-PD Subsystem



System Resources

Power System

The power system is described in detail in the section [Power on page 8](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). EZ-PD CCG2 can operate from three different power sources over the range of 2.7 to 5.5 V and has three different power modes, transitions between which are managed by the power system. EZ-PD CCG2 provides Sleep and Deep Sleep low-power modes.

Clock System

The clock system for EZ-PD CCG2 consists of the Internal Main Oscillator (IMO) and the Internal Low-power Oscillator (ILO).

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG2 has two SCBs, which can be configured to implement an I²C, SPI, or UART interface. The hardware I²C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I²C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I²C that creates a mailbox address range in the memory of EZ-PD CCG2 and effectively reduce I²C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I²C peripherals are compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/Os are implemented with GPIO in open-drain modes.

The I²C port on SCB 1 block of EZ-PD CCG2 is not completely compliant with the I²C spec in the following respects:

- The GPIO cells for SCB 1's I²C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG2 has six TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

GPIO

EZ-PD CCG2 has up to 10 GPIOs in addition to the I²C and SWD pins, which can also be used as GPIOs. The I²C pins from SCB 0 are overvoltage-tolerant. The number of available GPIOs vary with the package. The GPIO block implements the following:

- Seven drive strength modes:
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Pinouts

| Group | Name | Pin Map 24-QFN | Ball Location 20-CSP | Pin Map 14-DFN | Description |
|-----------------------------|-----------|----------------|----------------------|------------------|--|
| USB Type-C Port | CC1 | 2 | B4 | 3 | USB PD connector detect/Configuration Channel 1 |
| | CC2 | 1 | A4 | N/A | USB PD connector detect/Configuration Channel 2 |
| | RD1 | 3 | B3 | N/A | Dedicated Rd resistor pin for CC1 Must be left open for cable applications and connected together with CC1 ball for UFP or DFP with dead battery applications |
| GPIOs and serial interfaces | GPIO | 22 | C3 | N/A | GPIO / SPI_0_CLK / UART_0_RX |
| | GPIO | 18 | D3 | 13 | GPIO / SPI_0_MOSI / UART_0_TX |
| | GPIO | 13 | C2 | 10 | GPIO / I2C_1_SDA / SPI_1_MISO / UART_1_RX |
| | GPIO | 10 | D2 | N/A | GPIO / I2C_1_SCL / SPI_1_CLK / UART_1_TX |
| | GPIO | 15 | B2 | 11 | GPIO / SPI_1_SEL / UART_1_RTS |
| | GPIO | 14 | N/A | N/A | GPIO |
| | GPIO | 17 | N/A | N/A | GPIO |
| | GPIO | 21 | N/A | N/A | GPIO |
| | GPIO | 23 | N/A | N/A | GPIO |
| | GPIO | 24 | N/A | N/A | GPIO |
| | I2C_0_SCL | 20 | A3 | 1 | GPIO / I2C_0_SCL / SPI_0_MISO / UART_0_RTS |
| | I2C_0_SDA | 19 | A2 | 14 | GPIO / I2C_0_SDA / SPI_0_SEL / UART_0_CTS |
| | SWD_IO | 11 | E2 | 8 | SWD IO / GPIO / UART_1_CTS / SPI_1_MOSI |
| SWD_CLK | 12 | D1 | 9 | SWD clock / GPIO | |
| RESET | XRES | 16 | B1 | 12 | Reset input |
| POWER | VCONN1 | 5 | E4 | 5 | VCONN 1 input (4.0 V to 5.5 V) |
| | VCONN2 | 4 | C4 | 4 | VCONN 2 input (4.0 V to 5.5 V) |
| | VDDIO | 8 | E1 | N/A | 1.71-V to 5.5-V supply for I/Os |
| | VCCD | 7 | A1 | 6 | 1.8-V regulator output for filter capacitor |
| | VDDD | 9 | E3 | 7 | VDDD supply input/output (2.7 V to 5.5 V) |
| | VDDD | 6 | | | VDDD supply input/output (2.7 V to 5.5 V) |
| | VSS | EPAD | N/A | EPAD | Ground supply |
| | VSS | | D4 | 2 | Ground supply |
| | VSS | | C1 | | Ground supply |

Power

The following power system diagram shows the set of power supply pins as implemented in EZ-PD CCG2.

EZ-PD CCG2 can operate from three different power sources. VCONN1 and VCONN2 pins can be used as connections to the VCONN pins on a Type-C plug of a cable or VCONN-powered accessory. Each of these inputs support operation over 4.0 to 5.5 V. An internal isolation between VCONN1 and VCONN2 pins is provided allowing them to be at different levels simultaneously. CCG2 can be used in EMCA applications with only one or both VCONN pins as power sources. This is illustrated later in the section on Applications. Besides being power inputs, each VCONN pin is also internally connected to a R_A termination resistor required for EMCA and VCONN-powered accessories.

EZ-PD CCG2 can also be operated from 2.7 to 5.5 V when operated from the VDDD supply pin. VCONN-powered accessory applications require that CCG2 work down to 2.7 V. In such applications, both the VDDD and VCONN pins should be connected to the VCONN pin of the Type-C plug in the accessory.

In UFP, DFP, and DRP applications, CCG2 can be operated from VDDD as the only supply input. In such applications, the VCONN pins are left open. In DFP applications, the lowest VDDD level that CCG2 can operate is 3.0 V due to the need to support disconnect detection thresholds of up to 2.7 V.

A separate I/O supply pin, VDDIO, allows the GPIOs to operate at levels from 1.71 to 5.5 V. The VDDIO pin can be equal to or less than the voltages connected to the VCONN1, VCONN2, and VDDD pins. The independent VDDIO supply is not available on the 14-DFN package. On this package, the VDDIO rail is internally connected to the VDDD rails.

The VCCD output of EZ-PD CCG2 must be bypassed to ground via an external capacitor (in the range of 1 to 1.6 μF ; X5R ceramic or better).

Bypass capacitors must be used from VDDD and VCONN pins to ground; typical practice for systems in this frequency range is to use a 0.1- μF capacitor. Note that these are simply rules of thumb and that for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of the power supply bypass capacitors is shown in [Figure 6](#).



Application Diagrams

Figure 7. Passive EMCA Application – Single EZ-PD CCG2 Per Cable

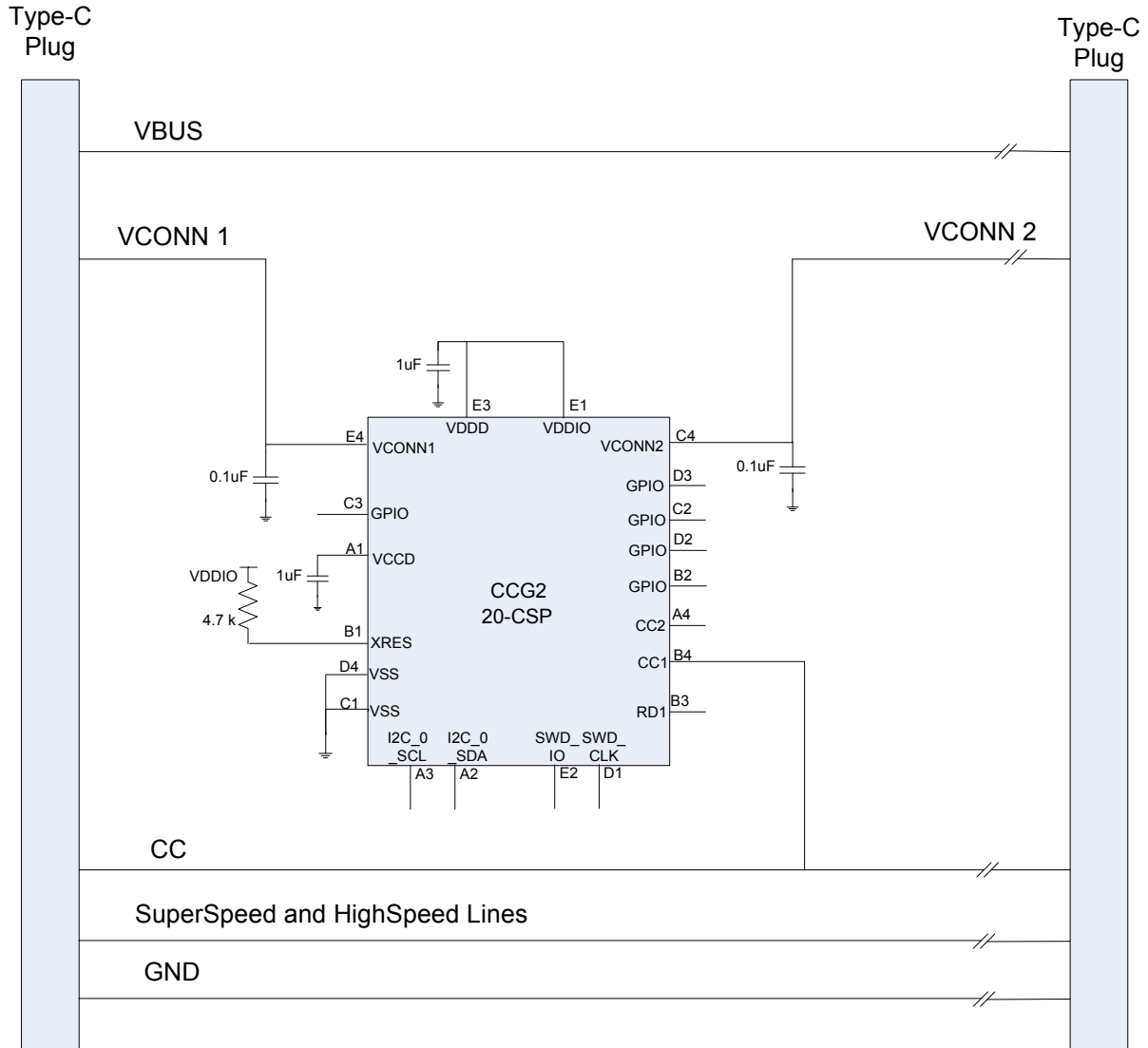


Figure 8. Passive EMCA Application – Single EZ-PD CCG2 Per Plug



Figure 9. Upstream Facing Port (UFP) Application – Tablet with a Type-C Port



Figure 10. Dual Role Port (DRP) Application



Figure 11. Downstream Facing Port (DFP) Application



Figure 12. USB Type-C to HDMI/DVI/VGA Dongle Application Diagram



Figure 13. USB Type-C to Display Port Application Diagram

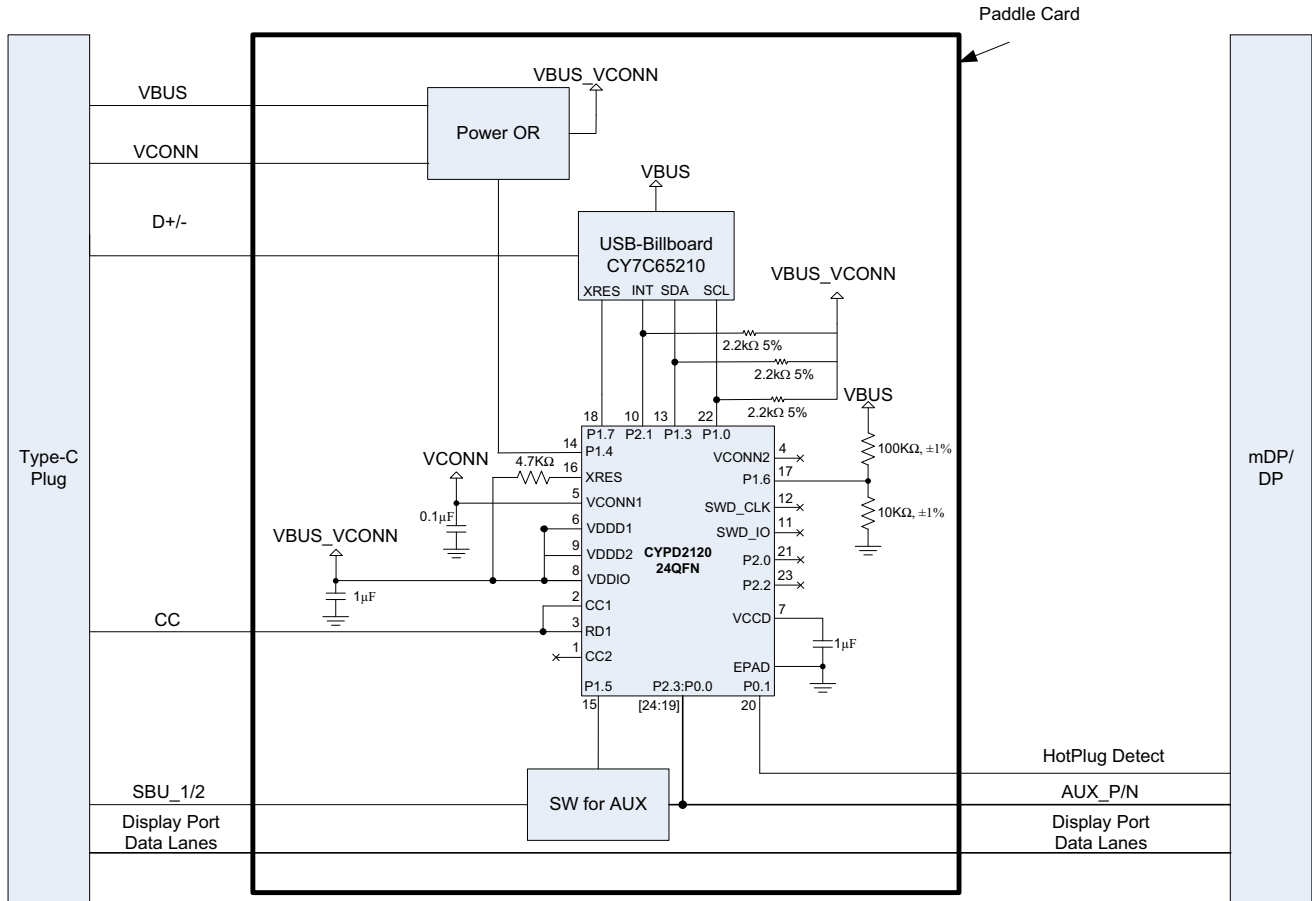


Figure 14. CCG2 in Dock/Monitor Application Diagram



CCG2 connected on the Upstream Port

CCG2 connected on the Downstream Port

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings^[1]

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------------------------|--|-------|-----|-------------------------|-------|--|
| V _{DDD_MAX} | Digital supply relative to V _{SS} | -0.5 | - | 6 | V | Absolute max |
| V _{CONN1_MAX} | Max supply voltage relative to V _{SS} | - | - | 6 | V | Absolute max |
| V _{CONN2_MAX} | Max supply voltage relative to V _{SS} | - | - | 6 | V | Absolute max |
| V _{DDIO_MAX} | Max supply voltage relative to V _{SS} | - | - | 6 | V | Absolute max |
| V _{GPIO_ABS} | GPIO voltage | -0.5 | - | V _{DDIO} + 0.5 | V | Absolute max |
| V _{CC_ABS} | Absolute max voltage for CC1 and CC2 pins | - | - | 6 | V | Absolute max |
| I _{GPIO_ABS} | Maximum current per GPIO | -25 | - | 25 | mA | Absolute max |
| I _{GPIO_injection} | GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS} | -0.5 | - | 0.5 | mA | Absolute max, current injected per pin |
| ESD_HBM | Electrostatic discharge human body model | 2200 | - | - | V | - |
| ESD_CDM | Electrostatic discharge charged device model | 500 | - | - | V | - |
| LU | Pin current for latch-up | -200 | - | 200 | mA | - |
| ESD_IEC_CON | Electrostatic discharge IEC61000-4-2 | 8000 | - | - | V | Contact discharge on CC1, CC2, VCONN1, and VCONN2 pins |
| ESD_IEC_AIR | Electrostatic discharge IEC61000-4-2 | 15000 | - | - | V | Air discharge for pins CC1, CC2, VCONN1, and VCONN2 |

Note

- Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Device Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 3.0 V to 5.5 V, except where noted.

Table 2. DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--|-----------------------|--|------|-----|-----|-------|--|
| SID.PWR#1 | V _{DDD} | Power supply input voltage | 2.7 | – | 5.5 | V | UFP Applications |
| SID.PWR#1_A | V _{DDD} | Power supply input voltage | 3.0 | – | 5.5 | V | DFP/DRP Applications |
| SID.PWR#23 | V _{CONN1} | Power supply input voltage | 4.0 | – | 5.5 | V | – |
| SID.PWR#23_A | V _{CONN2} | Power supply input voltage | 4.0 | – | 5.5 | V | – |
| SID.PWR#13 | V _{DDIO} | GPIO power supply | 1.71 | – | 5.5 | V | – |
| SID.PWR#24 | V _{CCD} | Output voltage (for core logic) | – | 1.8 | – | V | – |
| SID.PWR#15 | C _{EFC} | External regulator voltage bypass on V _{CCD} | 1 | 1.3 | 1.6 | μF | X5R ceramic or better |
| SID.PWR#16 | C _{EXC} | Power supply decoupling capacitor on V _{DDD} | – | 1 | – | μF | X5R ceramic or better |
| SID.PWR#25 | | Power Supply Decoupling Capacitor on V _{CONN1} and V _{CONN2} | – | 0.1 | – | μF | X5R ceramic or better |
| Active Mode, V_{DDD} = 2.7 to 5.5 V. Typical values measured at V_{DD} = 3.3 V. | | | | | | | |
| SID.PWR#12 | I _{DD12} | Supply current | – | 7.5 | – | mA | V _{CONN1} or V _{CONN2} = 5 V, T _A = 25 °C, CC I/O IN Transmit or Receive, R _A disconnected, no I/O sourcing current, CPU at 12 MHz |
| Sleep Mode, V_{DDD} = 2.7 to 5.5 V | | | | | | | |
| SID25A | I _{DD20A} | I ² C wakeup. WDT ON. IMO at 48 MHz | – | 2.0 | 3.0 | mA | V _{DDD} = 3.3 V, T _A = 25 °C, all blocks except CPU are ON, CC I/O ON, no I/O sourcing current |
| Deep Sleep Mode, V_{DDD} = 2.7 to 3.6 V (Regulator on) | | | | | | | |
| SID_DS_RA | I _{DD_DS_RA} | V _{CONN1} = 5.0, R _A termination disabled | – | 100 | – | μA | V _{CONN1} , V _{CONN2} = 5 V, T _A = 25 °C. R _A termination disabled on V _{CONN1} and V _{CONN2} , see SID.PD.7. VCONN leaker circuits turned off during deep sleep |
| SID34 | I _{DD29} | V _{DDD} = 2.7 to 3.6 V. I ² C wakeup and WDT ON | – | 50 | – | μA | R _A switch disabled on V _{CONN1} and V _{CONN2} . V _{DDD} = 3.3 V, T _A = 25 °C |
| SID_DS | I _{DD_DS} | V _{DDD} = 2.7 to 3.6 V. CC wakeup ON | – | 2.5 | – | μA | Power source = V _{DDD} , Type-C not attached, CC enabled for wakeup, R _p disabled |
| XRES Current | | | | | | | |
| SID307 | I _{DD_XR} | Supply current while XRES asserted | – | 1 | 10 | μA | – |

Table 3. AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------|------------------------|--|-----|-----|-----|-------|--|
| SID.CLK#4 | F _{CPU} | CPU frequency | DC | – | 48 | MHz | 3.0 V ≤ V _{DD} ≤ 5.5 V |
| SID.PWR#20 | T _{SLEEP} | Wakeup from sleep mode | – | 0 | – | μs | Guaranteed by characterization |
| SID.PWR#21 | T _{DEEPSLEEP} | Wakeup from Deep Sleep mode | – | – | 35 | μs | 24-MHz IMO. Guaranteed by characterization |
| SID.XRES#5 | T _{XRES} | External reset pulse width | 5 | – | – | μs | Guaranteed by characterization |
| SYS.FES#1 | T _{PWR_RDY} | Power-up to “Ready to accept I2C / CC command” | – | 5 | 25 | ms | Guaranteed by characterization |

I/O

Table 4. I/O DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------|--------------------------------|--|--------------------------|-----|-------------------------|-------|--|
| SID.GIO#37 | V _{IH} ^[2] | Input voltage HIGH threshold | 0.7 × V _{DDIO} | – | – | V | CMOS input |
| SID.GIO#38 | V _{IL} | Input voltage LOW threshold | – | – | 0.3 × V _{DDIO} | V | CMOS input |
| SID.GIO#39 | V _{IH} ^[2] | LVTTL input, V _{DDIO} < 2.7 V | 0.7 × V _{DDIO} | – | – | V | – |
| SID.GIO#40 | V _{IL} | LVTTL input, V _{DDIO} < 2.7 V | – | – | 0.3 × V _{DDIO} | V | – |
| SID.GIO#41 | V _{IH} ^[2] | LVTTL input, V _{DDIO} ≥ 2.7 V | 2.0 | – | – | V | – |
| SID.GIO#42 | V _{IL} | LVTTL input, V _{DDIO} ≥ 2.7 V | – | – | 0.8 | V | – |
| SID.GIO#33 | V _{OH} | Output voltage HIGH level | V _{DDIO} – 0.6 | – | – | V | I _{OH} = 4 mA at 3-V V _{DDIO} |
| SID.GIO#34 | V _{OH} | Output voltage HIGH level | V _{DDIO} – 0.5 | – | – | V | I _{OH} = 1 mA at 1.8-V V _{DDIO} |
| SID.GIO#35 | V _{OL} | Output voltage LOW level | – | – | 0.6 | V | I _{OL} = 4 mA at 1.8-V V _{DDIO} |
| SID.GIO#36 | V _{OL} | Output voltage LOW level | – | – | 0.6 | V | I _{OL} = 8 mA at 3 V V _{DDIO} |
| SID.GIO#5 | R _{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID.GIO#6 | R _{PULLDOWN} | Pull-down resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| SID.GIO#16 | I _{IL} | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, V _{DDIO} = 3.0 V. Guaranteed by characterization |
| SID.GIO#17 | C _{IN} | Input capacitance | – | – | 7 | pF | Guaranteed by characterization |
| SID.GIO#43 | V _{HYSTTL} | Input hysteresis LVTTL | 25 | 40 | – | mV | V _{DDIO} ≥ 2.7 V. Guaranteed by characterization. |
| SID.GPIO#44 | V _{HYS CMOS} | Input hysteresis CMOS | 0.05 × V _{DDIO} | – | – | mV | Guaranteed by characterization |
| SID69 | I _{DIODE} | Current through protection diode to V _{DDIO} /V _{SS} | – | – | 100 | μA | Guaranteed by characterization |
| SID.GIO#45 | I _{TOT_GPIO} | Maximum total source or sink chip current | – | – | 200 | mA | Guaranteed by characterization |

Note

 2. V_{IH} must not exceed V_{DDIO} + 0.2 V.

Table 5. I/O AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|-------------|-----|-----|-----|-------|--|
| SID70 | T _{RISEF} | Rise time | 2 | – | 12 | ns | 3.3-V V _{DDIO} , Clload = 25 pF |
| SID71 | T _{FALLF} | Fall time | 2 | – | 12 | ns | 3.3-V V _{DDIO} , Clload = 25 pF |

XRES
Table 6. XRES DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------|----------------------|------------------------------|-------------------------|-----|--------------------------|-------|--------------------------------|
| SID.XRES#1 | V _{IH} | Input voltage HIGH threshold | 0.7 × V _{DDIO} | – | – | V | CMOS input |
| SID.XRES#2 | V _{IL} | Input voltage LOW threshold | – | – | 0.3 × V _{DDIO} | V | CMOS input |
| SID.XRES#3 | C _{IN} | Input capacitance | – | – | 7 | pF | Guaranteed by characterization |
| SID.XRES#4 | V _{HYSXRES} | Input voltage hysteresis | – | – | 0.05 × V _{DDIO} | mV | Guaranteed by characterization |

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins
Table 7. PWM AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------|-----------------------|------------------------------|-----|------------------|-----|-------|--|
| SID.TCPWM.3 | T _{CPWMFREQ} | Operating frequency | – | F _c | – | MHz | F _c max = CLK_SYS. Maximum = 48 MHz. |
| SID.TCPWM.4 | T _{PWMENEXT} | Input trigger pulse width | – | 2/F _c | – | ns | For all Trigger Events |
| SID.TCPWM.5 | T _{PWMEXT} | Output trigger pulse width | – | 2/F _c | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | T _{CRES} | Resolution of counter | – | 1/F _c | – | ns | Minimum time between successive counts |
| SID.TCPWM.5B | PWM _{RES} | PWM resolution | – | 1/F _c | – | ns | Minimum pulse width of PWM output |
| SID.TCPWM.5C | Q _{RES} | Quadrature inputs resolution | – | 1/F _c | – | ns | Minimum pulse width between quadrature-phase inputs |

I²C
Table 8. Fixed I²C DC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---|-----|-----|-----|-------|--------------------|
| SID149 | I _{I2C1} | Block current consumption at 100 kbps | – | – | 60 | μA | – |
| SID150 | I _{I2C2} | Block current consumption at 400 kbps | – | – | 185 | μA | – |
| SID151 | I _{I2C3} | Block current consumption at 1 Mbps | – | – | 390 | μA | – |
| SID152 | I _{I2C4} | I ² C enabled in Deep Sleep mode | – | – | 1.4 | μA | – |

Table 9. Fixed I²C AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Mbps | – |

Table 10. Fixed UART DC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|---|-----|-----|-----|-------|--------------------------------|
| SID160 | I _{UART1} | Block current consumption at 100 Kbits/sec | – | – | 125 | μA | Guaranteed by characterization |
| SID161 | I _{UART2} | Block current consumption at 1000 Kbits/sec | – | – | 312 | μA | Guaranteed by characterization |

Table 11. Fixed UART AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------------------|
| SID162 | F _{UART} | Bit rate | – | – | 1 | Mbps | Guaranteed by characterization |

Table 12. Fixed SPI DC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|--|-----|-----|-----|-------|--------------------------------|
| SID163 | I _{SPI1} | Block current consumption at 1Mbits/sec | – | – | 360 | μA | Guaranteed by characterization |
| SID164 | I _{SPI2} | Block current consumption at 4 Mbits/sec | – | – | 560 | μA | Guaranteed by characterization |
| SID165 | I _{SPI3} | Block current consumption at 8 Mbits/sec | – | – | 600 | μA | Guaranteed by characterization |

Table 13. Fixed SPI AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---|-----|-----|-----|-------|--------------------------------|
| SID166 | F _{SPI} | SPI Operating frequency (Master; 6X oversampling) | – | – | 8 | MHz | Guaranteed by characterization |

Table 14. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---|-----|-----|-----|-------|--|
| SID167 | T _{DMO} | MOSI Valid after SClock driving edge | – | – | 15 | ns | Guaranteed by characterization |
| SID168 | T _{DSI} | MISO Valid before SClock capturing edge | 20 | – | – | ns | Full clock, late MISO sampling. Guaranteed by characterization |
| SID169 | T _{HMO} | Previous MOSI data hold time | 0 | – | – | ns | Referred to Slave capturing edge. Guaranteed by characterization |

Table 15. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|--|-----|-----|---------------------------|-------|---|
| SID170 | T _{DMI} | MOSI Valid before Sclock Capturing edge | 40 | – | – | ns | Guaranteed by characterization |
| SID171 | T _{DSO} | MISO Valid after Sclock driving edge | – | – | 42 + 3 * T _{CPU} | ns | T _{CPU} = 1/F _{CPU} . Guaranteed by characterization. |
| SID171A | T _{DSO_EXT} | MISO Valid after Sclock driving edge in Ext Clk mode | – | – | 48 | ns | Guaranteed by characterization |
| SID172 | T _{HSD} | Previous MISO data hold time | 0 | – | – | ns | Guaranteed by characterization |
| SID172A | T _{SSELSCK} | SSEL Valid to first SCK Valid edge | 100 | – | – | ns | Guaranteed by characterization |

Memory
Table 16. Flash AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|--|---|-------|-----|-----|---------|--------------------------------|
| SID.MEM#4 | T _{ROWWRITE} ^[3] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes |
| SID.MEM#3 | T _{ROWERASE} ^[3] | Row erase time | – | – | 13 | ms | – |
| SID.MEM#8 | T _{ROWPROGRAM} ^[3] | Row program time after erase | – | – | 7 | ms | – |
| SID178 | T _{BULKERASE} ^[3] | Bulk erase time (32 KB) | – | – | 35 | ms | – |
| SID180 | T _{DEVPROG} ^[3] | Total device program time | – | – | 7.5 | seconds | Guaranteed by characterization |
| SID181 | F _{END} | Flash endurance | 100 K | – | – | cycles | Guaranteed by characterization |
| SID182 | F _{RET1} | Flash retention. T _A ≤ 55 °C, 100 K P/E cycles | 20 | – | – | years | Guaranteed by characterization |
| SID182A | F _{RET2} | Flash retention. T _A ≤ 85 °C, 10 K P/E cycles | 10 | – | – | years | Guaranteed by characterization |

Note

- It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources
Power-on-Reset (POR) with Brown Out
Table 17. Imprecise Power On Reset (PRES)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|----------------------|------|-----|------|-------|--------------------------------|
| SID185 | V _{RISEIPOR} | Rising trip voltage | 0.80 | – | 1.50 | V | Guaranteed by characterization |
| SID186 | V _{FALLIPOR} | Falling trip voltage | 0.75 | – | 1.4 | V | Guaranteed by characterization |

Table 18. Precise Power On Reset (POR)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|--|------|-----|------|-------|--------------------------------|
| SID190 | V _{FALLPPOR} | BOD trip voltage in active and sleep modes | 1.48 | – | 1.62 | V | Guaranteed by characterization |
| SID192 | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep | 1.1 | – | 1.5 | V | Guaranteed by characterization |

SWD Interface
Table 19. SWD Interface Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|--------------|--|--------|-----|---------|-------|---------------------------------------|
| SID.SWD#1 | F_SWDCLK1 | $3.3\text{ V} \leq V_{DDIO} \leq 5.5\text{ V}$ | – | – | 14 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID.SWD#2 | F_SWDCLK2 | $1.8\text{ V} \leq V_{DDIO} \leq 3.3\text{ V}$ | – | – | 7 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID.SWD#3 | T_SWDI_SETUP | $T = 1/f\text{ SWDCLK}$ | 0.25*T | – | – | ns | Guaranteed by characterization |
| SID.SWD#4 | T_SWDI_HOLD | $T = 1/f\text{ SWDCLK}$ | 0.25*T | – | – | ns | Guaranteed by characterization |
| SID.SWD#5 | T_SWDO_VALID | $T = 1/f\text{ SWDCLK}$ | – | – | 0.5 * T | ns | Guaranteed by characterization |
| SID.SWD#6 | T_SWDO_HOLD | $T = 1/f\text{ SWDCLK}$ | 1 | – | – | ns | Guaranteed by characterization |

Internal Main Oscillator
Table 20. IMO DC Specifications
(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---------------------------------|-----|-----|------|-------|--------------------|
| SID218 | I _{IMO} | IMO operating current at 48 MHz | – | – | 1000 | μA | – |

Table 21. IMO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------|------------------------|---|-----|-----|-----|-------|--------------------------------|
| SID.CLK#13 | F _{IMOTOL} | Frequency variation at 24, 36, and 48 MHz (trimmed) | – | – | ±2 | % | – |
| SID226 | T _{STARTIMO} | IMO startup time | – | – | 7 | μs | Guaranteed by characterization |
| SID229 | T _{JITRMSIMO} | RMS jitter at 48 MHz | – | 145 | – | ps | Guaranteed by characterization |
| F _{IMO} | – | IMO frequency | 24 | – | 48 | MHz | – |

Internal Low-Speed Oscillator
Table 22. ILO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|---------------------------------|-----|-----|------|-------|--------------------------------|
| SID231 | I _{ILO} | ILO operating current at 32 kHz | – | 0.3 | 1.05 | μA | Guaranteed by Characterization |
| SID233 | I _{ILOLEAK} | ILO leakage current | – | 2 | 15 | nA | Guaranteed by Design |

Table 23. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|-----------------------|------------------|-----|-----|-----|-------|--------------------------------|
| SID234 | T _{STARTILO} | ILO startup time | – | – | 2 | ms | Guaranteed by characterization |
| SID236 | T _{ILODUTY} | ILO duty cycle | 40 | 50 | 60 | % | Guaranteed by characterization |
| SID.CLK#5 | F _{ILO} | ILO Frequency | 20 | 40 | 80 | kHz | – |

Power Down
Table 24. PD DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|----------------|---|------|------|------|-------|--|
| SID.PD.1 | Rp_std | DFP CC termination for default USB Power | 64 | 80 | 96 | μA | – |
| SID.PD.2 | Rp_1.5A | DFP CC termination for 1.5A power | 166 | 180 | 194 | μA | – |
| SID.PD.3 | Rp_3.0A | DFP CC termination for 3.0A power | 304 | 330 | 356 | μA | – |
| SID.PD.4 | Rd | UFP CC termination | 4.59 | 5.1 | 5.61 | kΩ | – |
| SID.PD.5 | Rd_DB | UFP Dead Battery CC termination on RD1 and CC2 | 4.08 | 5.1 | 6.12 | kΩ | All supplies forced to 0 V and 0.6 V applied at RD1 or CC2 |
| SID.PD.6 | R _A | Power cable termination | 0.8 | 1.0 | 1.2 | kΩ | All supplies forced to 0 V and 0.2 V applied at V _{CONN1} or V _{CONN2} |
| SID.PD.7 | Ra_OFF | Power cable termination - Disabled | 0.4 | 0.75 | – | MΩ | 2.7 V applied at V _{CONN1} or V _{CONN2} with R _A disabled |
| SID.PD.8 | Rleak_1 | V _{CONN} leaker for 0.1-μF load | – | – | 216 | kΩ | Managed Active Cable (MAC) discharge |
| SID.PD.9 | Rleak_2 | V _{CONN} leaker for 0.5-μF load | – | – | 41.2 | kΩ | |
| SID.PD.10 | Rleak_3 | V _{CONN} leaker for 1.0-μF load | – | – | 19.6 | kΩ | |
| SID.PD.11 | Rleak_4 | V _{CONN} leaker for 2.0-μF load | – | – | 9.8 | kΩ | |
| SID.PD.12 | Rleak_5 | V _{CONN} leaker for 5.0-μF load | – | – | 4.1 | kΩ | |
| SID.PD.13 | Rleak_6 | V _{CONN} leaker for 10-μF load | – | – | 2.0 | kΩ | |
| SID.PD.14 | Ileak | Leaker on V _{CONN1} and V _{CONN2} for discharge upon cable detach | 150 | – | – | μA | – |

Analog to Digital Converter

Table 25. ADC DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|------------|----------------------------|------|-----|-----|-------|--------------------------------|
| SID.ADC.1 | Resolution | ADC resolution | – | 8 | – | bits | Guaranteed by characterization |
| SID.ADC.2 | INL | Integral non-linearity | –1.5 | – | 1.5 | LSB | Guaranteed by characterization |
| SID.ADC.3 | DNL | Differential non-linearity | –2.5 | – | 2.5 | LSB | Guaranteed by characterization |
| SID.ADC.4 | Gain Error | Gain error | –1 | – | 1 | LSB | Guaranteed by characterization |

Table 26. ADC AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|-----------|--|-----|-----|-----|-------|--------------------------------|
| SID.ADC.5 | SLEW_Max | Rate of change of sampled voltage signal | – | – | 3 | V/ms | Guaranteed by characterization |

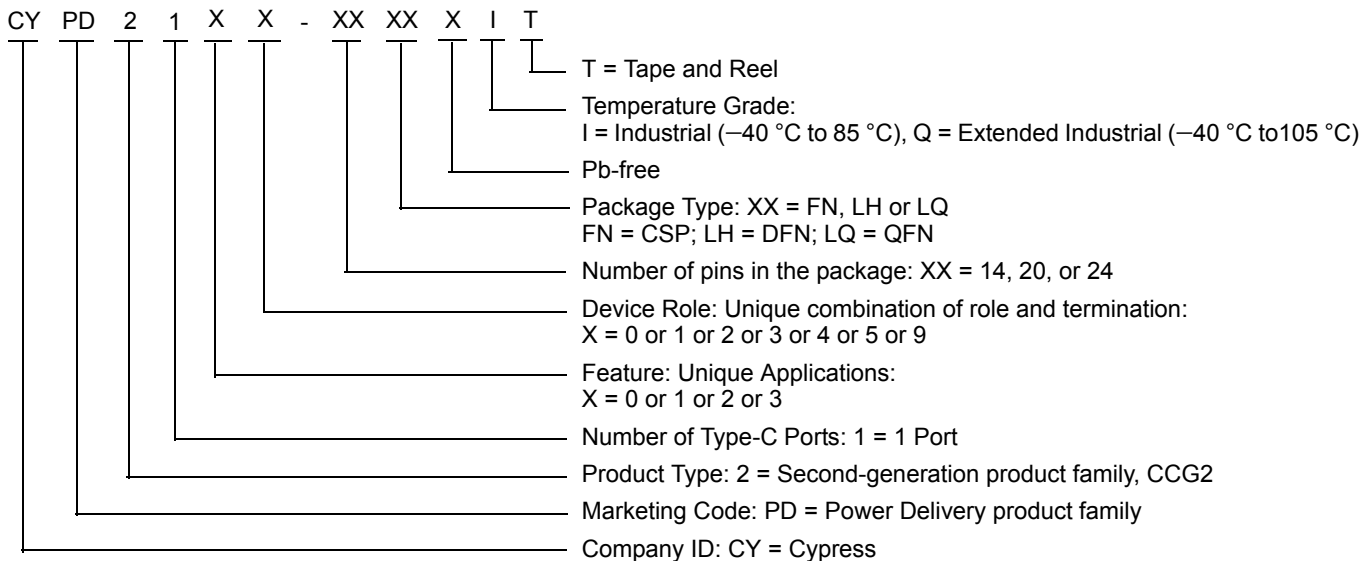
Ordering Information

The EZ-PD CCG2 part numbers and features are listed in [Table 27](#).

Table 27. EZ-PD CCG2 Ordering Information

| Part Number | Application | Type-C Ports | Termination Resistor | Role | Package |
|------------------|------------------------------|--------------|---|--------------|-------------|
| CYPD2103-20FNXIT | Cable | 1 | R _A ^[4] | Cable | 20-ball CSP |
| CYPD2103-14LHXIT | Cable | 1 | R _A ^[4] | Cable | 14-pin DFN |
| CYPD2104-20FNXIT | Accessory | 1 | R _D ^[5] | Accessory | 20-ball CSP |
| CYPD2105-20FNXIT | Active Cable | 1 | R _A ^[4] | Active Cable | 20-ball CSP |
| CYPD2119-24LQXIT | C-DP | 1 | R _D ^[5] | UFP | 24-pin QFN |
| CYPD2120-24LQXIT | C-HDMI | 1 | R _D ^[5] | UFP | 24-pin QFN |
| CYPD2121-24LQXIT | Dock/Monitor Upstream port | 1 | R _P ^[6] , R _D ^[5] | DRP | 24-pin QFN |
| CYPD2122-20FNXIT | Tablet | 1 | R _P ^[6] , R _D ^[5] | DRP | 20-ball CSP |
| CYPD2122-24LQXIT | Notebook | 1 | R _P ^[6] , R _D ^[5] | DRP | 24-pin QFN |
| CYPD2125-24LQXIT | Dock/Monitor Downstream port | 1 | R _P ^[6] | DFP | 24-pin QFN |
| CYPD2134-24LQXIT | DFP | 1 | R _P ^[6] | DFP | 24-pin QFN |
| CYPD2134-24LQXQT | DFP | 1 | R _P ^[6] | DFP | 24-pin QFN |

Ordering Code Definitions



Notes

4. Termination resistor denoting an EMCA.
5. Termination resistor denoting an accessory or upstream facing port.
6. Termination resistor denoting a downstream facing port.

Packaging

Table 28. Package Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------------|---|---------------------|-----|-----|-----|-------|
| T _A | Operating ambient temperature | Industrial | -40 | 25 | 85 | °C |
| | | Extended Industrial | | | 105 | °C |
| T _J | Operating junction temperature | Industrial | -40 | - | 100 | °C |
| | | Extended Industrial | | | 125 | °C |
| T _{JA} | Package θ _{JA} (20-ball WLCSP) | - | - | 66 | - | °C/W |
| T _{JC} | Package θ _{JC} (20-ball WLCSP) | - | - | 0.7 | - | °C/W |
| T _{JA} | Package θ _{JA} (14-pin DFN) | - | - | 31 | - | °C/W |
| T _{JC} | Package θ _{JC} (14-pin DFN) | - | - | 59 | - | °C/W |
| T _{JA} | Package θ _{JA} (24-pin QFN) | - | - | 22 | - | °C/W |
| T _{JC} | Package θ _{JC} (24-pin QFN) | - | - | 29 | - | °C/W |

Table 29. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time within 5 °C of Peak Temperature |
|---------------|--------------------------|--|
| 20-ball WLCSP | 260 °C | 30 seconds |
| 14-pin DFN | 260 °C | 30 seconds |
| 24-pin QFN | 260 °C | 30 seconds |

Table 30. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|---------------|-------|
| 20-ball WLCSP | MSL 1 |
| 14-pin DFN | MSL 3 |
| 24-pin QFN | MSL 3 |

Figure 15. 20-ball WLCSP (1.63 × 2.03 × 0.55 mm) FN20B Package Outline, 001-95010

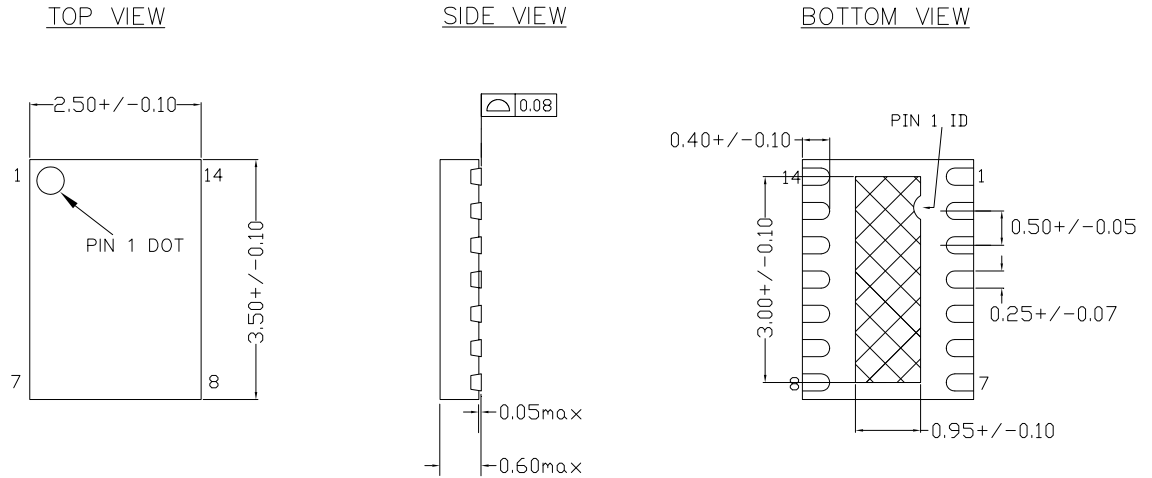


NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-95010 *A

Figure 16. 14-pin DFN (2.5 × 3.5 × 0.6 mm), LH14A, 0.95 × 3.00 E-Pad (Sawn) Package Outline, 001-96312



NOTES :

1. HATCH AREA IS SOLDERABLE EXPOSED METAL
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-96312 **

Figure 17. 24-Pin QFN (4 × 4 × 0.55 mm), LQ24A, 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937



NOTES :

1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Acronyms

Table 31. Acronyms Used in this Document

| Acronym | Description |
|--------------------------|---|
| ADC | analog-to-digital converter |
| API | application programming interface |
| ARM® | advanced RISC machine, a CPU architecture |
| CC | configuration channel |
| CCG2 | Cable Controller Generation 2 |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| CS | current sense |
| DFP | downstream facing port |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DRP | dual role port |
| EEPROM | electrically erasable programmable read-only memory |
| EMCA | a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output |
| IC | integrated circuit |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| I/O | input/output, see also GPIO |
| LVD | low-voltage detect |
| LVTTTL | low-voltage transistor-transistor logic |
| MCU | microcontroller unit |
| NC | no connect |
| NMI | nonmaskable interrupt |

Table 31. Acronyms Used in this Document (continued)

| Acronym | Description |
|---------|--|
| NVIC | nested vectored interrupt controller |
| opamp | operational amplifier |
| OCP | overcurrent protection |
| OVP | overvoltage protection |
| PCB | printed circuit board |
| PD | power delivery |
| PGA | programmable gain amplifier |
| PHY | physical layer |
| POR | power-on reset |
| PRES | precise power-on reset |
| PSoC® | Programmable System-on-Chip™ |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RX | receive |
| SAR | successive approximation register |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SPI | Serial Peripheral Interface, a communications protocol |
| SRAM | static random access memory |
| SWD | serial wire debug, a test protocol |
| TX | transmit |
| Type-C | a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| USB | Universal Serial Bus |
| USBIO | USB input/output, CCG2 pins used to connect to a USB port |
| XRES | external reset I/O pin |

Document Conventions

Units of Measure

Table 32. Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------|
| °C | degrees Celsius |
| Hz | hertz |
| KB | 1024 bytes |
| kHz | kilohertz |
| kΩ | kilo ohm |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| μA | microampere |
| μF | microfarad |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| V | volt |

Document History Page

| Description Title: EZ-PD™ CCG2 Datasheet USB Type-C Port Controller | | | | |
|---|---------|-----------------|-----------------|---|
| Document Number: 001-93912 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *E | 4680071 | GAYA | 03/07/2015 | Release to web |
| *F | 4718374 | AKN | 04/09/2015 | Added 24-pin QFN pin and package information. Added DRP and DFP Application diagrams |
| *G | 4774142 | AKN | 06/15/2015 | Changed datasheet status from Preliminary to Final. Updated Logic Block Diagram. Changed number of GPIOs to 10 and added a note about the number of GPIOs varying depending on the package. Updated Power and Digital Peripherals section. Updated Application diagrams. Added SID.PWR#1_A parameter. Added CYPD2122-20FNXIT part in Ordering Information. Removed Errata. |
| *H | 4979175 | VGT | 10/23/2015 | Updated Figure 1 and Figure 5. Added VCC_ABS spec and updated the SID.ADC.4 parameter. Added "Guaranteed by characterization" note for the following specs: SID.GIO#16, SID.GIO#17, SID.XRES#3, SID 160 to SID 172A, SID 2226, SID 229, SID.ADC.1 to SID.ADC.5. |
| *I | 5028128 | VGT | 12/04/2015 | Updated Application Diagrams : Added Figure 12 . Added Figure 13 . Added Figure 14 . Updated Ordering Information . Added part numbers CYPD2119-24LQXIT, CYPD2120-24LQXIT, CYPD2121-24LQXIT, CYPD2125-24LQXIT. |
| *J | 5186972 | VGT | 03/28/2016 | Updated temperature ranges in Features . Updated Table 28 . Updated Ordering Information . |

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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331