

NLSF308

Quad 2-Input AND Gate

The NLSF308 is an advanced high speed CMOS 2-input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: $t_{PD} = 4.3 \text{ ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2.0 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8 \text{ V}$ (Max)
- Function Compatible with Other Standard Logic Families
- QFN-16 Package
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V;
Machine Model; > 200 V
- Chip Complexity: 24 FETs or 6 Equivalent Gates
- Pb-Free Package is Available*

FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |



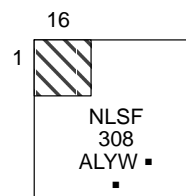
ON Semiconductor®

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**QFN-16
MN SUFFIX
CASE 485G**

MARKING DIAGRAM



NLSF308 = Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package
 (Note: Microdot may be in either location)

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|---------------------|--------------------|
| NLSF308MNR2 | QFN-16 | 3000 / Tape & Reel |
| NLSF308MNR2G | QFN-16 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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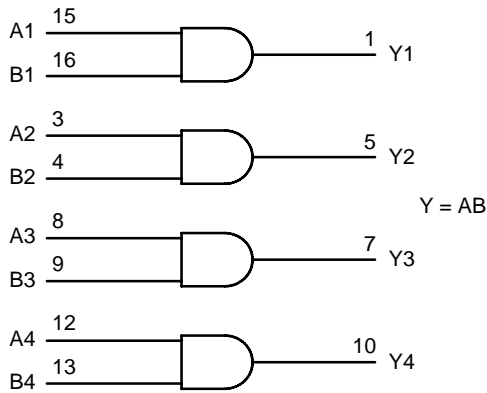


Figure 1. LOGIC DIAGRAM

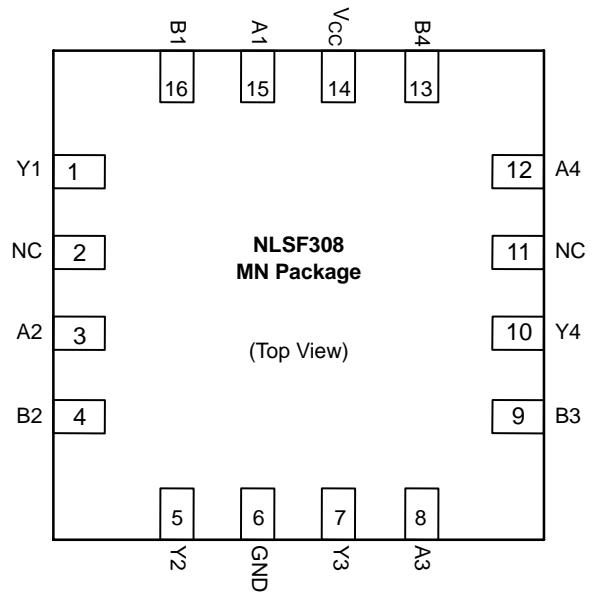


Figure 2. PIN ASSIGNMENT (QFN-16)

MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|--|-----------|------------------------|-------------|
| DC Supply Voltage | V_{CC} | -0.5 to + 7.0 | V |
| DC Input Voltage | V_{in} | -0.5 to + 7.0 | V |
| DC Output Voltage | V_{out} | -0.5 to $V_{CC} + 0.5$ | V |
| Input Diode Current | I_{IK} | -20 | mA |
| Output Diode Current | I_{OK} | ± 20 | mA |
| DC Output Current, per Pin | I_{out} | ± 25 | mA |
| DC Supply Current, V_{CC} and GND Pins | I_{CC} | ± 50 | mA |
| Power Dissipation in Still Air | P_D | 450 | mW |
| Storage Temperature | T_{stg} | -65 to + 150 | $^{\circ}C$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|--------------------------|------------|-----|----------|-------------|
| DC Supply Voltage | V_{CC} | 2.0 | 5.5 | V |
| DC Input Voltage | V_{in} | 0 | 5.5 | V |
| DC Output Voltage | V_{out} | 0 | V_{CC} | V |
| Operating Temperature | T_A | -40 | + 85 | $^{\circ}C$ |
| Input Rise and Fall Time | t_r, t_f | 0 | 100 | ns/V |
| | | 0 | 20 | |

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DC ELECTRICAL CHARACTERISTICS

| Parameter | Test Conditions | Symbol | V _{CC} V | T _A = 25°C | | | T _A = - 40 to 85°C | | Unit |
|-----------------------------------|---|-----------------|----------------------|-------------------------------|-------------------|-------------------------------|-------------------------------|-------------------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| Minimum High-Level Input Voltage | | V _{IH} | 2.0 3.0 to 5.5 | 1.50 V _{CC} x 0.7 | | | 1.50 V _{CC} x 0.7 | | V |
| Maximum Low-Level Input Voltage | | V _{IL} | 2.0 3.0 to 5.5 | | | 0.50 V _{CC} x 0.3 | | 0.50 V _{CC} x 0.3 | V |
| Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OH} = -50 μA | V _{OH} | 2.0 3.0 4.5 | 1.9 2.9 4.4 | 2.0 3.0 4.5 | | 1.9 2.9 4.4 | | V |
| | V _{in} = V _{IH} or V _{IL} I _{OH} = -4 mA, I _{OH} = -8 mA | | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | |
| Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OL} = 50 μA | V _{OL} | 2.0 3.0 4.5 | | 0.0 0.0 0.0 | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | V |
| | V _{in} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | |
| Maximum Input Leakage Current | V _{in} = 5.5 V or GND | | 0 to 5.5 | | | ± 0.1 | | ± 1.0 | μA |
| Maximum Quiescent Supply Current | V _{in} = V _{CC} or GND | | 5.5 | | | 2.0 | | 20.0 | μA |

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

| Parameter | Test Conditions | Symbol | T _A = 25°C | | | T _A = - 40 to 85°C | | Unit | |
|--|--|--|---|------------|-------------|-------------------------------|--------------|------|----|
| | | | Min | Typ | Max | Min | Max | | |
| Maximum Propagation Delay, A or B to Y | V _{CC} = 3.3 ± 0.3 V, C _L = 15 pF, C _L = 50 pF | t _{PLH} , t _{PHL} | | 6.2 8.7 | 8.8 12.3 | 1.0 1.0 | 10.5 14.0 | ns | |
| | V _{CC} = 5.0 ± 0.5 V, C _L = 15 pF, C _L = 50 pF | | | 4.3 5.8 | 5.9 7.9 | 1.0 1.0 | 7.0 9.0 | | |
| Maximum Input Capacitance | | C _{in} | | 4 | 10 | | 10 | pF | |
| Power Dissipation Capacitance (Note 1) | | C _{PD} | Typical @ 25°C, V _{CC} = 5.0 V | | | | | 18 | pF |

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per gate). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, C_L = 50 pF, V_{CC} = 5.0 V)

| Characteristic | Symbol | T _A = 25°C | | Unit |
|--|------------------|-----------------------|------|------|
| | | Typ | Max | |
| Quiet Output Maximum Dynamic V _{OL} | V _{OLP} | 0.3 | 0.8 | V |
| Quiet Output Minimum Dynamic V _{OL} | V _{OLV} | -0.3 | -0.8 | V |
| Minimum High Level Dynamic Input Voltage | V _{IHD} | | 3.5 | V |
| Maximum Low Level Dynamic Input Voltage | V _{ILD} | | 1.5 | V |

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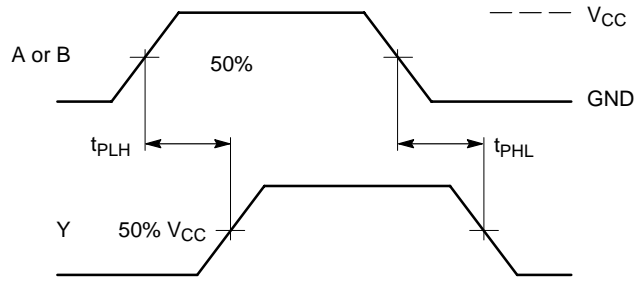
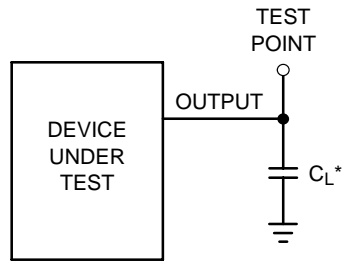


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

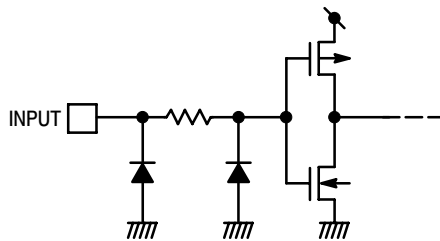
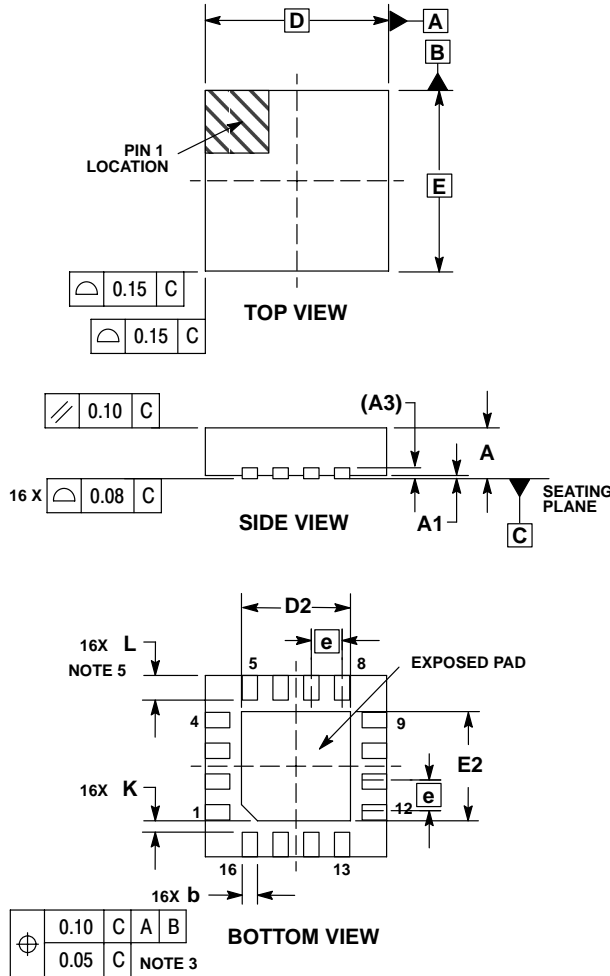


Figure 5. Input Equivalent Circuit

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PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G-01
ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 3.00 | BSC |
| D2 | 1.65 | 1.85 |
| E | 3.00 | BSC |
| E2 | 1.65 | 1.85 |
| e | 0.50 | BSC |
| K | 0.18 | TYP |
| L | 0.30 | 0.50 |

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