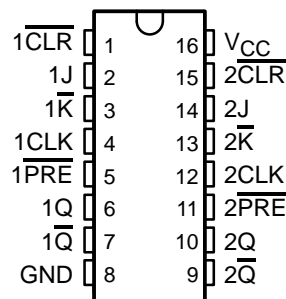


# CD54AC109, CD74AC109 DUAL J- $\bar{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **$\pm 24$ -mA Output Drive Current**  
– Fanout to 15 F Devices
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

CD54AC109 . . . F PACKAGE  
CD74AC109 . . . E OR M PACKAGE  
(TOP VIEW)



## description/ordering information

The 'AC109 devices contain two independent J- $\bar{K}$  positive-edge-triggered flip-flops. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the J and  $\bar{K}$  inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and  $\bar{K}$  inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding  $\bar{K}$  and tying J high. They also can perform as D-type flip-flops if J and  $\bar{K}$  are tied together.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC109E	CD74AC109E
	SOIC – M	Tape and reel	CD74AC109M96	AC109M
	CDIP – F	Tube	CD54AC109F3A	CD54AC109F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# CD54AC109, CD74AC109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

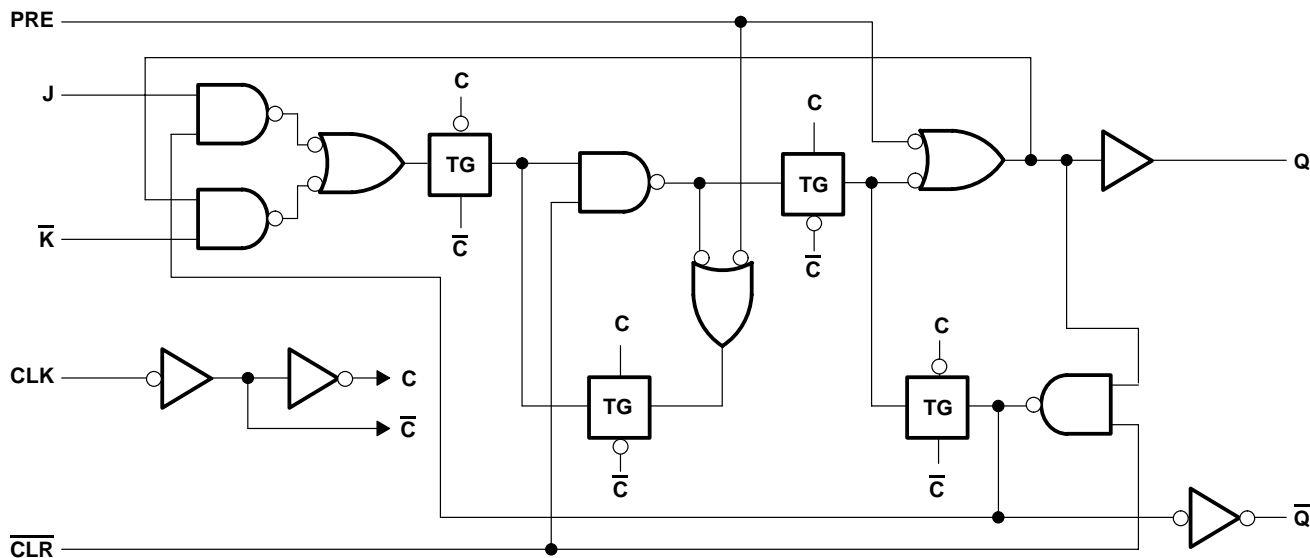
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FUNCTION TABLE  
(each flip-flop)

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\overline{\text{K}}$	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q <sub>0</sub>	$\overline{\text{Q}}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	$\overline{\text{Q}}_0$

† Unpredictable and unstable condition if both  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  go low simultaneously

## logic diagram, each flip-flop (positive logic)



# CD54AC109, CD74AC109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ V or $V_I > V_{CC}$ ) (see Note 1) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ V or $V_O > V_{CC}$ ) (see Note 1) .....	±50 mA
Continuous output current, $I_O$ ( $V_O > 0$ V or $V_O < V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package .....	67°C/W
M package .....	73°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 1.5$ V		1.2	1.2	1.2		V
		$V_{CC} = 3$ V		2.1	2.1	2.1		
		$V_{CC} = 5.5$ V		3.85	3.85	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.5$ V			0.3		0.3	V
		$V_{CC} = 3$ V			0.9		0.9	
		$V_{CC} = 5.5$ V			1.65		1.65	
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 4.5$ V to 5.5 V		–24	–24	–24	–24	mA
$I_{OL}$	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V		24	24	24	24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.5$ V to 3 V		50	50	50	50	ns/V
		$V_{CC} = 3.6$ V to 5.5 V		20	20	20	20	

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**CD54AC109, CD74AC109**  
**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS**  
**WITH CLEAR AND PRESET**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	1.5 V	1.4		1.4		1.4		V
			3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
		I <sub>OH</sub> = -4 mA	3 V	2.58		2.4		2.48		
		I <sub>OH</sub> = -24 mA	4.5 V	3.94		3.7		3.8		
		I <sub>OH</sub> = -50 mA†	5.5 V			3.85				
I <sub>OH</sub> = -75 mA†	5.5 V					3.85				
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	1.5 V		0.1		0.1		0.1	V
			3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
		I <sub>OL</sub> = 12 mA	3 V		0.36		0.5		0.44	
		I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5		0.44	
		I <sub>OL</sub> = 50 mA†	5.5 V				1.65			
I <sub>OL</sub> = 75 mA†	5.5 V						1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		5.5 V		±0.1		±1		±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		5.5 V		4		80		40	μA
C <sub>i</sub>					10		10		10	pF

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 1.5 V (unless otherwise noted)**

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		8		9	MHz
t <sub>w</sub>	Pulse duration	CLK high or low		63	55	ns
		CLR or PRE low		56	49	
t <sub>su</sub>	Setup time, before CLK↑	J or K̄		69	61	ns
t <sub>h</sub>	Hold time, after CLK↑	J or K̄		0	0	ns
t <sub>rec</sub>	Recovery time, before CLK↑	CLR↑ or PRE↑		31	27	ns



# CD54AC109, CD74AC109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)**

			-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		71		81		MHz
$t_w$	Pulse duration	CLK high or low	7		6		ns
		$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$	6.3		5.5		
$t_{\text{su}}$	Setup time, before CLK $\uparrow$	J or $\overline{\text{K}}$	7.7		6.8		ns
$t_h$	Hold time, after CLK $\uparrow$	J or $\overline{\text{K}}$	0		0		ns
$t_{\text{rec}}$	Recovery time, before CLK $\uparrow$	$\overline{\text{CLR}}\uparrow$ or $\overline{\text{PRE}}\uparrow$	3.5		3.1		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted)**

			-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency		100		114		MHz
$t_w$	Pulse duration	CLK high or low	5		4.4		ns
		$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$	4.5		3.9		
$t_{\text{su}}$	Setup time, before CLK $\uparrow$	J or $\overline{\text{K}}$	5.5		4.8		ns
$t_h$	Hold time, after CLK $\uparrow$	J or $\overline{\text{K}}$	0		0		ns
$t_{\text{rec}}$	Recovery time, before CLK $\uparrow$	$\overline{\text{CLR}}\uparrow$ or $\overline{\text{PRE}}\uparrow$	2.5		2.2		ns

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 1.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			8		9		MHz
$t_{\text{PLH}}$	CLK	Q or $\overline{\text{Q}}$	129		117		ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		153		139		
$t_{\text{PHL}}$	CLK	Q or $\overline{\text{Q}}$	129		117		ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		153		139		

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{\text{max}}$			71		81		MHz
$t_{\text{PLH}}$	CLK	Q or $\overline{\text{Q}}$	3.6	14.4	3.7	13.1	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		4.3	17.1	4.4	15.5	
$t_{\text{PHL}}$	CLK	Q or $\overline{\text{Q}}$	3.6	14.4	3.7	13.1	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		4.3	17.1	4.4	15.5	

**CD54AC109, CD74AC109**  
**DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS**  
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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$f_{max}$			100		114		MHz
$t_{PLH}$	CLK	Q or $\bar{Q}$	2.6	10.3	2.7	9.4	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		3.1	12.2	3.2	11.1	
$t_{PHL}$	CLK	Q or $\bar{Q}$	2.6	10.3	2.7	9.4	ns
	$\overline{\text{CLR}}$ or $\overline{\text{PRE}}$		3.1	12.2	3.2	11.1	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

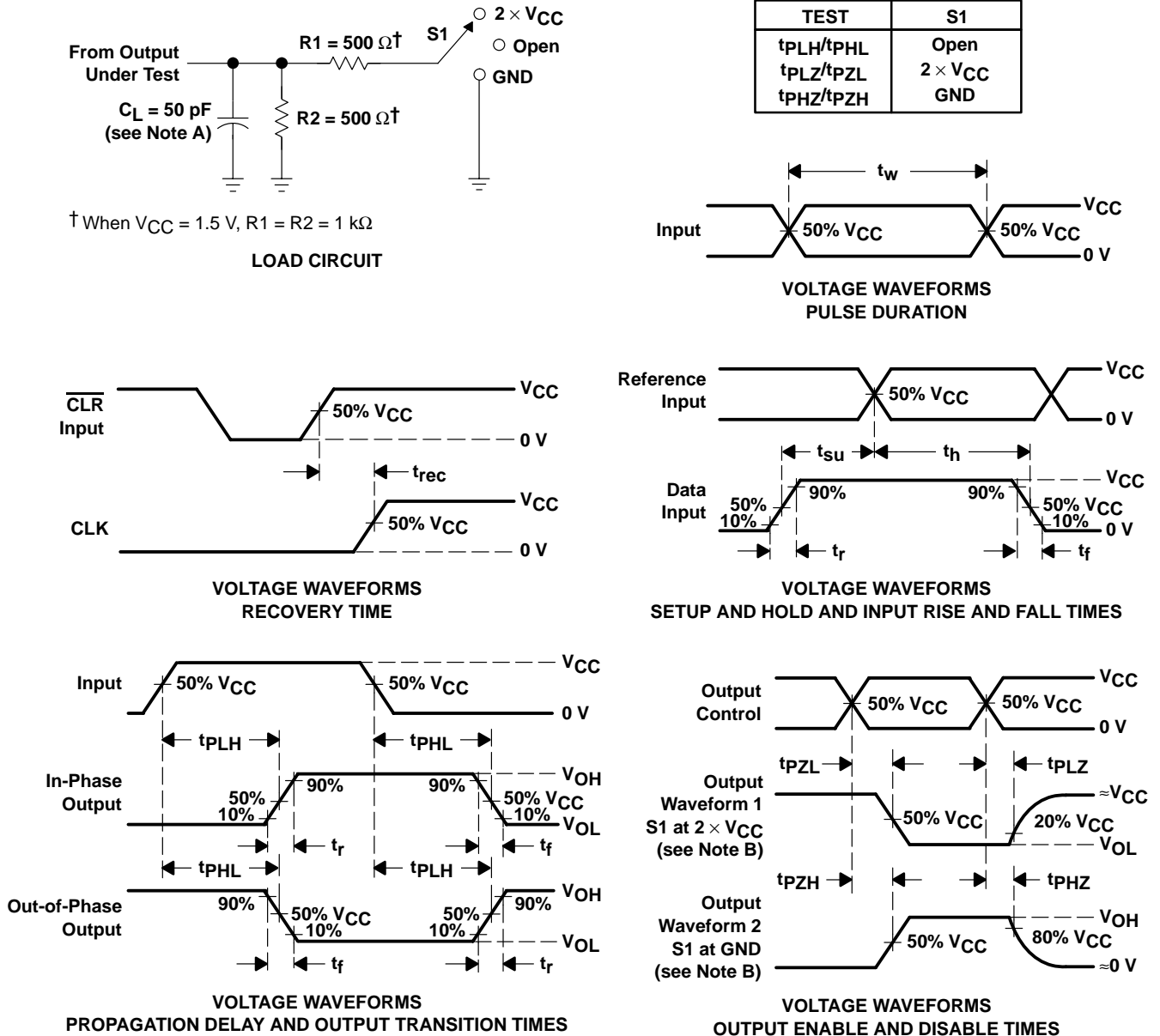
PARAMETER		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	56	pF



# CD54AC109, CD74AC109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 3\text{ ns}$ ,  $t_f = 3\text{ ns}$ . Phase relationships between waveforms are arbitrary.
  - D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - E. The outputs are measured one at a time with one input transition per measurement.
  - F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - H.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - I. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD54AC109F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54AC109F3A	<a href="#">Samples</a>
CD74AC109E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC109E	<a href="#">Samples</a>
CD74AC109EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC109E	<a href="#">Samples</a>
CD74AC109M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC109M	<a href="#">Samples</a>
CD74AC109M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC109M	<a href="#">Samples</a>
CD74AC109M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC109M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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**OTHER QUALIFIED VERSIONS OF CD54AC109, CD74AC109 :**

- Catalog: [CD74AC109](#)
- Military: [CD54AC109](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC109M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC109M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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