

Phase Control Thyristors (Hockey PUK Version), 790 A


TO-200AC (B-PUK)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AC (B-PUK)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912


**RoHS
COMPLIANT**

TYPICAL APPLICATIONS

- DC motor control
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY

Package	TO-200AC (B-PUK)
Diode variation	Single SCR
$I_{T(AV)}$	790 A
V_{DRM}/V_{RRM}	2000 V, 2200 V, 2400 V
V_{TM}	2.07 V
I_{GT}	100 mA
T_J	-40 °C to 125 °C

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		790	A
	T_{hs}	55	°C
$I_{T(RMS)}$		1557	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	10 100	A
	60 Hz	10 700	
I^2t	50 Hz	510	kA ² s
	60 Hz	475	
V_{DRM}/V_{RRM}		2000 to 2400	V
t_q	Typical	200	µs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST650C..L	20	2000	2100	80
	22	2200	2300	
	24	2400	2500	



ABSOLUTE MAXIMUM RATINGS							
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS	
Maximum average on-state current at heatsink temperature	I _{T(AV)}	180° conduction, half sine wave Double side (single side) cooled			790 (324)	A	
					55 (85)	°C	
Maximum RMS on-state current	I _{T(RMS)}	DC at 25 °C heatsink temperature double side cooled			1857	A	
Maximum peak, one-cycle non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	10 100		
		t = 8.3 ms			10 700		
		t = 10 ms	100 % V _{RRM} reapplied		8600		
		t = 8.3 ms			9150		
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		510		kA ² s
		t = 8.3 ms			475		
		t = 10 ms	100 % V _{RRM} reapplied		370		
		t = 8.3 ms			347		
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			5100	kA ² √s	
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			1.04	V	
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.13		
Low level value of on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.61	mΩ	
High level value of on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			0.35		
Maximum on-state voltage	V _{TM}	I _{pk} = 1700 A, T _J = T _J maximum, t _p = 10 ms sine pulse			2.07	V	
Maximum holding current	I _H	T _J = 25 °C, anode supply 12 V resistive load			600	mA	
Typical latching current	I _L				1000		

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω, t _r ≤ 1 μs T _J = T _J maximum, anode voltage ≤ 80 % V _{DRM}	1000	A/μs
Typical delay time	t _d	Gate current 1 A, di _g /dt = 1 A/μs V _d = 0.67 % V _{DRM} , T _J = 25 °C	1.0	μs
Maximum turn-off time	t _q	I _{TM} = 750 A, T _J = T _J maximum, di/dt = 60 A/μs V _R = 50, dV/dt = 20 V/μs, Gate 0 V 100 Ω, t _b = 500 μs	200	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}			500 V/μs
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied			80 mA



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				typ.	max.	
Maximum peak gate power	P _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		10.0		W
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum, f = 50 Hz, d% = 50		2.0		
Maximum peak positive gate current	I _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		3.0		A
Maximum peak positive gate voltage	+ V _{GM}			20		V
Maximum peak negative gate voltage	- V _{GM}			5.0		
DC gate current required to trigger	I _{GT}	T _J = -40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	200	-	mA
		T _J = 25 °C		100	200	
		T _J = 125 °C		50	-	
DC gate voltage required to trigger	V _{GT}	T _J = -40 °C		2.5	-	V
		T _J = 25 °C		1.8	3.0	
		T _J = 125 °C		1.1	-	
DC gate current not to trigger	I _{GD}	T _J = T _J maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V _{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating temperature range	T _J		-40 to 125	°C
Maximum storage temperature range	T _{Stg}		-40 to 150	
Maximum thermal resistance, junction to heatsink	R _{thJ-hs}	DC operation single side cooled	0.073	K/W
		DC operation double side cooled	0.031	
Maximum thermal resistance, case to heatsink	R _{thC-hs}	DC operation single side cooled	0.011	
		DC operation double side cooled	0.006	
Mounting force, ± 10 %			14 700 (1500)	N (kg)
Approximate weight			255	g
Case style		See dimensions - link at the end of datasheet	TO-200AC (B-PUK)	

ΔR_{thJ-hs} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	Single Side	Double Side	Single Side	Double Side		
180°	0.009	0.009	0.006	0.006	T _J = T _J maximum	K/W
120°	0.011	0.011	0.011	0.011		
90°	0.014	0.014	0.015	0.015		
60°	0.020	0.020	0.021	0.021		
30°	0.036	0.036	0.036	0.036		

Note

- The table above shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC

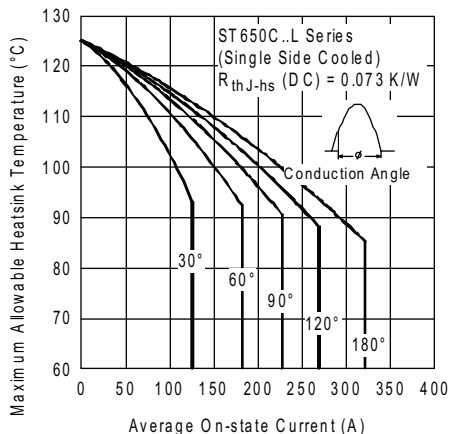


Fig. 1 - Current Ratings Characteristics

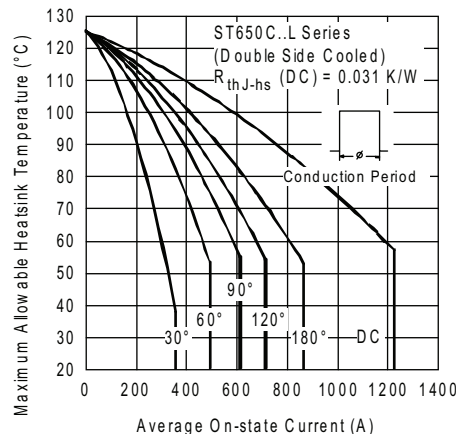


Fig. 4 - Current Ratings Characteristics

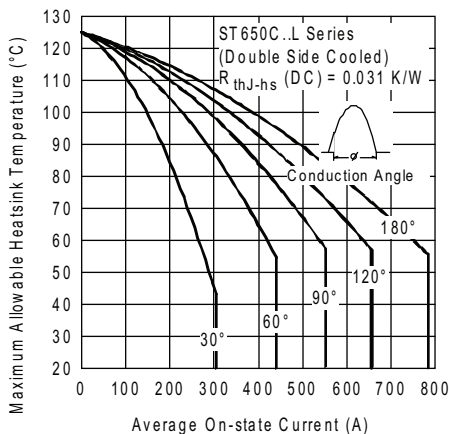


Fig. 2 - Current Ratings Characteristics

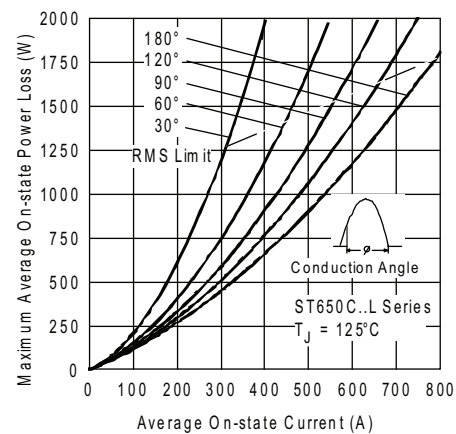


Fig. 5 - On-State Power Loss Characteristics

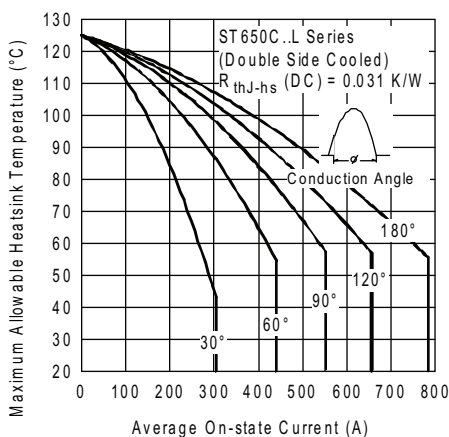


Fig. 3 - Current Ratings Characteristics

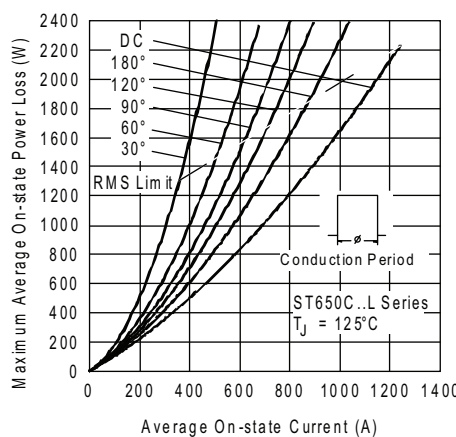


Fig. 6 - On-State Power Loss Characteristics

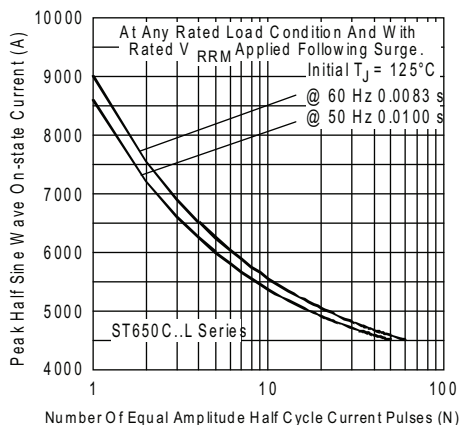


Fig. 7 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

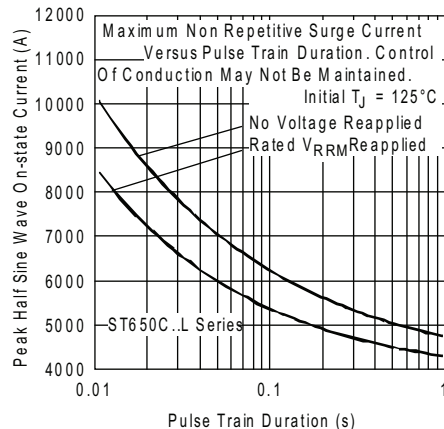


Fig. 8 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

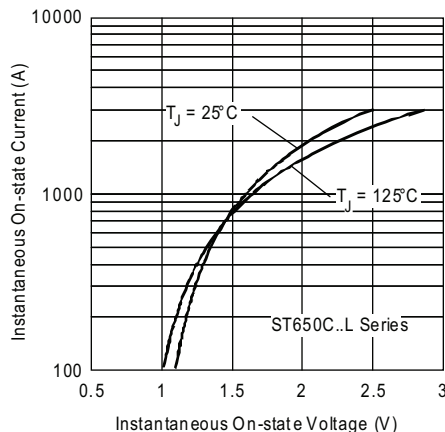


Fig. 9 - On-State Voltage Drop Characteristics

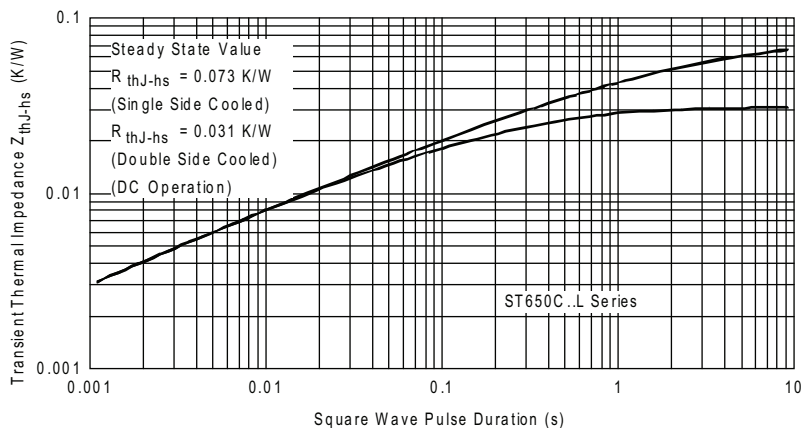


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

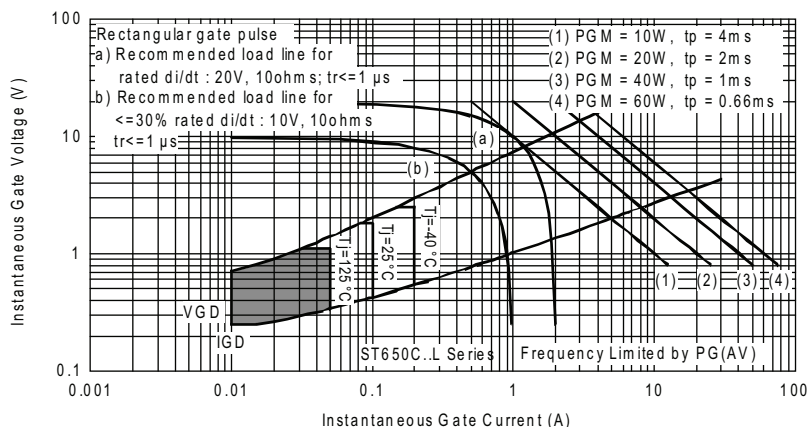


Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code

VS-	ST	65	0	C	24	L	1	-
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(1)

(2)

(3)

(4)

(5)

(6)

(7)

(8)

(9)

- 1** - Vishay Semiconductors product
- 2** - Thyristor
- 3** - Essential part number
- 4** - 0 = Converter grade
- 5** - C = Ceramic PUK
- 6** - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- 7** - L = PUK case TO-200AC (B-PUK)
- 8** - 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)
1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)
2 = Eyelet terminals (gate and auxiliary cathode soldered leads)
3 = Fast-on terminals (gate and auxiliary cathode soldered leads)
- 9** - Critical dV/dt : • None = 500 V/ μs (standard selection)
• L = 1000 V/ μs (special selection)

LINKS TO RELATED DOCUMENTS

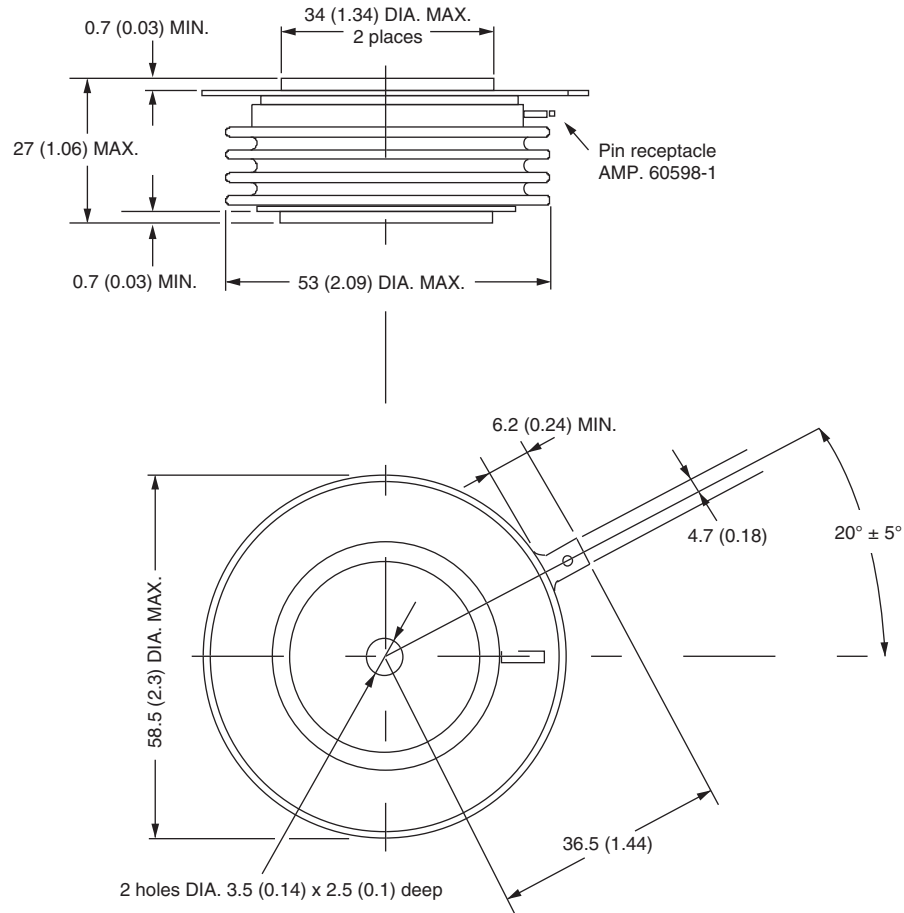
Dimensions

www.vishay.com/doc?95076

TO-200AC (B-PUK)

DIMENSIONS in millimeters (inches)

Creepage distance: 36.33 (1.430) minimum
Strike distance: 17.43 (0.686) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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