CS42L51

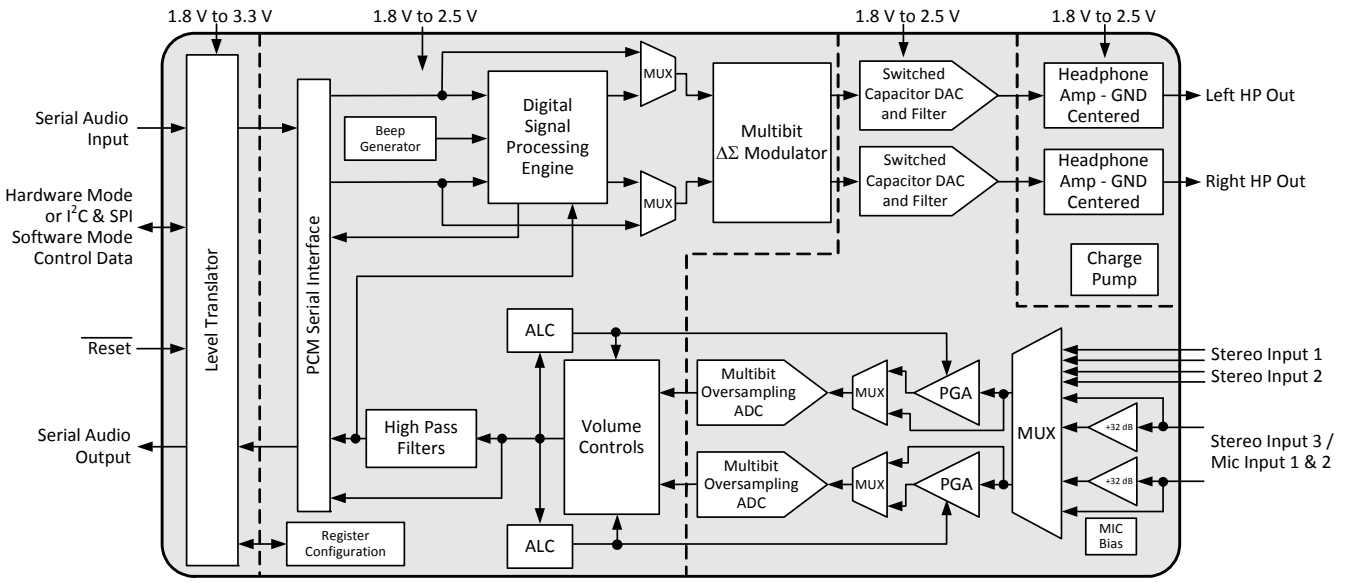
Low-Power, Stereo Codec with Headphone Amp

DIGITAL-TO-ANALOG FEATURES

- 98-dB dynamic range (A-weighted)
- -86-dB THD+N
- Headphone amplifier - GND centered
  - On-chip charge pump provides –VA_HP
  - No DC-blocking capacitor required
  - 46-mW power into stereo 16 Ω @ 1.8 V
  - 88-mW power into stereo 16 Ω @ 2.5 V
  - -75 dB THD+N
- Digital signal processing engine
  - Bass & treble tone control, de-emphasis
  - PCM + ADC mix with independent volume control
  - Master digital volume control
  - Soft ramp & zero-cross transitions
- Beep generator
  - Tone selections across two octaves
  - Separate volume control
  - Programmable on & off time intervals
  - Continuous, periodic or one-shot beep selections
- Programmable peak-detect and limiter
- Pop and click suppression

ANALOG-TO-DIGITAL FEATURES

- 98-dB dynamic range (A-weighted)
- -88-dB THD+N
- Analog gain controls
  - +32-dB or +16-dB mic preamplifiers
  - Analog programmable gain amplifier (PGA)
- +20-dB digital boost
- Programmable automatic level control (ALC)
  - Noise gate for noise suppression
  - Programmable threshold and attack/release rates
- Independent channel control
- Digital volume control
- High-pass filter disable for DC measurements
- Stereo 3:1 analog input MUX
- Dual mic inputs
  - Programmable, low noise mic bias levels
  - Differential mic mix for common mode noise rejection
- Very low 64 Fs oversampling clock reduces power consumption



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SYSTEM FEATURES

- 24-bit converters
- 4–96-kHz sample rate
- Multibit delta–sigma architecture
- Low power operation
  - Stereo playback: 12.93 mW @ 1.8 V
  - Stereo record and playback: 20.18 mW @ 1.8 V
- Variable power supplies
  - 1.8–2.5 V digital & analog
  - 1.8–3.3 V interface logic
- Power down management
  - ADC, DAC, codec, mic preamplifier, PGA
- Software Mode (I²C™ and SPI™ control)
- Hardware mode (stand-alone control)
- Digital routing/mixes:
  - Analog out = ADC + Digital In
  - Digital out = ADC + Digital In
  - Internal digital loopback
  - Mono mixes
- Flexible clocking options
  - Master or slave operation
  - High-impedance digital output option (for easy MUXing between the codec and other data sources)
  - Quarter-speed mode (i.e., Allows 8 kHz Fs while maintaining a flat noise floor up to 16 kHz)

APPLICATIONS

- HDD and flash-based portable audio players
- MD players/recorders
- PDAs
- Personal media players
- Portable game consoles
- Digital voice recorders
- Digital camcorders
- Digital cameras
- Smart phones

GENERAL DESCRIPTION

The CS42L51 is a highly integrated, 24-bit, 96-kHz, low power stereo codec. Based on multi-bit, delta-sigma modulation, it allows infinite sample rate adjustment between 4 kHz and 96 kHz. Both the ADC and DAC offer many features suitable for low power, portable system applications.

The ADC input path allows independent channel control of a number of features. An input multiplexer selects between line-level or microphone level inputs for each channel. The microphone input path includes a selectable programmable-gain pre-amplifier stage and a low noise MIC bias voltage supply. A PGA is available for line or microphone inputs and provides analog gain with soft ramp and zero-cross transitions. The ADC also features a digital volume attenuator with soft ramp transitions. A programmable ALC and Noise Gate monitor the input signals and adjust the volume levels appropriately.

The DAC output path includes a digital signal processing engine. Tone Control provides bass and treble adjustment of four selectable corner frequencies. The Mixer allows independent volume control for both the ADC mix and the PCM mix, as well as a master digital volume control for the analog output. All volume level changes may be configured to occur on soft ramp and zero-cross transitions. The DAC also includes de-emphasis, limiting functions and a beep generator delivering tones selectable across a range of two full octaves.

The stereo headphone amplifier is powered from a separate positive supply and the integrated charge pump provides a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates external DC-blocking capacitors.

In addition to its many features, the CS42L51 operates from a low-voltage analog and digital core, making this codec ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS42L51 is available in a 32-pin QFN package in both Commercial (-10 to +70° C) and Automotive grades (-40 to +85° C). The CDB42L51 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 83 for complete details.

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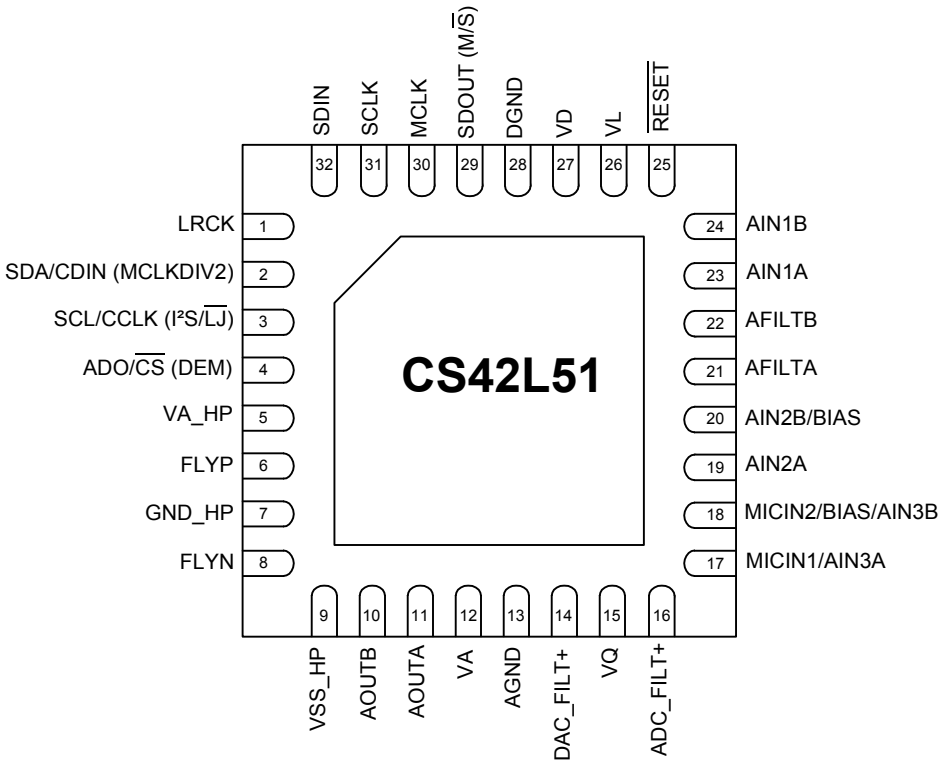
1. PIN DESCRIPTIONS - SOFTWARE (HARDWARE) MODE



Pin Name	#	Pin Description
LRCK	1	**Left Right Clock** (*Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SDA/CDIN (MCLKDIV2)	2	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C Mode. CDIN is the input data line for the control port interface in SPI Mode.
		MCLK Divide by 2 (*Input*) - Hardware Mode: Divides the MCLK by 2 prior to all internal circuitry.
SCL/CCLK (I²S/LJ)	3	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
		Interface Format Selection (*Input*) - Hardware Mode: Selects between I²S & Left-Justified interface formats for the ADC & DAC.
AD0/CS (DEM)	4	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** (*Input*) - AD0 is a chip address pin in I²C Mode; CS is the chip-select signal for SPI format.
		De-Emphasis *(Input)* - Hardware Mode: Enables/disables the de-emphasis filter.
VA_HP	5	**Analog Power For Headphone** *(Input)* **-** Positive power for the internal analog headphone section.
FLYP	6	**Charge Pump Cap Positive Node** *(Input)* **-** Positive node for the external charge pump capacitor.
GND_HP	7	**Analog Ground** (*Input*) - Ground reference for the internal headphone/charge pump section.
FLYN	8	**Charge Pump Cap Negative Node** *(Input)* **-** Negative node for the external charge pump capacitor.
VSS_HP	9	**Negative Voltage From Charge Pump** *(Output)* **-** Negative voltage rail for the internal analog headphone section.

AOUTB AOUTA	10 11	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table
VA	12	**Analog Power** (*Input*) - Positive power for the internal analog section.
AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
DAC_FILT+	14	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
VQ	15	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
ADC_FILT+	16	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
MICIN1/ AIN3A	17	**Microphone Input 1** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
MICIN2/ BIAS/AIN3B	18	**Microphone Input 2** (*Input/Output*) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AIN2A	19	**Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
AIN2B/BIAS	20	**Analog Input** (*Input/Output*) - The full-scale level is specified in the ADC Analog Characteristics specification table. This pin can also be configured as an output to provide a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
AFILTA AFILTB	21 22	**Filter Connection** (*Output*) - Filter connection for the ADC inputs.
AIN1A AIN1B	23 24	**Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
$\overline{\text{RESET}}$	25	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VL	26	**Digital Interface Power** (*Input*) - Determines the required signal level for the serial audio interface and host control port. Refer to the Recommended Operating Conditions for appropriate voltages.
VD	27	**Digital Power** (*Input*) - Positive power for the internal digital section.
DGND	28	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDOUT (M/$\overline{\text{S}}$)	29	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data. **Serial Port Master/Slave** (*Input/Output*) - Hardware Mode Startup Option: Selects between Master and Slave Mode for the serial port.
MCLK	30	**Master Clock** (*Input*) - Clock source for the delta-sigma modulators.
SCLK	31	**Serial Clock** *(Input/Output*) - Serial clock for the serial audio interface.
SDIN	32	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
Thermal Pad	-	Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 79.

1.1 Digital I/O Pin Characteristics

The logic level for each input should not exceed the maximum ratings for the VL power supply.

Pin Name SW/(HW)	I/O	Driver	Receiver
$\overline{\text{RESET}}$	Input	-	1.8 V - 3.3 V
SCL/CCLK ($I^2S/\overline{LJ}$)	Input	-	1.8 V - 3.3 V, with Hysteresis
SDA/CDIN (MCLKDIV2)	Input/Output	1.8 V - 3.3 V, CMOS/Open Drain	1.8 V - 3.3 V, with Hysteresis
AD0/$\overline{\text{CS}}$ (DEM)	Input	-	1.8 V - 3.3 V
MCLK	Input	-	1.8 V - 3.3 V
LRCK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SCLK	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDOUT ($M/\overline{S}$)	Input/Output	1.8 V - 3.3 V, CMOS	1.8 V - 3.3 V
SDIN	Input	-	1.8 V - 3.3 V

Table 1. I/O Power Rails

2. TYPICAL CONNECTION DIAGRAMS

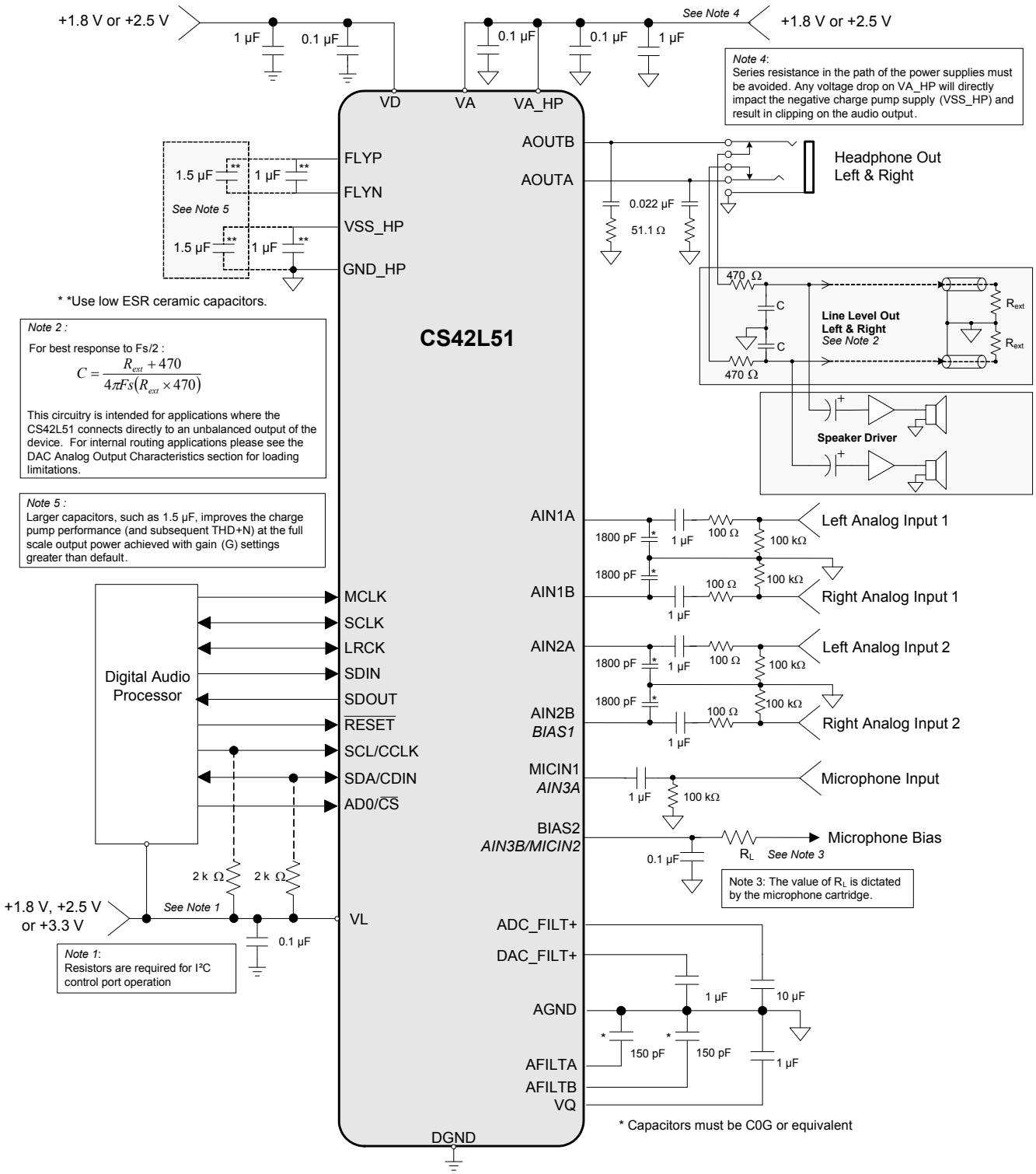


Figure 1. Typical Connection Diagram (Software Mode)

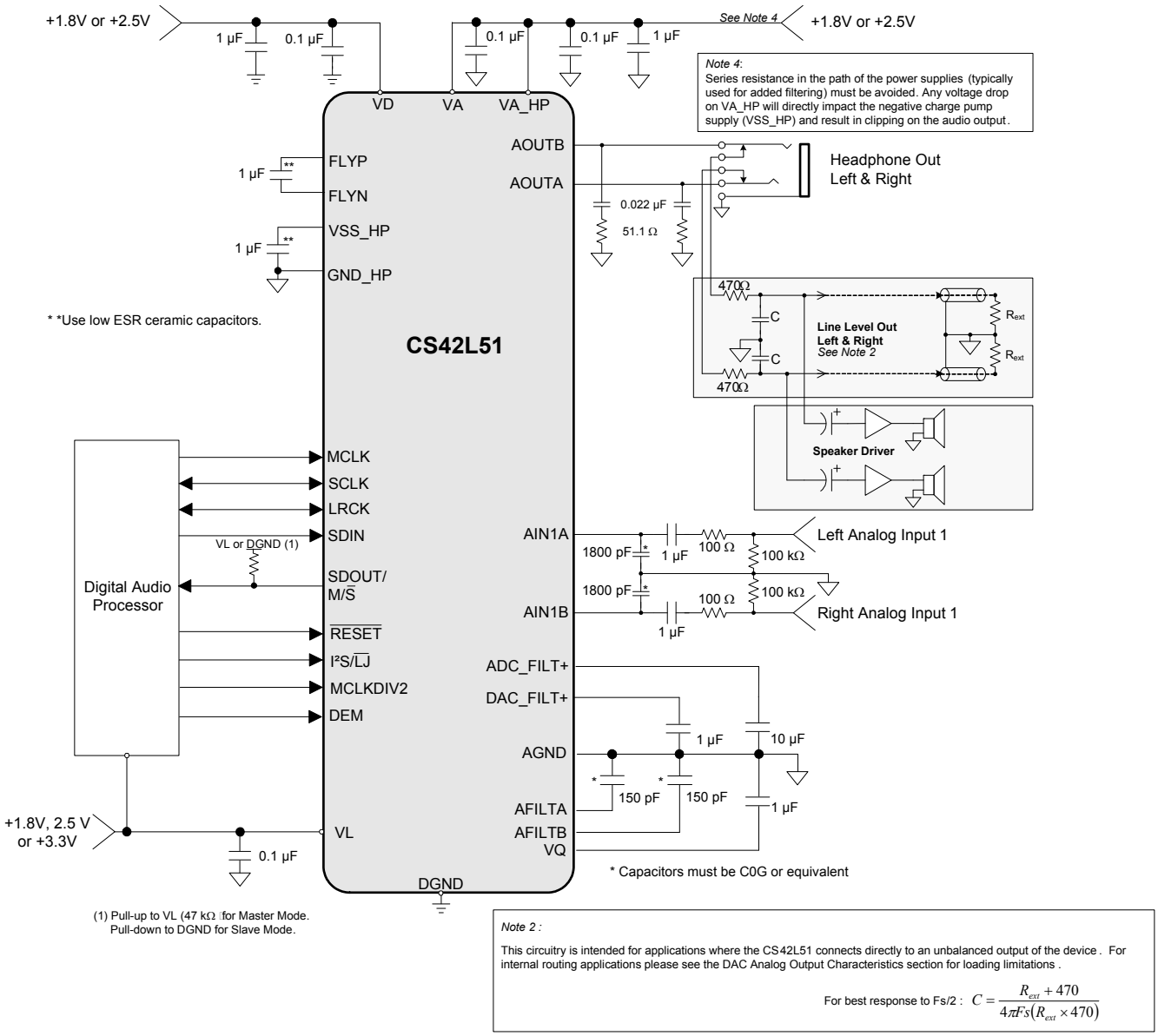


Figure 2. Typical Connection Diagram (Hardware Mode)

3. CHARACTERISTIC AND SPECIFICATION TABLES

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25° C.)

SPECIFIED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply (Note 1)				
Analog Core	VA	1.65	2.63	V
Headphone Amplifier	VA_HP	1.65	2.63	V
Digital Core	VD	1.65	2.63	V
Serial/Control Port Interface	VL	1.65	3.47	V
Ambient Temperature Commercial - CNZ Automotive - DNZ	T_A	-10 -40	+70 +85	°C °C

Note:

1. The device will operate properly over the full range of the analog, headphone amplifier, digital core and serial/control port interface supplies.

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply Analog Digital Serial/Control Port Interface	VA, VA_HP VD VL	-0.3 -0.3 -0.3	3.0 3.0 4.0	V V V
Input Current (Note 2)	I_{in}	-	±10	mA
External Voltage Applied to Analog Input (Note 3)	V_{IN}	AGND-0.3	VA+0.3	V
External Voltage Applied to Analog Output	V_{IN}	-VA_HP - 0.3	+VA_HP + 0.3	V
External Voltage Applied to Digital Input (Note 3)	V_{IND}	-0.3	VL+ 0.3	V
Ambient Operating Temperature (power applied)	T_A	-50	+115	°C
Storage Temperature	T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA = 2.5 V (nominal) Min	Typ	Max	VA = 1.8 V (nominal) Min	Typ	Max	Unit
Analog In to ADC (PGA bypassed)								
Dynamic Range	A-weighted	93	99	-	90	96	-	dB
	unweighted	90	96	-	87	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-80	-	-84	-78	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-	-	-33	-	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
PGA Setting: +12 dB	A-weighted	85	91	-	82	88	-	dB
	unweighted	82	88	-	79	85	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88	-81	-	-86	-80	dB
	-60 dBFS	-	-35	-	-	-32	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-85	-79	-	-83	-77	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	78	-	-	75	-	dB
	unweighted	-	74	-	-	71	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	SDOUT Code with HPF On	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
DAC Isolation (Note 5)		-	70	-	-	70	-	dB
Full-scale Input Voltage	ADC	0.74•VA	0.78•VA	0.82•VA	0.74•VA	0.78•VA	0.82•VA	Vpp
	PGA (0 dB)	0.75•VA	0.794•VA	0.83•VA	0.75•VA	0.794•VA	0.83•VA	Vpp
	MIC (+16 dB)		0.129•VA			0.129•VA		Vpp
	MIC (+32 dB)		0.022•VA			0.022•VA		Vpp
Input Impedance (Note 6)	ADC	-	20	-	-	20	-	kΩ
	PGA	-	39	-	-	39	-	kΩ
	MIC	-	50	-	-	50	-	kΩ

Notes:

4. Referred to the typical full-scale voltage. Applies to all THD+N and Dynamic Range values in the table.
5. Measured with DAC delivering full-scale output power into 16 Ω.
6. Measured between AINxx and AGND.

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to full scale): 1 kHz through passive input filter; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA = 2.5 V (nominal) Min	Typ	Max	VA = 1.8 V (nominal) Min	Typ	Max	Unit
Analog In to ADC								
Dynamic Range	A-weighted	91	99	-	88	96	-	dB
	unweighted	78	96	-	85	93	-	dB
Total Harmonic Distortion + Noise	-1 dBFS	-	-86	-78	-	-84	-76	dB
	-20 dBFS	-	-76	-	-	-73	-	dB
	-60 dBFS	-	-36	-	-	-33	-	dB
Analog In to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
PGA Setting: +12 dB	A-weighted	83	91	-	80	88	-	dB
	unweighted	80	88	-	77	85	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88	-80	-	-86	-78	dB
	-60 dBFS	-	-35	-	-	-32	-	dB
PGA Setting: +12 dB	-1 dBFS	-	-85	-77	-	-83	-75	dB
Analog In to MIC Pre-Amp (+16 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	86	-	-	83	-	dB
	unweighted	-	83	-	-	80	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-76	-	-	-74	-	dB
Analog In to MIC Pre-Amp (+32 dB) to PGA to ADC								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	-	78	-	-	75	-	dB
	unweighted	-	74	-	-	71	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-74	-	-	-71	-	dB
Other Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.1	-	-	0.1	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	SDOUT Code with HPF On	-	352	-	-	352	-	LSB
Input								
Interchannel Isolation		-	90	-	-	90	-	dB
DAC Isolation (Note 5)		-	70	-	-	70	-	dB

Parameter (Note 4)		VA = 2.5 V (nominal) Min	Typ	Max	VA = 1.8 V (nominal) Min	Typ	Max	Unit
Full-scale Input Voltage	ADC	0.74•VA	0.78•VA	0.82•VA	0.74•VA	0.78•VA	0.82•VA	Vpp
	PGA (0 dB)	0.75•VA	0.794•VA	0.83•VA	0.75•VA	0.794•VA	0.83•VA	Vpp
	MIC (+16 dB)		0.129•VA			0.129•VA		Vpp
	MIC (+32 dB)		0.022•VA			0.022•VA		Vpp
Input Impedance (Note 6)	ADC	18	-	-	18	-	-	kΩ
	PGA	40	-	-	40	-	-	kΩ
	MIC	50	-	-	50	-	-	kΩ

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 7)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.46	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		33	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
High-Pass Filter Characteristics (48 kHz Fs)					
Frequency Response	-3.0 dB	-	3.7	-	Hz
	-0.13 dB	-	24.2	-	Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	10^5/Fs	0	s

Note:

7. Response is clock-dependent and will scale with Fs. Note that the response plots (Figure 33 to Figure 41) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs. HPF parameters are for Fs = 48 kHz.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 3), and test load R_L = 16 Ω, C_L = 10 pF (see Figure 3) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 8)		VA = 2.5V (nominal) Min	Typ	Max	VA = 1.8V (nominal) Min	Typ	Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-78	-	-88	-82	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	92	98	-	89	95	-	dB
	unweighted	89	95	-	86	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-69	-	-75	-69	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 Ω or 10 kΩ								
Output Parameters (Note 9)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)		0.6047			0.6047		
Full-scale Output Voltage (2•G•MI•VA) (Note 9)		See Line Output Voltage Characteristics, page 17						Vpp
Full-scale Output Power (Note 9)		See Headphone Output Power Characteristics, page 18,						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 10)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 10)	-	-	150	-	-	150	pF

Notes:

8. One LSB of triangular PDF dither is added to data.
9. Full-scale output voltage and power is determined by the gain setting, G, in register "Headphone Analog Gain (HP_GAIN[2:0])" on page 56. High gain settings at certain VA and VA_HP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output. See Figures 27–30.

10. See Figure 3. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology, C_L will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz and 96 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output (see Figure 3), and test load R_L = 16 Ω, C_L = 10 pF (see Figure 3) for the headphone output. HP_GAIN[2:0] = 011.)

Parameter (Note 8)		**VA = 2.5V** (nominal) Min	Typ	Max	**VA = 1.8V** (nominal) Min	Typ	Max	Unit
R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-86	-73	-	-88	-80	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-86	-	-	-88	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
R_L = 16 Ω								
Dynamic Range								
18 to 24-Bit	A-weighted	90	98	-	87	95	-	dB
	unweighted	87	95	-	84	92	-	dB
16-Bit	A-weighted	-	96	-	-	93	-	dB
	unweighted	-	93	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-75	-67	-	-75	-67	dB
	-20 dB	-	-75	-	-	-72	-	dB
	-60 dB	-	-35	-	-	-32	-	dB
16-Bit	0 dB	-	-75	-	-	-75	-	dB
	-20 dB	-	-73	-	-	-70	-	dB
	-60 dB	-	-33	-	-	-30	-	dB
Other Characteristics for R_L = 16 or 10 kΩ								
Output Parameters (Note 9)	Modulation Index (MI)	-	0.6787	-	-	0.6787	-	
	Analog Gain Multiplier (G)		0.6047			0.6047		
Full-scale Output Voltage (2•G•MI•VA) (Note 9)		See Line Output Voltage Characteristics, page 17						Vpp
Full-scale Output Power (Note 9)		See Headphone Output Power Characteristics, page 18,						mW
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 10)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 10)	-	-	150	-	-	150	pF

LINE OUTPUT VOLTAGE CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 3).

Parameter			VA = 2.5V (nominal)			VA = 1.8V (nominal)			Unit
			Min	Typ	Max	Min	Typ	Max	
AOUTx Voltage Into R_L = 10 kΩ									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	1.34	-	-	0.97	-	V_{pp}
		2.5 V	-	1.34	-	-	0.97	-	V_{pp}
001	0.4571	1.8 V	-	1.55	-	-	1.12	-	V_{pp}
		2.5 V	-	1.55	-	-	1.12	-	V_{pp}
010	0.5111	1.8 V	-	1.73	-	-	1.25	-	V_{pp}
		2.5 V	-	1.73	-	-	1.25	-	V_{pp}
011 (default)	0.6047	1.8 V	-	2.05	-	1.41	1.48	1.55	V_{pp}
		2.5 V	1.95	2.05	2.15	-	1.48	-	V_{pp}
100	0.7099	1.8 V	-	2.41	-	-	1.73	-	V_{pp}
		2.5 V	-	2.41	-	-	1.73	-	V_{pp}
101	0.8399	1.8 V	-	2.85	-		2.05		V_{pp}
		2.5 V	-	2.85	-	-	2.05	-	V_{pp}
110	1.0000	1.8 V	-	3.39	-	-	2.44	-	V_{pp}
		2.5 V	-	3.39	-	-	2.44	-	V_{pp}
111	1.1430	1.8 V	(See (Note 11)				2.79		V_{pp}
		2.5 V	-	3.88	-	-	2.79	-	V_{pp}

Note:

11. VA_HP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.

HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Sample Frequency = 48 kHz; test load R_L = 16 Ω, C_L = 10 pF (see Figure 3).

Parameter			VA = 2.5V (nominal) Min	Typ	Max	VA = 1.8V (nominal) Min	Typ	Max	Unit
AOUTx Power Into R_L = 16 Ω									
HP_GAIN[2:0]	Analog Gain (G)	VA_HP							
000	0.3959	1.8 V	-	14	-	-	7	-	mW_{rms}
		2.5 V	-	14	-	-	7	-	mW_{rms}
001	0.4571	1.8 V	-	19	-	-	10	-	mW_{rms}
		2.5 V	-	19	-	-	10	-	mW_{rms}
010	0.5111	1.8 V	-	23	-	-	12	-	mW_{rms}
		2.5 V	-	23	-	-	12	-	mW_{rms}
011 (default)	0.6047	1.8 V		(Note 11)		-	17	-	mW_{rms}
		2.5 V	-	32	-	-	17	-	mW_{rms}
100	0.7099	1.8 V		(Note 11)		-	23	-	mW_{rms}
		2.5 V	-	44	-	-	23	-	mW_{rms}
101	0.8399	1.8 V					(Note 9)		mW_{rms}
		2.5 V				-	32	-	mW_{rms}
110	1.0000	1.8 V							mW_{rms}
		2.5 V							mW_{rms}
111	1.1430	1.8 V							mW_{rms}
		2.5 V							mW_{rms}

(Note 9, 11)

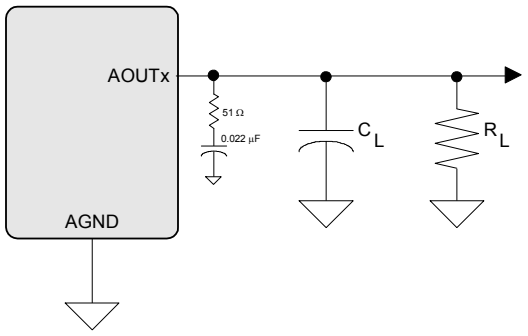


Figure 3. Headphone Output Test Load

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 12)		Min	Typ	Max	Unit
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.08	dB
Passband	to -0.05 dB corner to -3 dB corner	0 0	- -	0.4780 0.4996	Fs Fs
StopBand		0.5465	-	-	Fs
StopBand Attenuation (Note 13)		50	-	-	dB
Group Delay		-	10.4/Fs	-	s
De-emphasis Error	Fs = 32 kHz Fs = 44.1 kHz Fs = 48 kHz	- - -	- - -	+1.5/+0 +0.05/-0.25 -0.2/-0.4	dB dB dB

Notes:

12. Response is clock dependent and will scale with Fs. Note that the response plots (Figure 38 to Figure 41 on page 80) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
13. Measurement Bandwidth is from Stopband to 3 Fs.

SWITCHING SPECIFICATIONS - SERIAL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDOUT C_{LOAD} = 15 pF.)

Parameters		Symbol	Min	Max	Units
$\overline{\text{RESET}}$ pin Low Pulse Width (Note 14)			1	-	ms
MCLK Frequency			1.024	38.4	MHz
MCLK Duty Cycle (Note 15)			45	55	%
Slave Mode					
Input Sample Rate (LRCK)	Quarter-Speed Mode Half-Speed Mode Single-Speed Mode Double-Speed Mode	F_s F_s F_s F_s	4 8 4 50	12.5 25 50 100	kHz kHz kHz kHz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Setup Time Before SCLK Rising Edge		$t_{s(LK-SK)}$	40	-	ns
LRCK Edge to SDOUT MSB Output Delay		$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{h(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

Parameters		Symbol	Min	Max	Units
Master Mode (Note 16)					
Output Sample Rate (LRCK)	All Speed Modes (Note 17)	F_s	-	$\frac{MCLK}{128}$	Hz
LRCK Duty Cycle			45	55	%
SCLK Frequency		$1/t_P$	-	$64 \cdot F_s$	Hz
SCLK Duty Cycle			45	55	%
LRCK Edge to SDOUT MSB Output Delay		$t_{d(MSB)}$	-	52	ns
SDOUT Setup Time Before SCLK Rising Edge		$t_{s(SDO-SK)}$	20	-	ns
SDOUT Hold Time After SCLK Rising Edge		$t_{h(SK-SDO)}$	30	-	ns
SDIN Setup Time Before SCLK Rising Edge		$t_{s(SD-SK)}$	20	-	ns
SDIN Hold Time After SCLK Rising Edge		t_h	20	-	ns

14. After powering up the CS42L51, $\overline{\text{RESET}}$ should be held low after the power supplies and clocks are settled.
15. See "Example System Clock Frequencies" on page 77 for typical MCLK frequencies.
16. See"Master" on page 38.
17. "MCLK" refers to the external master clock applied.

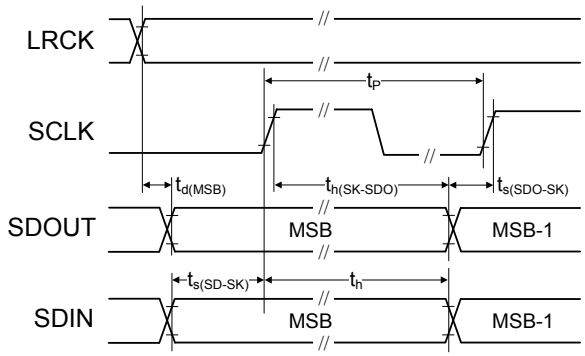


Figure 5. Serial Audio Interface Master Mode Timing

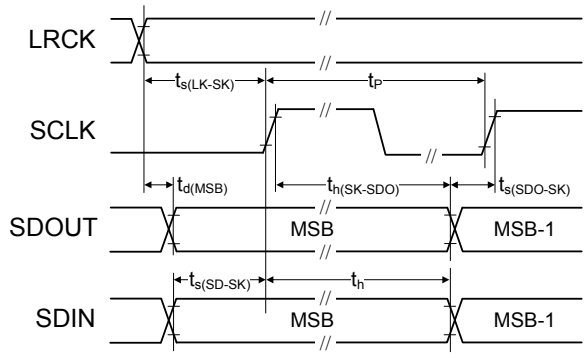


Figure 4. Serial Audio Interface Slave Mode Timing

SWITCHING SPECIFICATIONS - I²C CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL, SDA C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 18)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	3450	ns

18. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

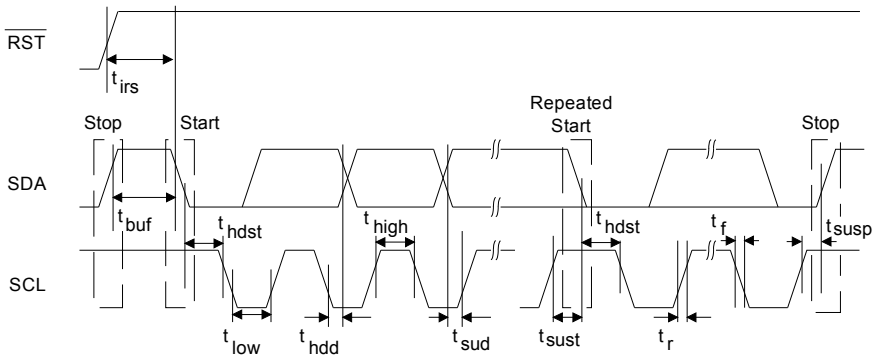


Figure 6. Control Port Timing - I²C

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VL)

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6.0	MHz
$\overline{\text{RESET}}$ Rising Edge to $\overline{\text{CS}}$ Falling		t_{srs}	20	-	ns
$\overline{\text{CS}}$ Falling to CCLK Edge		t_{css}	20	-	ns
$\overline{\text{CS}}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 19)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 20)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 20)	t_{f2}	-	100	ns

19. Data must be held for sufficient time to bridge the transition time of CCLK.
20. For f_{sck} <1 MHz.

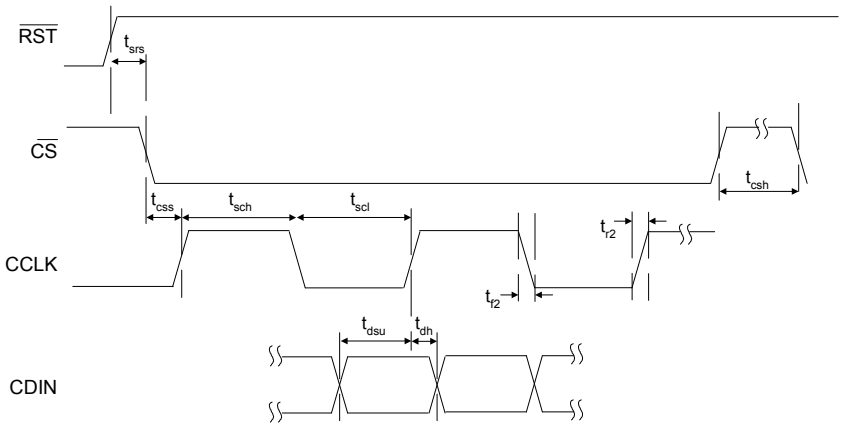


Figure 7. Control Port Timing - SPI Format

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Min	Typ	Max	Units
VQ Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink (Note 21)		-	-	10	µA
DAC_FILT+ Nominal Voltage		-	VA	-	V
ADC_FILT+ Nominal Voltage		-	VA	-	V
VSS_HP Characteristics					
Nominal Voltage		-	-0.8•(VA_HP)	-	V
DC Current Source		-		10	µA
MIC BIAS Characteristics					
Nominal Voltage	MICBIAS_LVL[1:0] = 00	-	0.8•VA	-	V
	MICBIAS_LVL[1:0] = 01	-	0.7•VA	-	V
	MICBIAS_LVL[1:0] = 10	-	0.6•VA	-	V
	MICBIAS_LVL[1:0] = 11	-	0.5•VA	-	V
DC Current Source		-	-	1	mA
Power Supply Rejection Ratio (PSRR)	1 kHz	-	50	-	dB
Power Supply Rejection Ratio (PSRR) (Note 22)	1 kHz	-	60	-	dB

21. The DC current draw represents the allowed current draw from the VQ pin due to typical leakage through electrolytic de-coupling capacitors.
22. Valid with the recommended capacitor values on DAC_FILT+, ADC_FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 23)	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	µA
Input Capacitance		-	10	pF
1.8 V - 3.3 V Logic				
High-Level Output Voltage (I_{OH} = -100 µA)	V_{OH}	VL - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)	V_{OL}	-	0.2	V
High-Level Input Voltage	V_{IH}	0.68•VL	-	V
Low-Level Input Voltage	V_{IL}	-	0.32•VL	V

23. See “Digital I/O Pin Characteristics” on page 8 for serial and control port power rails.

POWER CONSUMPTION

See (Note 24)

	Operation	Power Control Registers 02h PDN_DACB	PDN_DACA	PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN	03h PDN_MICB	PDN_MICA	PDN_MICBIAS	V	Typical Current (mA) i_{VA_HP}	i_{VA}	i_{VD}	i_{VL} (Note 25)	Total Power (mW_{rms})
1	Off (Note 26)	x	x	x	x	x	x	x	x	x	x	1.8	0	0	0	0	0
												2.5	0	0	0	0	0
2	Standby (Note 27)	x	x	x	x	x	x	1	x	x	x	1.8	0	0.01	0.02	0	0.05
												2.5	0	0.01	0.03	0	0.10
3	Mono Record ADC	1	1	1	1	1	0	0	1	1	1	1.8	0	1.85	2.03	0.03	7.05
												2.5	0	2.07	3.05	0.05	12.94
	PGA to ADC	1	1	1	0	1	0	0	1	1	1	1.8	0	2.35	2.03	0.03	7.95
												2.5	0	2.58	3.08	0.05	14.29
	MIC to PGA to ADC (with Bias)	1	1	1	0	1	0	0	1	0	0	1.8	0	3.67	2.05	0.03	10.36
												2.5	0	3.95	3.09	0.05	17.71
	MIC to PGA to ADC (no Bias)	1	1	1	0	1	0	0	1	0	1	1.8	0	3.27	2.03	0.03	9.61
												2.5	0	3.52	3.08	0.05	16.62
4	Stereo Record ADC	1	1	1	1	0	0	0	1	1	1	1.8	0	2.69	2.12	0.03	8.72
												2.5	0	2.93	3.18	0.04	15.40
	PGA to ADC	1	1	0	0	0	0	0	1	1	1	1.8	0	3.65	2.12	0.03	10.45
												2.5	0	3.91	3.17	0.04	17.84
	MIC to PGA to ADC (no Bias)	1	1	0	0	0	0	0	0	0	1	1.8	0	5.48	2.11	0.03	13.73
												2.5	0	5.76	3.17	0.04	22.45
5	Mono Playback	1	0	1	1	1	1	0	1	1	1	1.8	1.66	1.40	2.35	0.01	9.74
												2.5	2.03	1.71	3.48	0.02	18.08
6	Stereo Playback	0	0	1	1	1	1	0	1	1	1	1.8	2.77	2.05	2.35	0.01	12.93
												2.5	3.21	2.50	3.49	0.02	23.02
7	Mono Record & Playback PGA in (no MIC) to Mono Out	1	0	1	0	1	0	0	1	1	1	1.8	1.66	3.63	2.73	0.03	14.49
												2.5	2.03	4.16	4.08	0.05	25.79
8	Phone Monitor MIC (with bias) in to Mono Out	1	0	1	0	1	0	0	1	0	0	1.8	1.66	4.95	2.75	0.03	16.90
												2.5	2.03	5.52	4.08	0.05	29.20
9	Stereo Record & Playback PGA in (no MIC) to Stereo Out	0	0	0	0	0	0	0	1	1	1	1.8	2.77	5.59	2.82	0.03	20.18
												2.5	3.21	6.28	4.19	0.04	34.30

24. Unless otherwise noted, test conditions are as follows: All zeros input, slave mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation.
25. VL current will slightly increase in master mode.
26. $\overline{\text{RESET}}$ pin 25 held LO, all clocks and data lines are held LO.
27. $\overline{\text{RESET}}$ pin 25 held HI, all clocks and data lines are held HI.

4. APPLICATIONS

4.1 Overview

4.1.1 Architecture

The CS42L51 is a highly integrated, low power, 24-bit audio CODEC comprised of stereo analog-to-digital converters (ADC), and stereo digital-to-analog converters (DAC) designed using multi-bit delta-sigma techniques. The DAC operates at an oversampling ratio of 128Fs and the ADC operates at 64Fs, where Fs is equal to the system sample rate. The different clock rates maximize power savings while maintaining high performance. The CODEC operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

4.1.2 Line & MIC Inputs

The analog input portion of the CODEC allows selection from and configuration of multiple combinations of stereo and microphone (MIC) sources. Six line inputs with configuration for two MIC inputs (or one MIC input with common mode rejection), two MIC bias outputs and independent channel control (including a high-pass filter disable function) are available. A Programmable Gain Amplifier (PGA), MIC boost, and Automatic Level Control (ALC), with noise gate settings, provide analog gain and adjustment. Digital volume controls, including gain, boost, attenuation and inversion are also available.

4.1.3 Line & Headphone Outputs

The analog output portion of the D/A includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages. Eight gain settings for the headphone amplifier are available.

4.1.4 Signal Processing Engine

A signal processing engine is available to process serial input D/A data before output to the DAC. The D/A data has independent volume controls and mixing functions such as mono mixes and left/right channel swaps. A Tone Control provides bass and treble at four selectable corner frequencies. An automatic level control provides limiting capabilities at programmable attack and release rates, maximum thresholds and soft ramping. A 15/50 μs de-emphasis filter is also available at a 44.1 kHz sample rate.

4.1.5 Beep Generator

A beep may be generated internally at select frequencies across approximately two octave major scales and configured to occur continuously, periodically or at single time intervals controlled by the user. Volume may be controlled independently.

4.1.6 Device Control (Hardware or Software Mode)

In Software Mode, all functions and features may be controlled via a two-wire I²C or three-wire SPI control port interface. In Hardware Mode, a limited feature set may be controlled via stand-alone control pins.

4.1.7 Power Management

Two Software Mode control registers provide independent power-down control of the ADC, DAC, PGA, MIC pre-amp and MIC bias, allowing operation in select applications with minimal power consumption.

4.2 Hardware Mode

A limited feature-set is available when the CODEC powers up in Hardware Mode (see "Recommended Power-Up Sequence" on page 40) and may be controlled via stand-alone control pins. Table 2 shows a list of functions/features, the default configuration and the associated stand-alone control available.

Hardware Mode Feature/Function Summary			
Feature/Function	**Default Configuration**	**Stand-Alone Control**	**Note**
Power Control Codec PGAx ADCx DACx MIC Bias MICx Pre-amplifier	Powered Up Powered Up Powered Up Powered Up Powered Down Powered Down	-	-
Auto-Detect	Enabled	-	-
Speed Mode Serial Port Slave Serial Port Master	Auto-Detect Speed Mode Single-Speed Mode	-	-
MCLK Divide	(Selectable)	"MCLKDIV2" pin 2	see Section 4.5 on page 37
Serial Port Master / Slave Selection	(Selectable)	"M/$\overline{S}$" pin 29	see Section 4.5 on page 37
Interface Control ADC DAC	(Selectable)	"I²S/$\overline{LJ}$" pin 3	see Section 4.6 on page 39
ADC Volume & Gain Digital Boost Soft Ramp Zero Cross Invert PGAx Attenuator ALC Noise Gate	Disabled Disabled Disabled Disabled 0 dB 0 dB Disabled Disabled	-	-
ADCx High-Pass Filter ADCx High-Pass Filter Freeze	Enabled Continuous DC Subtraction	-	-
Line/MIC Input Select	AIN1A to PGAA AIN1B to PGAB	-	-
DAC Volume & Gain HP Gain AOUTx Volume Invert Soft Ramp Zero Cross	G = 0.6047 0 dB Disabled Enabled Disabled	-	-
DAC De-Emphasis	(Selectable)	"DEM" pin 4	see Section on page 33
Signal Processing Engine (SPE) Mix Beep Tone Control Peak Detect and Limiter	Disabled Disabled Disabled Disabled	-	-
Data Selection	Data Input (PCM) to DAC	-	-
Channel Mix ADC DAC	ADCA = L; ADCB = R PCMA = L; PCMB = R	-	-
Charge Pump Frequency	(64xFs)/7	-	-

Table 2. Hardware Mode Feature Summary

4.3 Analog Inputs

AINxA and AINxB are the analog inputs, internally biased to VQ, that accepts line-level and MIC-level signals, allowing various gain and signal adjustments for each channel.

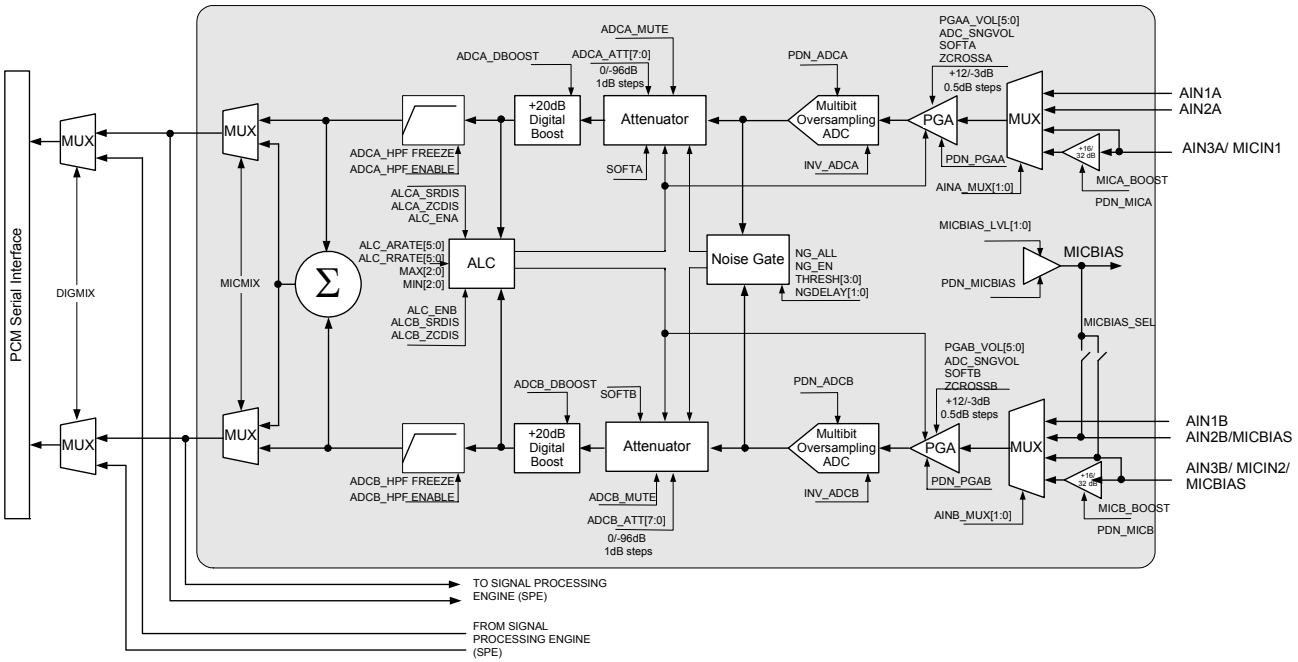


Figure 8. Analog Input Architecture

4.3.1 Digital Code, Offset & DC Measurement

The ADC output data is in two's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively and cause the ADC overflow bit to be set to a '1'.

Given the two's complement format, low-level signals may cause the MSB of the serial data to periodically toggle between '1' and '0', possibly introducing noise into the system as the bit switches back and forth. To prevent this phenomena, a constant DC offset is added to the serial data bringing the low-level signal just above the point at which the MSB would normally toggle, thus reducing the noise introduced. Note that this offset is not removed (refer to "Analog Input Characteristics (Commercial - CNZ)" on page 12 and/or "Analog Input Characteristics (Automotive - DNZ)" on page 13 for the specified offset level).

The CODEC may be used to measure DC voltages by disabling the high-pass filter for the designated channel. DC levels are measured relative to VQ and will be decoded as positive two's complement binary numbers above VQ and negative two's complement binary numbers below VQ.

Software Controls:	"Status (Address 20h) (Read Only)" on page 71, "ADC Control (Address 06h)" on page 53.

4.3.2 High-Pass Filter and DC Offset Calibration

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the high-pass filter is “frozen” during normal operation, the current value of the DC offset for the corresponding channel is held. It is this DC offset that will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CODECwith the high-pass filter enabled and the DC offset not “frozen” until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Freezing the DC offset.

The high-pass filters are controlled using the ADCx_HPFRZ and ADCx_HPFEN bits.

If a particular ADC channel is used to measure DC voltages, the high-pass filter may be disabled using the ADCx_HPFEN bit.

Software Controls:	“ADC Control (Address 06h)” on page 53.

4.3.3 Digital Routing

The digital output of the ADC may be internally routed to the signal processing engine (SPE) for playback of analog input signals. Volume to the DAC may be controlled using the ADCMIX[6:0] bits. The serial input data may also be routed to the ADC serial interface using the DIGMIX bit. This is useful for recording a digital mix along with the analog input.

Software Controls:	“ADCx Mixer Volume Control: ADCA (Address 0Eh) & ADCB (Address 0Fh)” on page 60, “Interface Control (Address 04h)” on page 51.

4.3.4 Differential Inputs

The stereo pair inputs act as a single differential input when the MICMIX bit is enabled. This provides common mode rejection of noise in digitally intense PCBs, where the microphone signal traverses long traces, or across long microphone cables as illustrated in Figure 9.

Since the mixer provides a differential combination of the two signals, the potential input mix may exceed the maximum full-scale input and result in clipping. The level out of the mixer, therefore, is automatically attenuated 6 dB. Gain may be applied using either the analog PGA or MIC Pre-amp or the digital ADCMIX volume control to re-adjust a small signal to desired levels.

The analog inputs may also be used as a differential input pair as shown in Figure 10. The two channels are differentially combined when the MICMIX bit is enabled.

4.3.4.1 External Passive Components

The microphone input is internally biased to VQ. Input signals must be AC coupled using external capacitors with values consistent with the desired high-pass filter design. The MICINx input resistance of 50 kΩ may be combined with an external capacitor of 1 μF to achieve the cutoff frequency defined by the equation,

$$fc = \frac{1}{2\pi(50\ k\Omega)(1\ \mu F)} = 3.18\ Hz$$

An electrolytic capacitor must be placed such that the positive terminal is positioned relative to the side with the greater bias voltage. The MICBIAS voltage level is controlled by the MICBIAS_LVL[1:0] bits.

The MICBIAS series resistor must be selected based on the requirements of the particular microphone used. The MICBIAS output pin is selected using the MICBIAS_SEL bit.

Software Controls:	“Interface Control (Address 04h)” on page 51, “MIC Control (Address 05h)” on page 52.

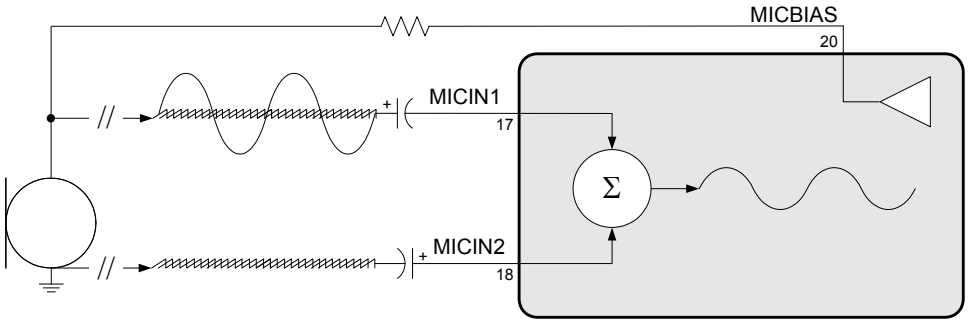


Figure 9. MIC Input Mix with Common Mode Rejection

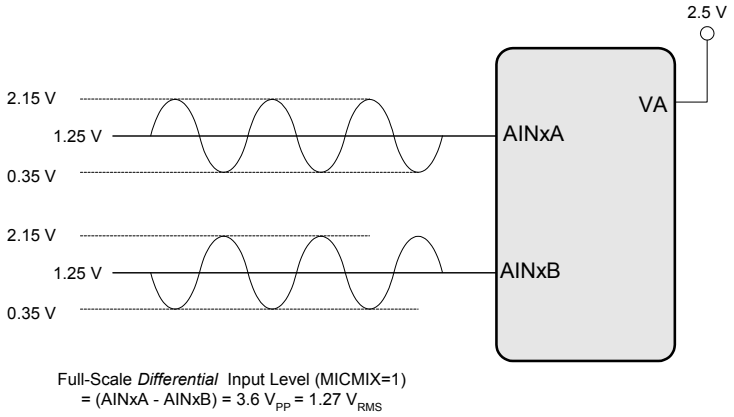


Figure 10. Differential Input

4.3.5 Analog Input Multiplexer

A stereo 4-to-1 analog input multiplexer selects between a line-level input source, or a mic-level input source, depending on the PDN_PGAx and AINx_MUX[1:0] bit settings. Signals may be routed to or bypassed around the PGA. To conserve power, the PGAs may be powered down allowing the user to select from multiple line-level sources and route the stereo signal directly to the ADC. When using the MIC preamp, however, the PGA must be powered up.

Analog input channel B may also be used as an output for the MIC bias voltage. The MICBIAS_SEL bit routes the bias voltage to either of two pins. The multiplexer must then select from the remainder of the two input channels.

The ADC, PGA and MIC pre-amplifier each has an associated input resistance. When selecting between these paths, the input resistance to the CODEC will change accordingly. Refer to the input resistance characteristics in the Characteristic and Specification Tables for the input resistance of each path.

Software Controls:	"Power Control 1 (Address 02h)" on page 48, "MIC Control (Address 05h)" on page 52 "ADCx Input Select, Invert & Mute (Address 07h)" on page 55.

4.3.6 MIC & PGA Gain

The MIC-level input passes through a +16 dB or +32 dB analog gain stage prior to the input multiplexer, allowing it to be used for microphone level signals without the need for any external gain. The PGA must be powered up when using the MIC pre-amp.

The PGA stage provides an additional +12 dB to -3 dB of analog gain in 0.5 dB steps.

Software Controls:	"Power Control 1 (Address 02h)" on page 48, "ADCx Input Select, Invert & Mute (Address 07h)" on page 55, "ALCX & PGAX Control: ALCA, PGAA (Address 0Ah) & ALCB, PGAB (Address 0Bh)" on page 58, "MIC Control (Address 05h)" on page 52.

4.3.7 Automatic Level Control (ALC)

When enabled, the ALC monitors the analog input signal after the digital attenuator, detects when peak levels exceed the maximum threshold settings and lowers, first, the PGA gain settings and then increases the digital attenuation levels at a programmable attack rate and maintains the resulting level below the maximum threshold.

When input signal levels fall below the minimum threshold, digital attenuation levels are decreased first and the PGA gain is then increased at a programmable release rate and maintains the resulting level above the minimum threshold.

Attack and release rates are affected by the ADC soft ramp/zero-cross settings and sample rate, Fs. ALC soft ramp and zero-cross dependency may be independently enabled/disabled.

Recommended settings: Best level control may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. **Note: 1.)** The maximum realized gain must be set in the PGAx_VOL register. The ALC will only apply the gain set in the PGAx_VOL. **2.)** The ALC maintains the output signal between the MIN and MAX thresholds. As the input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Software Controls:	"ALC Enable & Attack Rate (Address 1Ch)" on page 68, "ALC Release Rate (Address 1Dh)" on page 69, "ALC Threshold (Address 1Eh)" on page 69, "ALCX & PGAX Control: ALCA, PGAA (Address 0Ah) & ALCB, PGAB (Address 0Bh)" on page 58.

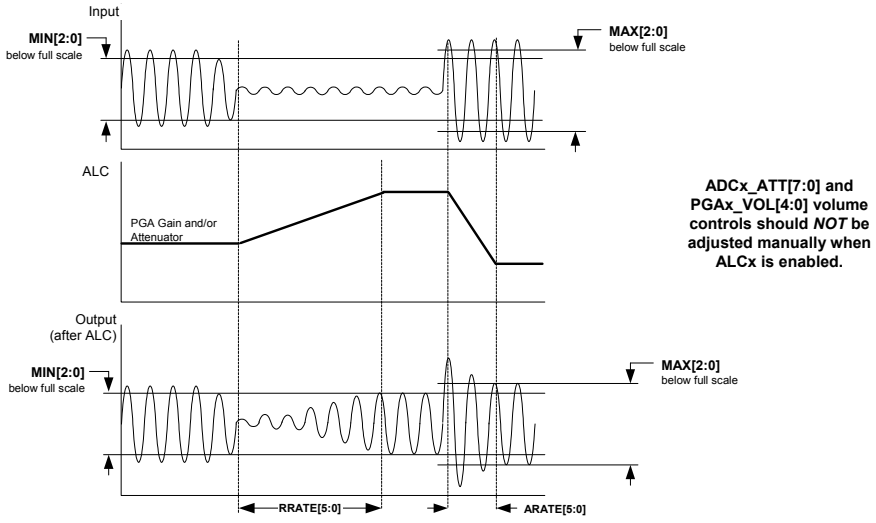


Figure 11. ALC

4.3.8 Noise Gate

The noise gate may be used to mute signal levels that fall below a programmable threshold. This prevents the ALC from applying gain to noise. A programmable delay may be used to set the minimum time before the noise gate attacks the signal.

Maximum noise gate attenuation levels will depend on the gain applied in either the PGA or MIC pre-amplifier. For example: If both +32 dB pre-amplification and +12 dB programmable gain is applied, the maximum attenuation that the noise gate achieves will be 52 dB (-96 + 32 + 12) below full-scale.

Ramp-down time to the maximum setting is affected by the SOFTx bit.

Recommended settings: For best results, enable soft ramp for the digital attenuator. When the analog inputs are configured for differential signals (see "Differential Inputs" on page 28), enable the NG_ALL bit to trigger the noise gate only when *both* inputs fall below the threshold.

Software Controls:	"Noise Gate Configuration & Misc. (Address 1Fh)" on page 70, "ADC Control (Address 06h)" on page 53.

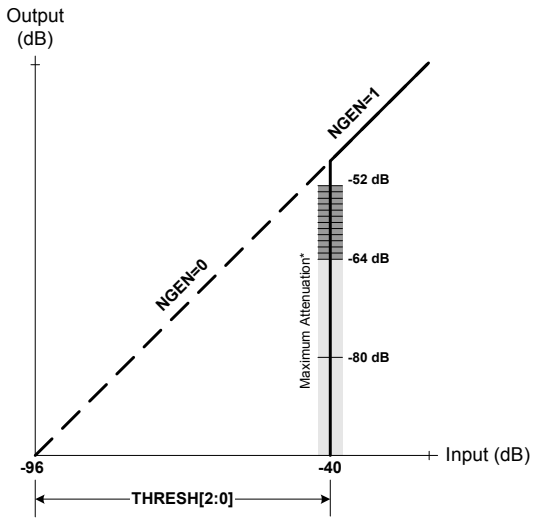


Figure 12. Noise Gate Attenuation

4.4 Analog Outputs

AOUTA and AOUTB are the ground-centered line or headphone outputs. Various signal processing options are available, including digital mixes with the ADC signal and an internal Beep Generator. The desired path to the DAC must be selected using the DATA_SEL[1:0] bits.

Software Controls:	“DAC Control (Address 09h)” on page 57.

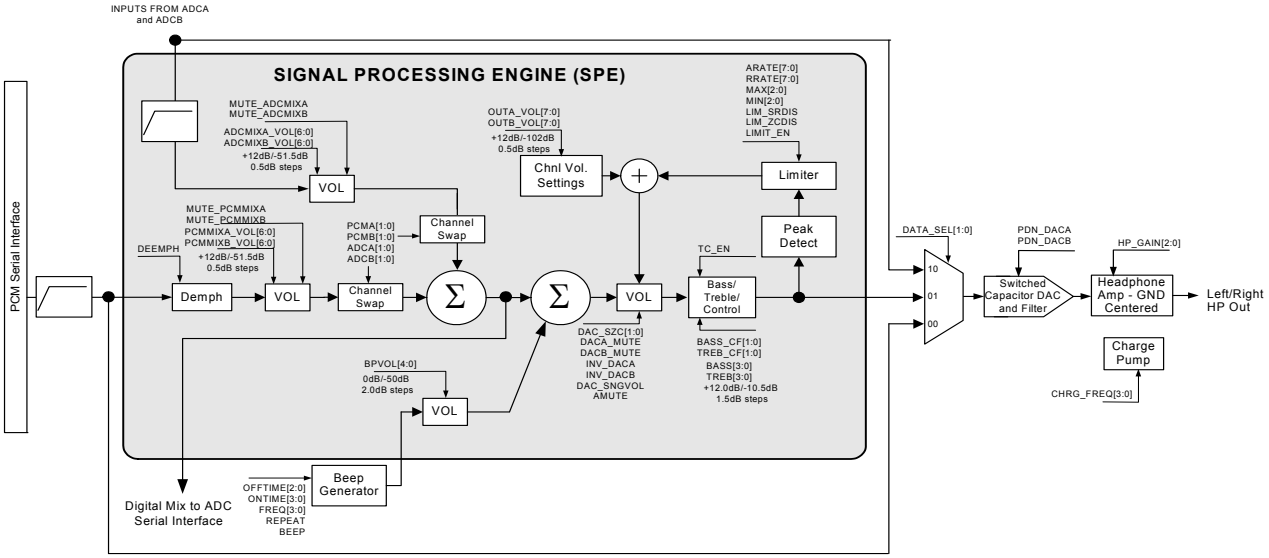


Figure 13. Output Architecture

4.4.1 *De-Emphasis Filter*

The codec includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in Figure 14. The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction. De-emphasis is only available in Single-Speed Mode.

Software Controls:	“DAC Control (Address 09h)” on page 57.		
Hardware Control:	Pin	Setting	Selection
	“DEM” pin 4.	LO	No De-Emphasis
		HI	De-Emphasis Applied

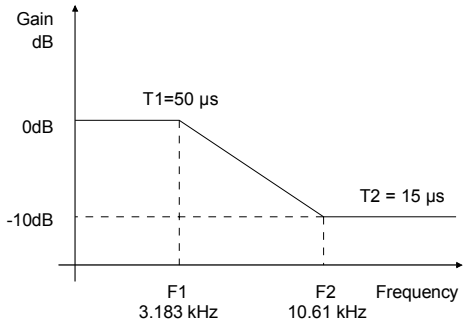


Figure 14. De-Emphasis Curve

4.4.2 Volume Controls

Three digital volume control functions are implemented, offering independent control over the ADC and PCM signal paths into the mixer as well as a combined control over the mixed signals. All volume controls are programmable to ramp in increments of 0.125 dB at a rate controlled by the DAC soft ramp/zero-cross settings.

All signal paths may also be independently muted via mute control bits. When enabled, each bit attenuates the signal to its maximum value. When the mute bit is disabled, the signal returns to the attenuation level set in the respective volume control register. The attenuation is ramped up and down at the rate specified by the DAC_SZC[1:0] bits.

Software Controls:	"ADCx Mixer Volume Control: ADCA (Address 0Eh) & ADCB (Address 0Fh)" on page 60, "PCMX Mixer Volume Control: PCMA (Address 10h) & PCMB (Address 11h)" on page 61, "AOUTx Volume Control: AOUTA (Address 16h) & AOUTB (Address 17h)" on page 65, "DAC Output Control (Address 08h)" on page 56.

4.4.3 Mono Channel Mixer

A channel mixer may be used to create a mix of the left and right channels for the ADC data. This mix allows the user to produce a MONO signal from a stereo source. The mixer may also be used to implement a left/right channel swap.

Software Controls:	"PCM Channel Mixer (Address 18h)" on page 65.

4.4.4 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple and single (one-shot) beeps. Sixteen on and eight off times are available.

Note: The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the Beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, AOUTx_VOL[7:0], will affect the Beep volume, DAC volume may alternatively be controlled using the PCMMIXx_VOL[6:0] bits.

Software Controls:	"Beep Frequency & Timing Configuration (Address 12h)" on page 61, "Beep Off Time & Volume (Address 13h)" on page 62, "Beep Configuration & Tone Configuration (Address 14h)" on page 63

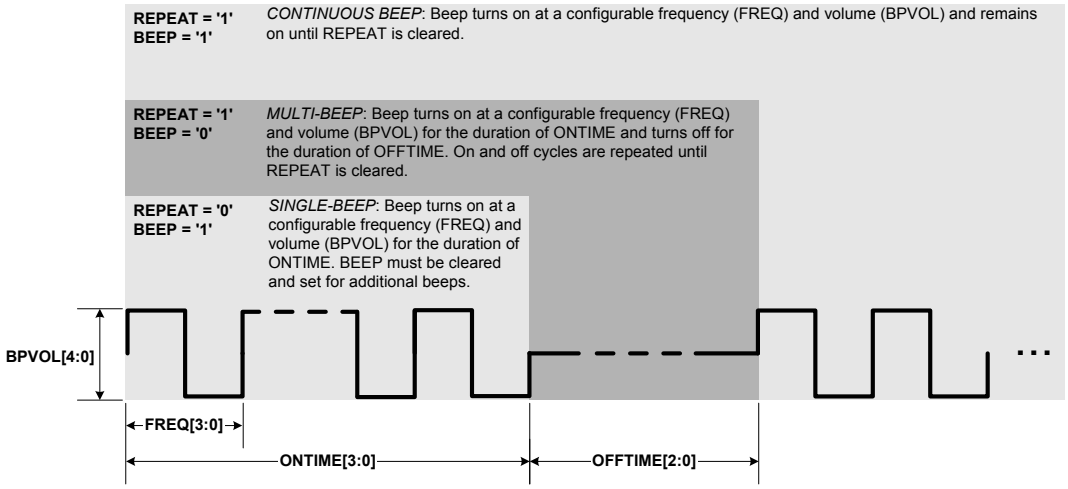


Figure 15. Beep Configuration Options

4.4.5 Tone Control

Shelving filters are used to implement bass and treble (boost and cut) with four selectable corner frequencies. Boosting will affect peak detect and limiting when levels exceed the maximum threshold settings.

Software Controls:	"Tone Control (Address 15h)" on page 64.

4.4.6 Limiter

When enabled, the limiter monitors the digital input signal before the DAC modulator, detects when levels exceed the maximum threshold settings and lowers the AOUT volume at a programmable attack rate below the maximum threshold. When the input signal level falls below the maximum threshold, the AOUT volume returns to its original level set in the Volume Control register at a programmable release rate. Attack and release rates are affected by the DAC soft ramp/zero-cross settings and sample rate, Fs. Limiter soft ramp and zero-cross dependency may be independently enabled/disabled.

Recommended settings: Best limiting performance may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. The "cushion" bits allow the user to set a threshold slightly below the maximum threshold for hysteresis control - this cushions the sound as the limiter attacks and releases.

Note:

1. When the Limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be realized using the PCMMIXx_VOL[6:0] bits.
2. The Limiter maintains the output signal between the CUSH and MAX thresholds. As the digital input signal level changes, the level-controlled output may not always be the same but will always fall within the thresholds.

Software Controls:	"Limiter Release Rate Register (Address 1Ah)" on page 67, "Limiter Attack Rate Register (Address 1Bh)" on page 68, "DAC Control (Address 09h)" on page 57

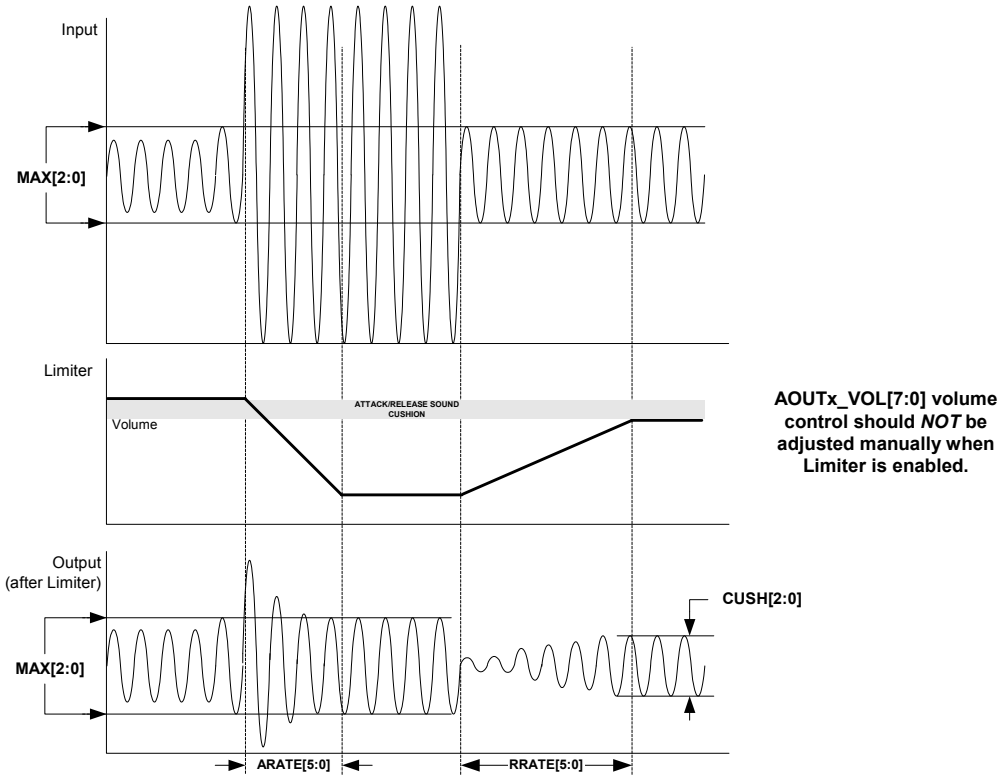


Figure 16. Peak Detect & Limiter

4.4.7 *Line-Level Outputs and Filtering*

The codec contains on-chip buffer amplifiers capable of producing line level single-ended outputs on AOUTA and AOUTB. These amplifiers are ground centered and do not have any DC offset. A load stabilizer circuit, shown in the "Typical Connection Diagram (Software Mode)" on page 9 and the "Typical Connection Diagram (Hardware Mode)" on page 10, is required on the analog outputs. This allows the DAC amplifiers to drive line or headphone outputs.

Also shown in the Typical Connection diagrams is the recommended passive output filter to support higher impedances such as those found on the inputs to operational amplifiers. "Rext", shown in the typical connection diagrams, is the input impedance of the receiving device.

The invert and digital gain controls may be used to provide phase and/or amplitude compensation for an external filter.

The delta-sigma conversion process produces high frequency noise beyond the audio passband, most of which is removed by the on-chip analog filters. The remaining out-of-band noise can be attenuated using an off-chip low pass filter.

Software Controls:	"DAC Output Control (Address 08h)" on page 56, "AOUTx Volume Control: AOUTA (Address 16h) & AOUTB (Address 17h)" on page 65.

4.4.8 On-Chip Charge Pump

An on-chip charge pump derives a negative supply voltage from the VA_HP supply. This provides dual rail supplies allowing a full-scale output swing centered around ground and eliminates the need for large, DC-blocking capacitors. Added benefits include greater pop suppression and improved low frequency (bass) response. **Note:** Series resistance in the path of the power supplies must be avoided. Any voltage drop on the VA_HP supply will directly impact the derived negative voltage on the charge pump supply, VSS_HP, and may result in clipping.

The FLYN and FLYP pins connect to internal switches that charges and discharges the external capacitor attached, at a default switching frequency. This frequency may be adjusted in the control port registers. Increasing the charge-pumping capacitor will slightly decease the pumping frequency. The capacitor connected to VSS_HP acts as a charge reservoir for the negative supply as well as a filter for the ripple induced by the charge pump. Increasing this capacitor will decrease the ripple on VSS_HP. Refer to the typical connection diagrams in Figure 1 on page 9 or Figure 2 on page 10 for the recommended capacitor values for the charge pump circuitry.

Software Controls:	"Charge Pump Frequency (Address 21h)" on page 72.

4.5 Serial Port Clocking

The CODEC serial audio interface port operates either as a slave or master. It accepts externally generated clocks in slave mode and will generate synchronous clocks derived from an input master clock (MCLK) in master mode.

The frequency of the MCLK must be an integer multiple of, and synchronous with, the system sample rate, Fs. The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked into or out of the device.

The SPEED and MCLKDIV2 software control bits or the SDOUT/(M/$\overline{S}$) and MCLKDIV2 stand-alone control pins, configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. The value on the SDOUT pin is latched immediately after powering up in Hardware Mode.

Software Control:	"MIC Power Control & Speed Control (Address 03h)" on page 49, "DAC Control (Address 09h)" on page 57.		
Hardware Control:	**Pin**	**Setting**	**Selection**
	"SDOUT, M/$\overline{S}$" pin 29	47 kΩ Pull-down	Slave
		47 kΩ Pull-up	Master
	"MCLKDIV2" pin 2	LO	No Divide
		HI	MCLK is divided by 2 prior to all internal circuitry.

4.5.1 Slave

LRCK and SCLK are inputs in Slave Mode. The speed of the CODEC is automatically determined based on the input MCLK/LRCK ratio when the Auto-Detect function is enabled. Certain input clock ratios will then require an internal divide-by-two of MCLK* using either the MCLKDIV2 bit or the MCLKDIV2 stand-alone control pin.

Additional clock ratios are allowed when the Auto-Detect function is disabled; but the appropriate speed mode must be selected using the SPEED[1:0] bits.

Auto-Detect	QSM	HSM	SSM	DSM
Disabled (Software Mode only)	512, 768, 1024, 1536, 2048, 3072	256, 384, 512, 768, 1024, 1536	128, 192, 256, 384, 512, 768	128, 192, 256, 384
Enabled	1024, 1536, 2048*, 3072*	512, 768, 1024*, 1536*	256, 384, 512*, 768*	128, 192, 256*, 384*

*MCLKDIV2 must be enabled.

Table 3. MCLK/LRCK Ratios

4.5.2 Master

LRCK and SCLK are internally derived from the internal MCLK (after the divide, if MCLKDIV2 is enabled). In Hardware Mode the CODEC operates in single-speed only. In Software Mode, the CODEC operates in either quarter-, half-, single- or double-speed depending on the setting of the SPEED[1:0] bits.

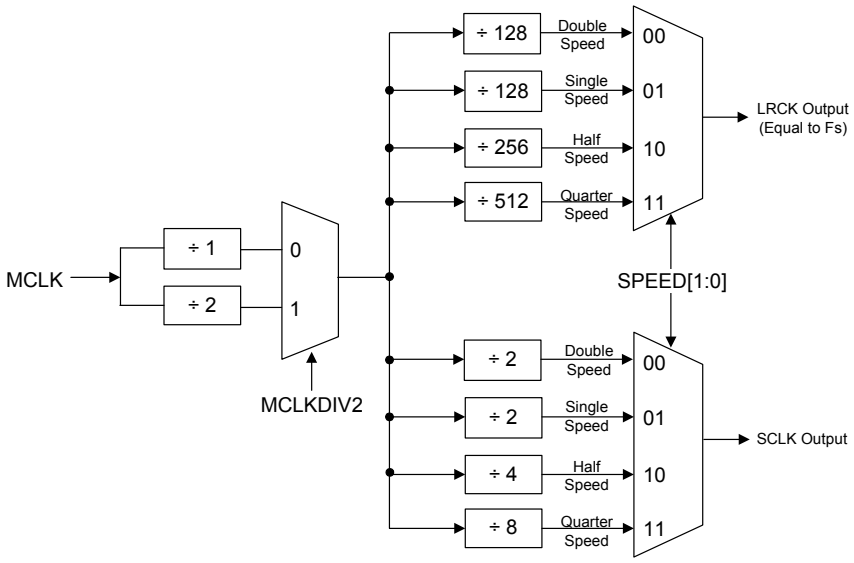


Figure 17. Master Mode Timing

4.5.3 High-Impedance Digital Output

The serial port may be placed on a clock/data bus that allows multiple masters for the serial port I/O without the need for external buffers. The 3ST_SP bit places the internal buffers for these I/O in a high-impedance state, allowing another device to transmit serial port data without bus contention.

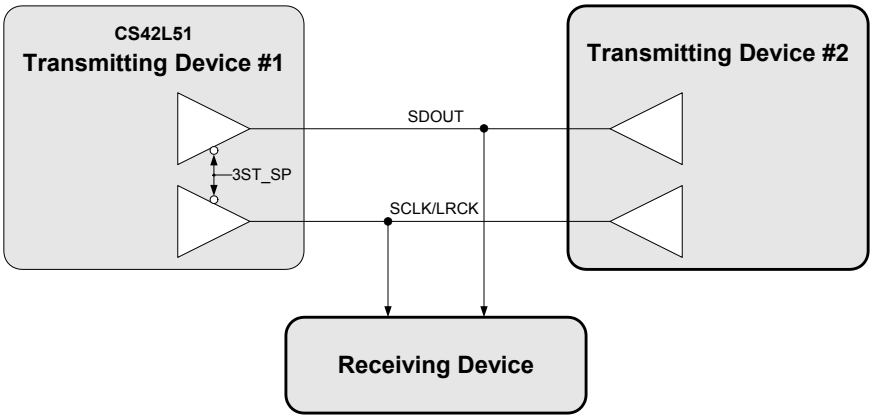


Figure 18. Tri-State Serial Port

4.5.4 Quarter- and Half-Speed Mode

Quarter-Speed Mode (QSM) and Half-Speed Mode (HSM) allow lower sample rates while maintaining a relatively flat noise floor in the typical audio band of 20 Hz - 20 kHz. Single-Speed Mode (SSM) will allow lower frequency sample rates; however, the DAC's noise floor, that normally rises out-of-band, will scale with the lower sample rate and begin to rise within the audio band. QSM and HSM corrects for most of this scaling, effectively increasing the dynamic range of the codec at lower sample rates, relative to SSM.

4.6 Digital Interface Formats

The serial port operates in standard I²S, Left-Justified or Right-Justified (DAC only) digital interface formats with varying bit depths from 16 to 24. Data is clocked out of the ADC or into the DAC on the rising edge of SCLK. Figures 19-21 illustrate the general structure of each format. Refer to "Switching Specifications - Serial Port" on page 19 for exact timing relationship between clocks and data.

Software Control:	"Interface Control (Address 04h)" on page 51.		
Hardware Control:	**Pin**	**Setting**	**Selection**
	"I²S/$\overline{LJ}$" pin 3	LO	Left-Justified Interface
		HI	I²S Interface

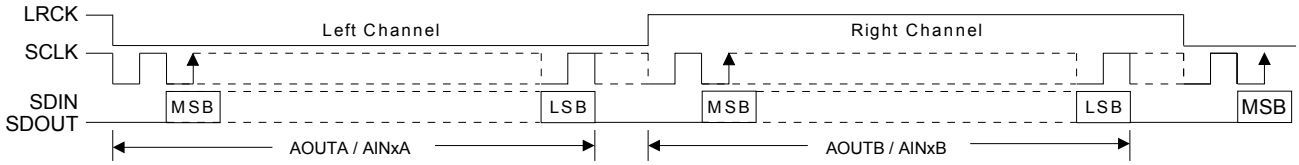


Figure 19. I²S Format

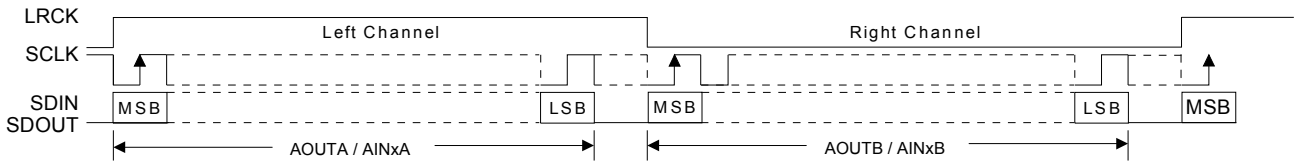


Figure 20. Left-Justified Format

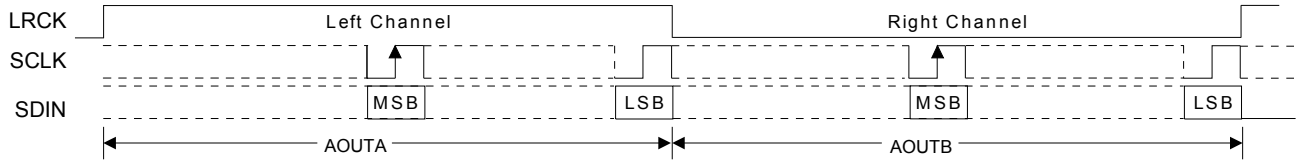


Figure 21. Right-Justified Format (DAC only)

4.7 Initialization

The initialization and Power-Down sequence flowchart is shown in Figure 22 on page 42. The CODEC enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma modulators and control port registers are reset. The internal voltage reference, multi-bit DAC and ADC and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-Down state until the $\overline{\text{RESET}}$ pin is brought high. The control port is accessible once $\overline{\text{RESET}}$ is high and the desired register settings can be loaded per the interface descriptions in "Software Mode" on page 42. If a valid write sequence to the control port is not made within approximately 10 ms, the CODEC will enter Hardware Mode.

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage references, DAC_FILT+ and ADC_FILT+ will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

4.8 Recommended Power-Up Sequence

1. Hold $\overline{\text{RESET}}$ low until the power supplies are stable; no specific power supply sequencing is required.
2. Bring $\overline{\text{RESET}}$ high. After approximately 10 ms, the device will enter Hardware Mode.
3. For Software Mode operation, set the PDN bit to '1'b in under 10 ms. This will place the device in "standby".
4. Load the desired register settings while keeping the PDN bit set to '1'b.
5. Start MCLK to the appropriate frequency, as discussed in Section 4.5. SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
6. Set the PDN bit to '0'b.
7. Bring $\overline{\text{RESET}}$ low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.9 Recommended Power-Down Sequence

To minimize audible pops when turning off or placing the CODEC in standby,

1. Mute the DACs and ADCs.
2. Disable soft ramp and zero-cross volume transitions.
3. Set the PDN bit to 1.
4. Wait at least 100 µs.
   The codec will be fully powered down after this 100 µs delay. Prior to the removal of the master clock (MCLK), this delay of at least 100 µs must be implemented after step 3 to avoid premature disruption of the codec's power down sequence.

   A disruption in the codec's power down sequence (i.e. removing the MCLK signal before this 100 µs delay) has consequences on the headphone amplifier: The charge pump may stop abruptly, causing the headphone amplifiers to drive the outputs up to the +VA_HP supply.

   The disruption of the codec's power down sequence may also cause clicks and pops on the output of the DACs as the modulator holds the last output level before the MCLK signal was removed.
5. Optionally, MCLK may be removed at this time.
6. To achieve the lowest operating quiescent current, bring $\overline{\text{RESET}}$ low. All control port registers will be reset to their default state.
7. Power Supply Removal (Option 1): Switch power supplies to a high impedance state.
8. Power Supply Removal (Option 2): To minimize pops when the power supplies are pulled to ground, a discharge resistor must be added in parallel with the capacitor on the FILT+ pin. With a 1 MΩ resistor and a 2.2 µF capacitor on FILT+, FILT+ will ramp to ground in approximately 5 seconds. A 1 MΩ resistor on FILT+ reduces the full scale input/output voltage by approximately 0.25 dB.

   After step 5, wait the required time for FILT+ to ramp to ground before pulling VA to ground.

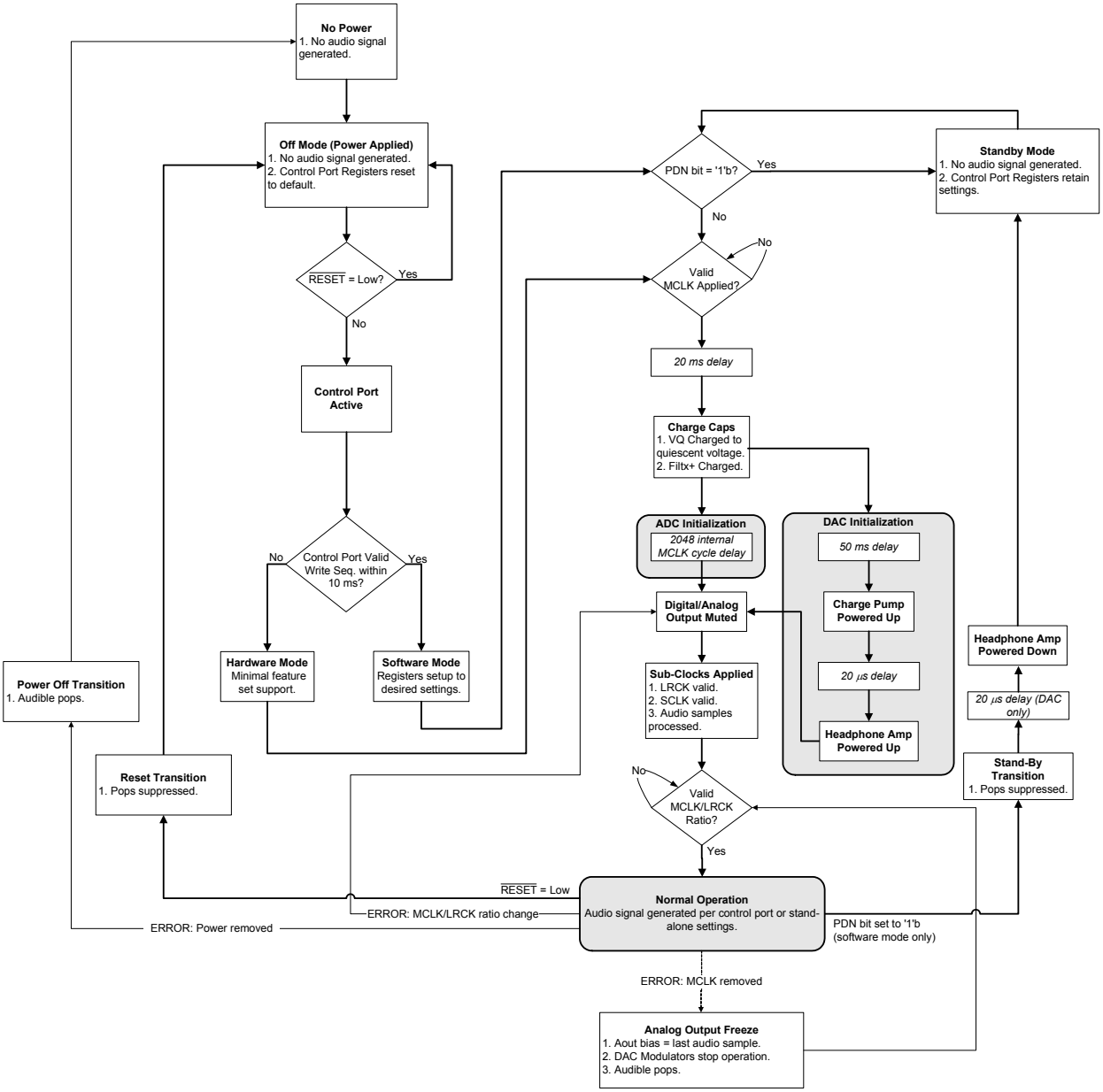


Figure 22. Initialization Flowchart

4.10 Software Mode

The control port is used to access the registers allowing the CODEC to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The device enters software mode only after a successful write command using one of two software protocols: SPI or I²C, with the device acting as a slave. The SPI protocol is permanently selected whenever there is a high-to-low transition on the AD0/CS pin after reset. If using the I²C protocol, pin AD0/CS should be permanently connected to either VL or GND; this option allows the user to slightly alter the chip address as desired.

4.10.1 SPI Control

In Software Mode, $\overline{CS}$ is the CS42L51 chip-select signal, CCLK is the control port bit clock (input into the CS42L51 from the microcontroller), CDIN is the input data line from the microcontroller. Data is clocked in on the rising edge of CCLK. The CODEC supports only write operations. Read requests are ignored.

Figure 23 shows the operation of the control port in Software Mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001010. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP.

There is MAP auto-increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, the MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

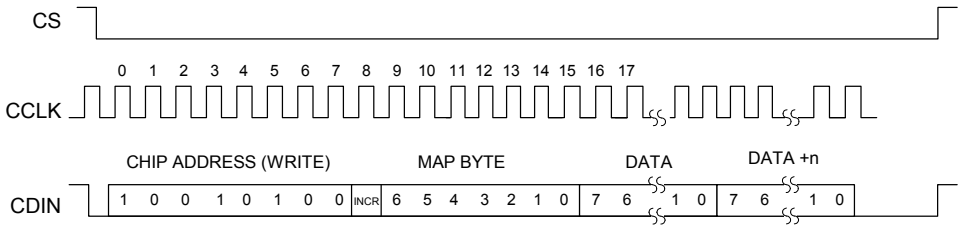


Figure 23. Control Port Timing in SPI Mode

4.10.2 I²C Control

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pin AD0 forms the least significant bit of the chip address and should be connected through a resistor to VL or DGND as desired. The state of the pin is sensed while the CS42L51 is reset.

The signal timings for a read and write cycle are shown in Figure 24 and Figure 25. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS42L51 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100101. To communicate with a CS42L51, the chip address field, which is the first byte sent to the CS42L51, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS42L51 after each input byte is read and is input to the CS42L51 from the microcontroller after each transmitted byte.

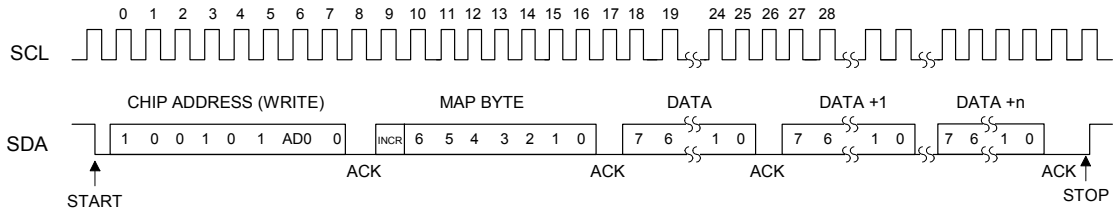


Figure 24. Control Port Timing, I²C Write

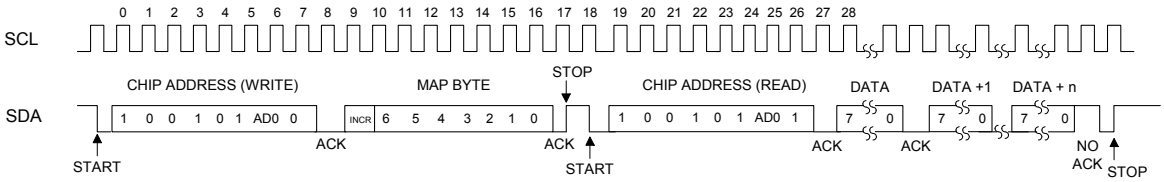


Figure 25. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 25, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 100101x0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto-increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 100101x1 (chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.10.3 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudo code above for implementation details.

4.10.3.1 Map Increment (INCR)

The device has MAP auto-increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

5. REGISTER QUICK REFERENCE

Software mode register defaults are as shown. “Reserved” registers must maintain their default state.

Addr	Function	7	6	5	4	3	2	1	0
01h	ID	Chip_ID4	Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID2	Rev_ID1	Rev_ID0
	p 48 default	1	1	0	1	1	0	0	1
02h	Power Ctl. 1	Reserved	PDN_DACB	PDN_DACA	PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN
	p 48 default	0	0	0	0	0	0	0	0
03h	Speed Ctl. & Power Ctl. 2	AUTO	SPEED1	SPEED0	3-ST_SP	PDN_MICB	PDN_MICA	PDN_ MICBIAS	MCLKDIV2
	p 49 default	1	0	1	0	1	1	1	0
04h	Interface Ctl.	SDOUT->SDIN	M/$\overline{S}$	DAC_DIF2	DAC_DIF1	DAC_DIF0	ADC_I²S/$\overline{LJ}$	DIGMIX	MICMIX
	p 51 default	0	0	0	0	0	0	0	0
05h	MIC Control & Misc.	ADC_SNGVOL	ADCB_ DBOOST	ADCA_ DBOOST	MICBIAS_ SEL	MICBIAS_ LVL1	MICBIAS_ LVL0	MICB_ BOOST	MICA_ BOOST
	p 52 default	0	0	0	0	0	0	0	0
06h	ADC Control	ADCB_HPF EN	ADCB_HP FRZ	ADCA_HPF EN	ADCA_HP FRZ	SOFTB	ZCROSSB	SOFTA	ZCROSSA
	p 53 default	1	0	1	0	0	0	0	0
07h	ADC Input Select , Invert, Mute	AINB_MUX1	AIN- B_MUX0	AINA_MUX1	AINA_MUX0	INV_ADCB	INV_ADCA	ADCB_ MUTE	ADCA_ MUTE
	p 55 default	0	0	0	0	0	0	0	0
08h	DAC Output Control	HP_GAIN2	HP_GAIN1	HP_GAIN0	DAC_SNG VOL	INV_PCMB	INV_PCMA	DACB_ MUTE	DACA_ MUTE
	p 56 default	0	1	1	0	0	0	0	0
09h	DAC Control	DATA_SEL1	DATA_SEL0	FREEZE	Reserved	DEEMPH	AMUTE	DAC_SZC1	DAC_SZC0
	p 57 default	0	0	0	0	0	1	1	0
0Ah	ALCA SZC & PGAA Vol- ume	ALCA_SR DIS	ALCA_ZC DIS	Reserved	PGAA VOL4	PGAA VOL3	PGAA VOL2	PGAA VOL1	PGAA VOL0
	p 58 default	0	0	0	0	0	0	0	0
0Bh	ALCB SZC & PGAB Vol- ume	ALCB_SR DIS	ALCB_ZC DIS	Reserved	PGAB VOL4	PGAB VOL3	PGAB VOL2	PGAB VOL1	PGAB VOL0
	p 58 default	0	0	0	0	0	0	0	0
0Ch	ADCA Atten- uator	ADCA_ ATT7	ADCA_ ATT6	ADCA_ ATT5	ADCA_ ATT4	ADCA_ ATT3	ADCA_ ATT2	ADCA_ ATT1	ADCA_ ATT0
	p 59 default	0	0	0	0	0	0	0	0
0Dh	ADCB Atten- uator	ADCB_ ATT7	ADCB_ ATT6	ADCB_ ATT5	ADCB_ ATT4	ADCB_ ATT3	ADCB_ ATT2	ADCB_ ATT1	ADCB_ ATT0
	p 59 default	0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
0Eh	Vol. Control ADCMIXA	MUTE_ADC MIXA	ADCMIXA VOL6	ADCMIXA VOL5	ADCMIXA VOL4	ADCMIXA VOL3	ADCMIXA VOL2	ADCMIXA VOL1	ADCMIXA VOL0
	p 60 default	1	0	0	0	0	0	0	0
0Fh	Vol. Control ADCMIXB	MUTE_ADC MIXB	ADCMIXB VOL6	ADCMIXB VOL5	ADCMIXB VOL4	ADCMIXB VOL3	ADCMIXB VOL2	ADCMIXB VOL1	ADCMIXB VOL0
	p 60 default	1	0	0	0	0	0	0	0
10h	Vol. Control PCMMIXA	MUTE_PCM MIXA	PCMMIXA VOL6	PCMMIXA VOL5	PCMMIXA VOL4	PCMMIXA VOL3	PCMMIXA VOL2	PCMMIXA VOL1	PCMMIXA VOL0
	p 61 default	1	0	0	0	0	0	0	0
11h	Vol. Control PCMMIXB	MUTE_PCM MIXB	PCMMIXB VOL6	PCMMIXB VOL5	PCMMIXB VOL4	PCMMIXB VOL3	PCMMIXB VOL2	PCMMIXB VOL1	PCMMIXB VOL0
	p 61 default	1	0	0	0	0	0	0	0
12h	BEEP Freq. & OnTime	FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0
	p 61 default	0	0	0	0	0	0	0	0
13h	BEEP Off Time & Vol.	OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0
	p 62 default	0	0	0	0	0	0	0	0
14h	BEEP Control & Tone Config	REPEAT	BEEP	Reserved	TREB_CF1	TREB_CF0	BASS_CF1	BASS_CF0	TC_EN
	p 63 default	0	0	0	0	0	0	0	0
15h	Tone Control	TREB3	TREB2	TREB1	TREB0	BASS3	BASS2	BASS1	BASS0
	p 64 default	1	0	0	0	1	0	0	0
16h	Vol. Control AOUTA	AOUTA_ VOL7	AOUTA_ VOL6	AOUTA_ VOL5	AOUTA_ VOL4	AOUTA_ VOL3	AOUTA_ VOL2	AOUTA_ VOL1	AOUTA_ VOL0
	p 65 default	0	0	0	0	0	0	0	0
17h	Vol. Control AOUTB	AOUTB_ VOL7	AOUTB_ VOL6	AOUTB_ VOL5	AOUTB_ VOL4	AOUTB_ VOL3	AOUTB_ VOL2	AOUTB_ VOL1	AOUTB_ VOL0
	p 65 default	0	0	0	0	0	0	0	0
18h	PCM & ADC Channel Mixer	PCMA1	PCMA0	PCMB1	PCMB0	ADCA1	ADCA0	ADCB1	ADCB0
	p 65 default	0	0	0	0	0	0	0	0
19h	Limiter Threshold & SZC Disable	MAX2	MAX1	MAX0	CUSH2	CUSH1	CUSH0	LIM_SRDIS	LIM_ZCDIS
	p 66 default	0	0	0	0	0	0	0	0
1Ah	Limiter Config & Release Rate	LIMIT_EN	LIMIT_ALL	LIM_R-RATE5	LIM_R-RATE4	LIM_R-RATE3	LIM_R-RATE2	LIM_R-RATE1	LIM_R-RATE0
	p 67 default	0	1	1	1	1	1	1	1

Addr	Function	7	6	5	4	3	2	1	0
1Bh	Limiter Attack Rate	Reserved	Reserved	LIM_ARATE5	LIM_ARATE4	LIM_ARATE3	LIM_ARATE2	LIM_ARATE1	LIM_ARATE0
	p 68 default	0	0	0	0	0	0	0	0
1Ch	ALC Enable & Attack Rate	ALC_ENB	ALC_ENA	ALC_A-RATE5	AAL-C_RATE4	ALC_A-RATE3	ALC_A-RATE2	ALC_A-RATE1	ALC_A-RATE0
	p 68 default	0	0	0	0	0	0	0	0
1Dh	ALC Release Rate	Reserved	Reserved	ALC_R-RATE5	ALC_R-RATE4	ALC_R-RATE3	ALC_R-RATE2	ALC_R-RATE1	ALC_R-RATE0
	p 69 default	0	0	1	1	1	1	1	1
1Eh	ALC Thresh-old	MAX2	MAX1	MAX0	MIN2	MIN1	MIN0	Reserved	Reserved
	p 69 default	0	0	0	0	0	0	0	0
1Fh	Noise Gate Config	NG_ALL	NG_EN	NG_BOOST	THRESH2	THRESH1	THRESH0	NGDELAY1	NGDELAY0
	p 70 default	0	0	0	0	0	0	0	0
20h	Status	Reserved	SP_CLK ERR	SPEB_OVFL	SPEA_OVFL	PCMA_OVFL	PCMB_OVFL	ADCA_OVFL	ADCB_OVFL
	p 71 default	0	0	0	0	0	0	0	0
21h	Charge Pump Frequency	CHRG_ FREQ3	CHRG_ FREQ2	CHRG_ FREQ1	CHRG_ FREQ0	Reserved	Reserved	Reserved	Reserved
	p 72 default	0	1	0	1	0	0	0	0

6. REGISTER DESCRIPTION

All registers are read/write except for the chip I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is listed in each bit description.
All “Reserved” registers must maintain their default state.

Note: Certain functions are only available when the “Signal Processing Engine to DAC” option is selected using the DATA_SEL[1:0] bits, as described in section “DAC Data Selection (DATA_SEL[1:0])” on page 57.

6.1 Chip I.D. and Revision Register (Address 01h) (Read Only)

7	6	5	4	3	2	1	0
Chip_ID4	Chip_ID3	Chip_ID2	Chip_ID1	Chip_ID0	Rev_ID2	Rev_ID1	Rev_ID0

Chip I.D. (Chip_ID[4:0])

Default: 11011

Function:

I.D. code for the CS42L51. Permanently set to 11011.

Chip Revision (Rev_ID[2:0])

Default: 001

Function:

CS42L51 revision level. Revision B is coded as 001. Revision A is coded as 000.

6.2 Power Control 1 (Address 02h)

7	6	5	4	3	2	1	0
Reserved	PDN_DACB	PDN_DACA	PDN_PGAB	PDN_PGAA	PDN_ADCB	PDN_ADCA	PDN

Notes:

1. To activate the power-down sequence for individual channels (A or B,) *both* channels must first be powered down either by enabling the PDN bit or by enabling the power-down bits for both channels. Enabling the power-down bit on an individual channel basis after the CODEC has fully powered up will mute the selected channel without achieving any power savings.

Recommended channel power-down sequence: 1.) Enable the PDN bit, 2.) enable power-down for the select channels, 3.) disable the PDN bit.

Power Down DAC X (PDN_DACX)

Default: 0

0 - Disable
1 - Enable

Function:

DAC channel x will either enter a power-down or muted state when this bit is enabled. See above.

Power Down PGA X (PDN_PGAX)

Default: 0

0 - Disable
1 - Enable

Function:

PGA channel x will either enter a power-down or muted state when this bit is enabled. See Power Control 1 (Address 02h) page 48 above.

This bit is used in conjunction with AINx_MUX bits to determine the analog input path to the ADC. Refer to "ADCX Input Select Bits (AINX_MUX[1:0])" on page 55 for the required settings.

Power Down ADC X (PDN_ADCX)

Default: 0

0 - Disable
1 - Enable

Function:

ADC channel x will either enter a power-down or muted state when this bit is enabled. See Note 1 on page 48.

Power Down (PDN)

Default: 0

0 - Disable
1 - Enable

Function:

The entire CODEC will enter a low-power state when this function is enabled. The contents of the control port registers are retained in this mode.

6.3 MIC Power Control & Speed Control (Address 03h)

7	6	5	4	3	2	1	0
AUTO	SPEED1	SPEED0	3-ST_SP	PDN_MICB	PDN_MICA	PDN_MICBIAS	MCLKDIV2

Auto-Detect Speed Mode (AUTO)

Default: 1

0 - Disable
1 - Enable

Function:

Enables the auto-detect circuitry for detecting the speed mode of the CODEC when operating as a slave. When AUTO is enabled, the MCLK/LRCK ratio must be implemented according to Table 3 on page 38. The SPEED[1:0] bits are ignored when this bit is enabled. Speed is determined by the MCLK/LRCK ratio.

Speed Mode (SPEED[1:0])

Default: 01

11 - Quarter-Speed Mode (QSM) - 4 to 12.5 kHz sample rates
10 - Half-Speed Mode (HSM) - 12.5 to 25 kHz sample rates
01 - Single-Speed Mode (SSM) - 4 to 50 kHz sample rates
00 - Double-Speed Mode (DSM) - 50 to 100 kHz sample rates

Function:

Sets the appropriate speed mode for the CODEC in Master or Slave Mode. QSM is optimized for 8 kHz sample rate and HSM is optimized for 16 kHz sample rate. These bits are ignored when the AUTO bit is enabled (see Auto-Detect Speed Mode (AUTO) above).

Tri-State Serial Port Interface (3ST_SP)

Default: 0

0 - Disable
1 - Enable

Function:

When enabled and the device is configured as a master, all serial port outputs (clocks and data) are placed in a high impedance state. If the serial port is configured as a slave, only the SDOUT pin will be placed in a high-impedance state. The other signals will remain as inputs.

Power Down MIC X (PDN_MICX)

Default: 1

0 - Disable
1 - Enable

Function:

When enabled, the microphone pre-amplifier for channel x will be in a power-down state.

Power Down MIC BIAS (PDN_MICBIAS)

Default: 1

0 - Disable
1 - Enable

Function:

When enabled, the microphone bias circuit will be in a power-down state.

MCLK Divide By 2 (MCLKDIV2)

Default: 0

0 - Disabled
1 - Divide by 2

Function:

Divides the input MCLK by 2 prior to all internal circuitry. This bit is ignored when the AUTO bit is disabled in Slave Mode.

6.4 Interface Control (Address 04h)

7	6	5	4	3	2	1	0
SDOUT->SDIN	M/S	DAC_DIF2	DAC_DIF1	DAC_DIF0	ADC_I²S/LJ	DIGMIX	MICMIX

SDOUT to SDIN Loopback (SDOUT->SDIN)

Default: 0

0 - Disabled; SDOUT internally disconnected from SDIN
1 - Enabled; SDOUT internally connected to SDIN

Function:

Internally loops the signal on the SDOUT pin to SDIN.

Master/Slave Mode (M/$\overline{S}$)

Default: 0

0 - Slave
1 - Master

Function:

Selects either master or slave operation for the serial port.

DAC Digital Interface Format (DAC_DIF[2:0])

Default = 000

DAC_DIF[2:0]	Description	Figure
000	Left-Justified, up to 24-bit data	20 on page 40
001	I²S, up to 24-bit data	19 on page 39
010	Right-Justified, 24-bit data	21 on page 40
011	Right-Justified, 20-bit data	21 on page 40
100	Right-Justified, 18-bit data	21 on page 40
101	Right-Justified, 16-bit data	21 on page 40
110	Reserved	-
100	Reserved	-

Function:

Selects the digital interface format used for the data in on SDIN. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in the section “Digital Interface Formats” on page 39.

ADC I²S or Left-Justified (ADC_I²S/$\overline{LJ}$)

Default: 0

0 - Left-Justified
1 - I²S

Function:

Selects either the I²S or Left-Justified digital interface format for the data on SDOUT. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in this section .

Digital Mix (DIGMIX)

Default: 0

DIGMIX	DATA_SEL[1:0]	Mix Selected
0	xx	No Mix: ADC to ADC serial port, SDOUT data.
1	00	No Mix: SDIN data to ADC serial port, SDOUT data.
	01	Mix: ADC + SDIN data to ADC serial port, SDOUT data.
	10	No Mix: ADC to ADC serial port, SDOUT data.
	11	Reserved

Function:

Selects between the ADC or a digital mix of the ADC and DAC into the serial port to the SDOUT pin. This mix function is affected by the data select bits DATA_SEL[1:0].

Microphone Mix (MICMIX)

Default: 0

0 - Disabled; No Mix: Left/Right Channel to ADC serial port, SDOUT.
1 - Enabled; Mix: Differential mix ((A-B)/2)to ADC serial port, SDOUT.

Function:

Selects between the ADC stereo mix or a differential mix of analog inputs A and B.

6.5 MIC Control (Address 05h)

7	6	5	4	3	2	1	0
ADC_SNGVOL	ADCB_DBOOST	ADCA_DBOOST	MICBIAS_SEL	MICBIAS_LVL1	MICBIAS_LVL0	MICB_BOOST	MICA_BOOST

ADC Single Volume Control (ADC_SNGVOL)

Default: 0

0 - Disabled
1 - Enabled

Function:

The individual PGA Volume (PGAx_VOLx) and ADC channel attenuation (ADCx_ATTx) levels as well as the ALC A and B enable (ALC_ENx) are independently controlled by their respective control registers when this function is disabled. When enabled, the volume on both channels is determined by the ADCA Attenuator Control register, or the PGAA Control register, and the ADCB Attenuator and PGAB Control registers are ignored. The ALC enable control for channel B is controlled by the ALC A enable when the ADC_SNGVOL bit is enabled and the ALC_ENB control register is ignored.

ADCx 20 dB Digital Boost (ADCx_DBOOST)

Default: 0

0 - Disabled
1 - Enabled

Function:

Applies a 20 dB digital gain to the input signal on ADC channel x, regardless of the input path.

MIC Bias Select (MICBIAS_SEL)

Default: 0

0 - MICBIAS on AIN3B/MICIN2 pin
1 - MICBIAS on AIN2B pin

Function:

Determines the output pin for the internally generated MICBIAS signal. If set to '0'b, the MICBIAS is output on the AIN3B/MICIN2 pin. If set to '1'b, the MICBIAS is output on the AIN2B pin.

MIC Bias Level (MICBIAS_LVL[1:0])

Default: 00

00 - 0.8 x VA
01 - 0.7 x VA
10 - 0.6 x VA
11 - 0.5 x VA

Function:

Determines the output voltage level of the MICBIAS output.

MIC X Preamplifier Boost (MICX_BOOST)

Default: 0

0 - +16 dB Gain
1 - +32 dB Gain

Function:

Determines the amount of gain applied to the microphone preamplifier for channel x.

6.6 ADC Control (Address 06h)

7	6	5	4	3	2	1	0
ADCB_HPFEN	ADCB_HPFRZ	ADCA_HPFEN	ADCA_HPFRZ	SOFTB	ZCROSSB	SOFTA	ZCROSSA

ADCX High-Pass Filter Enable (ADCX_HPFEN)

Default: 1

0 - High-pass filter is disabled
1 - High-pass filter is enabled

Function:

When this bit is set, the internal high-pass filter will be enabled for ADCx. When set to '0', the high-pass filter will be disabled. For DC measurements, this bit must be cleared to '0'. See "ADC Digital Filter Characteristics" on page 14.

ADCX High-Pass Filter Freeze (ADCX_HPFRZ)

Default: 0

0 - Continuous DC Subtraction
1 - Frozen DC Subtraction

Function:

The high-pass filter works by continuously subtracting a measure of the DC offset from the output of the decimation filter. If the ADCx_HPFRZ bit is taken high during normal operation, the current value of the DC offset is frozen, and this DC offset will continue to be subtracted from the conversion result. For DC measurements, this bit must be set to '1'. See "ADC Digital Filter Characteristics" on page 14.

Soft Ramp CHX Control (SOFTX)

Default: 0

0 - Disabled
1 - Enabled

Function:

Soft Ramp allows level changes to be implemented via an incremental ramp. ADCx_ATT[7:0] digital attenuation changes are ramped from the current level to the new level at a rate of 0.125 dB per LRCK period. PGAx_VOL[4:0] gain changes are ramped in 0.5 dB steps every 16 LRCK periods.

Soft Ramp & Zero Cross Enabled
When used in conjunction with the ZCROSSx bit, the PGAx_VOL[4:0] gain changes will occur in 0.5 dB steps and be implemented on a signal zero-crossing.

Zero Cross CHX Control (ZCROSSX)

Default: 0

0 - Disabled
1 - Enabled

Function:

Zero Cross Enable dictates that signal level changes will occur on a signal zero-crossing to minimize audible artifacts. The requested level change will occur after a timeout period of 1024 sample periods (approximately 10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero-crossing. The zero-cross function is independently monitored and implemented for each channel.

Soft Ramp & Zero Cross Enabled
When used in conjunction with the SOFTx bit, the PGAx_VOL[4:0] gain changes will occur in 0.5 dB steps and be implemented on a signal zero-crossing.

The ADC Attenuator ADCx_ATT[7:0] is not affected by the ZCROSSx bit.

SOFTx	**ZCROSSx**	**Analog PGA Volume** (PGAx_VOL[4:0])	**Digital Attenuator** (ADCx_ATT[7:0])
0	0	Volume changes immediately.	Volume changes immediately.
0	1	Volume changes at next zero-cross time.	Volume changes immediately.
1	0	Volume changes in 0.5 dB steps.	Change volume in 0.125 dB steps.
1	1	Volume changes in 0.5 dB steps at every signal zero-cross.	Change volume in 0.125 dB steps.

6.7 ADCx Input Select, Invert & Mute (Address 07h)

7	6	5	4	3	2	1	0
AINB_MUX1	AINB_MUX0	AINA_MUX1	AINA_MUX0	INV_ADCB	INV_ADCA	ADCB_MUTE	ADCA_MUTE

ADCX Input Select Bits (AINX_MUX[1:0])

Default: 00

PDN_PGAx	AINx_MUX[1:0]	Selected Path to ADC
0	00	AIN1x-->PGAx
0	01	AIN2x-->PGAx
0	10	AIN3x/MICINx-->PGAx
0	11	AIN3x/MICINx-->Pre-Amp*(+16/+32 dB Gain)*-->PGAx
1	00	AIN1x
1	01	AIN2x
1	10	AIN3x/MICINx
1	11	Reserved

Function:

Selects the specified analog input signal into ADCx. The microphone pre-amplifier is only available when PDN_PGAx is disabled. See Figure 26.

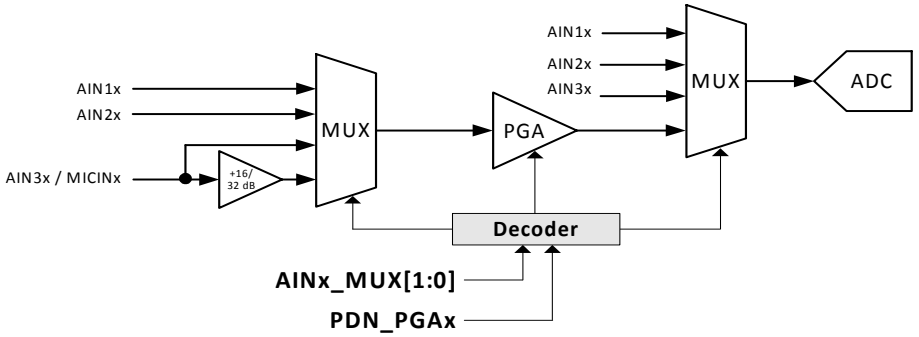


Figure 26. AIN & PGA Selection

ADCX Invert Signal Polarity (INV_ADCX)

Default: 0

0 - Disabled
1 - Enabled

Function:

When enabled, this bit will invert the signal polarity of the ADC x channel.

ADCX Channel Mute (ADCX_MUTE)

Default: 0

0 - Disabled
1 - Enabled

Function:

The output of channel x ADC will mute when enabled. The muting function is affected by the ADCx Soft bit (SOFT).

6.8 DAC Output Control (Address 08h)

7	6	5	4	3	2	1	0
HP_GAIN2	HP_GAIN1	HP_GAIN0	DAC_ SNGVOL	INV_PCMB	INV_PCMA	DACB_MUTE	DACA_MUTE

Headphone Analog Gain (HP_GAIN[2:0])

Default: 011

HP_GAIN[2:0]	Gain Setting
000	0.3959
001	0.4571
010	0.5111
011	0.6047
100	0.7099
101	0.8399
110	1.0000
111	1.1430

Function:

These bits select the gain multiplier for the headphone/line outputs. See "Line Output Voltage Characteristics" on page 17 and "Headphone Output Power Characteristics" on page 18.

DAC Single Volume Control (DAC_SNGVOL)

Default: 0

Function:

The individual channel volume levels are independently controlled by their respective Volume Control registers when this function is disabled. When enabled, the volume on all channels is determined by the AOUTA Volume Control register and the AOUTB Volume Control register is ignored.

PCMX Invert Signal Polarity (INV_PCMX)

Default: 0

0 - Disabled
1 - Enabled

Function:

When enabled, this bit will invert the signal polarity of the PCM x channel.

DACX Channel Mute (DACX_MUTE)

Default: 0

0 - Disabled
1 - Enabled

Function:

The output of channel x DAC will mute when enabled. The muting function is affected by the DACx Soft and Zero Cross bits (DACx_SZC[1:0]).

6.9 DAC Control (Address 09h)

7	6	5	4	3	2	1	0
DATA_SEL1	DATA_SEL0	FREEZE	Reserved	DEEMPH	AMUTE	DAC_SZC1	DAC_SZC0

DAC Data Selection (DATA_SEL[1:0])

Default: 00

00 - PCM Serial Port to DAC
01 - Signal Processing Engine to DAC
10 - ADC Serial Port to DAC
11 - Reserved

Function:

Selects the digital signal source for the DAC.

Note: Certain functions are only available when the “Signal Processing Engine to DAC” option is selected using these bits.

Freeze Controls (FREEZE)

Default: 0

Function:

This function will freeze the previous settings of, and allow modifications to be made to all control port registers without the changes taking effect until the FREEZE is disabled. To have multiple changes in the control port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

Note:

1. This bit should only be used to synchronize run-time controls, such as volume and mute, during normal operation. Using this bit before the relevant circuitry begins normal operation could cause the change to take effect immediately, ignoring the FREEZE bit.

DAC De-Emphasis Control (DEEMPH)

Default: 0

0 - No De-Emphasis
1 - De-Emphasis Enabled

Function:

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control.

Enables the digital filter to apply the standard 15μs/50μs digital de-emphasis filter response for a sample rate of 44.1 kHz.

Analog Output Auto MUTE (AMUTE)

Default: 0

0 - Auto Mute Disabled
1 - Auto Mute Enabled

Function:
Enables (or disables) Automatic Mute of the analog outputs after 8192 “0” samples on each digital input channel.

DAC Soft Ramp and Zero Cross Control (DAC_SZC[1:0])

Default = 10

00 - Immediate Change
01 - Zero Cross
10 - Soft Ramp
11 - Soft Ramp on Zero Crossings

Function:

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control

Immediate Change

When Immediate Change is selected all volume-level changes will take effect immediately in one step.

Zero Cross

This setting dictates that signal-level changes, either by gain changes, attenuation changes or muting, will occur on a signal zero-crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 1024 and 2048 sample periods (21.3 ms to 42.7 ms at 48 kHz sample rate) if the signal does not encounter a zero-crossing. The zero-cross function is independently monitored and implemented for each channel. **Note:** The LIM_SRDIS bit is ignored.

Soft Ramp

Soft Ramp allows level changes, either by gain changes, attenuation changes or muting, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 0.5 dB per 4 left/right clock periods.

Soft Ramp on Zero Crossing

This setting dictates that signal-level changes, either by gain changes, attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero-crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero-crossing. The zero-cross function is independently monitored and implemented for each channel. **Note:** The LIM_SRDIS bit is ignored.

6.10 ALCX & PGAX Control: ALCA, PGAA (Address 0Ah) & ALCB, PGAB (Address 0Bh)

7	6	5	4	3	2	1	0
ALCX_SRDIS	ALCX_ZCDIS	Reserved	PGAX_VOL4	PGAX_VOL3	PGAX_VOL2	PGAX_VOL1	PGAX_VOL0

ALCX Soft Ramp Disable (ALCX_SRDIS)

Default: 0

0 - Off
1 - On

Function:

Overrides the SOFTx bit setting for the ADC. When this bit is set, the ALC attack rate in the PGA will not be dictated by the soft ramp setting. ALC volume-level changes will take effect in one step.

ALCX Zero Cross Disable (ALCX_ZCDIS)

Default: 0

0 - Off
1 - On

Function:

Overrides the ZCROSSx bit setting for the ADC. When this bit is set, the ALC attack rate in the PGA will not be dictated by the zero-cross setting. ALC volume-level changes will take effect immediately in one step.

PGA X Gain Control (PGAX_VOL[4:0])

Default: 00000

Binary Code	Volume Setting
11000	+12 dB
…	…
01010	+5 dB
…	…
00000	0 dB
11111	-0.5 dB
11110	-1 dB
…	…
11001	-3 dB
11010	-3 dB

Function:

The PGAx Gain Control register allows independent setting of the signal levels in 0.5 dB increments as dictated by the ADCx Soft and Zero Cross bits (SOFTx & ZCROSSx) from +12 dB to -3 dB. Gain settings are decoded as shown in the table above. The gain changes are implemented as dictated by the ALCX Soft & Zero Cross bits (ALCX_SRDIS & ALCX_ZCDIS).

Note: When the ALC is enabled, the PGA is automatically controlled and should not be adjusted manually.

6.11 ADCx Attenuator: ADCA (Address 0Ch) & ADCB (Address 0Dh)

7	6	5	4	3	2	1	0
ADCx_ATT7	ADCx_ATT6	ADCx_ATT5	ADCx_ATT4	ADCx_ATT3	ADCx_ATT2	ADCx_ATT1	ADCx_ATT0

ADCX Attenuation Control (ADCX_ATT[7:0])

Default: 00h

Binary Code	Volume Setting
0111 1111	0 dB
…	…
0000 0000	0 dB
1111 1111	-1 dB
1111 1110	-2 dB
…	…
1010 0000	-96 dB
…	…
1000 0000	-96 dB

Function:

The level of ADCX can be adjusted in 1.0 dB increments as dictated by the ADCx Soft and Zero Cross bits (SOFTx & ZCROSSx) from 0 to -96 dB. Levels are decoded in two's complement, as shown in the table above.

Note: When the ALC is enabled, the Attenuator and PGA volume is automatically controlled and should not be adjusted manually.

6.12 ADCx Mixer Volume Control: ADCA (Address 0Eh) & ADCB (Address 0Fh)

7	6	5	4	3	2	1	0
MUTE_ADCMIXx	ADCMIXx_VOL6	ADCMIXx_VOL5	ADCMIXx_VOL4	ADCMIXx_VOL3	ADCMIXx_VOL2	ADCMIXx_VOL1	ADCMIXx_VOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

ADCX Mixer Channel Mute (MUTE_ADCMIXX)

Default: 1

0 - Disabled
1 - Enabled

Function:

The ADC channel X input to the output mixer will mute when enabled. The muting function is affected by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]).

ADCX Mixer Volume Control (ADCMIXX_VOL[6:0])

Default = 000 0000

Binary Code	Volume Setting
001 1000	+12.0 dB
…	…
000 0000	0 dB
111 1111	-0.5 dB
111 1110	-1.0 dB
…	…
001 1001	-51.5 dB

Function:

The level of the ADCX input to the output mixer can be adjusted in 0.5 dB increments as dictated by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]) from +12 to -51.5 dB. Levels are decoded as shown in the table above.

6.13 PCMX Mixer Volume Control: PCMA (Address 10h) & PCMB (Address 11h)

7	6	5	4	3	2	1	0
MUTE_ PCMMIXx	PCMMIXx_ VOL6	PCMMIXx_ VOL5	PCMMIXx_ VOL4	PCMMIXx_ VOL3	PCMMIXx_ VOL2	PCMMIXx_ VOL1	PCMMIXx_ VOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

PCMX Mixer Channel Mute (MUTE_PCMMIXX)

Default = 1

0 - Disabled
1 - Enabled

Function:

The PCM channel X input to the output mixer will mute when enabled. The muting function is affected by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]).

PCMX Mixer Volume Control (PCMMIXX_VOL[6:0])

Default: 000 0000

Binary Code	Volume Setting
001 1000	+12.0 dB
…	…
000 0000	0 dB
111 1111	-0.5 dB
111 1110	-1.0 dB
…	…
001 1001	-51.5 dB

Function:

The level of the PCMX input to the output mixer can be adjusted in 0.5 dB increments as dictated by the DACX Soft and Zero Cross bits (DACX_SZC[1:0]) from +12 to -51.5 dB. Levels are decoded as described in the table above.

6.14 Beep Frequency & Timing Configuration (Address 12h)

7	6	5	4	3	2	1	0
FREQ3	FREQ2	FREQ1	FREQ0	ONTIME3	ONTIME2	ONTIME1	ONTIME0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Beep Frequency (FREQ[3:0])

Default: 0000

FREQ[3:0]	Frequency Fs = 12, 24, 48 or 96 kHz	Pitch
0000	260.87 Hz	C4
0001	521.74 Hz	C5
0010	585.37 Hz	D5
0011	666.67 Hz	E5
0100	705.88 Hz	F5
0101	774.19 Hz	G5

FREQ[3:0]	Frequency Fs = 12, 24, 48 or 96 kHz	Pitch
0110	888.89 Hz	A5
0111	1000.00 Hz	B5
1000	1043.48 Hz	C6
1001	1200.00 Hz	D6
1010	1333.33 Hz	E6
1011	1411.76 Hz	F6
1100	1600.00 Hz	G6
1101	1714.29 Hz	A6
1110	2000.00 Hz	B6
1111	2181.82 Hz	C7

Function:

The frequency of the beep signal can be adjusted from 260.87 Hz to 2181.82 Hz. Beep frequency will scale directly with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to Figure 15 on page 35 for single, multiple and continuous beep configurations using the REPEAT and BEEP bits.

Beep On Time Duration (ONTIME[3:0])

Default: 0000

TIME[3:0]	On Time Fs = 12, 24, 48 or 96 kHz
0000	86 ms
…	…
1111	5.2 s

Function:

The on-duration of the beep signal can be adjusted from approximately 86 ms to 5.2 s. The on-duration will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to Figure 15 on page 35 for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits.

6.15 Beep Off Time & Volume (Address 13h)

7	6	5	4	3	2	1	0
OFFTIME2	OFFTIME1	OFFTIME0	BPVOL4	BPVOL3	BPVOL2	BPVOL1	BPVOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control in this register.

Beep Off Time (OFFTIME[2:0])

Default: 000

OFFTIME[2:0]	Off Time Fs = 12, 24, 48 or 96 kHz
000	1.23 s
001	2.58 s
010	3.90 s
011	5.20 s
100	6.60 s
101	8.05 s
110	9.35 s
111	10.80 s

Function:

The off-duration of the beep signal can be adjusted from approximately 75 ms to 680 ms. The off-duration will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode. Refer to Figure 15 on page 35 for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits.

Beep Volume (BPVOL[4:0])

Default: 00000

Binary Code	Volume Setting
00110	+12.0 dB
…	…
00000	0 dB
11111	-2 dB
11110	-4 dB
…	…
00111	-50 dB

Function:

The level of the beep into the output mixer can be adjusted in 2.0 dB increments from +12 dB to -50 dB. Refer to Figure 15 on page 35 for single-, multiple- and continuous-beep configurations using the REPEAT and BEEP bits. Levels are decoded as described in the table above.

6.16 Beep Configuration & Tone Configuration (Address 14h)

7	6	5	4	3	2	1	0
REPEAT	BEEP	Reserved	TREB_CF1	TREB_CF0	BASS_CF1	BASS_CF0	TC_EN

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control in this register.

Repeat Beep (REPEAT)

Default: 0

0 - Disabled
1 - Enabled

Function:

This bit is used in conjunction with the BEEP bit to mix a continuous or periodic beep with the analog output. Refer to Figure 15 on page 35 for a description of each configuration option.

Beep (BEEP)

Default: 0

0 - Disabled
1 - Enabled

Function:

This bit is used in conjunction with the REPEAT bit to mix a continuous or periodic beep with the analog output. **Note:** Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration. Refer to Figure 15 on page 35 for a description of each configuration option.

Treble Corner Frequency (TREB_CF[1:0])

Default: 00

00 - 5 kHz
01 - 7 kHz
10 - 10 kHz
11 - 15 kHz

Function:

The treble corner frequency is user selectable as shown above.

Bass Corner Frequency (BASS_CF[1:0])

Default: 00
00 - 50 Hz
01 - 100 Hz
10 - 200 Hz
11 - 250 Hz

Function:

The bass corner frequency is user-selectable as shown above.

Tone Control Enable (TC_EN)

Default = 0

0 - Disabled
1 - Enabled

Function:

The Bass and Treble tone control features are active when this bit is enabled.

6.17 Tone Control (Address 15h)

7	6	5	4	3	2	1	0
TREB3	TREB2	TREB1	TREB0	BASS3	BASS2	BASS1	BASS0

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control in this register.

Treble Gain Level (TREB[3:0])

Default: 1000 dB (No Treble Gain)

Binary Code	Gain Setting
0000	+12.0 dB
…	…
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
…	…
1111	-10.5 dB

Function:

The level of the shelving treble gain filter is set by Treble Gain Level. The level can be adjusted in 1.5 dB increments from +12.0 to -10.5 dB.

Bass Gain Level (BASS[3:0])

Default: 1000 dB (No Bass Gain)

Binary Code	Gain Setting
0000	+12.0 dB
…	…
0111	+1.5 dB
1000	0 dB
1001	-1.5 dB
…	…
1111	-10.5 dB

Function:

The level of the shelving bass gain filter is set by Bass Gain Level. The level can be adjusted in 1.5 dB increments from +10.5 to -10.5 dB.

6.18 AOUTx Volume Control: AOUTA (Address 16h) & AOUTB (Address 17h)

7	6	5	4	3	2	1	0
AOUTx_VOL7	AOUTx_VOL6	AOUTx_VOL5	AOUTx_VOL4	AOUTx_VOL3	AOUTx_VOL2	AOUTx_VOL1	AOUTx_VOL0

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control in this register.

AOUTX Volume Control (AOUTX_VOL[7:0])

Default = 00h

Binary Code	Volume Setting
0001 1000	+12.0 dB
…	…
0000 0000	0 dB
1111 1111	-0.5 dB
1111 1110	-1.0 dB
…	…
0011 0100	-102 dB
…	…
0001 1001	-102 dB

Function:

The analog output levels can be adjusted in 0.5 dB increments from +12 to -102 dB as dictated by the DAC Soft and Zero Cross bits (DACX_SZC[1:0]). Levels are decoded in unsigned binary as described in the table above.

Note: When the limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be achieved using the PCMMIXx_VOL[6:0] bits.

6.19 PCM Channel Mixer (Address 18h)

7	6	5	4	3	2	1	0
PCMA1	PCMA0	PCMB1	PCMB0	ADCA1	ADCA0	ADCB1	ADCB0

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control in this register.

Channel Mixer (PCMx[1:0] & ADCx[1:0])

Default: 00

PCMA[1:0] and/or ADCA[1:0]	AOUTA	PCMB[1:0] and/or ADCB[1:0]	AOUTB
00	L	00	R
01	$\frac{L+R}{2}$	01	$\frac{L+R}{2}$
10		10	
11	R	11	L

Function:

Implements mono mixes of the left and right channels as well as a left/right channel swap.

6.20 Limiter Threshold SZC Disable (Address 19h)

7	6	5	4	3	2	1	0
MAX2	MAX1	MAX0	CUSH2	CUSH1	CUSH0	LIM_SRDIS	LIM_ZCDIS

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Maximum Threshold (MAX[2:0])

Default: 000

MAX[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
101	-12
101	-18
110	-24
111	-30

Function:

Sets the maximum level, below full scale, at which to limit and attenuate the output signal at the attack rate. Bass, Treble and digital gain settings that boost the signal beyond the maximum threshold may trigger an attack.

Cushion Threshold (CUSH[2:0])

Default: 000

CUSH[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
101	-12
101	-18
110	-24
111	-30

Function:

Sets a cushion level below full scale. This setting is usually set slightly below the maximum (MAX[2:0]) threshold. The Limiter uses this cushion as a hysteresis point for the input signal as it maintains the signal below the maximum as well as below the cushion setting. This provides a more natural sound as the limiter attacks and releases.

Limiter Soft Ramp Disable (LIM_SRDIS)

Default: 0

0 - Off
1 - On

Function:

Overrides the DAC_SZC setting. When this bit is set, the Limiter attack and release rate will not be dictated by the soft ramp setting. **Note:** This bit is ignored when the zero-cross function is enabled (i.e. when DAC_SZC[1:0] = '01'b or '11'b.)

Limiter Zero Cross Disable (LIM_ZCDIS)

Default: 0

0 - Off
1 - On

Function:

Overrides the DAC_SZC setting. When this bit is set, the Limiter attack and release rate will not be dictated by the zero-cross setting.

6.21 Limiter Release Rate Register (Address 1Ah)

7	6	5	4	3	2	1	0
LIMIT_EN	LIMIT_ALL	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0

Note: The DATA_SEL[1:0] bits in reg09h must be set to '01'b to enable function control in this register.

Peak Detect and Limiter Enable (LIMIT_EN)

Default: 0

0 - Disabled
1 - Enabled

Function:

Limits the maximum signal amplitude to prevent clipping when this function is enabled. Peak Signal Limiting is performed by digital attenuation. **Note:** When the limiter is enabled, the AOUT Volume is automatically controlled and should not be adjusted manually. Alternative volume control may be realized using the PCMMIXx_VOL[6:0] bits.

Peak Signal Limit All Channels (LIMIT_ALL)

Default: 1

0 - Individual Channel
1 - Both channel A & B

Function:

When set to 0, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on the specific channel indicating clipping. The other channels will not be affected.

When set to 1, the peak signal limiter will limit the maximum signal amplitude to prevent clipping on both channels in response to any single channel indicating clipping.

Limiter RELEASE Rate (RRATE[5:0])

Default: 111111

Binary Code	Release Time
000000	Fastest Release
…	…
111111	Slowest Release

Function:

Sets the rate at which the limiter releases the digital attenuation from levels below the minimum setting in the limiter threshold register, and returns the analog output level to the AOUTx_VOL[7:0] setting.

The limiter release rate is user selectable but is also a function of the sampling frequency, Fs, and the DAC_SZC setting unless the disable bit is enabled.

6.22 Limiter Attack Rate Register (Address 1Bh)

7	6	5	4	3	2	1	0
Reserved	Reserved	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0

Note: The DATA_SEL[1:0] bits in reg09h must be set to ‘01’b to enable function control in this register.

Limiter Attack Rate (ARATE[5:0])

Default: 000000

Binary Code	Attack Time
000000	Fastest Attack
…	…
111111	Slowest Attack

Function:
Sets the rate at which the limiter attenuates the analog output from levels above the maximum setting in the limiter threshold register.

The limiter attack rate is user-selectable but is also a function of the sampling frequency, Fs, and the DAC_SZC setting unless the disable bit is enabled.

6.23 ALC Enable & Attack Rate (Address 1Ch)

7	6	5	4	3	2	1	0
ALC_ENB	ALC_ENA	ALC_ARATE5	ALC_ARATE4	ALC_ARATE3	ALC_ARATE2	ALC_ARATE1	ALC_ARATE0

ALC Enable (ALC_ENX)

Default: 0

0 - Disabled
1 - Enabled

Function:
Enables automatic level control for ADC channel x.

Notes:

1. When the ALC is enabled, the Attenuator and PGA volume is automatically controlled and should not be adjusted manually.
2. The ALC should only be configured while the power down bit is enabled.
3. The ALC is not available in passthrough mode.

ALC Attack Rate (ARATE[5:0])

Default: 000000

Binary Code	Attack Time
000000	Fastest Attack
…	…
111111	Slowest Attack

Function:
Sets the rate at which the ALC attenuates the analog input from levels above the maximum setting in the ALC threshold register.

The limiter attack rate is user-selectable but is also a function of the sampling frequency, Fs, and the SOFTx & ZCROSSx bit settings unless the disable bit for each function is enabled.

6.24 ALC Release Rate (Address 1Dh)

7	6	5	4	3	2	1	0
Reserved	Reserved	ALC_RRATE5	ALC_RRATE4	ALC_RRATE3	ALC_RRATE2	ALC_RRATE1	ALC_RRATE0

ALC Release Rate (RRATE[5:0])

Default: 111111

Binary Code	Release Time
000000	Fastest Release
…	…
111111	Slowest Release

Function:

Sets the rate at which the ALC releases the PGA & digital attenuation from levels below the minimum setting in the ALC threshold register, and returns the input level to the PGA_VOL[4:0] & ADCx_ATT[7:0] setting. The ALC release rate is user selectable, but is also a function of the sampling frequency, Fs, and the SOFTx & ZCROSS bit settings unless the disable bit for each function is enabled.

6.25 ALC Threshold (Address 1Eh)

7	6	5	4	3	2	1	0
MAX2	MAX1	MAX0	MIN2	MIN1	MIN0	Reserved	Reserved

Maximum Threshold (MAX[2:0])

Default: 000

MAX[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
100	-12
101	-18
110	-24
111	-30

Function:

Sets the maximum level, relative to full scale, at which to limit and attenuate the input signal at the attack rate.

Minimum Threshold (MIN[2:0])

Default: 000

MIN[2:0]	Threshold Setting (dB)
000	0
001	-3
010	-6
011	-9
100	-12
101	-18
110	-24
111	-30

Function:

Sets the minimum level at which to disengage the ALC's attenuation or amplify the input signal at a rate set in the release rate register until levels again reach this minimum threshold. The ALC uses this minimum as a hysteresis point for the input signal as it maintains the signal below the maximum as well as below the minimum setting. This provides a more natural sound as the ALC attacks and releases.

6.26 Noise Gate Configuration & Misc. (Address 1Fh)

7	6	5	4	3	2	1	0
NG_ALL	NG_EN	NG_BOOST	THRESH2	THRESH1	THRESH0	NGDELAY1	NGDELAY0

Noise Gate Channel Gang (NG_ALL)

Default: 0

0 - Disabled
1 - Enabled

Function:

Gangs the noise gate function for channel A and B. When enabled, both channels must fall below the threshold setting for the noise gate attenuation to take effect.

Noise Gate Enable (NG_EN)

Default: 0

0 - Disabled
1 - Enabled

Function:

Enables the noise gate. Maximum attenuation is relative to all gain settings applied.

Noise Gate Boost (NG_BOOST) and Threshold (THRESH[3:0])

Default: 000

THRESH[2:0]	Minimum Setting (NG_BOOST = '0'b)	Minimum Setting (NG_BOOST = '1'b)
000	-64 dB	-34 dB
001	-67 dB	-37 dB
010	-70 dB	-40 dB
011	-73 dB	-43 dB
100	-76 dB	-46 dB
101	-82 dB	-52 dB
110	Reserved	-58 dB
111	Reserved	-64 dB

Function:
Sets the threshold level of the noise gate. Input signals below the threshold level will be attenuated to -96 dB. NG_BOOST = '1'b adds 30 dB to the threshold settings.

Noise Gate Delay Timing (NGDELAY[1:0])

Default: 00

00 - 50 ms
01 - 100 ms
10 - 150 ms
11 - 200 ms

Function:

Sets the delay time before the noise gate attacks. Noise gate attenuation is dictated by the SOFTx & ZCROSS bit settings unless the disable bit for each function is enabled.

6.27 Status (Address 20h) (Read Only)

7	6	5	4	3	2	1	0
Reserved	SP_CLKERR	SPEA_OVFL	SPEB_OVFL	PCMA_OVFL	PCMB_OVFL	ADCA_OVFL	ADCB_OVFL

For all bits in this register, a "1" means the associated error condition has occurred at least once since the register was last read. A "0" means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0.

Serial Port Clock Error (SP_CLK Error)

Default: 0

Function:

Indicates an invalid MCLK to LRCK ratio. See "Serial Port Clocking" on page 37 for valid clock ratios.

Note: On initial power up and application of clocks, this bit will be high as the serial port re-synchronizes.

Signal Processing Engine Overflow (SPEX_OVFL)

Default: 0

Function:
Indicates a digital overflow condition within the data path after the signal processing engine.

PCMX Overflow (PCMX_OVFL)

Default: 0

Function:

Indicates a digital overflow condition within the data path of the PCM mix.

ADC Overflow (ADCX_OVFL)

Default = 0

Function:

Indicates that there is an over-range condition anywhere in the CS42L51 ADC signal path of each of the associated ADCs.

6.28 Charge Pump Frequency (Address 21h)

7	6	5	4	3	2	1	0
CHRG_-FREQ3	CHRG_-FREQ2	CHRG_-FREQ1	CHRG_-FREQ0	Reserved	Reserved	Reserved	Reserved

Charge Pump Frequency (CHRG_FREQ[3:0])

Default: 0101

N	CHRG_FREQ[3:0]	Frequency
0	0000	$\frac{64xFs}{N+2}$
...	...	
15	1111	

Function:

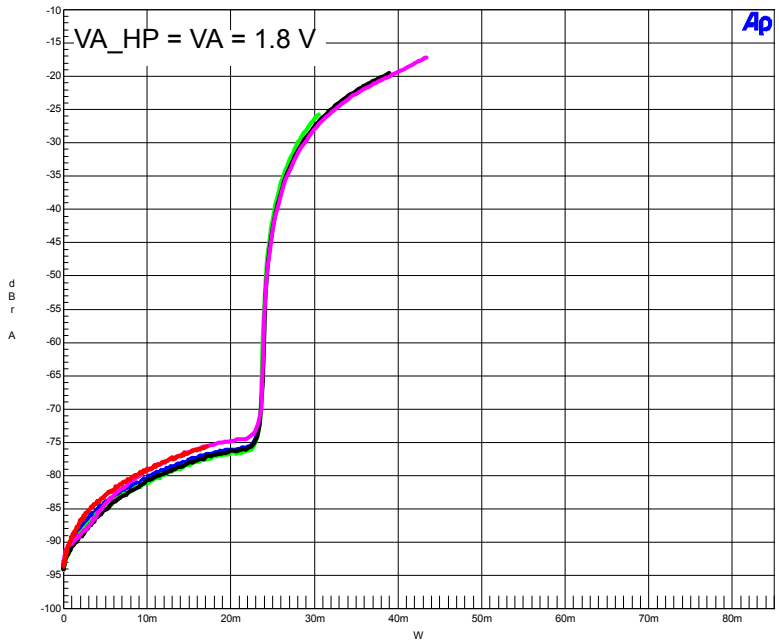
Alters the clocking frequency of the charge pump in 1/(N+2) fractions of the DAC oversampling rate, 128Fs, should the switching frequency interfere with other system frequencies such as those in the AM radio band.

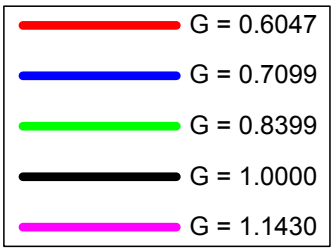
Note: Distortion performance may be affected.

7. ANALOG PERFORMANCE PLOTS

7.1 Headphone THD+N versus Output Power Plots

Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Fs = 48 kHz. Plots were taken from the CDB42L51 using an Audio Precision analyzer.

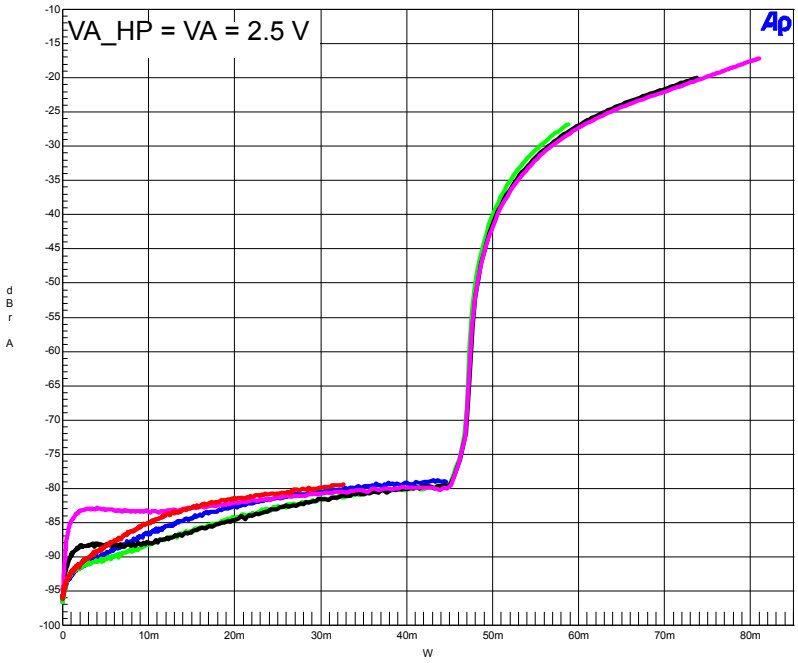


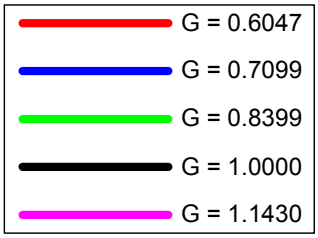


Legend

NOTE: Graph shows the output power *per channel* (i.e. Output Power = 23 mW into single 16 Ω and 46 mW into stereo 16 Ω with THD+N = -75 dB).

Figure 27. THD+N vs. Output Power per Channel at 1.8 V (16 Ω load)





Legend

NOTE: Graph shows the output power *per channel* (i.e. Output Power = 44 mW into single 16 Ω and 88 mW into stereo 16 Ω with THD+N = -75 dB).

Figure 28. THD+N vs. Output Power per Channel at 2.5 V (16 Ω load)

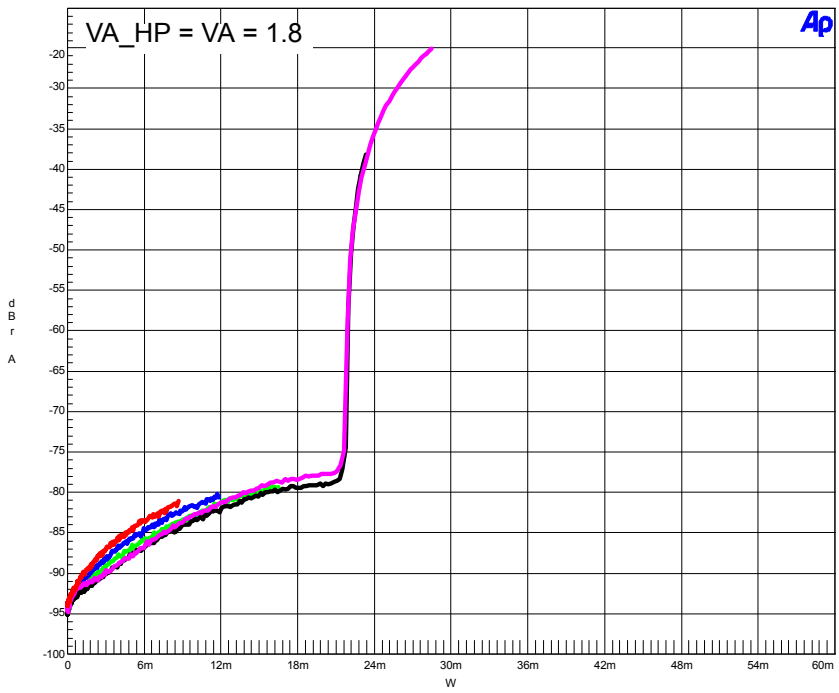


Figure 29. THD+N vs. Output Power per Channel at 1.8 V (32 Ω load)

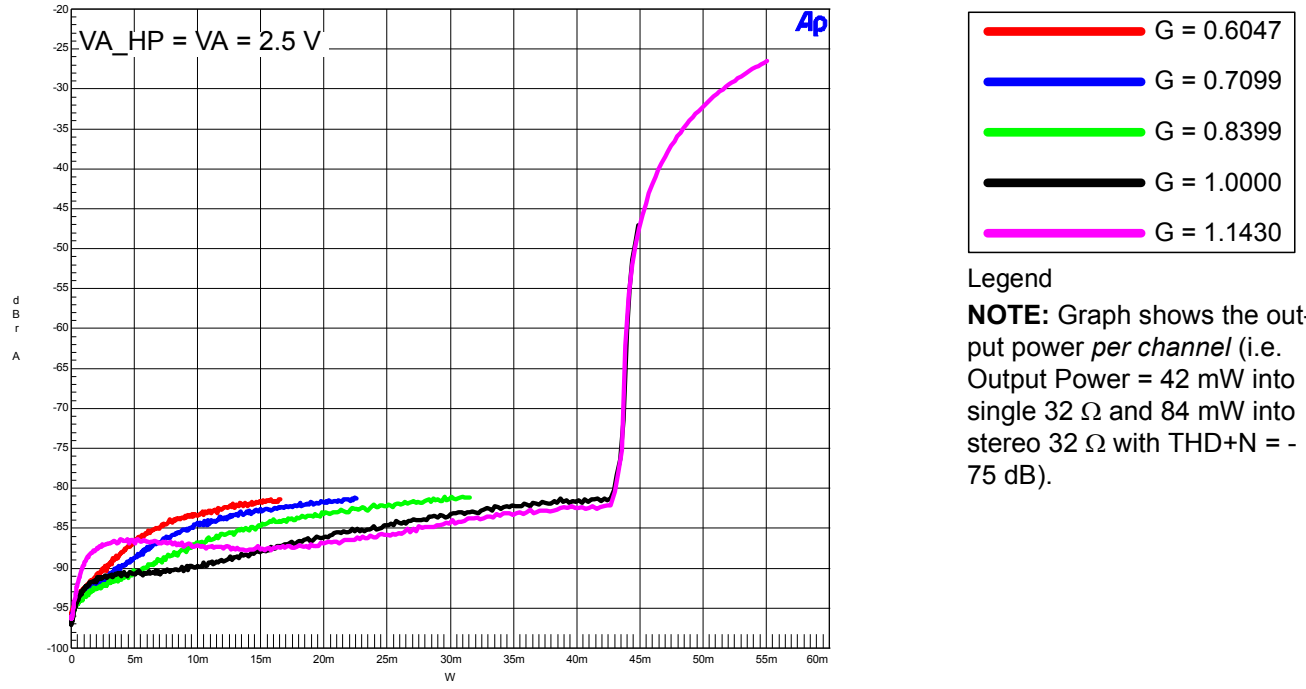


Figure 30. THD+N vs. Output Power per Channel at 2.5 V (32 Ω load)

7.2 Headphone Amplifier Efficiency

The architecture of the headphone amplifier is that of typical class AB amplifiers. Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; Power Consumption Mode 6 - Stereo Playback with 16 Ω load. HP_GAIN = 1.1430. Best efficiency is realized when the amplifier outputs maximum power.

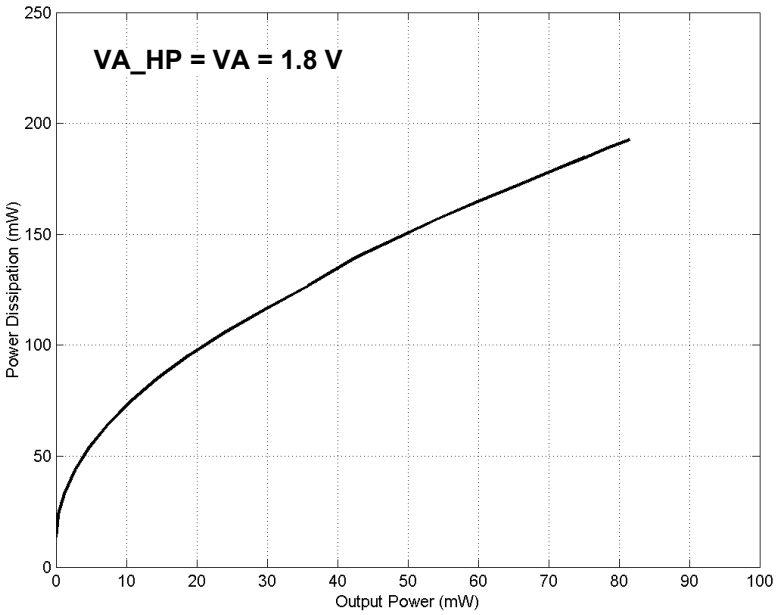


Figure 31. Power Dissipation vs. Output Power into Stereo 16 Ω

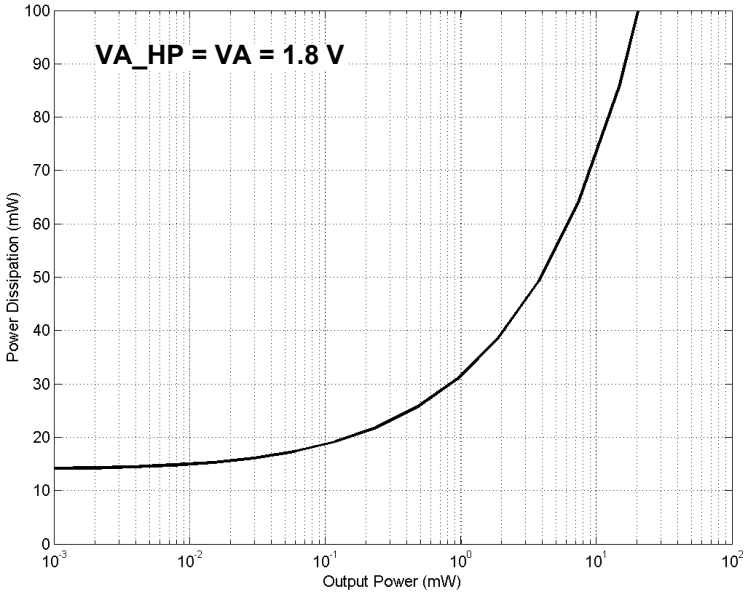


Figure 32. Power Dissipation vs. Output Power into Stereo 16 Ω (Log Detail)

7.3 ADC_FILT+ Capacitor Effects on THD+N

The value of the capacitor on the ADC_FILT+ pin, 16, affects the low frequency total harmonic distortion + noise (THD+N) performance of the ADC. Larger capacitor values yield significant improvement in THD+N at low frequencies. Figure 33 shows the THD+N versus frequency for the ADC analog input. Plots were taken from the CDB42L51 using an Audio Precision analyzer.

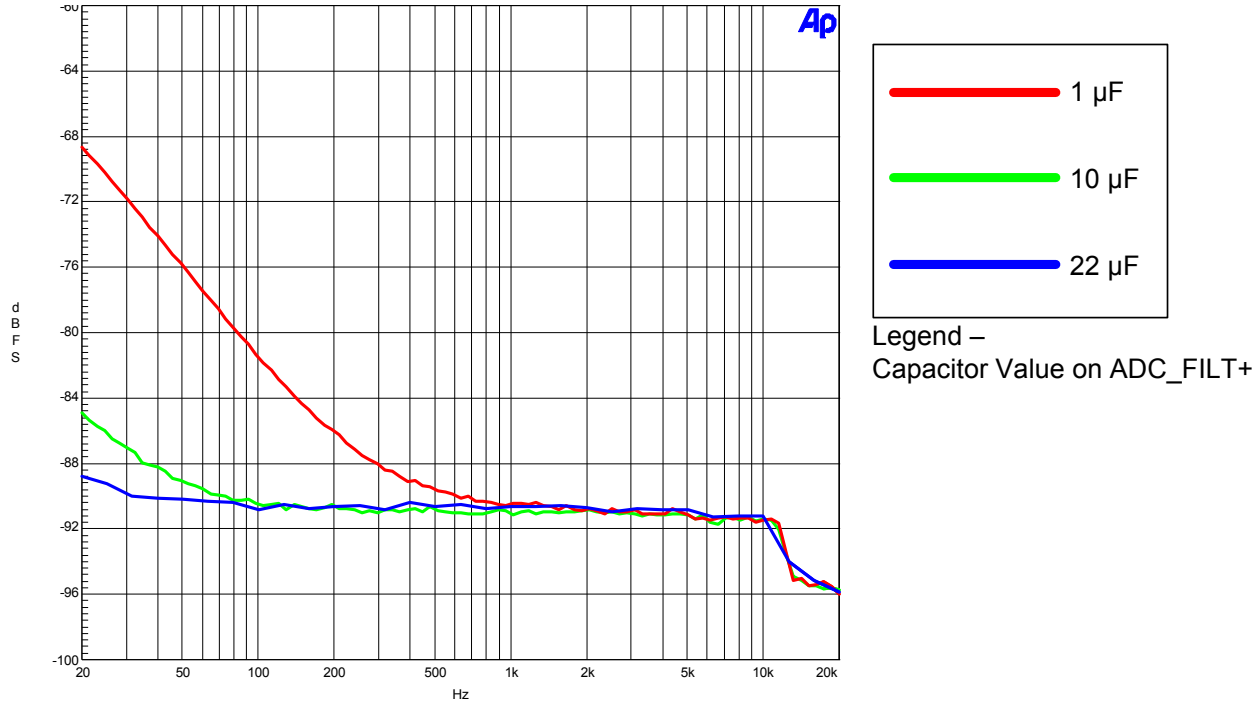


Figure 33. ADC THD+N vs. Frequency with Capacitor Effects

8. EXAMPLE SYSTEM CLOCK FREQUENCIES

8.1 Auto Detect Enabled

Sample Rate LRCK (kHz)	MCLK (MHz)			
	1024x	1536x	2048x*	3072x*
8	8.1920	12.2880	16.3840	24.5760
11.025	11.2896	16.9344	22.5792	33.8688
12	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	512x	768x	1024x*	1536x*
16	8.1920	12.2880	16.3840	24.5760
22.05	11.2896	16.9344	22.5792	33.8688
24	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	256x	384x	512x*	768x*
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	128x	192x	256x*	384x*
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

*The”MCLKDIV2” pin 4 must be set HI.

8.2 Auto Detect Disabled

Sample Rate LRCK (kHz)	MCLK (MHz)					
	512x	768x	1024x	1536x	2048x	3072x
8	-	6.1440	8.1920	12.2880	16.3840	24.5760
11.025	-	8.4672	11.2896	16.9344	22.5792	33.8688
12	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1536x
16	-	6.1440	8.1920	12.2880	16.3840	24.5760
22.05	-	8.4672	11.2896	16.9344	22.5792	33.8688
24	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	256x	384x	512x	768x
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640

Sample Rate LRCK (kHz)	MCLK (MHz)			
	128x	192x	256x	384x
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

9. PCB LAYOUT CONSIDERATIONS

9.1 Power Supply, Grounding

As with any high-resolution converter, the CS42L51 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 on page 9 shows the recommended power arrangements, with VA and VA_HP connected to clean supplies. VD, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS42L51 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS42L51 to minimize inductance effects. All signals, especially clocks, should be kept away from the DAC_FILT+/ADC_FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The DAC_FILT+/ADC_FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from DAC_FILT+/ADC_FILT+ and AGND. The CDB42L51 evaluation board demonstrates the optimum layout and power supply arrangements.

9.2 QFN Thermal Pad

The CS42L51 is available in a compact QFN package. The under side of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CS42L51 evaluation board demonstrates the optimum thermal pad and via configuration.

10.ADC & DAC DIGITAL FILTERS

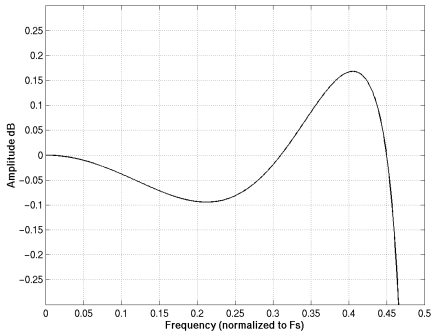


Figure 34. ADC Passband Ripple

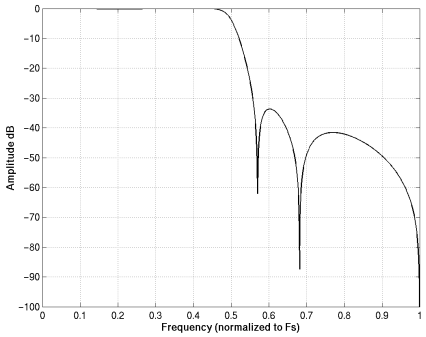


Figure 35. ADC Stopband Rejection

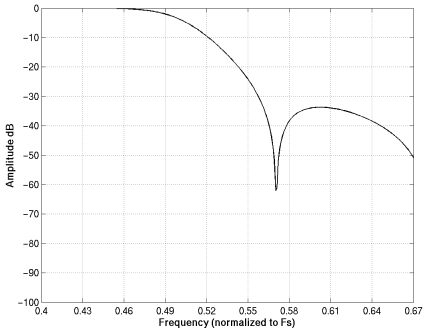


Figure 36. ADC Transition Band

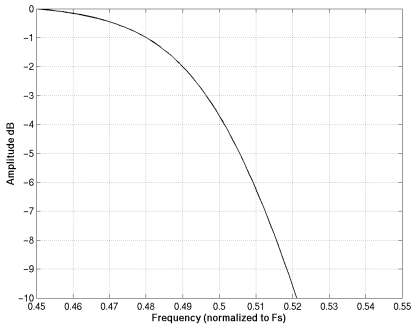


Figure 37. ADC Transition Band Detail

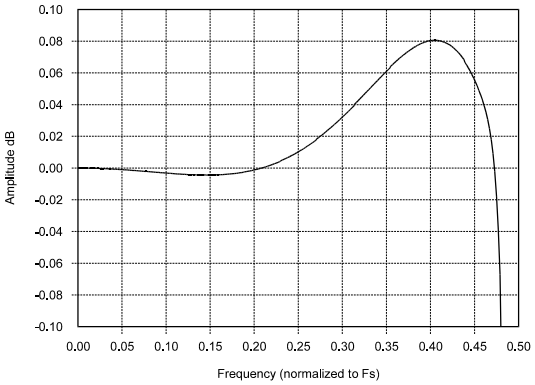


Figure 38. DAC Passband Ripple

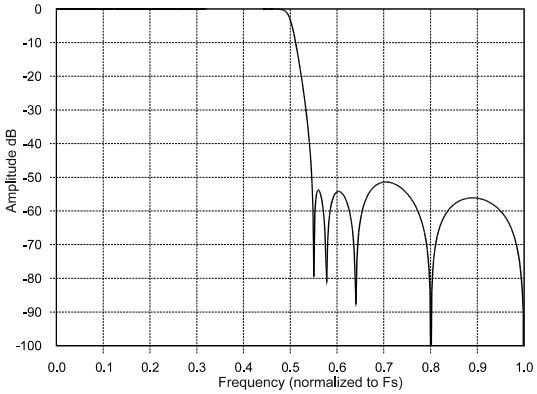


Figure 39. DAC Stopband

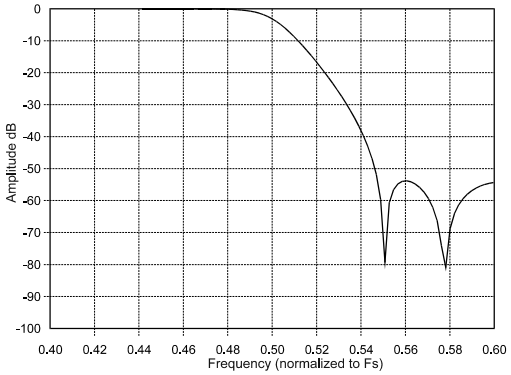


Figure 40. DAC Transition Band

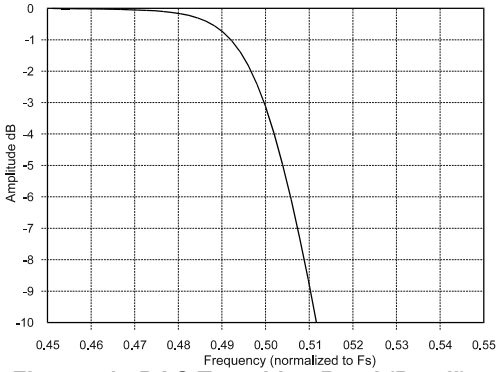


Figure 41. DAC Transition Band (Detail)

11.PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Offset Error

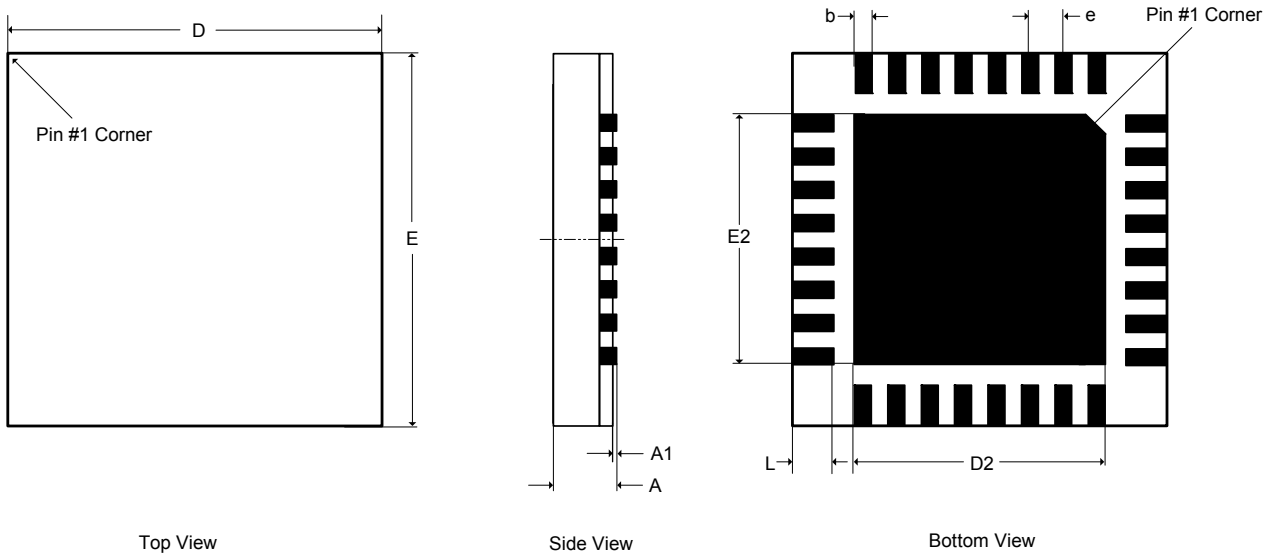
The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

12.PACKAGE DIMENSIONS

32L QFN (5 X 5 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0394	--	--	1.00	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0071	0.0091	0.0110	0.18	0.23	0.28	1,2
D		0.1969 BSC			5.00 BSC		1
D2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
E		0.1969 BSC			5.00 BSC		1
E2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
e		0.0197 BSC			0.50 BSC		1
L	0.0118	0.0157	0.0197	0.30	0.40	0.50	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

1. Dimensioning and tolerance per ASME Y 14.5M-1995.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board 4 Layer Board	θ_{JA}	- -	52 38	- -	°C/Watt

13.REFERENCES

1. Philips Semiconductor, *The I²C-Bus Specification: Version 2.1*, January 2000. http://www.semiconductors.philips.com

14.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS42L51	Low-Power Stereo codec with HP Amp for Portable Apps	32L-QFN	Yes	Commercial	-10 to +70° C	Rail	CS42L51-CNZ
						Tape & Reel	CS42L51-CNZR
				Automotive	-40 to +85° C	Rail	CS42L51-DNZ
						Tape & Reel	CS42L51-DNZR
CDB42L51	CS42L51 Evaluation Board	-	No	-	-	-	CDB42L51
CRD42L51	CS42L51 Reference Design	-	No	-	-	-	CRD42L51

15.REVISION HISTORY

Revision	Changes
F1 AUG '06	Final Release
F2 AUG '15	Updated voltage range in "Specified Operating Conditions" on page 11. Added and updated absolute maximum parameters in "Absolute Maximum Ratings" on page 11. Corrected Max passband frequency in "ADC Digital Filter Characteristics" on page 14. Updated Figure 13. Output Architecture on page 33. Updated Section 4.8 "Recommended Power-Up Sequence" on page 40. Updated Section 4.9 "Recommended Power-Down Sequence" on page 41. Updated Section 4.10 "Software Mode" on page 42. Added note 1 in the FREEZE control register in "DAC Control (Address 09h)" on page 57. Added "note" details for ALC configuration in "ALC Enable & Attack Rate (Address 1Ch)" on page 68.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
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