



PCA9516A

5-channel I²C-bus hub

Rev. 03 — 23 April 2009

Product data sheet

1. General description

The PCA9516A is a CMOS integrated circuit intended for application in I²C-bus and SMBus systems.

While retaining all the operating modes and features of the I²C-bus system, it permits extension of the I²C-bus by buffering both the data (SDAn) and the clock (SCLn) lines, thus enabling five buses of 400 pF.

The I²C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9516A enables the system designer to divide the bus into five segments off of a hub where any segment-to-segment transition sees only one repeater delay.

It can also be used to run different buses at 5 V and 3.3 V or 400 kHz and 100 kHz buses where the 100 kHz bus is isolated when 400 kHz operation of the other bus is required.

Two or more PCA9516As cannot be put in series. The PCA9516A design does not allow this configuration. Since there is no direction pin, slightly different 'legal' low voltage levels are used to avoid lock-up conditions between the input and the output of each repeater in the hub. A 'regular LOW' applied at the input of a PCA9516A will be propagated as a 'buffered LOW' with a slightly higher value on all the enabled outputs. When this 'buffered LOW' is applied to another PCA9515A, PCA9516A, or PCA9518A in series, the second PCA9515A, PCA9516A, or PCA9518A will not recognize it as a 'regular LOW' and will not propagate it as a 'buffered LOW' again. The PCA9510A/9511A/9513A/9514A and PCA9512A cannot be used in series with the PCA9515A, PCA9516A, or PCA9518A, but can be used in series with themselves since they use shifting instead of static offsets to avoid lock-up conditions.

2. Features

- 5 channel, bidirectional buffer
- I²C-bus and SMBus compatible
- Active HIGH individual repeater enable input
- Open-drain input/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins
- Operating supply voltage range of 2.3 V to 3.6 V
- 5.5 V tolerant I²C-bus and enable pins

- 0 Hz to 400 kHz clock frequency¹
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO16 and TSSOP16

3. Ordering information

Table 1. Ordering information

| Type number | Package | | |
|-------------|---------|---|----------|
| | Name | Description | Version |
| PCA9516AD | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| PCA9516APW | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

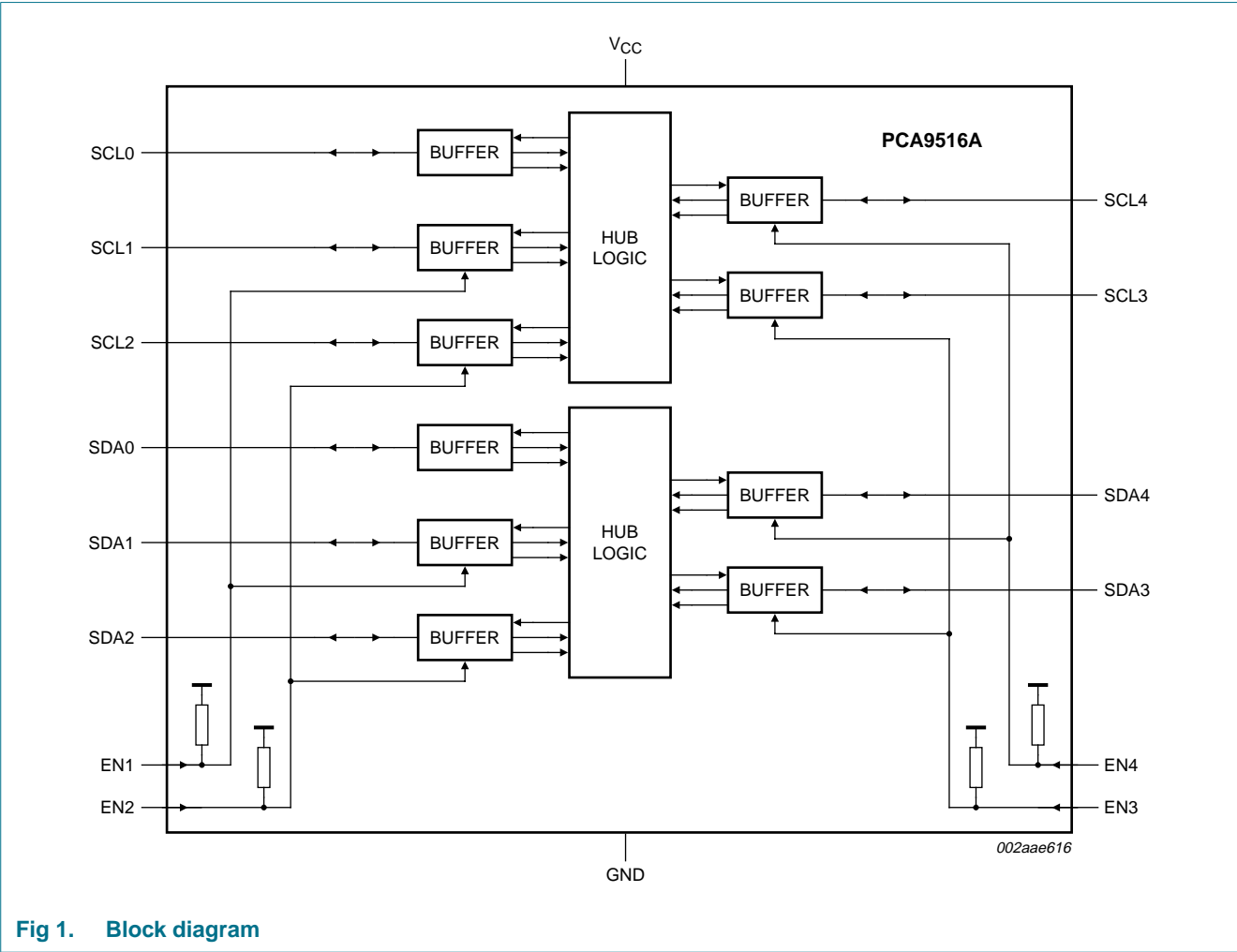
3.1 Ordering options

Table 2. Ordering options

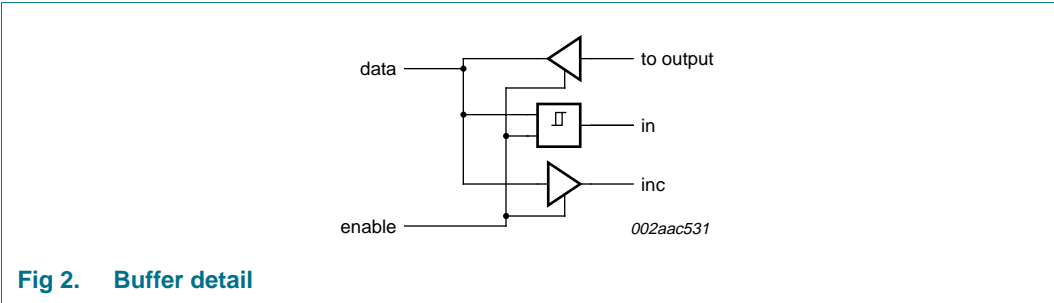
| Type number | Topside mark | Temperature range |
|-------------|--------------|-------------------------------------|
| PCA9516AD | PCA9516AD | T _{amb} = -40 °C to +85 °C |
| PCA9516APW | PA9516A | T _{amb} = -40 °C to +85 °C |

1. The maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

4. Block diagram



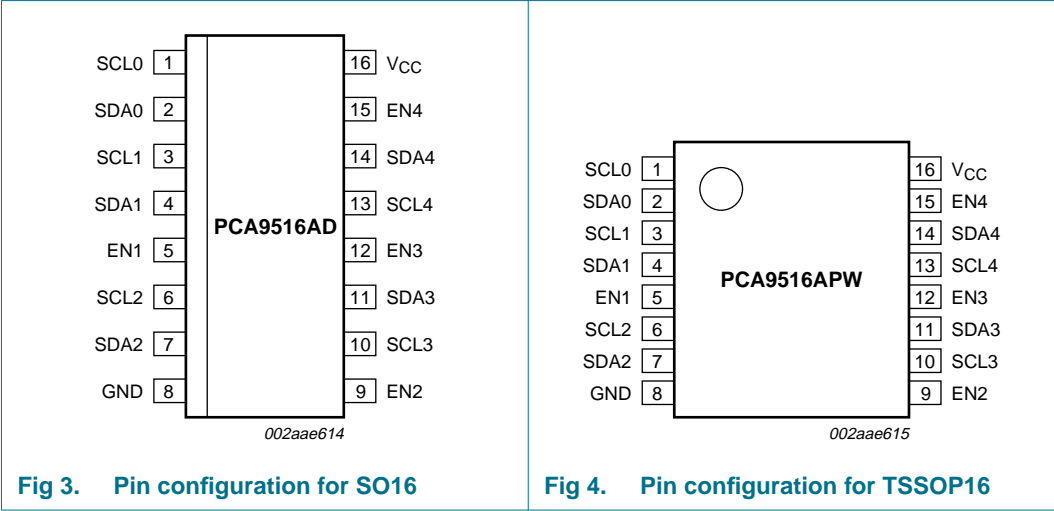
A more detailed view of [Figure 1](#) buffer is shown in [Figure 2](#).



The output pull-down of each internal buffer is set for approximately 0.5 V, while the input threshold of each internal buffer is set about 0.07 V lower, when the output is internally driven LOW. This prevents a lock-up condition from occurring.

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|--------------------------------|
| SCL0 | 1 | serial clock bus 0 |
| SDA0 | 2 | serial data bus 0 |
| SCL1 | 3 | serial clock bus 1 |
| SDA1 | 4 | serial data bus 1 |
| EN1 | 5 | active HIGH bus 1 enable input |
| SCL2 | 6 | serial clock bus 2 |
| SDA2 | 7 | serial data bus 2 |
| GND | 8 | supply ground |
| EN2 | 9 | active HIGH bus 2 enable input |
| SCL3 | 10 | serial clock bus 3 |
| SDA3 | 11 | serial data bus 3 |
| EN3 | 12 | active HIGH bus 3 enable input |
| SCL4 | 13 | serial clock bus 4 |
| SDA4 | 14 | serial data bus 4 |
| EN4 | 15 | active HIGH bus 4 enable input |
| V _{CC} | 16 | supply power |

6. Functional description

The PCA9516A is a five-way hub repeater, which enables I²C-bus and similar bus systems to be expanded with only one repeater delay and no functional degradation of system performance.

The PCA9516A contains five bidirectional, open-drain buffers specifically designed to support the standard low-level-contention arbitration of the I²C-bus. Except during arbitration or clock stretching, the PCA9516A acts like five pairs of non-inverting, open-drain buffers, one for SDA and one for SCL. Refer to [Figure 1 “Block diagram”](#).

6.1 Enable

The enable pins EN1 through EN4 are active HIGH and have internal pull-up resistors. Each enable pin ENn controls its associated SDAn and SCLn ports. When LOW, the ENn pin blocks the inputs from SDAn and SCLn as well as disabling the output drivers on the SDAn and SCLn pins. The enable pins should only change state when both the global bus and the local port are in an idle state to prevent system failures.

The active HIGH enable pins allow the use of open-drain drivers which can be wire-ORed to create a distributed enable where either centralized control signal (master) or spoke signal (submaster) can enable the channel when it is idle.

6.2 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus. (Standard open-collector configuration of the I²C-bus.) The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part is designed to work with Standard-mode and Fast-mode I²C-bus devices in addition to SMBus devices. Standard-mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard-mode devices and multiple masters are possible. Please see application note *AN255, “I²C/SMBus Repeaters, Hubs and Expanders”* for additional information on sizing resistors and precautions when using more than one PCA9515A/PCA9516A in a system or using the PCA9515A/PCA9516A in conjunction with the P82B96.

7. Application design-in information

A typical application is shown in [Figure 5](#). In this example, the system master is running on a 3.3 V I²C-bus while the slave is connected to a 5 V bus. All buses run at 100 kHz unless slave 3 is isolated, and then the master bus and slave 1 and slave 2 can run at 400 kHz.

Any segment of the hub can talk to any other segment of the hub. Bus masters and slaves can be located on all five segments with 400 pF load allowed on each segment.

Unused ports should be isolated by holding the enable pin (ENn) to GND and/or pulling SDAn/SCLn pins to V_{CC} through appropriately sized resistors. The primary bus master is normally connected to SDA0/SCL0. If the SDA0/SCL0 port is not used, the pins need to be pulled to V_{CC} through appropriately sized resistors.

The PCA9516A is 5.5 V tolerant so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9516A is pulled LOW by a device on the I²C-bus, a CMOS hysteresis type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side to also go LOW. The side driven LOW by the PCA9516A will typically be at $V_{OL} = 0.5$ V.

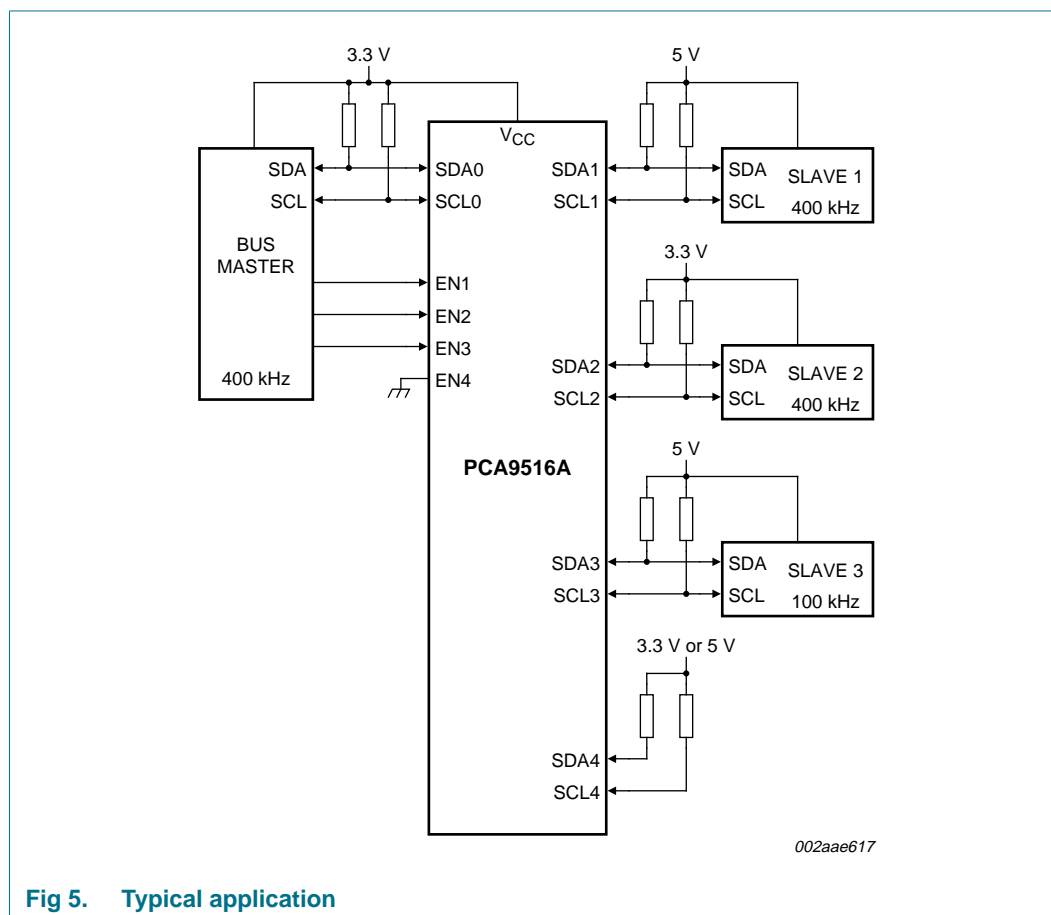


Fig 5. Typical application

In order to illustrate what would be seen in a typical application, refer to [Figure 6](#) and [Figure 7](#). If the bus master in [Figure 5](#) were to write to the slave through the PCA9516A, we would see the waveform shown in [Figure 6](#) on Bus 0. This looks like a normal I²C-bus transmission until the falling edge of the 8th clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it LOW through the PCA9516A. Because the V_{OL} of the PCA9516A is typically around 0.5 V, a step in the SDA will be seen. After the master has transmitted the 9th clock pulse, the slave releases the data line.

On the Bus 1 side of the PCA9516A, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9516A. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the slave device that is very close to ground in our example.

It is important to note that any arbitration or clock stretching events on Bus 1 require that the V_{OL} of the devices on Bus 1 be 70 mV below the V_{OL} of the PCA9516A (see $V_{OL} - V_{ILC}$ in [Section 9 "Static characteristics"](#)) to be recognized by the PCA9516A and then transmitted to Bus 0.

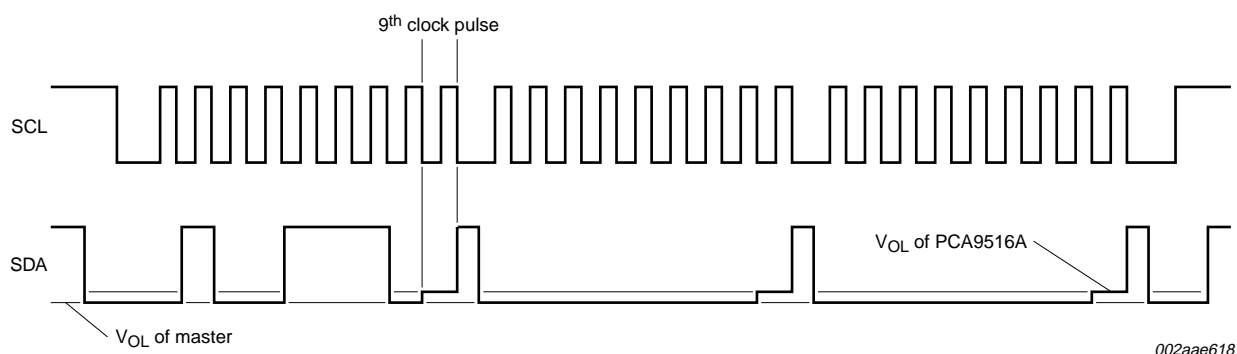


Fig 6. Bus 0 waveform

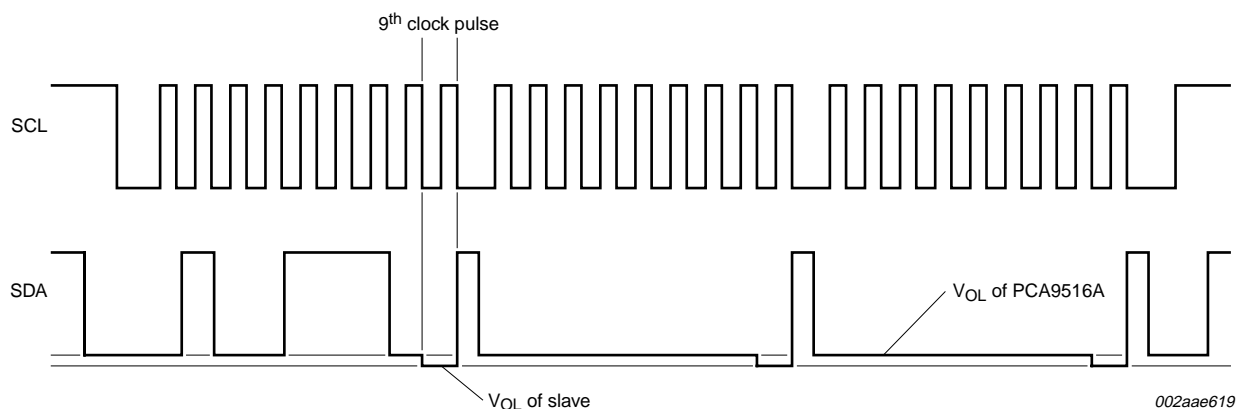


Fig 7. Bus 1 waveform

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages with respect to GND.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|------------------------------------|--------------|------|------|------|
| V _{CC} | supply voltage | | −0.5 | +7 | V |
| V _{bus} | voltage range I ² C-bus | SCLn or SDAn | −0.5 | +7 | V |
| I | DC current | any pin | - | 50 | mA |
| P _{tot} | total power dissipation | | - | 300 | mW |
| T _{stg} | storage temperature | | −55 | +125 | °C |
| T _{amb} | ambient temperature | operating | −40 | +85 | °C |

9. Static characteristics

Table 5. Static characteristics ($V_{CC} = 3.0\text{ V}$ to 3.6 V)

$V_{CC} = 3.0\text{ V}$ to 3.6 V ^[1]; $GND = 0\text{ V}$; $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit |
|--------------------------------------|--|--|---------------------|--------------------|--------------|------|
| Supplies | | | | | | |
| V_{CC} | supply voltage | | 3.0 | - | 3.6 | V |
| I_{CCH} | HIGH-level supply current | both channels HIGH; $V_{CC} = 3.6\text{ V}$; $SDAn = SCLn = V_{CC}$ | - | 2.1 | 5 | mA |
| I_{CCL} | LOW-level supply current | both channels LOW; $V_{CC} = 3.6\text{ V}$; one $SDAn$ and one $SCLn = GND$, other $SDAn$ and $SCLn$ open | - | 4.7 | 10 | mA |
| I_{CCLc} | contention LOW-level supply current | $V_{CC} = 3.6\text{ V}$; $SDAn = SCLn = GND$ | - | 4.0 | 10 | mA |
| Input SCLn; input/output SDAn | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{CC}$ | - | 5.5 | V |
| V_{IL} | LOW-level input voltage | | ^[3] -0.5 | - | $+0.3V_{CC}$ | V |
| V_{ILc} | contention LOW-level input voltage | | ^[3] -0.5 | - | +0.4 | V |
| V_{IK} | input clamping voltage | $I_I = -18\text{ mA}$ | - | - | -1.2 | V |
| I_{LI} | input leakage current | $V_I = 3.6\text{ V}$ | -1 | - | +1 | μA |
| I_{IL} | LOW-level input current | $SDAn, SCLn$; $V_I = 0.2\text{ V}$ | - | - | 5 | μA |
| V_{OL} | LOW-level output voltage | $I_{OL} = 0\text{ mA}$ or 6 mA | 0.47 | 0.52 | 0.6 | V |
| $V_{OL} - V_{ILc}$ | difference between LOW-level output and LOW-level input voltage contention | guaranteed by design | - | - | 70 | mV |
| C_i | input capacitance | $V_I = 3\text{ V}$ or 0 V | - | 6 | 10 | pF |
| Enable inputs EN1 to EN4 | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.8 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | 5.5 | V |
| I_{IL} | LOW-level input current | EN1 to EN4; $V_I = 0.2\text{ V}$ | - | -12 | -30 | μA |
| I_{LI} | input leakage current | | -1 | - | +1 | μA |
| C_i | input capacitance | $V_I = 3\text{ V}$ or 0 V | - | 6 | 7 | pF |

[1] For operation between published voltage ranges, refer to worst case parameter in both ranges.

[2] Typical value taken at 3.3 V and 25 °C.

[3] V_{IL} specification is for the first LOW level seen by the $SDAn/SCLn$ lines. V_{ILc} is for the second and subsequent LOW levels seen by the $SDAn/SCLn$ lines.

Table 6. Static characteristics ($V_{CC} = 2.3\text{ V}$ to 2.7 V) $V_{CC} = 2.3\text{ V}$ to 2.7 V ^[1]; $GND = 0\text{ V}$; $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[2] | Max | Unit |
|--------------------------------------|--|--|---------------------|--------------------|--------------|---------------|
| Supplies | | | | | | |
| V_{CC} | supply voltage | | 2.3 | - | 2.7 | V |
| I_{CCH} | HIGH-level supply current | both channels HIGH; $V_{CC} = 2.7\text{ V}$; $SDAn = SCLn = V_{CC}$ | - | 2.1 | 5 | mA |
| I_{CCL} | LOW-level supply current | both channels LOW; $V_{CC} = 2.7\text{ V}$; one $SDAn$ and one $SCLn = GND$, other $SDAn$ and $SCLn$ open | - | 4.6 | 10 | mA |
| I_{CCLc} | contention LOW-level supply current | $V_{CC} = 2.7\text{ V}$; $SDAn = SCLn = GND$ | - | 3.9 | 10 | mA |
| Input SCLn; input/output SDAn | | | | | | |
| V_{IH} | HIGH-level input voltage | | $0.7V_{CC}$ | - | 5.5 | V |
| V_{IL} | LOW-level input voltage | | ^[3] -0.5 | - | $+0.3V_{CC}$ | V |
| V_{ILc} | contention LOW-level input voltage | | ^[3] -0.5 | - | +0.4 | V |
| V_{IK} | input clamping voltage | $I_I = -18\text{ mA}$ | - | - | -1.2 | V |
| I_{LI} | input leakage current | $V_I = 2.7\text{ V}$ | -1 | - | +1 | μA |
| I_{IL} | LOW-level input current | $SDAn, SCLn$; $V_I = 0.2\text{ V}$ | - | - | 5 | μA |
| V_{OL} | LOW-level output voltage | $I_{OL} = 0\text{ mA}$ or 6 mA | 0.47 | 0.52 | 0.6 | V |
| $V_{OL} - V_{ILc}$ | difference between LOW-level output and LOW-level input voltage contention | guaranteed by design | - | - | 70 | mV |
| C_i | input capacitance | $V_I = 3\text{ V}$ or 0 V | - | 6 | 10 | pF |
| Enable inputs EN1 to EN4 | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.5 | - | +0.8 | V |
| V_{IH} | HIGH-level input voltage | | 1.5 | - | 5.5 | V |
| I_{IL} | LOW-level input current | EN1 to EN4; $V_I = 0.2\text{ V}$ | - | -10 | -30 | μA |
| I_{LI} | input leakage current | | -1 | - | +1 | μA |
| C_i | input capacitance | $V_I = 3\text{ V}$ or 0 V | - | 6 | 7 | pF |

[1] For operation between published voltage ranges, refer to worst case parameter in both ranges.

[2] Typical value taken at 2.5 V and 25 °C.

[3] V_{IL} specification is for the first LOW level seen by the $SDAn/SCLn$ lines. V_{ILc} is for the second and subsequent LOW levels seen by the $SDAn/SCLn$ lines.

10. Dynamic characteristics

Table 7. Dynamic characteristics ($V_{CC} = 2.3\text{ V}$ to 2.7 V)

$V_{CC} = 2.3\text{ V}$ to 2.7 V ; $GND = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-----------|------------------------------------|--------------------------|--------|--------------------|-----|------|
| t_{PHL} | HIGH to LOW propagation delay | Figure 8 | 45 | 93 | 150 | ns |
| t_{PLH} | LOW to HIGH propagation delay | Figure 8 | [2] 33 | 90 | 135 | ns |
| t_{THL} | HIGH to LOW output transition time | Figure 8 | - | 60 | - | ns |
| t_{TLH} | LOW to HIGH output transition time | Figure 8 | [2] - | 131 | - | ns |
| t_{su} | set-up time | ENn to START condition | 100 | - | - | ns |
| t_h | hold time | ENn after STOP condition | 130 | - | - | ns |

[1] Typical value taken at 2.5 V and $25\text{ }^{\circ}\text{C}$.

[2] Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

Table 8. Dynamic characteristics ($V_{CC} = 3.0\text{ V}$ to 3.6 V)

$V_{CC} = 3.0\text{ V}$ to 3.6 V ; $GND = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-----------|------------------------------------|--------------------------|--------|--------------------|-----|------|
| t_{PHL} | HIGH to LOW propagation delay | Figure 8 | 45 | 75 | 120 | ns |
| t_{PLH} | LOW to HIGH propagation delay | Figure 8 | [2] 33 | 60 | 83 | ns |
| t_{THL} | HIGH to LOW output transition time | Figure 8 | - | 47 | - | ns |
| t_{TLH} | LOW to HIGH output transition time | Figure 8 | [2] - | 130 | - | ns |
| t_{su} | set-up time | ENn to START condition | 100 | - | - | ns |
| t_h | hold time | ENn after STOP condition | 100 | - | - | ns |

[1] Typical value taken at 3.3 V and $25\text{ }^{\circ}\text{C}$.

[2] Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

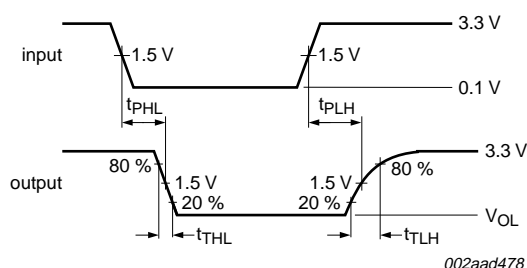
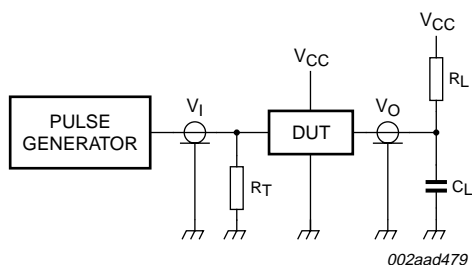


Fig 8. Propagation delay and transition times

11. Test information



R_L = load resistor; 1.35 k Ω .

C_L = load capacitance includes jig and probe capacitance; 50 pF.

R_T = termination resistance should be equal to Z_o of pulse generators.

Fig 9. Test circuit for open-drain outputs

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1

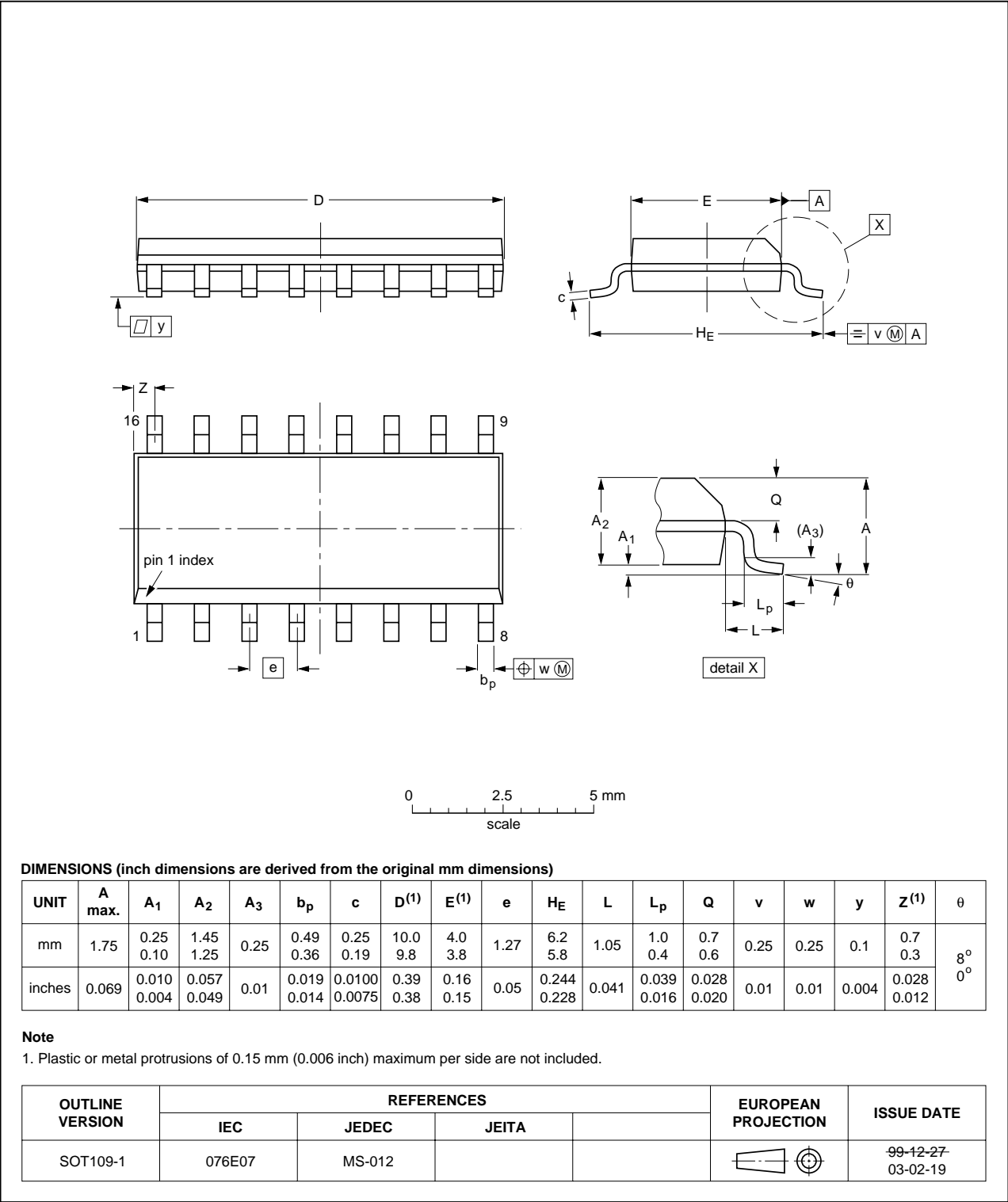


Fig 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

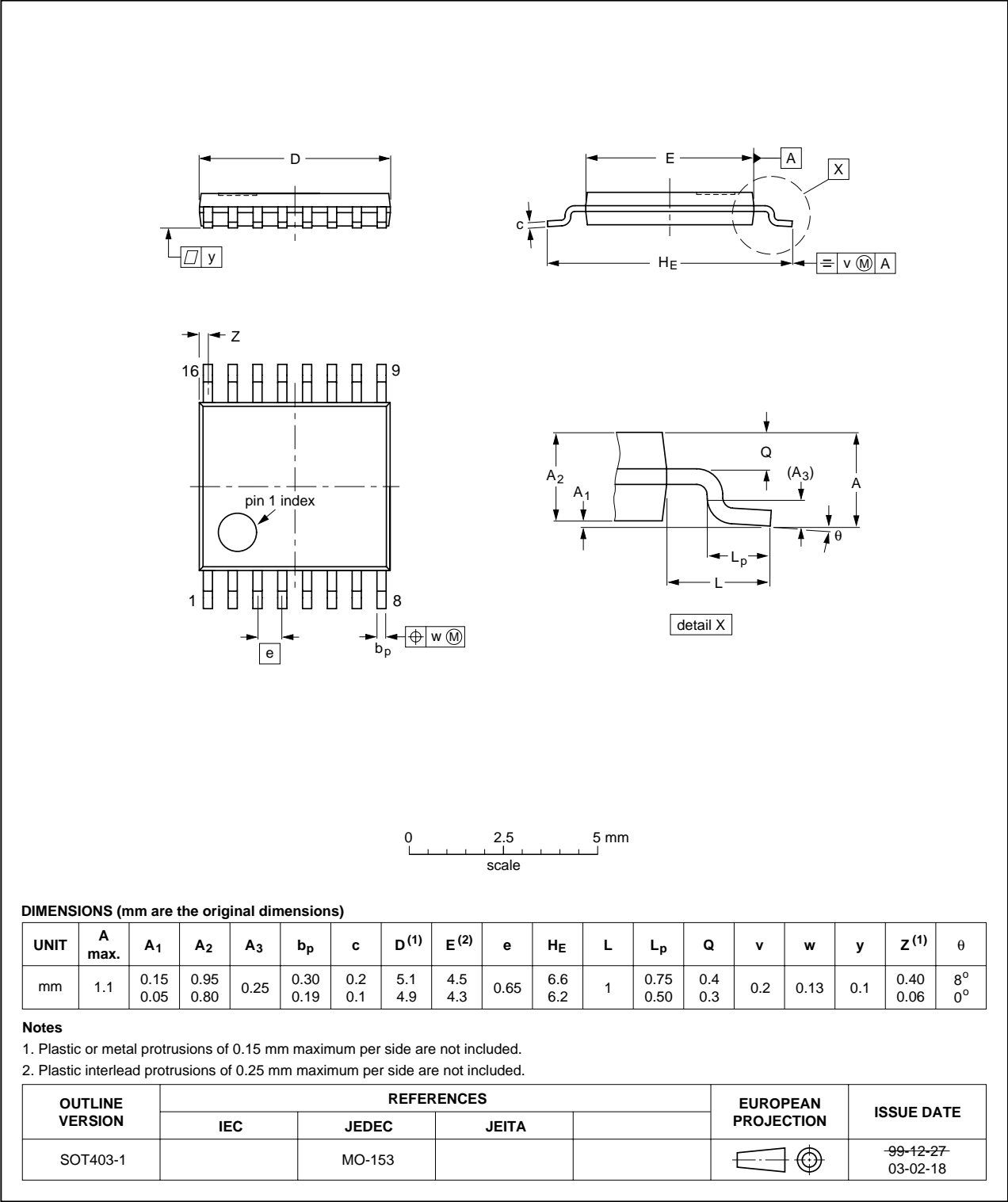


Fig 11. Package outline SOT403-1 (TSSOP16)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 12](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 9](#) and [10](#)

Table 9. SnPb eutectic process (from J-STD-020C)

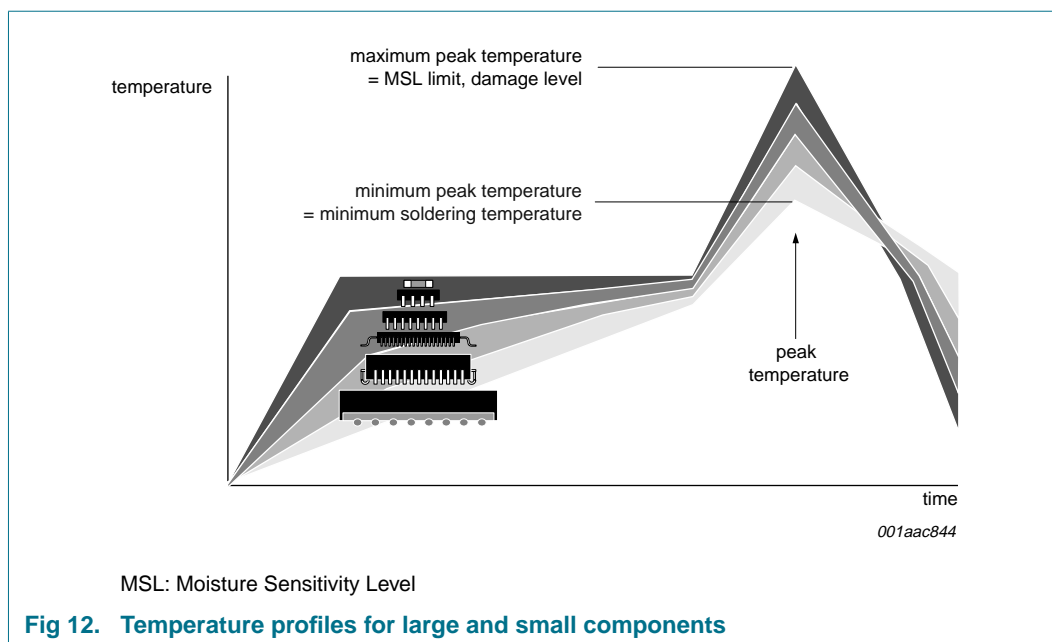
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 10. Lead-free process (from J-STD-020C)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 12](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

14. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|----------------------|---|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| I ² C-bus | Inter-Integrated Circuit bus |
| MM | Machine Model |
| RC | Resistor-Capacitor network |
| SMBus | System Management Bus |

15. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------------------|--|--------------------|---------------|------------|
| PCA9516A_3 | 20090423 | Product data sheet | - | PCA9516A_2 |
| Modifications: | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Section 1 “General description”, 5th paragraph: referenced part type numbers changed from “PCA951x” to “PCA951xA”• Added soldering information• Added Section 14 “Abbreviations” | | | |
| PCA9516A_2 (9397 750 14108) | 20040929 | Product data sheet | - | PCA9516A_1 |
| PCA9516A_1 (9397 750 13238) | 20040528 | Product data sheet | - | - |

16. Legal information

16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

| | | |
|-----------|--|-----------|
| 1 | General description | 1 |
| 2 | Features | 1 |
| 3 | Ordering information | 2 |
| 3.1 | Ordering options | 2 |
| 4 | Block diagram | 3 |
| 5 | Pinning information | 4 |
| 5.1 | Pinning | 4 |
| 5.2 | Pin description | 4 |
| 6 | Functional description | 5 |
| 6.1 | Enable | 5 |
| 6.2 | I ² C-bus systems | 5 |
| 7 | Application design-in information | 5 |
| 8 | Limiting values | 7 |
| 9 | Static characteristics | 8 |
| 10 | Dynamic characteristics | 10 |
| 11 | Test information | 11 |
| 12 | Package outline | 12 |
| 13 | Soldering of SMD packages | 14 |
| 13.1 | Introduction to soldering | 14 |
| 13.2 | Wave and reflow soldering | 14 |
| 13.3 | Wave soldering | 14 |
| 13.4 | Reflow soldering | 15 |
| 14 | Abbreviations | 16 |
| 15 | Revision history | 17 |
| 16 | Legal information | 18 |
| 16.1 | Data sheet status | 18 |
| 16.2 | Definitions | 18 |
| 16.3 | Disclaimers | 18 |
| 16.4 | Trademarks | 18 |
| 17 | Contact information | 18 |
| 18 | Contents | 19 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

founded by

PHILIPS

© NXP B.V. 2009.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 23 April 2009

Document identifier: PCA9516A_3

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

[PCA9516AD,112](#) [PCA9516AD,118](#) [PCA9516APW,112](#) [PCA9516APW,118](#)



**Стандарт
Электрон
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331