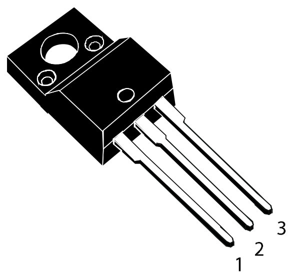
STF17N80K5

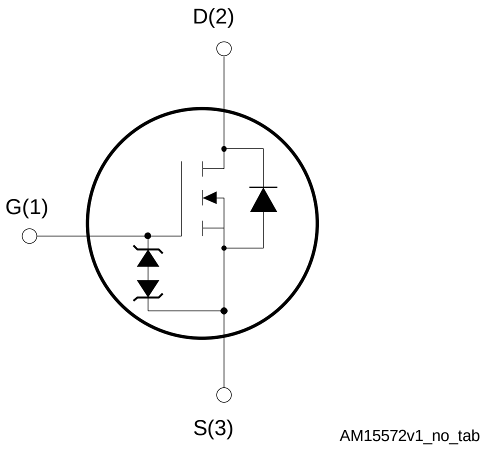
N-channel 800 V, 0.29 Ω typ., 14 A MDmesh™ K5 Power MOSFET in a TO-220FP package

Datasheet - production data



TO-220FP

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF17N80K5	800 V	0.34 Ω	14 A

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STF17N80K5	17N80K5	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	14	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	9	A
I_{DM} (2)	Drain current (pulsed)	56	A
P_{TOT}	Total dissipation at T_C = 25 °C	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)	2500	V
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
T_J	Operating junction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range	- 55 to 150	°C

Notes:

(1)Limited by maximum junction temperature.

(2)Pulse width limited by safe operating area

(3)I_{SD} ≤ 14 A, di/dt 100 A/µs; V_{DS} peak < $V_{(BR)DSS}$,V_{DD}= 400 V

(4)V_{DS} ≤ 640 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	4.2	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	4.7	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	340	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V T_C = 125 °C			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DD} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7 A		0.29	0.34	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	866	-	pF
C_{oss}	Output capacitance		-	64	-	pF
C_{rss}	Reverse transfer capacitance		-	0.42	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	142	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	51	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz , I_D= 0 A	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 14 A V_{GS}= 10 V See (*Figure 15: "Test circuit for gate charge behavior"*)	-	26	-	nC
Q_{gs}	Gate-source charge		-	7.2	-	nC
Q_{gd}	Gate-drain charge		-	15.2	-	nC

Notes:

(1)Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2)Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 400 V, I_D =7 A, R_G = 4.7 Ω V_{GS} = 10 V See (*Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	14.8	-	ns
t_r	Rise time		-	10.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	84.3	-	ns
t_f	Fall time		-	10.1	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
I_{SDM} (1)	Source-drain current (pulsed)		-		56	A
V_{SD} (2)	Forward on voltage	I_{SD} = 14 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 14 A, di/dt = 100 A/µs,V_{DD} = 60 V See *Figure 16: "Test circuit for inductive load switching and diode recovery times"*	-	439		ns
Q_{rr}	Reverrse recovery charge		-	6.37		µC
I_{RRM}	Reverse recovery current		-	29		A
t_{rr}	Reverse recovery time	I_{SD} = 14 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C See *Figure 16: "Test circuit for inductive load switching and diode recovery times"*	-	626		ns
Q_{rr}	Reverse recovery charge		-	8.36		µC
I_{RRM}	Reverse recovery current		-	26.7		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1mA, I_D= 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection,thus eliminating the need for additional external componentry.

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

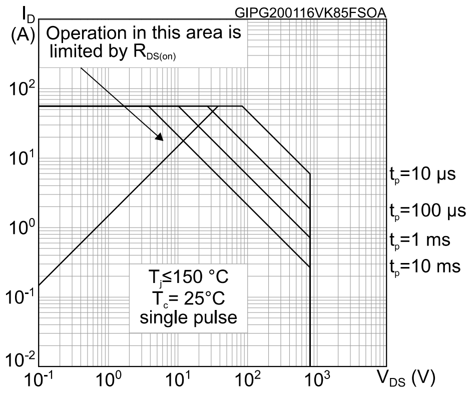


Figure 3: Thermal impedance

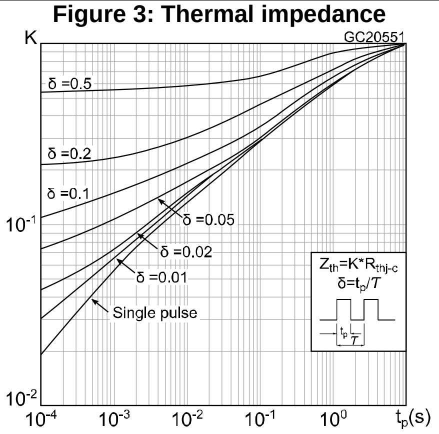


Figure 4: Output characteristics

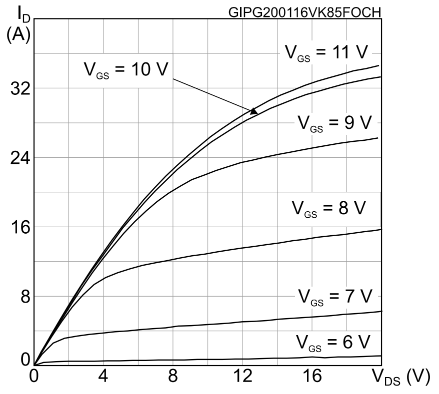


Figure 5: Transfer characteristics

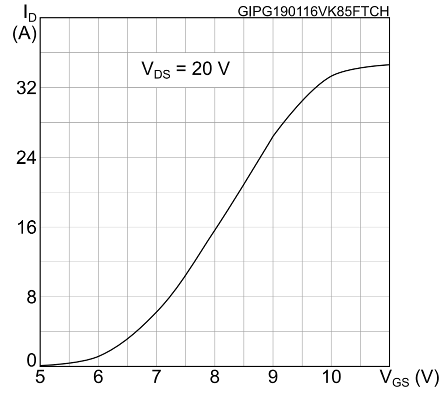


Figure 6: Gate charge vs gate-source voltage

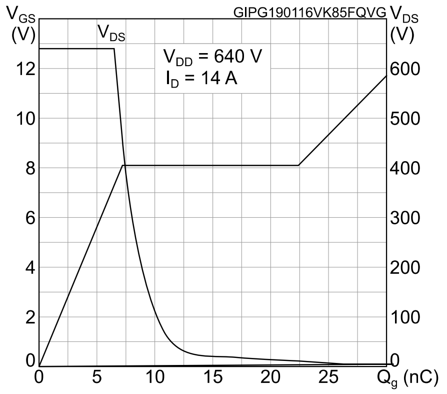


Figure 7: Static drain-source on-resistance

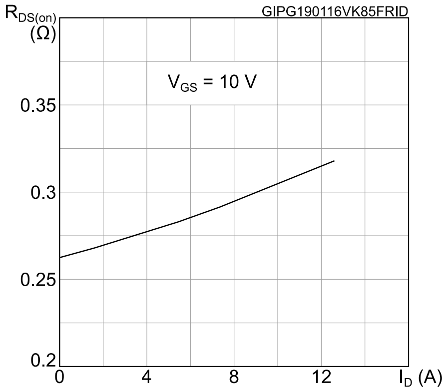


Figure 8: Capacitance variations

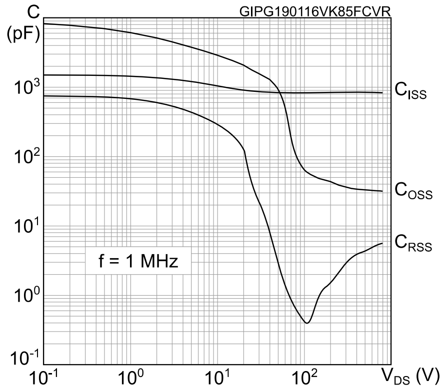


Figure 9: Normalized gate threshold voltage vs temperature

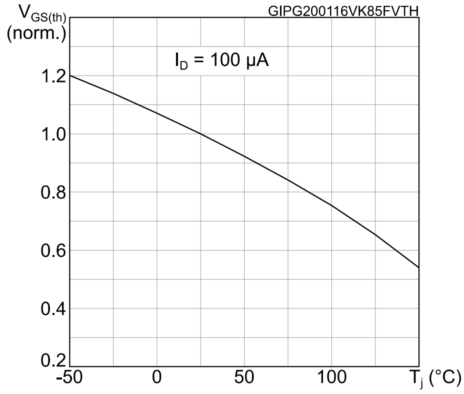


Figure 10: Normalized on-resistance vs temperature

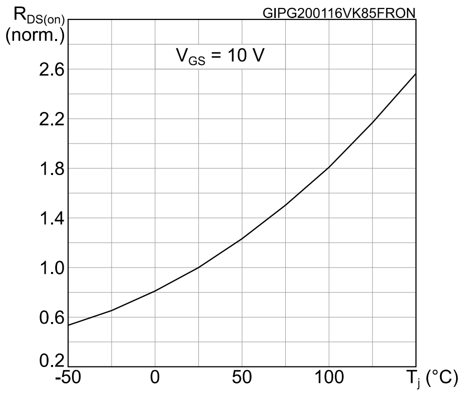


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

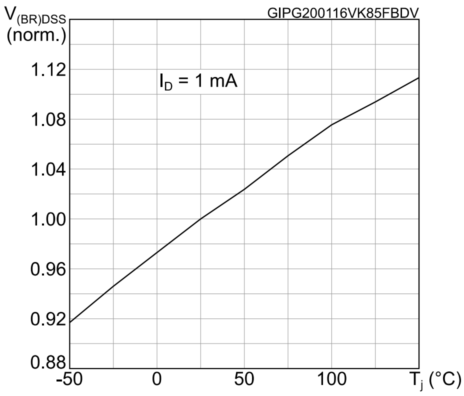


Figure 12: Source-drain diode forward characteristics

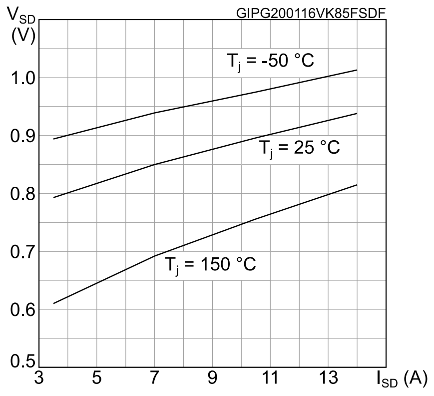
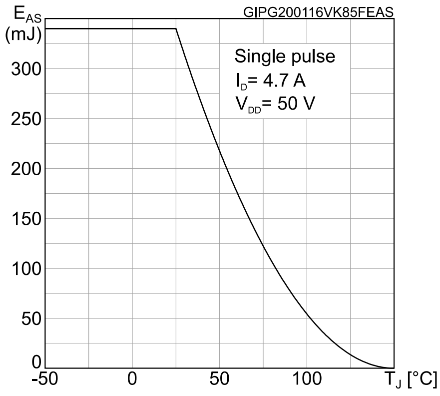


Figure 13: Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 14: Test circuit for resistive load switching times

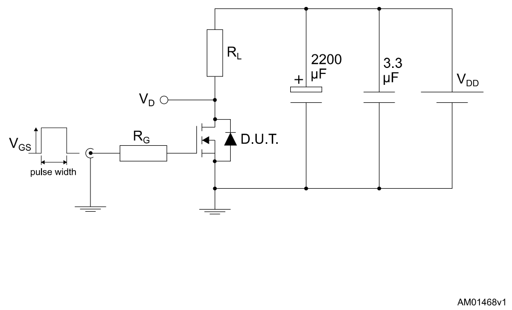


Figure 15: Test circuit for gate charge behavior

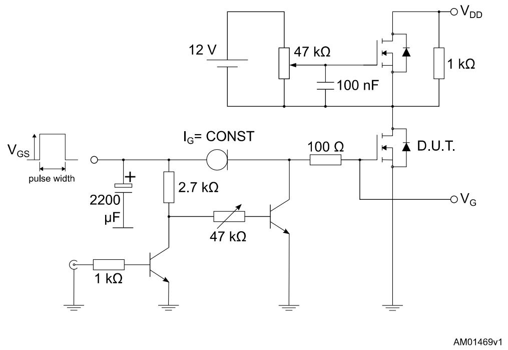


Figure 16: Test circuit for inductive load switching and diode recovery times

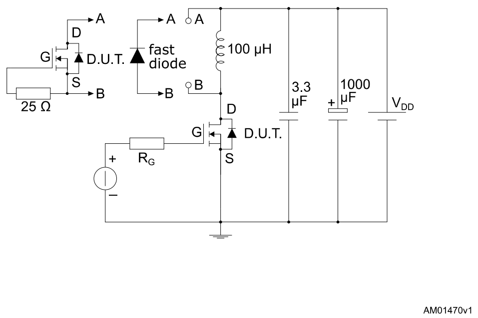


Figure 17: Unclamped inductive load test circuit

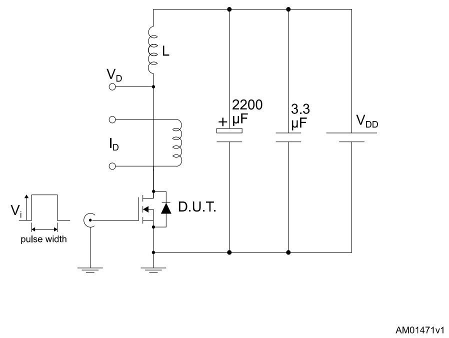


Figure 18: Unclamped inductive waveform

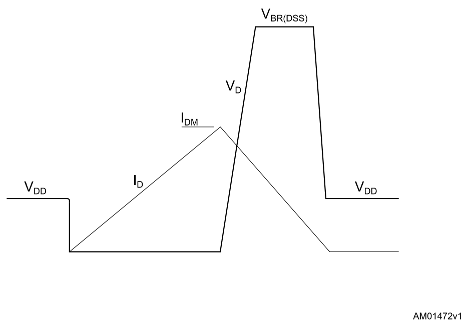
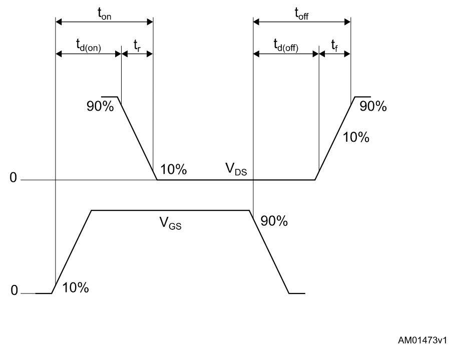


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 FP package information

Figure 20: TO-220FP package outline

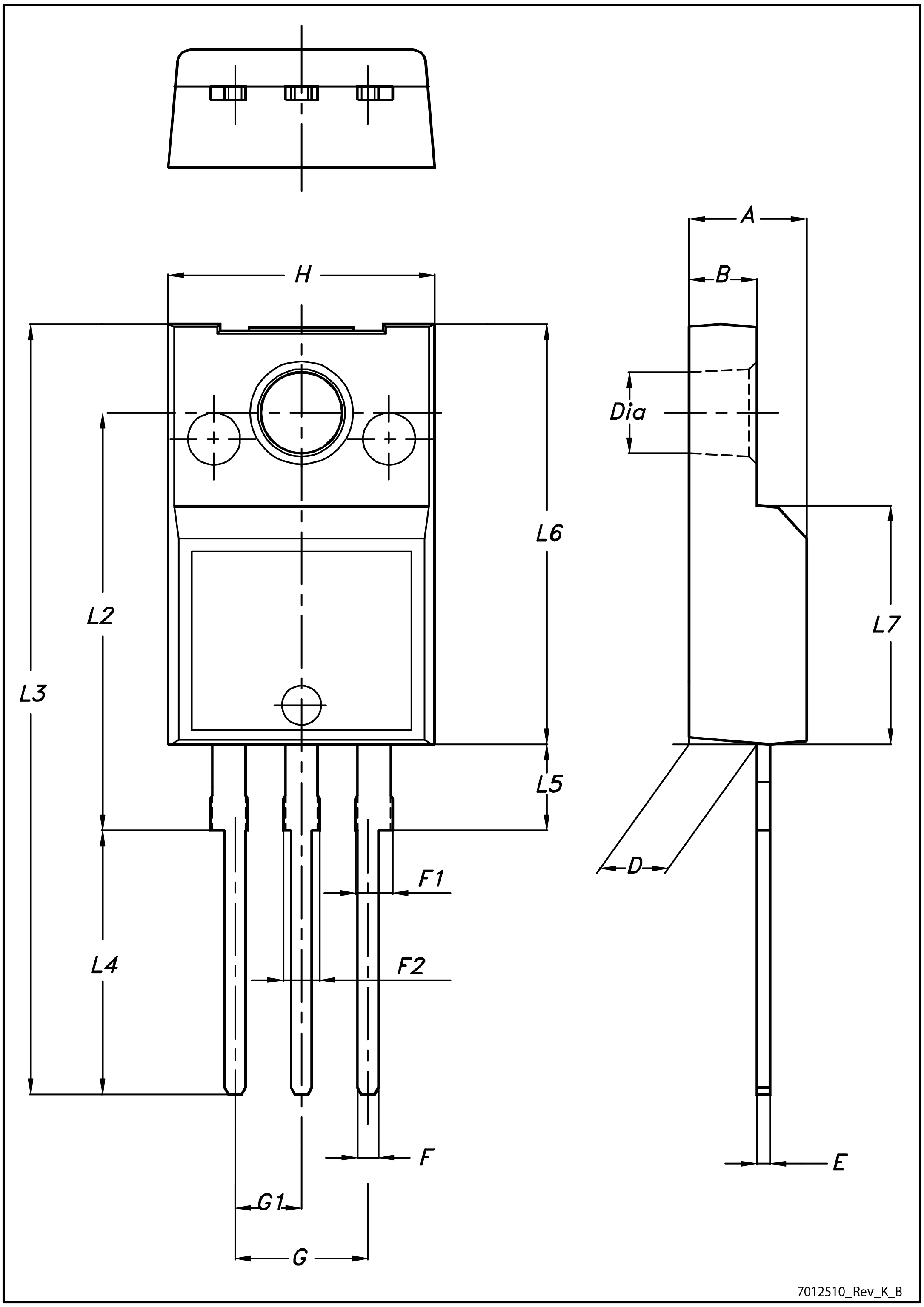


Table 10: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
31-Mar-2015	1	First release.
20-Jan-2016	2	Modified: *Table 4: "Avalanche characteristics"*, *Table 6: "Dynamic"*, *Table 7: "Switching times"*, and *Table 8: "Source-drain diode"* Added: *Section 3.1: "Electrical characteristics (curves)"* Minor text changes

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