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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

November 2009

FDY4000CZ
Complementary N & P-Channel PowerTrench® MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)} = 0.7\Omega$ at $V_{GS} = 4.5V$, $I_D = 600mA$
- Max $r_{DS(on)} = 0.85\Omega$ at $V_{GS} = 2.5V$, $I_D = 500mA$
- Max $r_{DS(on)} = 1.25\Omega$ at $V_{GS} = 1.8V$, $I_D = 150$ mA

Q2: P-Channel

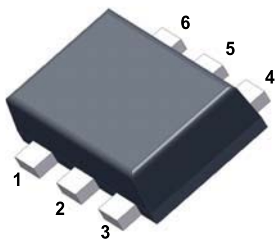
- Max $r_{DS(on)} = 1.2\Omega$ at $V_{GS} = -4.5V$, $I_D = -350mA$
- Max $r_{DS(on)} = 1.6\Omega$ at $V_{GS} = -2.5V$, $I_D = -300mA$
- Max $r_{DS(on)} = 2.7\Omega$ at $V_{GS} = -1.8V$, $I_D = -150mA$
- ESD protection diode (note 3)
- RoHS Compliant

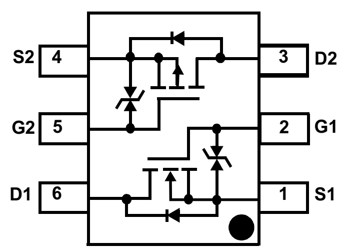
General Description

This Complementary N & P-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench® process to optimize the $r_{DS(ON)}$ @ V_{GS}= 2.5V and specify the $r_{DS(ON)}$ @ V_{GS} = 1.8V.

Applications

- Level shifting
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		20	-20	V
V_{GS}	Gate to Source Voltage		±12	±8	V
I_D	Drain Current -Continuous	(Note 1a)	600	-350	mA
	-Pulsed		1000	-1000	
P_D	Power Dissipation (Steady State)	(Note 1a)	625		mW
		(Note 1b)	446		
T_J, T_{STG}	Operating and Storage Jaunting Temperature Range		-55 to 150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	200	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	280	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
E	FDY4000CZ	SC89-6	7"	8mm	3000units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V I_D = -250μA, V_{GS} = 0V	Q1 Q2	20 -20			V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = -250μA, referenced to 25°C	Q1 Q2		15 -15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16V, V_{DS} =0V V_{DS} = -16V, V_{DS} =0V	Q1 Q2			1 -3	μA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±12V, V_{DS} = 0V V_{GS} = ±4.5V, V_{DS} = 0V V_{GS} = ±8V, V_{DS} = 0V	Q1 Q1 Q2			±10 ±1 ±10	μA
On Characteristics (note 2)							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA V_{GS} = V_{DS}, I_D = -250μA	Q1 Q2	0.6 -0.6	1.0 -1.0	1.5 -1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = -250μA, referenced to 25°C	Q1 Q2		-3 3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 600mA V_{GS} = 2.5V, I_D = 500mA V_{GS} = 1.8V, I_D = 150mA, V_{GS} = 4.5V, I_D = 600mA,T_J = 125°C	Q1		0.30 0.40 0.80 0.35	0.70 0.85 1.25 1.00	Ω
		V_{GS} = -4.5V, I_D = --350mA V_{GS} = -2.5V, I_D = -300mA V_{GS} = -1.8V, I_D = -150mA V_{GS} = -4.5V, I_D = -350mA, T_J =125°C	Q2		0.5 0.8 1.3 0.7	1.2 1.6 2.7 1.6	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 600mA V_{DS} = -5V, I_D = -350mA	Q1 Q2		1.8 1		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 V_{DS} = 10V, V_{GS} = 0V, f = 1MHz Q2 V_{DS} = -10V, V_{GS} = 0V, f = 1MHz	Q1 Q2		60 100		pF
C_{oss}	Output Capacitance		Q1 Q2		20 30		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		10 15		pF
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD}= 10V, I_D = 1A, V_{GS}= 4.5V, R_g = 6Ω Q2 V_{DD}= -10V, I_D = -0.5A, V_{GS}= -4.5V, R_g = 6Ω	Q1 Q2		6 6	12 12	ns
t_r	Rise Time		Q1 Q2		8 13	16 23	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		8 8	16 16	ns
t_f	Fall Time		Q1 Q2		2.4 1	4.8 2	ns
Q_g	Total Gate Charge	Q1 V_{DS}= 10V, I_D = 600mA, V_{GS}= 4.5V Q2 V_{DS}= -10V, I_D = -350mA, V_{GS}= -4.5V	Q1 Q2		0.8 1.0	1.1 1.4	nC
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		0.16 0.2		nC
Q_{gd}	Gate to Drain "Miller"Charge		Q1 Q2		0.26 0.3		nC

Electrical Characteristics T_J = 25°C unless otherwise noted

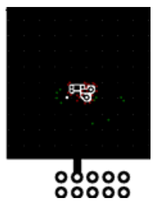
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units

Drain-Source Diode Characteristics

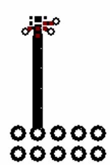
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 150mA (Note 2) V_{GS} = 0V, I_S = -150mA (Note 2)	Q1 Q2		0.7 -0.8	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 600mA, di/dt = 100A/µs	Q1 Q2		8 11		ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = -350mA, di/dt = 100A/µs	Q1 Q2		1 2		nC

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 200°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 280°C/W when mounted on a minimum pad of 2 oz copper

Scale 1:1 on letter size paper

2: Pulse Test : Pulse Width < 300us, Duty Cycle < 2.0%

3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics Q1 (N-Channel)

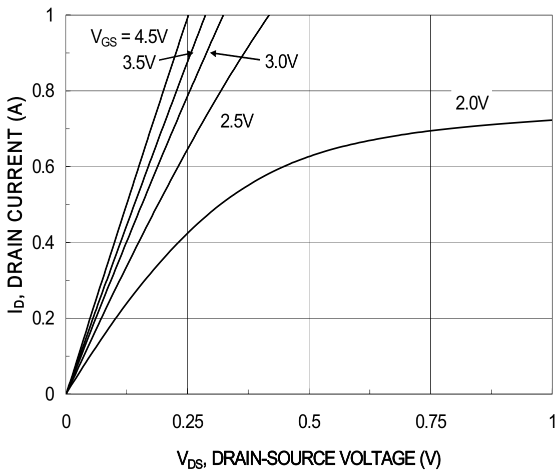


Figure 1. On-Region Characteristics

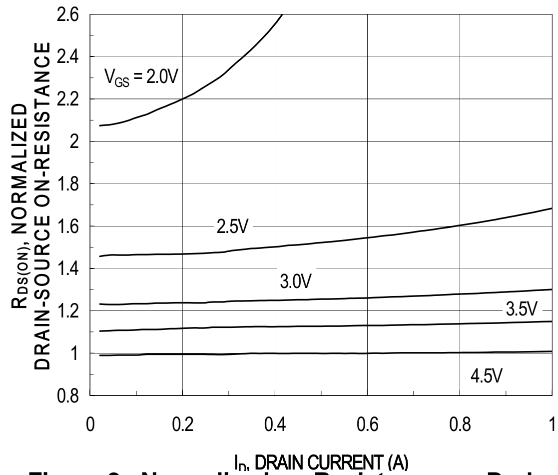


Figure 2. Normalized on-Resistance vs. Drain Current and Gate Voltage

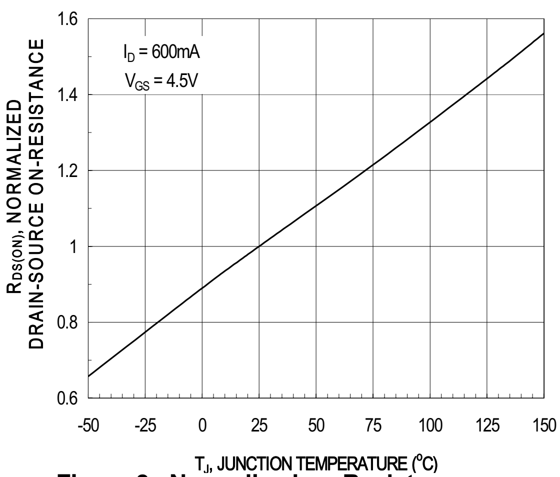


Figure 3. Normalized on-Resistance vs. Temperature

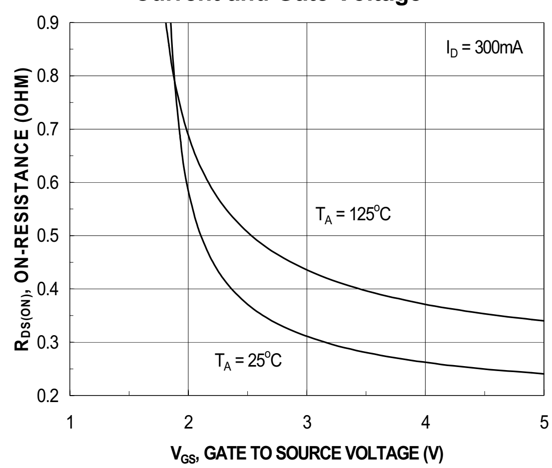


Figure 4. On-Resistance vs. Gate-to-Source Voltage

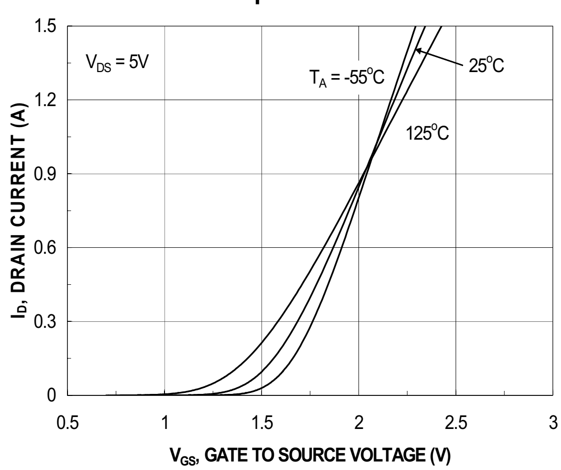


Figure 5. Transfer Characteristics

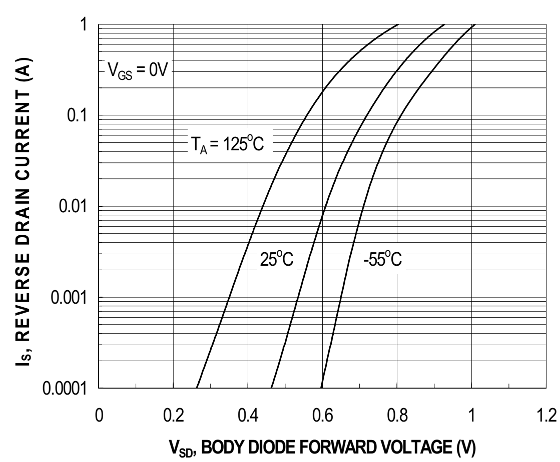


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current and Temperature

Typical Characteristics Q1 (N-Channel)

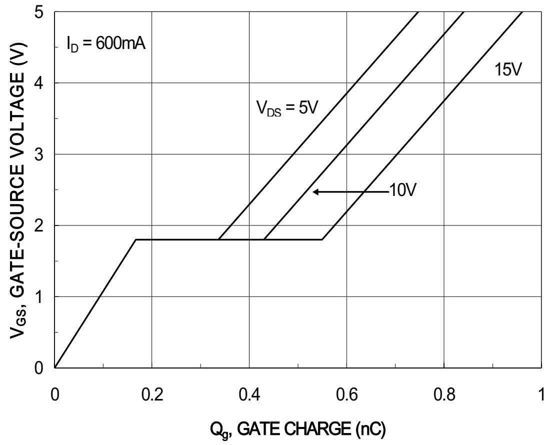


Figure 7. Gate Charge Characteristics

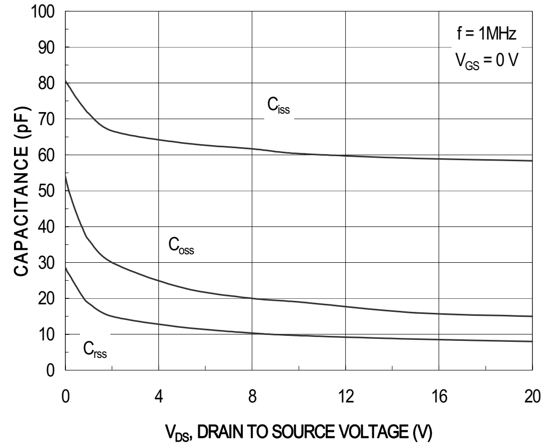


Figure 8. Capacitance vs. Drain to source voltage

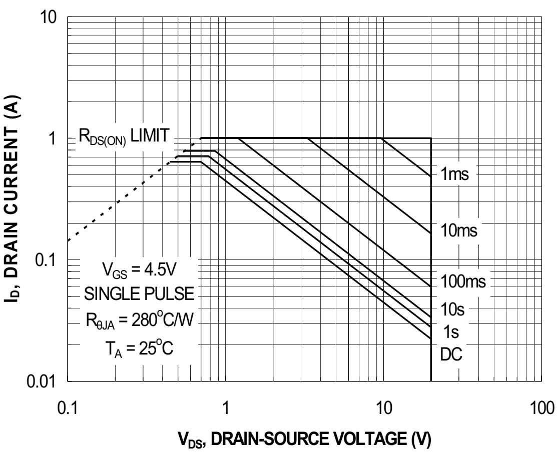


Figure 9. Maximum Safe Operating Area

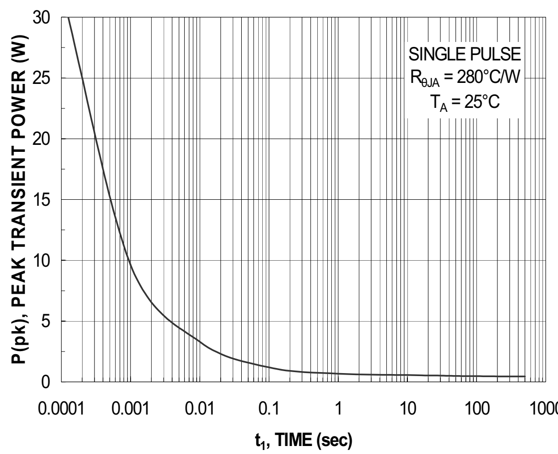


Figure 10. Single Pulse Maximum Power Dissipation

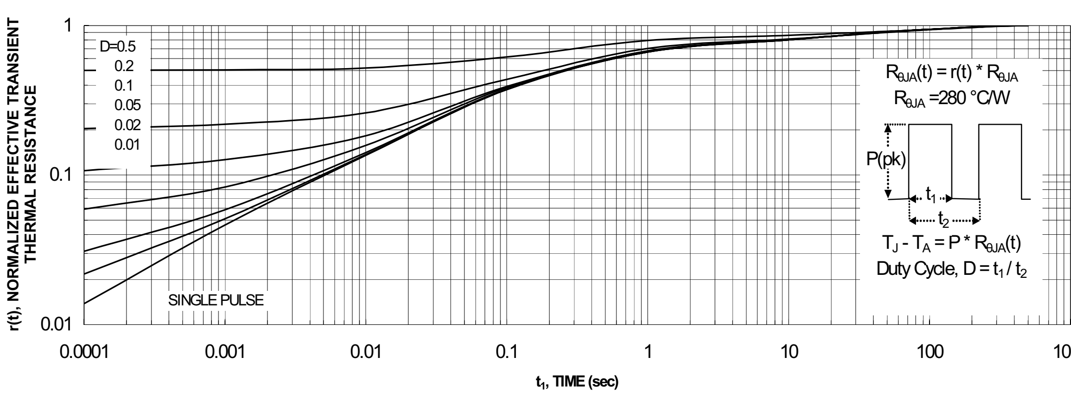


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics Q2 (P-Channel)

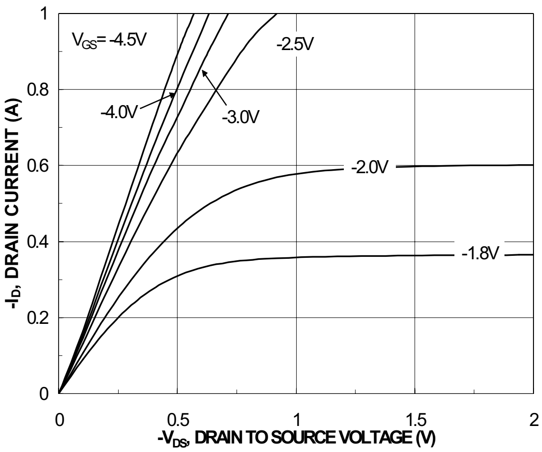


Figure 12. On-Region Characteristics

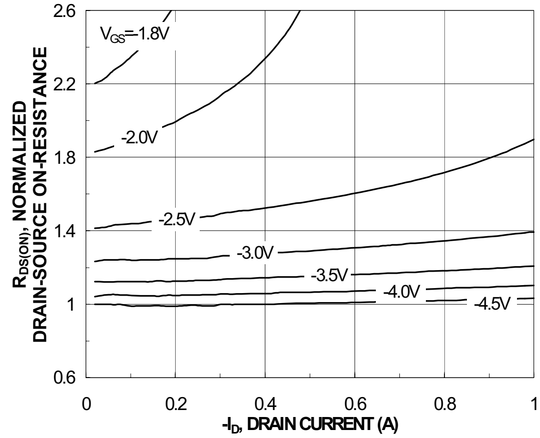


Figure 13. Normalized on-Resistance vs. Drain Current and Gate Voltage

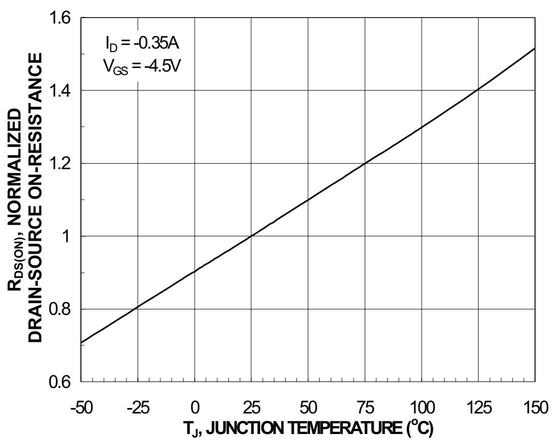


Figure 14. Normalized on-Resistance vs. Temperature

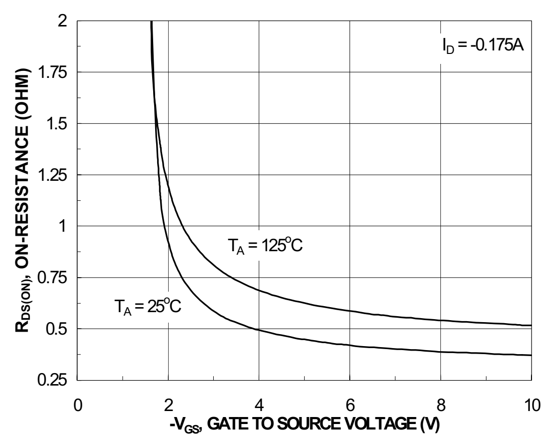


Figure 15. On-Resistance vs. Gate-to-Source Voltage

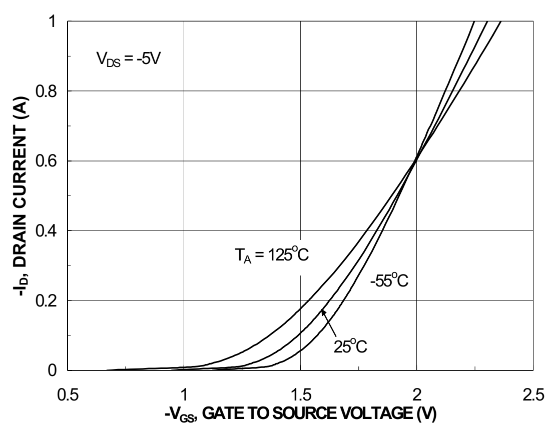


Figure 16. Transfer Characteristics

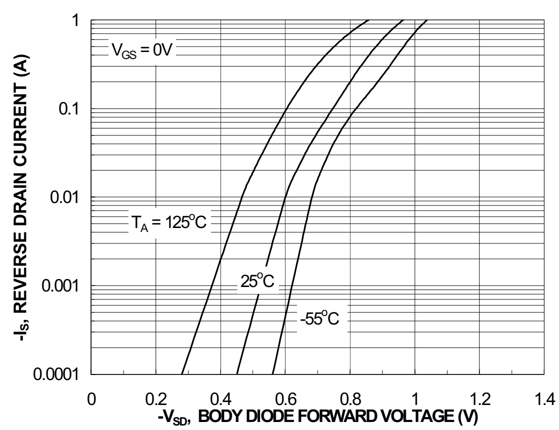


Figure 17. Source to Drain Diode Forward Voltage vs. Source Current and Temperature

Typical Characteristics Q2 (P-Channel)

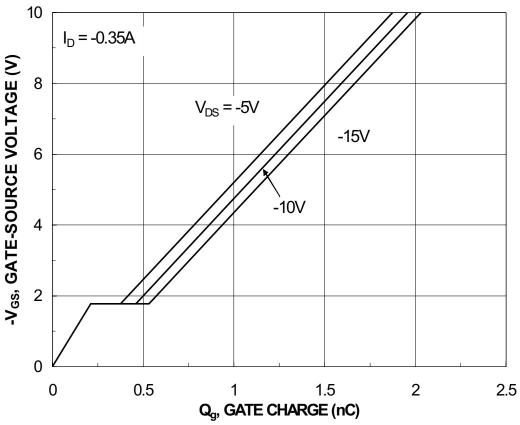


Figure 18. Gate Charge Characteristics

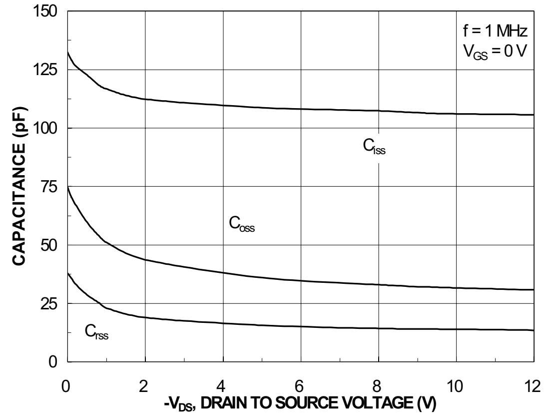


Figure 19. Capacitance vs. Drain to source voltage

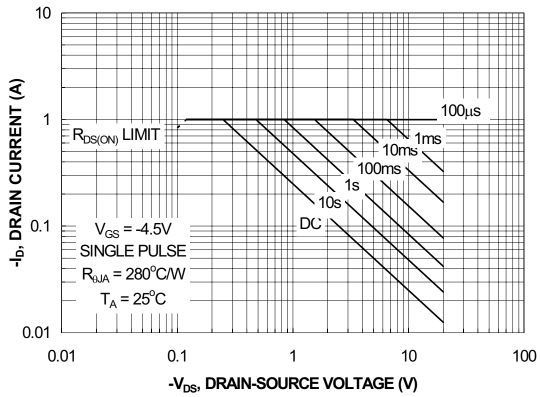


Figure 20. Maximum Safe Operating Area

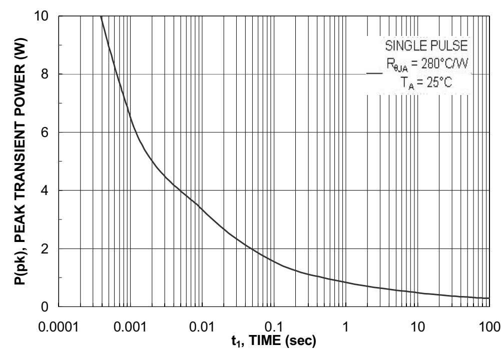


Figure 21. Single Pulse Maximum Power Dissipation

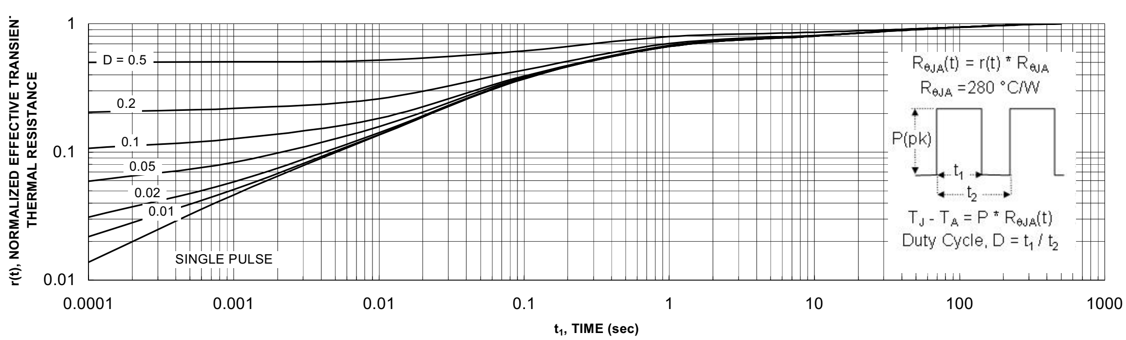
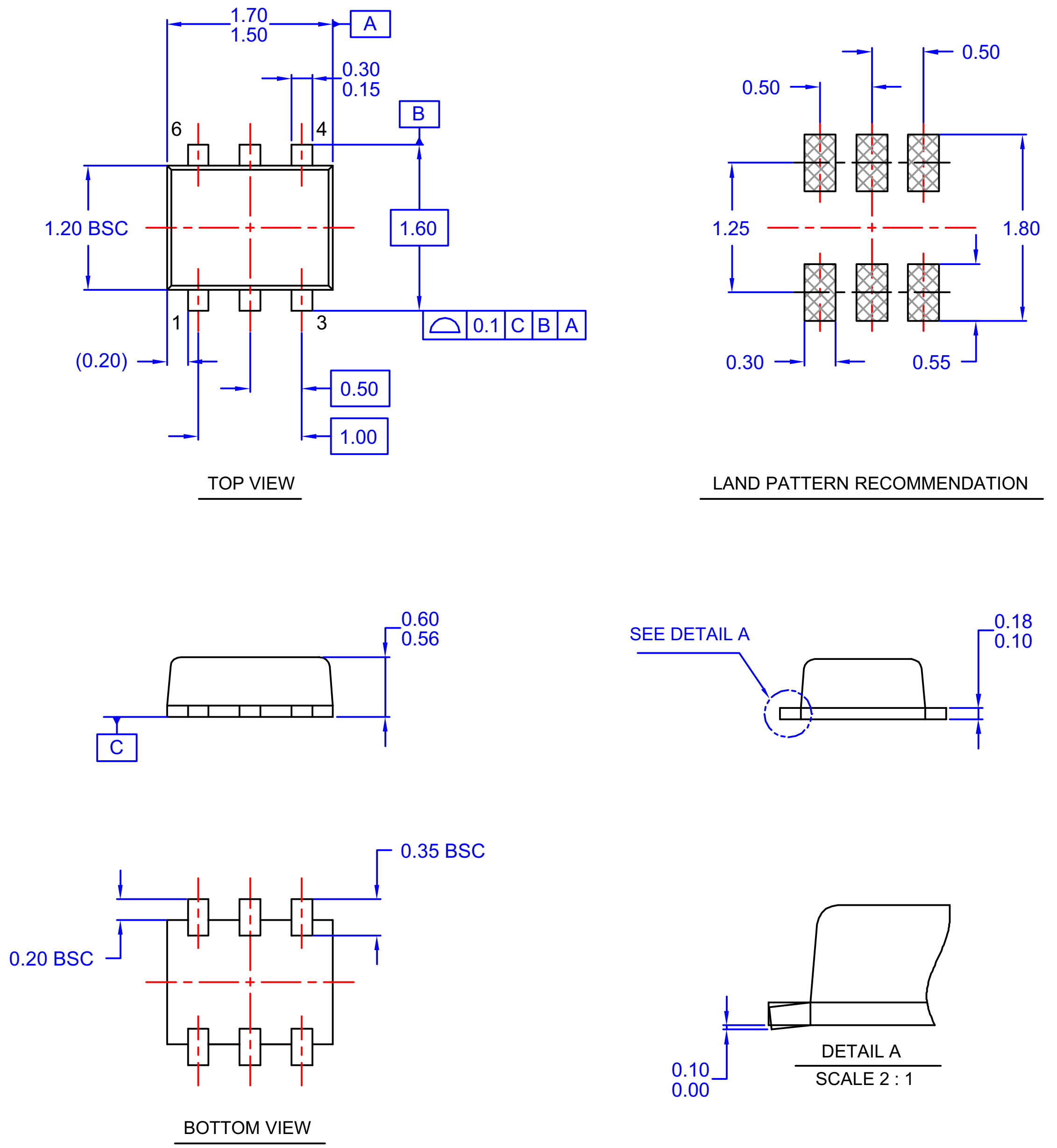


Figure 22. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES:
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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994
D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I41

PUBLICATION ORDERING INFORMATION

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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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