



# PCF8577C

## LCD direct/duplex driver with I<sup>2</sup>C-bus interface

Rev. 5 — 10 October 2014

Product data sheet

### 1. General description

The PCF8577C is an LCD driver which drives up to 32 segments directly, or 64 segments in a duplex configuration.

The two-line I<sup>2</sup>C-bus interface substantially reduces wiring overheads in remote display applications. I<sup>2</sup>C-bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode). To allow partial V<sub>DD</sub> shutdown, the ESD protection system of the SCL and SDA pins does not use a diode connected to V<sub>DD</sub>.

For a selection of NXP LCD segment drivers, see [Table 13 on page 25](#).

### 2. Features and benefits

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 V to 6 V
- Low power consumption
- I<sup>2</sup>C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I<sup>2</sup>C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display
- I<sup>2</sup>C-bus address: 0111 0100.

### 3. Ordering information

Table 1. Ordering information

| Type number | Package |  |          |
|-------------|---------|--|----------|
|             | Name    | Description                                  | Version  |
| PCF8577CT   | VSO40   | plastic very small outline package; 40 leads | SOT158-1 |



3.1 Ordering options

Table 2. Ordering options

| Product type number | Orderable part number | Sales item (12NC) | Delivery form          | IC revision |
|---------------------|-----------------------|-------------------|------------------------|-------------|
| PCF8577CT/3         | PCF8577CT/3,112       | 935278866112      | tube                   | 3           |
| PCF8577CT/3         | PCF8577CT/3,118       | 935278866118      | tape and reel, 13 inch | 3           |

4. Marking

Table 3. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PCF8577CT/3 | PCF8577CT    |

5. Block diagram

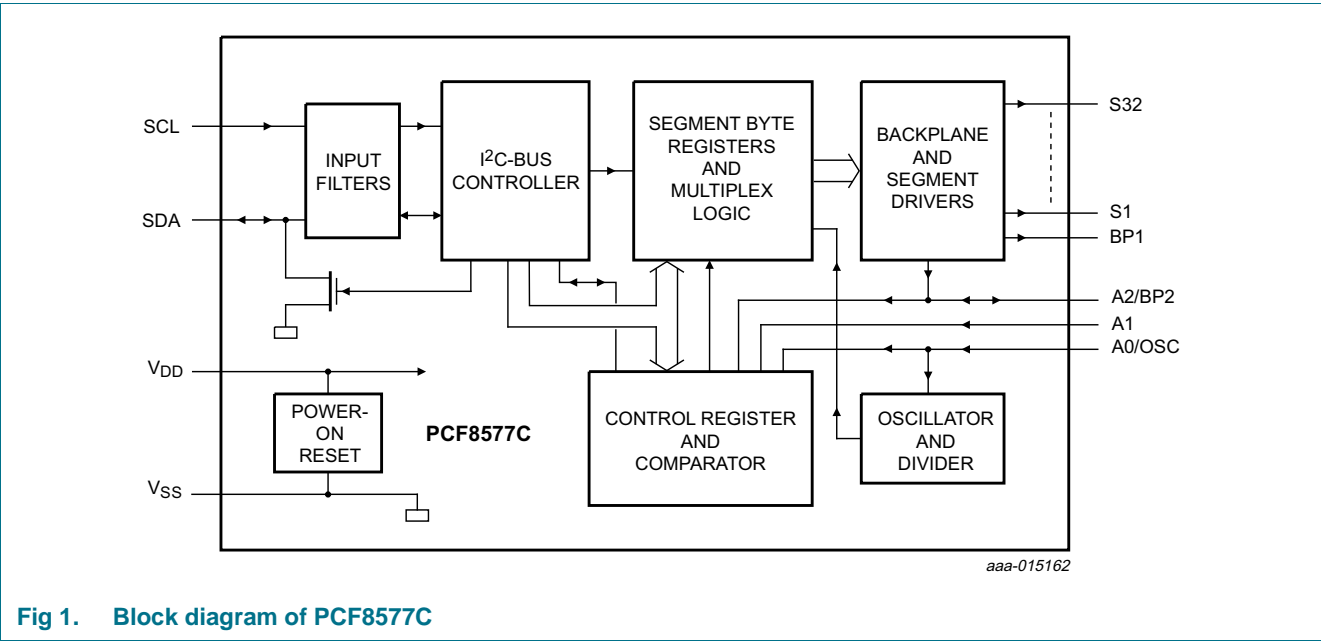


Fig 1. Block diagram of PCF8577C

6. Pinning information

6.1 Pinning

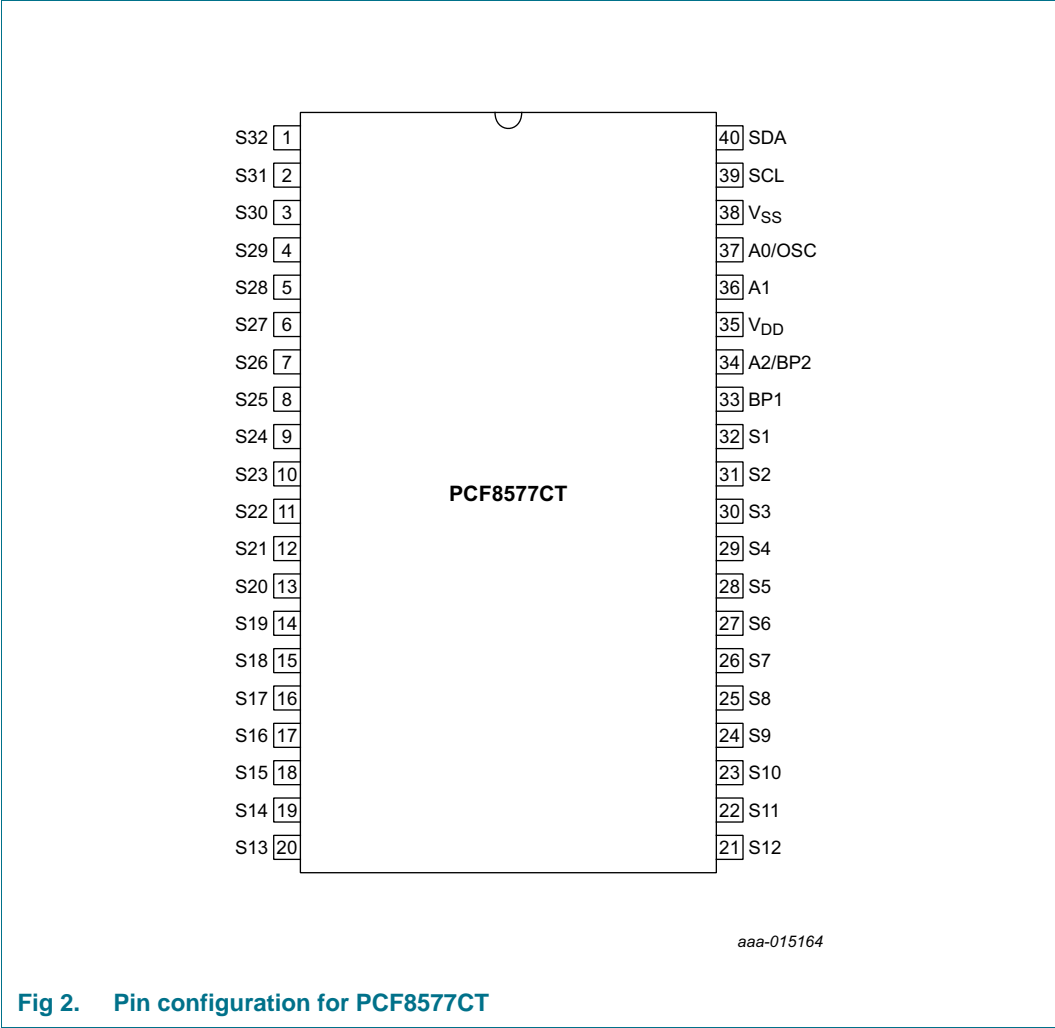


Fig 2. Pin configuration for PCF8577CT

## 6.2 Pin description

Table 4. Pin description

| Symbol          | Pin     | Type         | Description   |
|-----------------|---------|--------------|---|
| S32 to S1       | 1 to 32 | outputs      | segment outputs   |
| BP1             | 33      | input/output | cascaded sync input/backplane output                          |
| A2/BP2          | 34      | input/output | hardware address line and cascade sync input/backplane output |
| V <sub>DD</sub> | 35      | supply       | supply voltage  |
| A1              | 36      | input        | hardware address line input                                   |
| A0/OSC          | 37      | input        | hardware address line and oscillator pin input                |
| V <sub>SS</sub> | 38      | supply       | ground supply   |
| SCL             | 39      | input        | I <sup>2</sup> C-bus clock line input                         |
| SDA             | 40      | input/output | I <sup>2</sup> C-bus data line input/output                   |

## 7. Functional description

### 7.1 Hardware subaddress lines A0, A1, and A2

The hardware subaddress lines A0, A1, and A2 are used to program the device subaddress for each PCF8577C connected to the I<sup>2</sup>C-bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pinout requirements.

1. Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V<sub>SS</sub>. Line A0 is defined as HIGH (logic 1) when connected to V<sub>DD</sub>.
2. Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V<sub>SS</sub> or V<sub>DD</sub> respectively.
3. In the direct drive mode, the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V<sub>SS</sub> or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V<sub>DD</sub>.
4. In the duplex drive mode, the second backplane signal BP2 is required and the A2 signal is undefined. In this mode, device selection is made exclusively from lines A0 and A1.

### 7.2 Oscillator A0/OSC

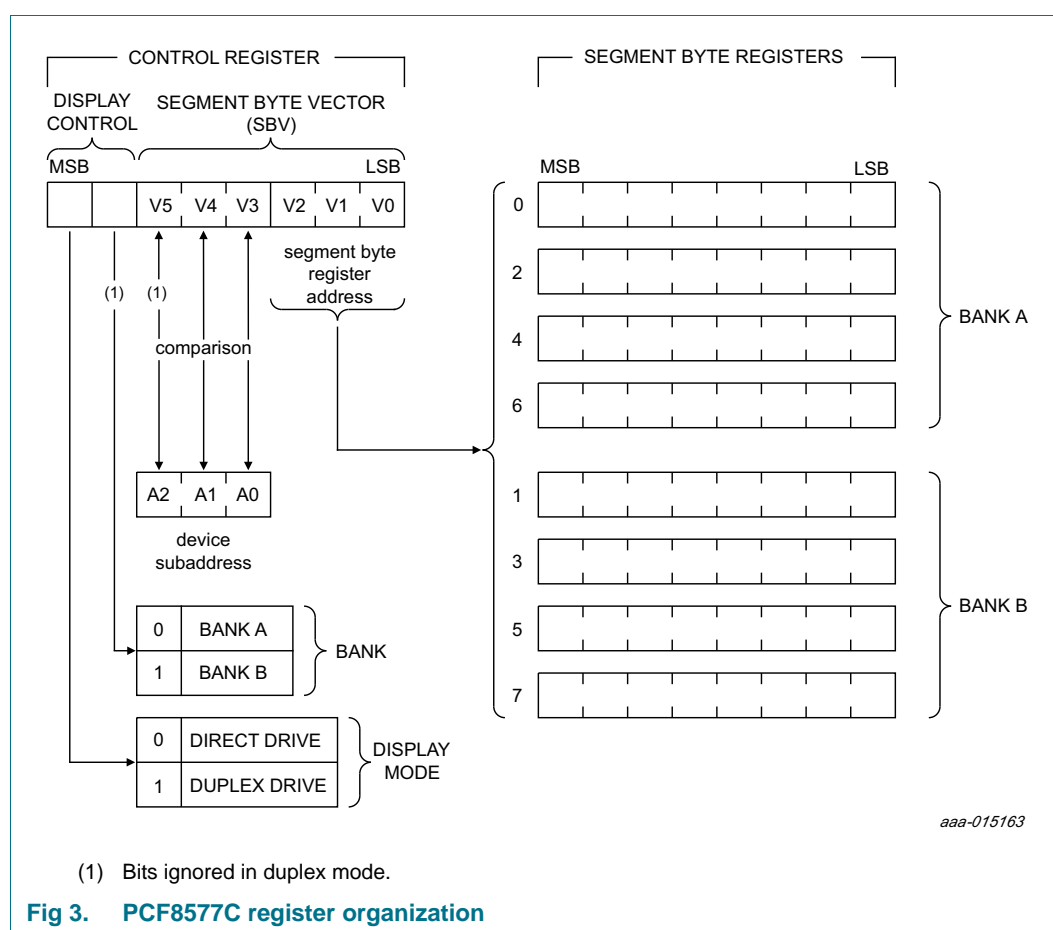
The PCF8577C has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator (see [Figure 13](#) and [Figure 14](#)). For correct start-up of the oscillator after power-on, the resistor and capacitor must be connected to the same V<sub>SS</sub>/V<sub>DD</sub> as the chip. In an expanded system containing more than one PCF8577C the backplane signals are usually common to all devices and only one oscillator is required. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V<sub>DD</sub> or V<sub>SS</sub> depending on the required state for A0. In the cascade mode, each PCF8577C is synchronized from the backplane signals.

### 7.3 User-accessible registers

There are nine user-accessible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even-numbered segment byte registers is called BANK A. Odd-numbered segment byte registers are called BANK B.

There is one slave address for the PCF8577C (see [Table 7](#)). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register always (see I<sup>2</sup>C-bus protocol, [Figure 10](#)), i.e. all addressed devices respond to control commands sent on the I<sup>2</sup>C-bus.

The control register is shown in more detail in [Figure 3](#). The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).



The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same, then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

## 7.4 Auto-incremented loading

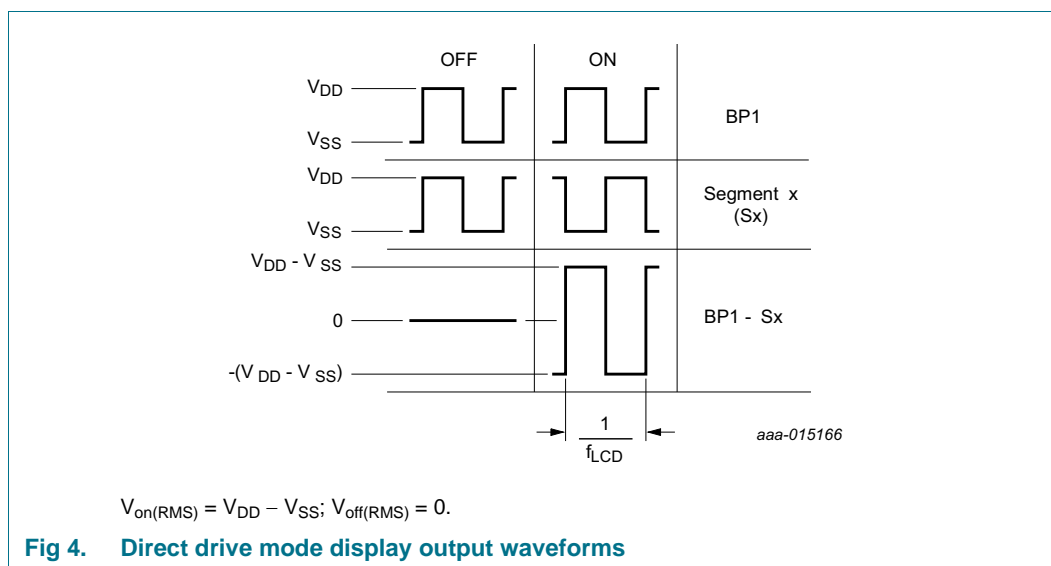
After each segment byte is loaded, the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries if the hardware subaddresses are arranged contiguously.

## 7.5 Direct drive mode

The PCF8577C is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode, only four bytes are required to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A), setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode, the SBV is auto-incremented by two after the loading of each segment byte register. This means, that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in [Figure 4](#).

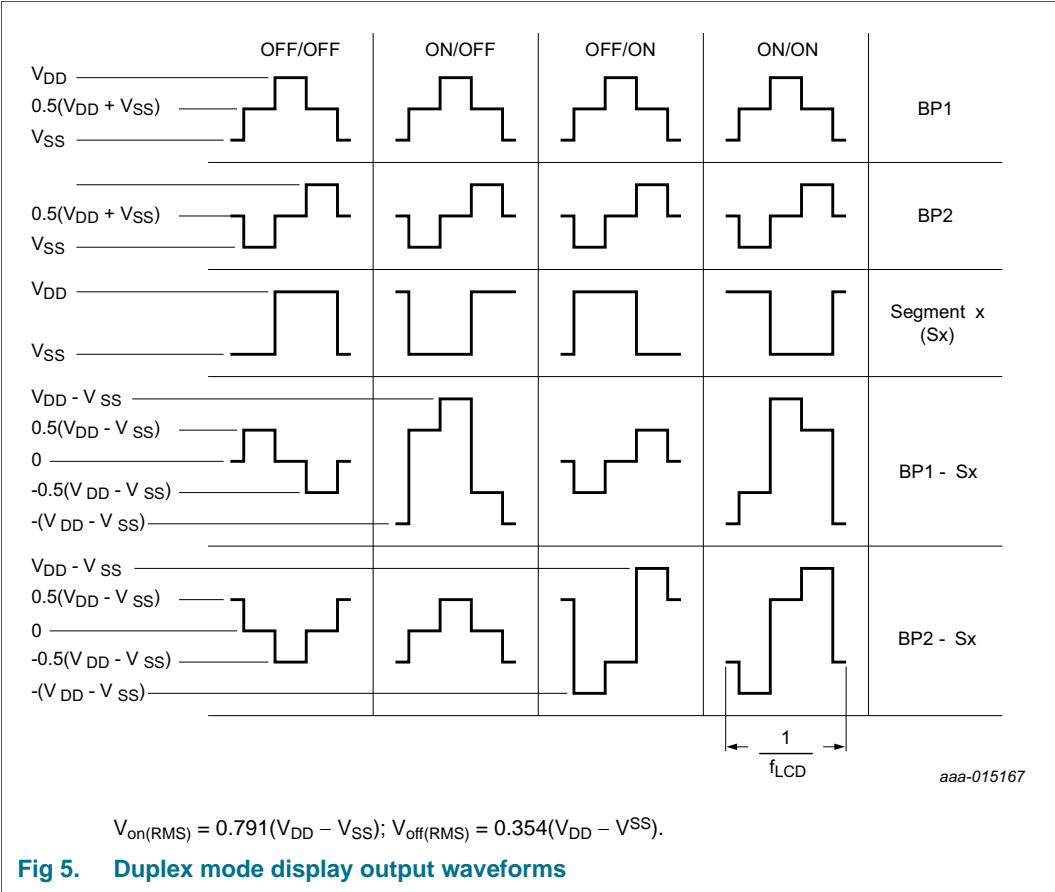


## 7.6 Duplex mode

The PCF8577C is set to the duplex mode by loading the MODE bit with logic 1. In this mode, a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are required to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in [Figure 5](#).



7.7 Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is given in [Table 5](#) and [Table 6](#).

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0, even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode. In duplex mode, even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 5. Segment byte-segment driver mapping in direct drive mode

| Mode | Bank | V2 | V1 | V0 | Segment/<br>Bit/<br>Register | 7<br>MSB | 6   | 5   | 4   | 3   | 2   | 1   | 0<br>LSB | Backplane |
|------|------|----|----|----|------------------------------|----------|-----|-----|-----|-----|-----|-----|----------|-----------|
| 0    | 0    | 0  | 0  | 0  | 0                            | S8       | S7  | S6  | S5  | S4  | S3  | S2  | S1       | BP1       |
| 0    | 1    | 0  | 0  | 1  | 1                            | S8       | S7  | S6  | S5  | S4  | S3  | S2  | S1       | BP1       |
| 0    | 0    | 0  | 1  | 0  | 2                            | S16      | S15 | S14 | S13 | S12 | S11 | S10 | S9       | BP1       |
| 0    | 1    | 0  | 1  | 1  | 3                            | S16      | S15 | S14 | S13 | S12 | S11 | S10 | S9       | BP1       |
| 0    | 0    | 1  | 0  | 0  | 4                            | S24      | S23 | S22 | S21 | S20 | S19 | S18 | S17      | BP1       |
| 0    | 1    | 1  | 0  | 1  | 5                            | S24      | S23 | S22 | S21 | S20 | S19 | S18 | S17      | BP1       |
| 0    | 0    | 1  | 1  | 0  | 6                            | S32      | S31 | S30 | S29 | S28 | S27 | S26 | S25      | BP1       |
| 0    | 1    | 1  | 1  | 1  | 7                            | S32      | S31 | S30 | S29 | S28 | S27 | S26 | S25      | BP1       |

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

Table 6. Segment byte-segment driver mapping in duplex mode

| Mode | Bank             | V2 | V1 | V0 | Segment/<br>Bit/<br>Register | 7<br>MSB | 6   | 5   | 4   | 3   | 2   | 1   | 0<br>LSB | Backplane |
|------|------------------|----|----|----|------------------------------|----------|-----|-----|-----|-----|-----|-----|----------|-----------|
| 1    | X <sup>[1]</sup> | 0  | 0  | 0  | 0                            | S8       | S7  | S6  | S5  | S4  | S3  | S2  | S1       | BP1       |
| 1    | X <sup>[1]</sup> | 0  | 0  | 1  | 1                            | S8       | S7  | S6  | S5  | S4  | S3  | S2  | S1       | BP2       |
| 1    | X <sup>[1]</sup> | 0  | 1  | 0  | 2                            | S16      | S15 | S14 | S13 | S12 | S11 | S10 | S9       | BP1       |
| 1    | X <sup>[1]</sup> | 0  | 1  | 1  | 3                            | S16      | S15 | S14 | S13 | S12 | S11 | S10 | S9       | BP2       |
| 1    | X <sup>[1]</sup> | 1  | 0  | 0  | 4                            | S24      | S23 | S22 | S21 | S20 | S19 | S18 | S17      | BP1       |
| 1    | X <sup>[1]</sup> | 1  | 0  | 1  | 5                            | S24      | S23 | S22 | S21 | S20 | S19 | S18 | S17      | BP2       |
| 1    | X <sup>[1]</sup> | 1  | 1  | 0  | 6                            | S32      | S31 | S30 | S29 | S28 | S27 | S26 | S25      | BP1       |
| 1    | X <sup>[1]</sup> | 1  | 1  | 1  | 7                            | S32      | S31 | S30 | S29 | S28 | S27 | S26 | S25      | BP2       |

[1] Don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

## 7.8 Power-on reset

At power-on reset the PCF8577C resets to a defined starting condition as follows:

1. Both backplane outputs are set to  $V_{SS}$  in master mode; to 3-state in cascade mode
2. All segment outputs are set to  $V_{SS}$
3. The segment byte registers and control register are cleared
4. The I<sup>2</sup>C-bus interface is initialized.



## 8. I<sup>2</sup>C-bus interface

### 8.1 Characteristics of the I<sup>2</sup>C-Bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the I<sup>2</sup>C-bus is not busy.

#### 8.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals.

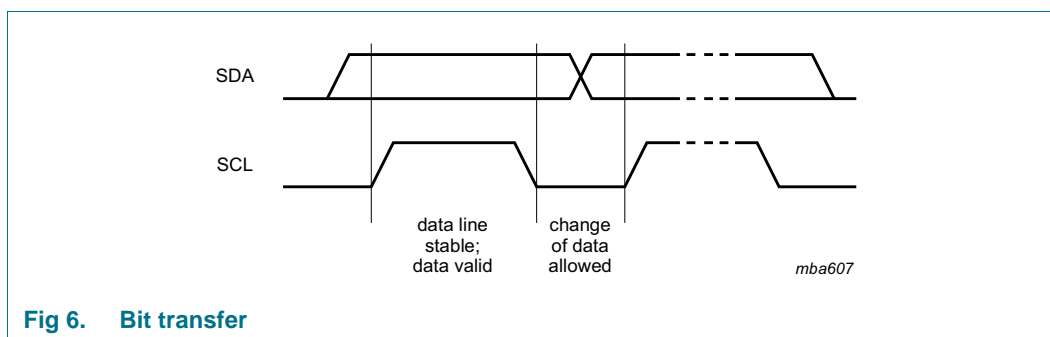


Fig 6. Bit transfer

#### 8.1.2 START and STOP conditions

Both data and clock lines remain HIGH when the I<sup>2</sup>C-bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

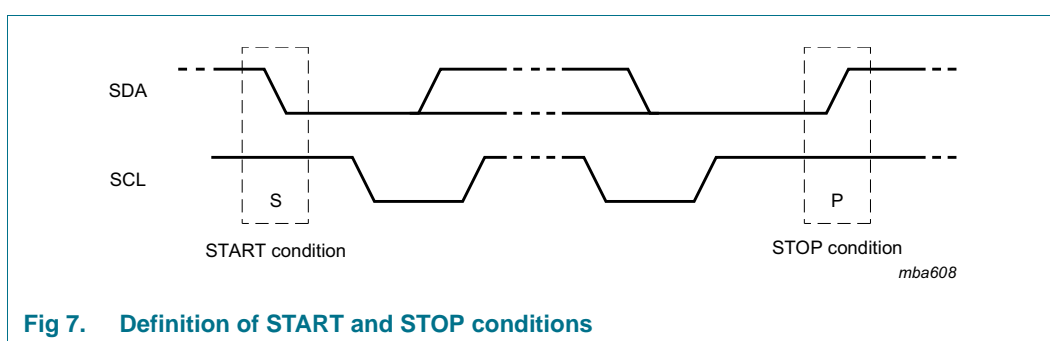


Fig 7. Definition of START and STOP conditions

#### 8.1.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

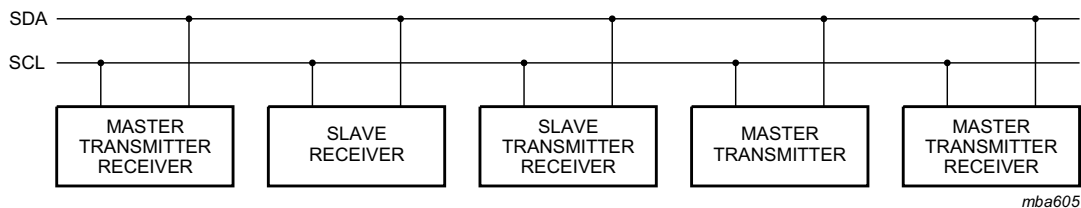


Fig 8. System configuration

8.1.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the I<sup>2</sup>C-bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

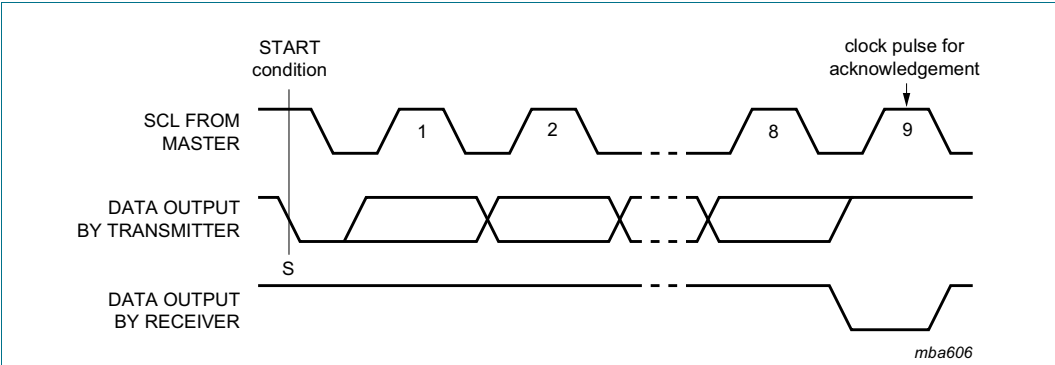


Fig 9. Acknowledgement of the I<sup>2</sup>C-bus

8.2 Slave address

The PCF8577C slave address is shown in [Table 7](#).

Table 7. I<sup>2</sup>C slave address byte

| Bit | Slave address |   |   |   |   |   |   | R/W      |
|-----|---------------|---|---|---|---|---|---|----------|
|     | 7<br>MSB      | 6 | 5 | 4 | 3 | 2 | 1 | 0<br>LSB |
|     | 0             | 1 | 1 | 1 | 0 | 1 | 0 | 0        |

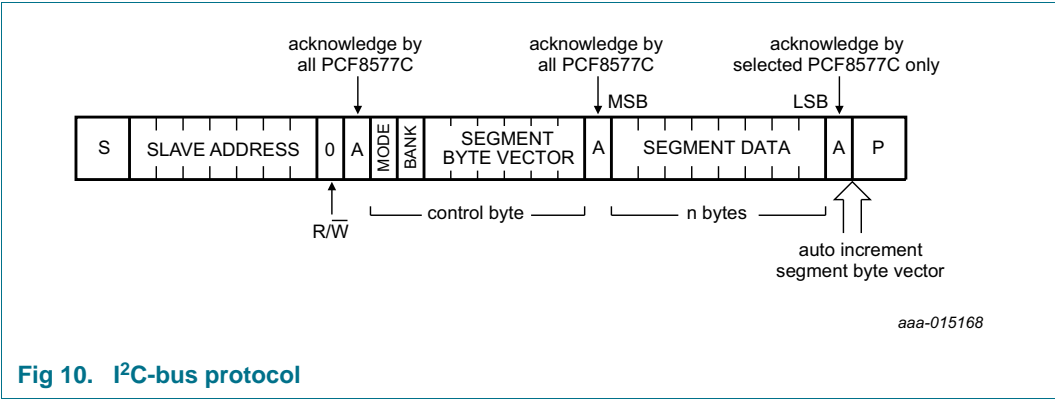
Before any data is transmitted on the I<sup>2</sup>C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

8.3 I<sup>2</sup>C-bus protocol

The PCF8577C I<sup>2</sup>C-bus protocol is shown in [Figure 10](#).


The PCF8577C is a slave receiver and has a fixed slave address (see [Table 7](#)). All PCF8577Cs with the same slave address acknowledge the slave address in parallel.

The second byte is always the control byte and is loaded into the control register of each PCF8577C connected to the I<sup>2</sup>C-bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a STOP (P) condition is given after the control byte acknowledge, the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data, only the selected PCF8577C gives an acknowledge. Loading is terminated by generating a STOP (P) condition.



9. Safety notes


CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.


Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage ( $V_{LCD}$ ) is on while the IC supply voltage ( $V_{DD}$ ) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts,  $V_{LCD}$  and  $V_{DD}$  must be applied or removed together.

CAUTION



Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

## 10. Limiting values

**Table 8. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol               | Parameter                          | Conditions   | Min                   | Max                   | Unit |
|----------------------|------------------------------------|--|-----------------------|-----------------------|------|
| V <sub>DD</sub>      | supply voltage                     |  | −0.5                  | +8.0                  | V    |
| V <sub>LCD</sub>     | LCD supply voltage                 | [1]  | V <sub>DD</sub> − 8.0 | V <sub>DD</sub>       | V    |
| V <sub>I</sub>       | input voltage                      |  | −0.5                  | V <sub>DD</sub> + 0.5 | V    |
| V <sub>O</sub>       | output voltage                     | on each of the pins<br>S1 to S32 and BP1 and BP2 [1] | −0.5                  | +8.0                  | V    |
| I <sub>I</sub>       | input current                      |  | −20                   | +20                   | mA   |
| I <sub>O</sub>       | output current                     |  | −25                   | +25                   | mA   |
| I <sub>DD</sub>      | supply current                     |  | −50                   | +50                   | mA   |
| I <sub>SS</sub>      | ground supply current              |  | −50                   | +50                   | mA   |
| I <sub>DD(LCD)</sub> | LCD supply current                 |  | −50                   | +50                   | mA   |
| P <sub>tot</sub>     | total power dissipation            |  | -                     | 500                   | mW   |
| P <sub>O</sub>       | output power                       |  | -                     | 100                   | mW   |
| V <sub>ESD</sub>     | electrostatic discharge<br>voltage | HBM [2]  | -                     | ±2000                 | V    |
|                      |                                    | MM [3]   | -                     | ±200                  | V    |
| I <sub>Iu</sub>      | latch-up current                   | [4]  | -                     | 100                   | mA   |
| T <sub>stg</sub>     | storage temperature                | [5]  | −65                   | +150                  | °C   |
| T <sub>amb</sub>     | ambient temperature                | operating device                                     | −40                   | +85                   | °C   |

[1] Values with respect to V<sub>DD</sub>.

[2] Pass level; Human Body Model (HBM), according to [Ref. 6 "JESD22-A114"](#).

[3] Pass level; Machine Model (MM), according to [Ref. 7 "JESD22-A115"](#).

[4] Pass level; latch-up testing according to [Ref. 8 "JESD78"](#) at maximum ambient temperature (T<sub>amb(max)</sub>).

[5] According to the store and transport requirements (see [Ref. 12 "UM10569"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

## 11. Static characteristics

**Table 9. Static characteristics**

$V_{DD} = 2.5\text{ V to }6\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }85\text{ °C}$ ; unless otherwise specified.

| Symbol          | Parameter                | Conditions  | Min             | Typ  | Max         | Unit              |
|-----------------|--------------------------|---|-----------------|------|-------------|-------------------|
| <b>Supplies</b> |                          |   |                 |      |             |                   |
| $V_{DD}$        | supply voltage           |   | 2.5             | -    | 6           | V                 |
| $I_{DD}$        | supply current           | no load;<br>$R_{OSC} = 1\text{ M}\Omega$ ;<br>$C_{OSC} = 680\text{ pF}$   | [1]             |      |             |                   |
|                 |                          | $f_{SCL} = 100\text{ kHz}$  | [1]             | -    | 50          | 125 $\mu\text{A}$ |
|                 |                          | $f_{SCL} = 0\text{ Hz}$   | [1]             | -    | 25          | 75 $\mu\text{A}$  |
|                 |                          | $V_{DD} = 5\text{ V}$ ;<br>$T_{amb} = 25\text{ °C}$   | [1]             | -    | 25          | 40 $\mu\text{A}$  |
|                 |                          | no load;<br>$f_{SCL} = 0\text{ Hz}$ ;<br>$A0/OSC = V_{DD}$ ;<br>$V_{DD} = 5\text{ V}$ ;<br>$T_{amb} = 25\text{ °C}$ | [1]             | -    | 10          | 20 $\mu\text{A}$  |
| $V_{POR}$       | power-on reset voltage   |   | [2]             | -    | 1.1         | 2.0 V             |
| <b>Logic</b>    |                          |   |                 |      |             |                   |
| $V_{IL}$        | LOW-level input voltage  | on pin A0   | 0               | -    | 0.05        | V                 |
|                 |                          | on pins A1, SCL, SDA  | 0               | -    | $0.3V_{DD}$ | V                 |
|                 |                          | on pin A2   | 0               | -    | 0.1         | V                 |
| $V_{IH}$        | HIGH-level input voltage | on pin A0   | $V_{DD} - 0.05$ | -    | $V_{DD}$    | V                 |
|                 |                          | on pin A1   | $0.7V_{DD}$     | -    | $V_{DD}$    | V                 |
|                 |                          | on pin A2   | $V_{DD} - 0.1$  | -    | $V_{DD}$    | V                 |
|                 |                          | on pins SCL, SDA  | $0.7V_{DD}$     | -    | 6           | V                 |
| $C_i$           | input capacitance        |   | [3]             | -    | 7           | pF                |
| $I_{OL}$        | LOW-level output current | output sink current;<br>on pin SDA;<br>$V_{OL} = 0.4\text{ V}$ ;<br>$V_{DD} = 5\text{ V}$ ;                         | 3               | -    | -           | mA                |
| $I_L$           | leakage current          | $V_I = V_{DD}\text{ or }V_{SS}$   |                 |      |             |                   |
|                 |                          | on pins A1, SCL, SDA  | -1              | -    | +1          | $\mu\text{A}$     |
|                 |                          | on pins A2/BP2, BP1   | -5              | -    | +5          | $\mu\text{A}$     |
|                 |                          | $V_I = V_{DD}$ ;<br>on pin A0/OSC   | -1              | -    | -           | $\mu\text{A}$     |
| $I_{pd}$        | pull-down current        | $V_I = V_{DD}$ ;<br>on pin A2/BP2   | -5              | -1.5 | -           | $\mu\text{A}$     |
| $I_{startup}$   | startup current          | oscillator;<br>$V_I = V_{SS}$   | -               | 1.2  | 5           | $\mu\text{A}$     |

**Table 9.** Static characteristics ...continued

$V_{DD} = 2.5\text{ V to }6\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }85\text{ °C}$ ; unless otherwise specified.

| Symbol             | Parameter                  | Conditions   | Min     | Typ      | Max  | Unit       |
|--------------------|----------------------------|--|---------|----------|------|------------|
| <b>LCD outputs</b> |                            |  |         |          |      |            |
| $V_{DC}$           | DC component of LCD driver |  | -       | $\pm 20$ | -    | mV         |
| $I_{OL}$           | LOW-level output current   | on pins S1 to S32;<br>$V_{DD} = 5\text{ V}$ ;<br>$V_{OL} = 0.8\text{ V}$             | [4] 0.3 | -        | -    | mA         |
| $I_{OH}$           | HIGH-level output current  | on pins S1 to S32;<br>$V_{DD} = 5\text{ V}$ ;<br>$V_{OH} = V_{DD} - 0.8\text{ V}$    | [4] -   | -        | -0.3 | mA         |
| $R_o$              | output resistance          | on pins BP1, BP2;<br>$V_o = V_{SS}$ or $V_{DD}$ or<br>$\frac{1}{2}(V_{SS} + V_{DD})$ | [5] -   | 0.4      | 5    | k $\Omega$ |

[1] Inputs at  $V_{SS}$  or  $V_{DD}$ .

[2] Resets all logic when  $V_{DD} < V_{POR}$ .

[3] Periodically sampled, not 100 % tested.

[4] Outputs measured one at a time.

[5] Outputs measured one at a time;  $V_{DD} = 5\text{ V}$ ;  $I_{load} = 100\text{ }\mu\text{A}$ .

## 12. Dynamic characteristics

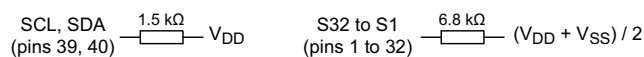
**Table 10. Dynamic characteristics**

$V_{DD} = 2.5\text{ V to }6\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }85\text{ °C}$ ; unless otherwise specified. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .

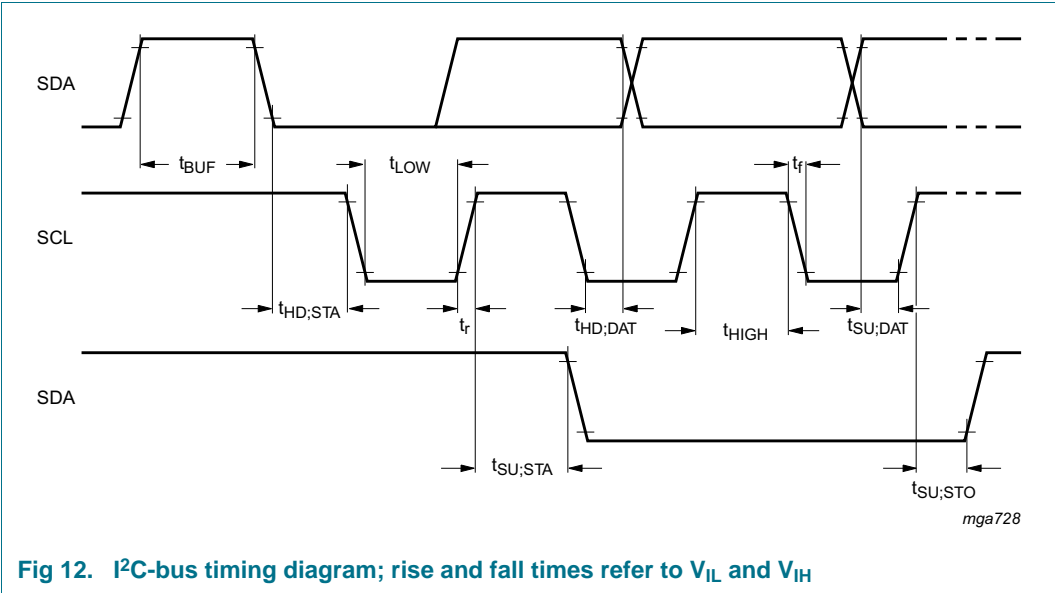
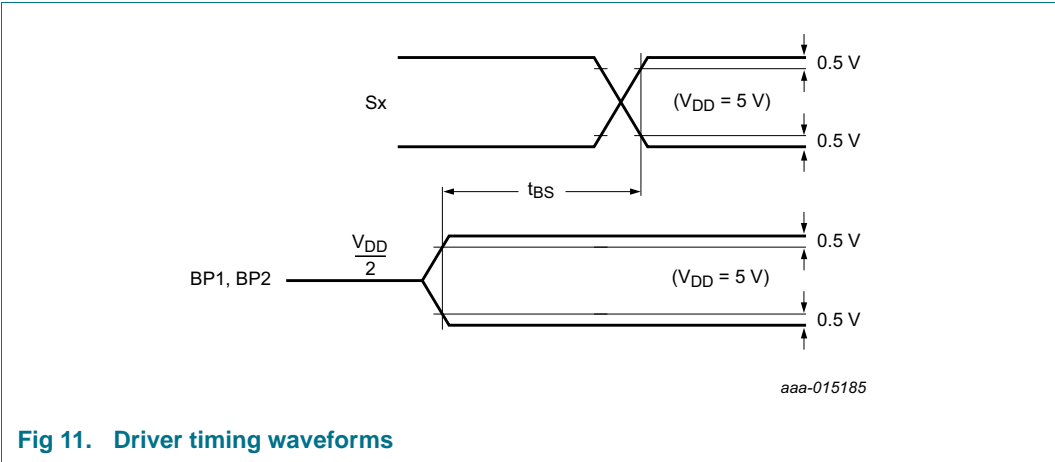
| Symbol                    | Parameter  | Conditions  | Min | Typ <sup>[1]</sup> | Max | Unit          |
|---------------------------|--|---|-----|--------------------|-----|---------------|
| $f_{LCD}$                 | display frequency                                | $R_{OSC} = 1\text{ M}\Omega$ ;<br>$C_{OSC} = 680\text{ pF}$ | 65  | 90                 | 120 | Hz            |
| $t_{BS}$                  | driver delays with test loads                    | $V_{DD} = 5\text{ V}$ <sup>[2]</sup>                        | -   | 20                 | 100 | $\mu\text{s}$ |
| <b>I<sup>2</sup>C-bus</b> |  |   |     |                    |     |               |
| $f_{SCL}$                 | SCL clock frequency                              |   | -   | -                  | 100 | kHz           |
| $t_{SW}$                  | tolerable spike width on I <sup>2</sup> C-bus    | $T_{amb} = 25\text{ °C}$                                    | -   | -                  | 100 | ns            |
| $t_{BUF}$                 | bus free time between a STOP and START condition |   | 4.7 | -                  | -   | $\mu\text{s}$ |
| $t_{SU;STA}$              | set-up time for a repeated START condition       |   | 4.0 | -                  | -   | $\mu\text{s}$ |
| $t_{HD;STA}$              | hold time (repeated) START condition             |   | 4.0 | -                  | -   | $\mu\text{s}$ |
| $t_{LOW}$                 | LOW period of the SCL clock                      |   | 4.7 | -                  | -   | $\mu\text{s}$ |
| $t_{HIGH}$                | HIGH period of the SCL clock                     |   | 4.0 | -                  | -   | $\mu\text{s}$ |
| $t_r$                     | rise time of both SDA and SCL signals            |   | -   | -                  | 1.0 | $\mu\text{s}$ |
| $t_f$                     | fall time of both SDA and SCL signals            |   | -   | -                  | 0.3 | $\mu\text{s}$ |
| $t_{SU;DAT}$              | data set-up time                                 |   | 250 | -                  | -   | ns            |
| $t_{HD;DAT}$              | data hold time                                   |   | 0   | -                  | -   | ns            |
| $t_{SU;STO}$              | set-up time for STOP condition                   |   | 4.0 | -                  | -   | $\mu\text{s}$ |

[1] Typical conditions:  $V_{DD} = 5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ .

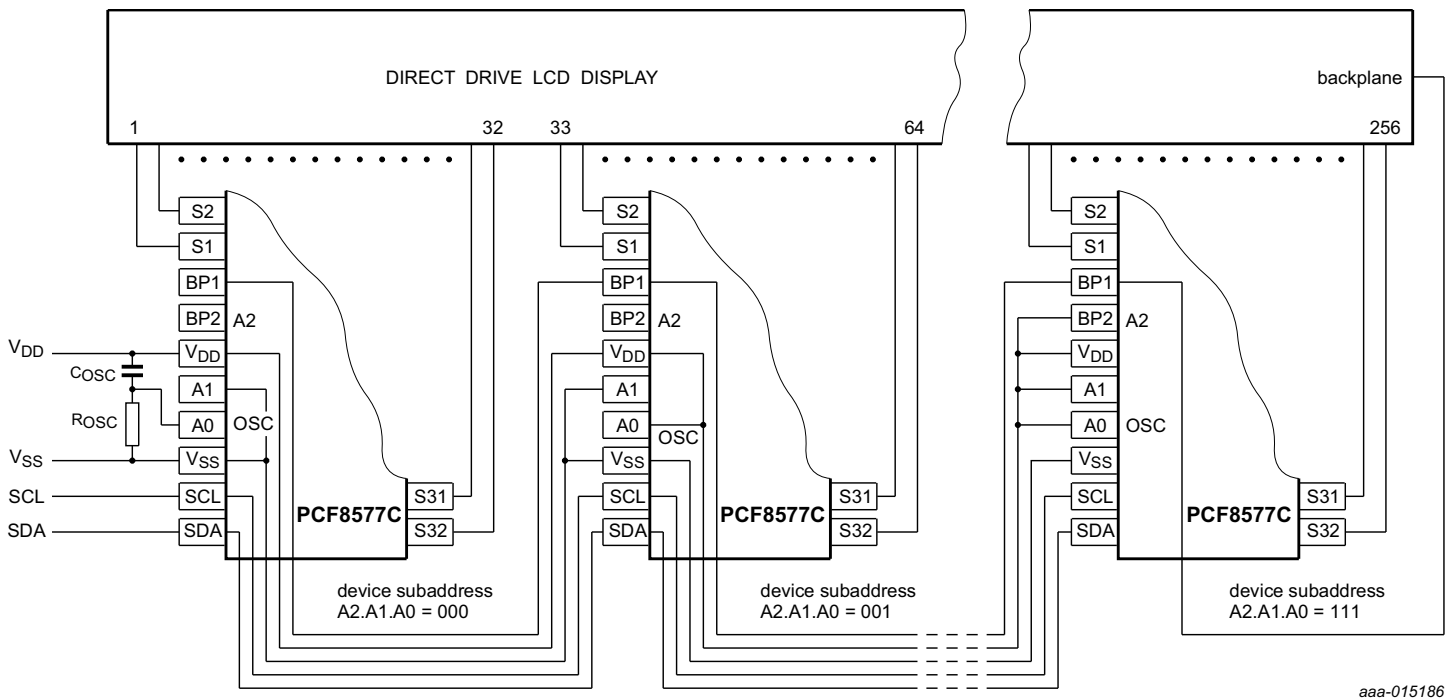
[2] Test loads:.



aaa-015184



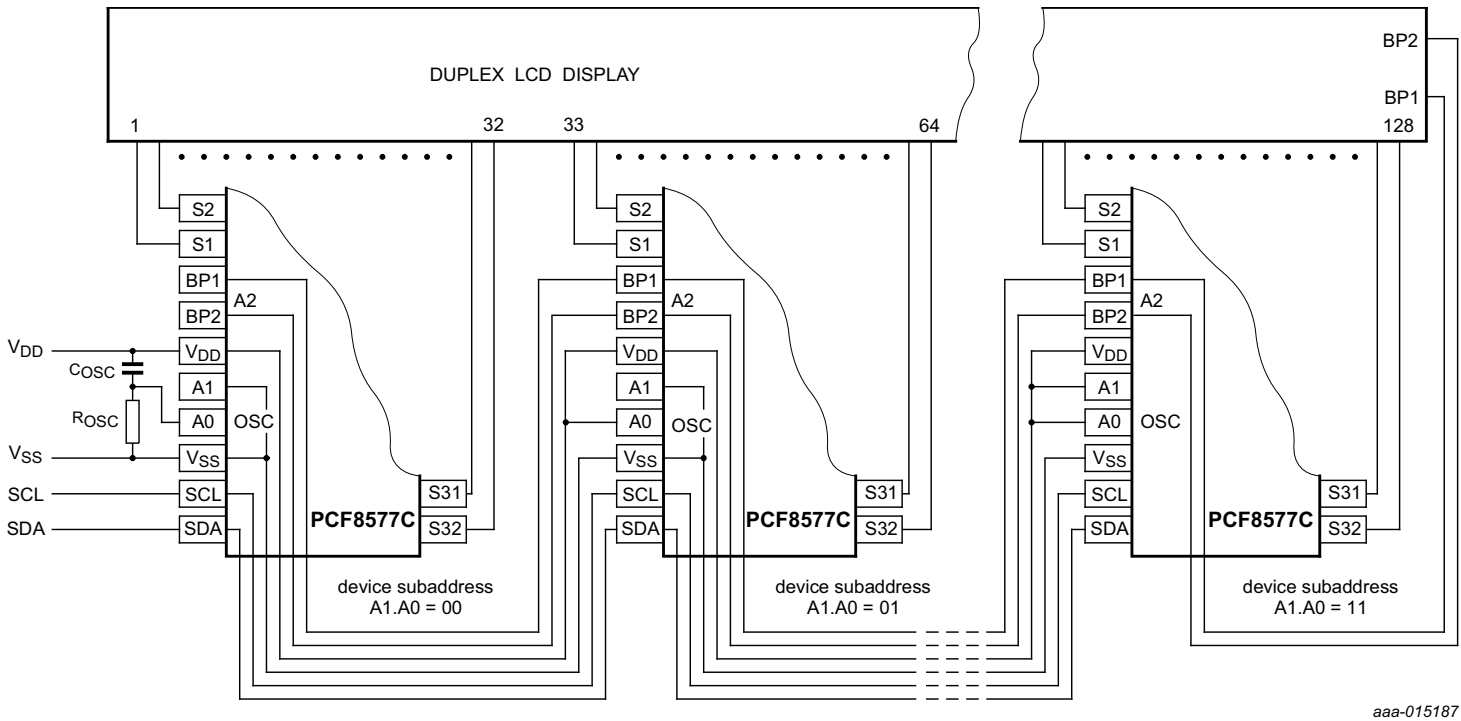




aaa-015186

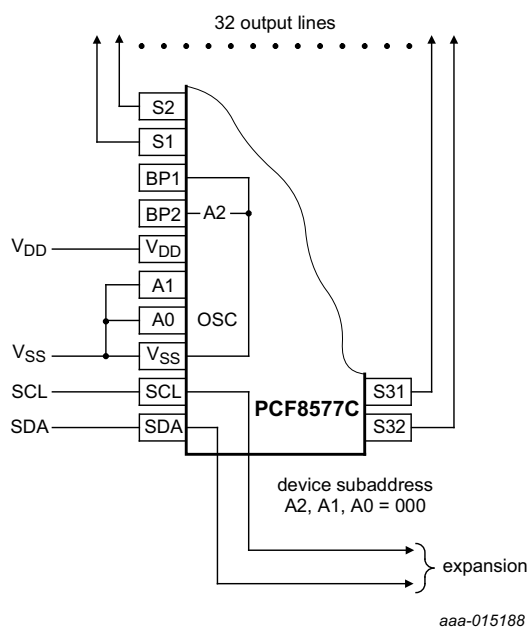
Fig 13. Direct display driver; expansion to 256 segments using eight PCF8577Cs

## 13. Application information



aaa-015187

Fig 14. Duplex display; expansion to 2 × 128 segments using four PCF8577Cs



MODE bit must always be set to logic 0 (direct drive).

Bank switching is permitted.

BP1 must always be connected to V<sub>SS</sub> and A0/OSC must be connected to either V<sub>DD</sub> or V<sub>SS</sub> (no LCD modulation).

**Fig 15. Use of PCF8577C as a 32-bit output expander in an I<sup>2</sup>C-bus application**

## 14. Package outline

VSO40: plastic very small outline package; 40 leads

SOT158-1

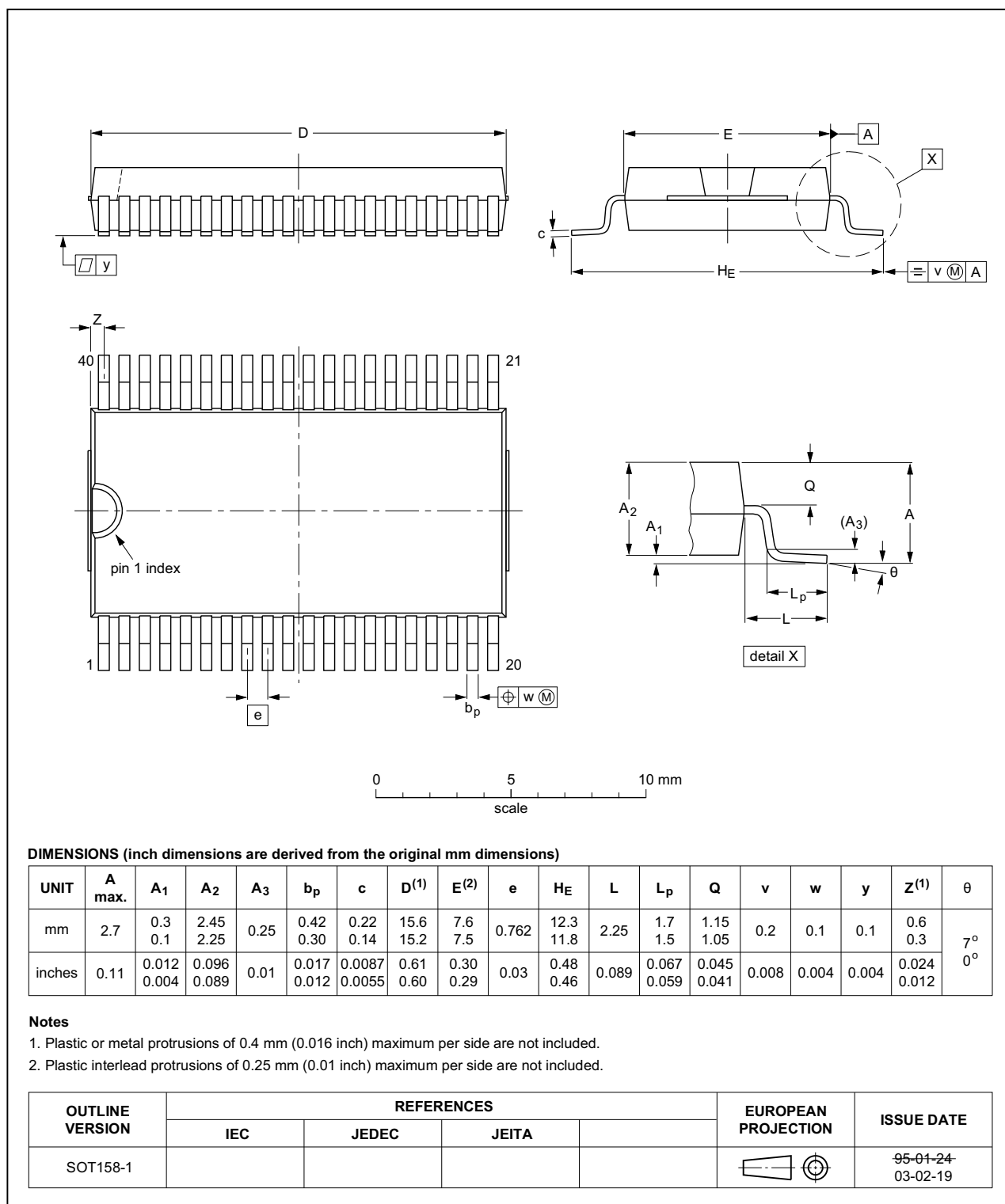


Fig 16. Package outline SOT158-1 (VSO40) of PCF8577CT

## 15. Packing information

### 15.1 Tape and reel information

For tape and reel packing information, see [Ref. 10 "SOT158-1\\_118" on page 27](#).

## 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 17](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 11](#) and [12](#)

**Table 11. SnPb eutectic process (from J-STD-020D)**

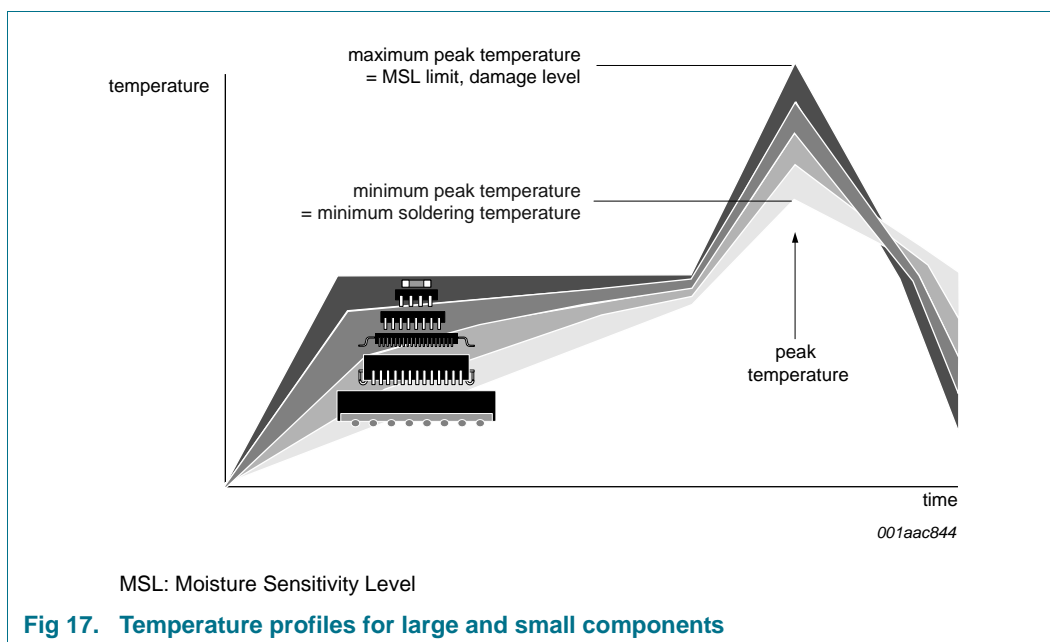
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 12. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 17](#).



For further information on temperature profiles, refer to Application Note *AN10365* "Surface mount reflow soldering description".

## 17. Footprint information

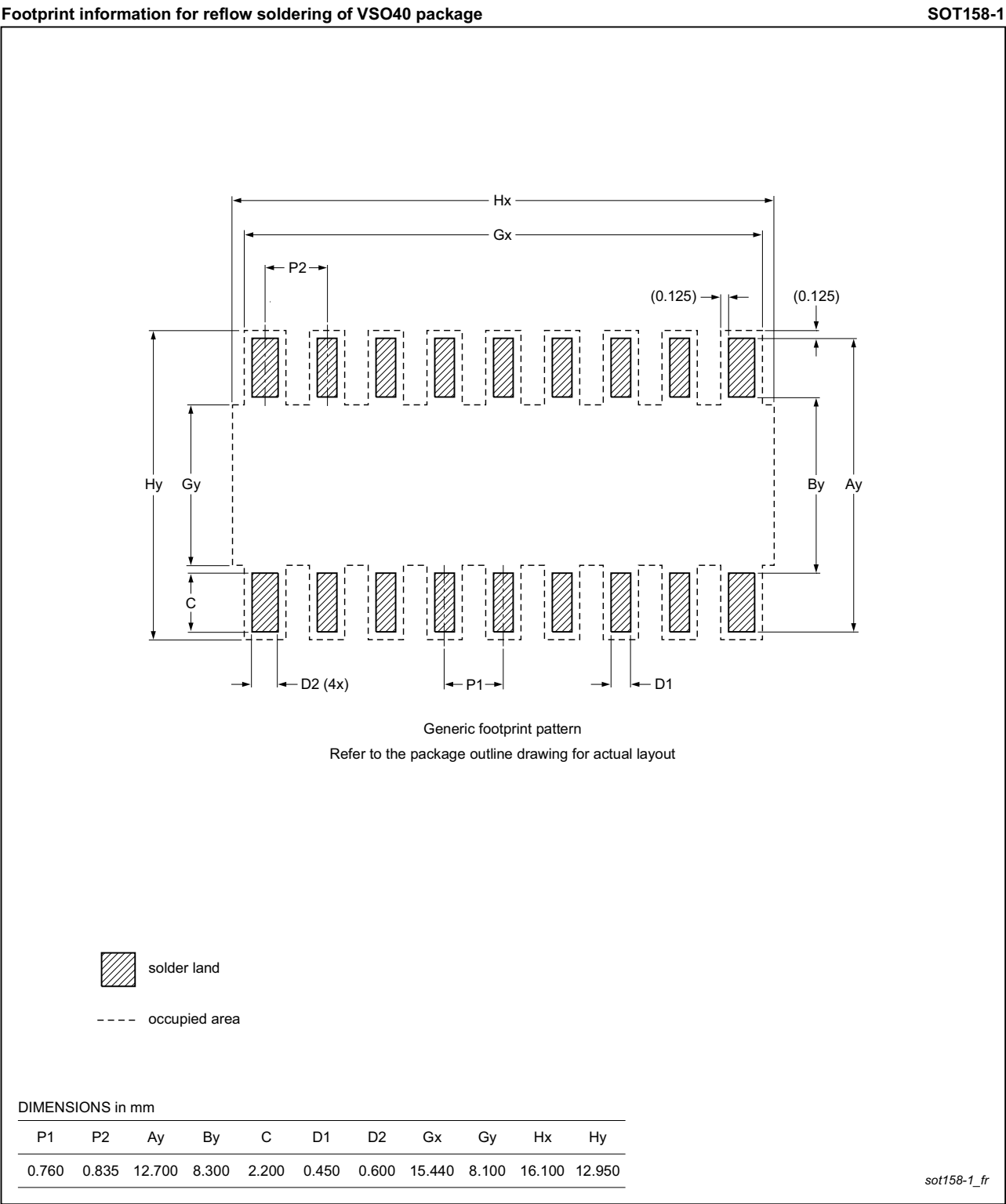


Fig 18. Footprint information for reflow soldering of SOT158-1 (VSO40) of PCF8577C



## 18. Appendix

### 18.1 LCD segment driver selection

Table 13. Selection of LCD segment drivers

| Type name  | Number of elements at MUX |     |     |     |     |     |     | V <sub>DD</sub> (V) | V <sub>LCD</sub> (V) | f <sub>fr</sub> (Hz)     | V <sub>LCD</sub> (V)<br>charge<br>pump | V <sub>LCD</sub> (V)<br>temperature<br>compensat. | T <sub>amb</sub> (°C) | Interface              | Package  | AEC-<br>Q100 |
|------------|---------------------------|-----|-----|-----|-----|-----|-----|---------------------|----------------------|--------------------------|--|---|-----------------------|------------------------|----------|--------------|
|            | 1:1                       | 1:2 | 1:3 | 1:4 | 1:6 | 1:8 | 1:9 |                     |                      |                          |  |   |                       |                        |          |              |
| PCA8553DTT | 40                        | 80  | 120 | 160 | -   | -   | -   | 1.8 to 5.5          | 1.8 to 5.5           | 32 to 256 <sup>[1]</sup> | N                                      | N   | -40 to 105            | I <sup>2</sup> C / SPI | TSSOP56  | Y            |
| PCA8546ATT | -                         | -   | -   | 176 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | N                                      | N   | -40 to 95             | I <sup>2</sup> C       | TSSOP56  | Y            |
| PCA8546BTT | -                         | -   | -   | 176 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | N                                      | N   | -40 to 95             | SPI                    | TSSOP56  | Y            |
| PCA8547AHT | 44                        | 88  | -   | 176 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 95             | I <sup>2</sup> C       | TQFP64   | Y            |
| PCA8547BHT | 44                        | 88  | -   | 176 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 95             | SPI                    | TQFP64   | Y            |
| PCF85134HL | 60                        | 120 | 180 | 240 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 6.5           | 82                       | N                                      | N   | -40 to 85             | I <sup>2</sup> C       | LQFP80   | N            |
| PCA85134H  | 60                        | 120 | 180 | 240 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 8             | 82                       | N                                      | N   | -40 to 95             | I <sup>2</sup> C       | LQFP80   | Y            |
| PCA8543AHL | 60                        | 120 | -   | 240 | -   | -   | -   | 2.5 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 105            | I <sup>2</sup> C       | LQFP80   | Y            |
| PCF8545ATT | -                         | -   | -   | 176 | 252 | 320 | -   | 1.8 to 5.5          | 2.5 to 5.5           | 60 to 300 <sup>[1]</sup> | N                                      | N   | -40 to 85             | I <sup>2</sup> C       | TSSOP56  | N            |
| PCF8545BTT | -                         | -   | -   | 176 | 252 | 320 | -   | 1.8 to 5.5          | 2.5 to 5.5           | 60 to 300 <sup>[1]</sup> | N                                      | N   | -40 to 85             | SPI                    | TSSOP56  | N            |
| PCF8536AT  | -                         | -   | -   | 176 | 252 | 320 | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | N                                      | N   | -40 to 85             | I <sup>2</sup> C       | TSSOP56  | N            |
| PCF8536BT  | -                         | -   | -   | 176 | 252 | 320 | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | N                                      | N   | -40 to 85             | SPI                    | TSSOP56  | N            |
| PCA8536AT  | -                         | -   | -   | 176 | 252 | 320 | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | N                                      | N   | -40 to 95             | I <sup>2</sup> C       | TSSOP56  | Y            |
| PCA8536BT  | -                         | -   | -   | 176 | 252 | 320 | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | N                                      | N   | -40 to 95             | SPI                    | TSSOP56  | Y            |
| PCF8537AH  | 44                        | 88  | -   | 176 | 276 | 352 | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 85             | I <sup>2</sup> C       | TQFP64   | N            |
| PCF8537BH  | 44                        | 88  | -   | 176 | 276 | 352 | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 85             | SPI                    | TQFP64   | N            |
| PCA8537AH  | 44                        | 88  | -   | 176 | 276 | 352 | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 95             | I <sup>2</sup> C       | TQFP64   | Y            |
| PCA8537BH  | 44                        | 88  | -   | 176 | 276 | 352 | -   | 1.8 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 95             | SPI                    | TQFP64   | Y            |
| PCA9620H   | 60                        | 120 | -   | 240 | 320 | 480 | -   | 2.5 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 105            | I <sup>2</sup> C       | LQFP80   | Y            |
| PCA9620U   | 60                        | 120 | -   | 240 | 320 | 480 | -   | 2.5 to 5.5          | 2.5 to 9             | 60 to 300 <sup>[1]</sup> | Y                                      | Y   | -40 to 105            | I <sup>2</sup> C       | Bare die | Y            |
| PCF8576DU  | 40                        | 80  | 120 | 160 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 6.5           | 77                       | N                                      | N   | -40 to 85             | I <sup>2</sup> C       | Bare die | N            |
| PCF8576EUG | 40                        | 80  | 120 | 160 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 6.5           | 77                       | N                                      | N   | -40 to 85             | I <sup>2</sup> C       | Bare die | N            |
| PCA8576FUG | 40                        | 80  | 120 | 160 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 8             | 200                      | N                                      | N   | -40 to 105            | I <sup>2</sup> C       | Bare die | Y            |
| PCF85133U  | 80                        | 160 | 240 | 320 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 6.5           | 82, 110 <sup>[2]</sup>   | N                                      | N   | -40 to 85             | I <sup>2</sup> C       | Bare die | N            |
| PCA85133U  | 80                        | 160 | 240 | 320 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 8             | 82, 110 <sup>[2]</sup>   | N                                      | N   | -40 to 95             | I <sup>2</sup> C       | Bare die | Y            |

Table 13. Selection of LCD segment drivers ...continued

| Type name  | Number of elements at MUX |     |     |     |     |     |     | V <sub>DD</sub> (V) | V <sub>LCD</sub> (V) | f <sub>fr</sub> (Hz)      | V <sub>LCD</sub> (V)<br>charge pump | V <sub>LCD</sub> (V)<br>temperature compensat. | T <sub>amb</sub> (°C) | Interface              | Package  | AEC-Q100 |
|------------|---------------------------|-----|-----|-----|-----|-----|-----|---------------------|----------------------|---------------------------|-------------------------------------|--|-----------------------|------------------------|----------|----------|
|            | 1:1                       | 1:2 | 1:3 | 1:4 | 1:6 | 1:8 | 1:9 |                     |                      |                           |                                     |  |                       |                        |          |          |
| PCA85233UG | 80                        | 160 | 240 | 320 | -   | -   | -   | 1.8 to 5.5          | 2.5 to 8             | 150, 220 <sup>[2]</sup>   | N                                   | N  | -40 to 105            | I <sup>2</sup> C       | Bare die | Y        |
| PCF85132U  | 160                       | 320 | 480 | 640 | -   | -   | -   | 1.8 to 5.5          | 1.8 to 8             | 60 to 90 <sup>[1]</sup>   | N                                   | N  | -40 to 85             | I <sup>2</sup> C       | Bare die | N        |
| PCA8530DUG | 102                       | 204 | -   | 408 | -   | -   | -   | 2.5 to 5.5          | 4 to 12              | 45 to 300 <sup>[1]</sup>  | Y                                   | Y  | -40 to 105            | I <sup>2</sup> C / SPI | Bare die | Y        |
| PCA85132U  | 160                       | 320 | 480 | 640 | -   | -   | -   | 1.8 to 5.5          | 1.8 to 8             | 60 to 90 <sup>[1]</sup>   | N                                   | N  | -40 to 95             | I <sup>2</sup> C       | Bare die | Y        |
| PCA85232U  | 160                       | 320 | 480 | 640 | -   | -   | -   | 1.8 to 5.5          | 1.8 to 8             | 117 to 176 <sup>[1]</sup> | N                                   | N  | -40 to 95             | I <sup>2</sup> C       | Bare die | Y        |
| PCF8538UG  | 102                       | 204 | -   | 408 | 612 | 816 | 918 | 2.5 to 5.5          | 4 to 12              | 45 to 300 <sup>[1]</sup>  | Y                                   | Y  | -40 to 85             | I <sup>2</sup> C / SPI | Bare die | N        |
| PCA8538UG  | 102                       | 204 | -   | 408 | 612 | 816 | 918 | 2.5 to 5.5          | 4 to 12              | 45 to 300 <sup>[1]</sup>  | Y                                   | Y  | -40 to 105            | I <sup>2</sup> C / SPI | Bare die | Y        |

[1] Software programmable.

[2] Hardware selectable.

## 19. References

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- [1] **AN10365** — Surface mount reflow soldering description
- [2] **AN10853** — ESD and EMC sensitivity of IC
- [3] **AN11267** — EMC and system level ESD design guidelines for LCD drivers
- [4] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [5] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [6] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [7] **JESD22-A115** — Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)
- [8] **JESD78** — IC Latch-Up Test
- [9] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [10] **SOT158-1\_118** — VSO40; Reel pack; SMD, 13", packing information
- [11] **UM10204** — I<sup>2</sup>C-bus specification and user manual
- [12] **UM10569** — Store and transport requirements

## 20. Revision history

Table 14. Revision history

| Document ID    | Release date   | Data sheet status  | Change notice | Supersedes   |
|----------------|--|--------------------|---------------|--------------|
| PCF8577C v.5   | 20141010   | Product data sheet | -             | PCF8577C v.4 |
| Modifications: | <ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Removed obsolete product types.</li></ul> |                    |               |              |
| PCF8577C v.4   | 19980730   | Product data sheet | -             | PCF8577C v.3 |
| PCF8577C v.3   | 19970328   | Product data sheet | -             | PCF8577C v.2 |
| PCF8577C v.2   | 19950608   | Product data sheet | -             | PCF8577C v.1 |

## 21. Legal information

### 21.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 23. Tables

|           |   |    |
|-----------|---|----|
| Table 1.  | Ordering information  | 1  |
| Table 2.  | Ordering options  | 2  |
| Table 3.  | Marking codes   | 2  |
| Table 4.  | Pin description   | 4  |
| Table 5.  | Segment byte-segment driver mapping in<br>direct drive mode | 8  |
| Table 6.  | Segment byte-segment driver mapping in<br>duplex mode       | 8  |
| Table 7.  | I <sup>2</sup> C slave address byte                         | 10 |
| Table 8.  | Limiting values   | 12 |
| Table 9.  | Static characteristics                                      | 13 |
| Table 10. | Dynamic characteristics                                     | 15 |
| Table 11. | SnPb eutectic process (from J-STD-020D)                     | 22 |
| Table 12. | Lead-free process (from J-STD-020D)                         | 22 |
| Table 13. | Selection of LCD segment drivers                            | 25 |
| Table 14. | Revision history  | 28 |

## 24. Figures

|         |   |    |
|---------|---|----|
| Fig 1.  | Block diagram of PCF8577C   | 2  |
| Fig 2.  | Pin configuration for PCF8577CT   | 3  |
| Fig 3.  | PCF8577C register organization  | 5  |
| Fig 4.  | Direct drive mode display output waveforms  | 6  |
| Fig 5.  | Duplex mode display output waveforms  | 7  |
| Fig 6.  | Bit transfer  | 9  |
| Fig 7.  | Definition of START and STOP conditions   | 9  |
| Fig 8.  | System configuration  | 10 |
| Fig 9.  | Acknowledgement of the I <sup>2</sup> C-bus   | 10 |
| Fig 10. | I <sup>2</sup> C-bus protocol   | 11 |
| Fig 11. | Driver timing waveforms   | 16 |
| Fig 12. | I <sup>2</sup> C-bus timing diagram; rise and fall times refer to $V_{IL}$ and $V_{IH}$ | 16 |
| Fig 13. | Direct display driver; expansion to 256 segments using eight PCF8577Cs                  | 17 |
| Fig 14. | Duplex display; expansion to $2 \times 128$ segments using four PCF8577Cs               | 18 |
| Fig 15. | Use of PCF8577C as a 32-bit output expander in an I <sup>2</sup> C-bus application      | 19 |
| Fig 16. | Package outline SOT158-1 (VSO40) of PCF8577CT   | 20 |
| Fig 17. | Temperature profiles for large and small components                                     | 23 |
| Fig 18. | Footprint information for reflow soldering of SOT158-1 (VSO40) of PCF8577CT             | 24 |



## 25. Contents

|           |   |           |           |                                      |           |
|-----------|---|-----------|-----------|--------------------------------------|-----------|
| <b>1</b>  | <b>General description</b> . . . . .                  | <b>1</b>  | <b>21</b> | <b>Legal information</b> . . . . .   | <b>29</b> |
| <b>2</b>  | <b>Features and benefits</b> . . . . .                | <b>1</b>  | 21.1      | Data sheet status . . . . .          | 29        |
| <b>3</b>  | <b>Ordering information</b> . . . . .                 | <b>1</b>  | 21.2      | Definitions . . . . .                | 29        |
| 3.1       | Ordering options . . . . .                            | 2         | 21.3      | Disclaimers . . . . .                | 29        |
| <b>4</b>  | <b>Marking</b> . . . . .                              | <b>2</b>  | 21.4      | Trademarks . . . . .                 | 30        |
| <b>5</b>  | <b>Block diagram</b> . . . . .                        | <b>2</b>  | <b>22</b> | <b>Contact information</b> . . . . . | <b>30</b> |
| <b>6</b>  | <b>Pinning information</b> . . . . .                  | <b>3</b>  | <b>23</b> | <b>Tables</b> . . . . .              | <b>31</b> |
| 6.1       | Pinning . . . . .                                     | 3         | <b>24</b> | <b>Figures</b> . . . . .             | <b>32</b> |
| 6.2       | Pin description . . . . .                             | 4         | <b>25</b> | <b>Contents</b> . . . . .            | <b>33</b> |
| <b>7</b>  | <b>Functional description</b> . . . . .               | <b>4</b>  |           |                                      |           |
| 7.1       | Hardware subaddress lines A0, A1, and A2 . . .        | 4         |           |                                      |           |
| 7.2       | Oscillator A0/OSC . . . . .                           | 4         |           |                                      |           |
| 7.3       | User-accessible registers . . . . .                   | 5         |           |                                      |           |
| 7.4       | Auto-incremented loading . . . . .                    | 6         |           |                                      |           |
| 7.5       | Direct drive mode . . . . .                           | 6         |           |                                      |           |
| 7.6       | Duplex mode . . . . .                                 | 6         |           |                                      |           |
| 7.7       | Display memory mapping . . . . .                      | 7         |           |                                      |           |
| 7.8       | Power-on reset . . . . .                              | 8         |           |                                      |           |
| <b>8</b>  | <b>I<sup>2</sup>C-bus interface</b> . . . . .         | <b>9</b>  |           |                                      |           |
| 8.1       | Characteristics of the I <sup>2</sup> C-Bus . . . . . | 9         |           |                                      |           |
| 8.1.1     | Bit transfer . . . . .                                | 9         |           |                                      |           |
| 8.1.2     | START and STOP conditions . . . . .                   | 9         |           |                                      |           |
| 8.1.3     | System configuration . . . . .                        | 9         |           |                                      |           |
| 8.1.4     | Acknowledge . . . . .                                 | 10        |           |                                      |           |
| 8.2       | Slave address . . . . .                               | 10        |           |                                      |           |
| 8.3       | I <sup>2</sup> C-bus protocol . . . . .               | 11        |           |                                      |           |
| <b>9</b>  | <b>Safety notes</b> . . . . .                         | <b>11</b> |           |                                      |           |
| <b>10</b> | <b>Limiting values</b> . . . . .                      | <b>12</b> |           |                                      |           |
| <b>11</b> | <b>Static characteristics</b> . . . . .               | <b>13</b> |           |                                      |           |
| <b>12</b> | <b>Dynamic characteristics</b> . . . . .              | <b>15</b> |           |                                      |           |
| <b>13</b> | <b>Application information</b> . . . . .              | <b>17</b> |           |                                      |           |
| <b>14</b> | <b>Package outline</b> . . . . .                      | <b>20</b> |           |                                      |           |
| <b>15</b> | <b>Packing information</b> . . . . .                  | <b>21</b> |           |                                      |           |
| 15.1      | Tape and reel information . . . . .                   | 21        |           |                                      |           |
| <b>16</b> | <b>Soldering of SMD packages</b> . . . . .            | <b>21</b> |           |                                      |           |
| 16.1      | Introduction to soldering . . . . .                   | 21        |           |                                      |           |
| 16.2      | Wave and reflow soldering . . . . .                   | 21        |           |                                      |           |
| 16.3      | Wave soldering . . . . .                              | 21        |           |                                      |           |
| 16.4      | Reflow soldering . . . . .                            | 22        |           |                                      |           |
| <b>17</b> | <b>Footprint information</b> . . . . .                | <b>23</b> |           |                                      |           |
| <b>18</b> | <b>Appendix</b> . . . . .                             | <b>25</b> |           |                                      |           |
| 18.1      | LCD segment driver selection . . . . .                | 25        |           |                                      |           |
| <b>19</b> | <b>References</b> . . . . .                           | <b>27</b> |           |                                      |           |
| <b>20</b> | <b>Revision history</b> . . . . .                     | <b>28</b> |           |                                      |           |

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