ISD5008

SINGLE-CHIP,

VOICE RECORD / PLAYBACK DEVICE

4-, 5-, 6- AND 8-SECOND DURATION

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ISD5008

Single-Chip Voice Record/Playback Device
4-, 5-, 6-, and 8-Minute Durations

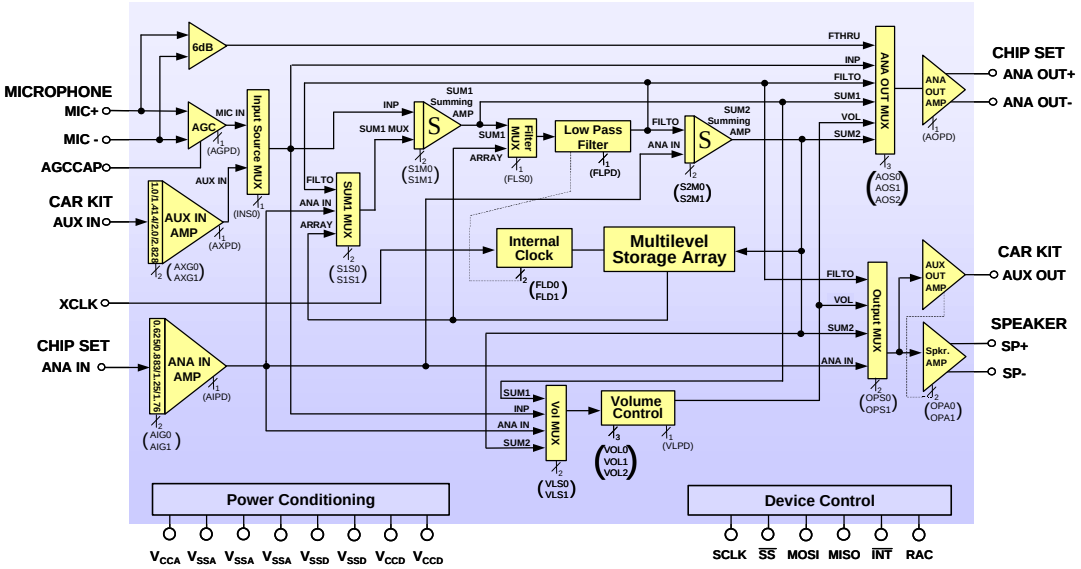
Preliminary Datasheet

ISD5008 PRODUCT SUMMARY

The ISD5008 ChipCorder product is a fully-integrated, single-chip solution which provides seamless integration of enhanced voice record and playback features for digital cellular phones (GSM, CDMA, TDMA, PDC, and PHS), automotive communications, GPS/navigation systems, and portable communication products. This low-power, 3-volt product enables customers to quickly and easily integrate 4 to 8 minutes of voice storage features such as one-way and two-way (full duplex) call record, voice memo record, and call screening/answering machine functionality.

Like other ChipCorder products, the ISD5008 integrates the sampling clock, anti-aliasing and smoothing filters, and the multi-level storage array on a single-chip. For enhanced voice features, the ISD5008 eliminates external circuitry by also integrating automatic gain control (AGC), a power amplifier/speaker driver, volume control, summing amplifiers, analog switches, and a car kit interface. Input level adjustable amplifiers are also included, providing a flexible interface for multiple applications.

Figure: ISD5008 Block Diagram



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Duration/sample rate selection is accomplished via software, allowing customers to optimize quality and duration for various features within the same end product.

The ISD5008 device is designed for use in a microprocessor- or microcontroller-based system. Address, control, and duration selection are accomplished through a Serial Peripheral Interface (SPI) or Microwire Serial Interface to minimize pin count.

Recordings are stored in on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through ISD's patented multilevel storage technology. Voice and audio signals are stored directly into solid-state memory in their natural, uncompressed form, providing superior quality voice and music reproduction.

ISD5008 FEATURES

FULLY-INTEGRATED SOLUTION

- Single-chip voice record/playback solution
- Integrated sampling clock, anti-aliasing and smoothing filters, and multi-level storage array
- Integrated analog features such as automatic gain control (AGC), audio gating switches, speaker driver (23mW with 8 ohm load), summing amplifiers, volume control, and an AUX IN/AUX OUT interface (e.g., for car kits).

LOW-POWER CONSUMPTION

- Single +3 volt supply
- Operating current:
  $I_{CC\ Play}$ = 15 mA (typical)
  $I_{CC\ Rec}$ = 25 mA (typical)
  $I_{CC\ Feedthru}$ = 12 mA (typical)
- Standby current:
  I_{SB} = 1 µA
- Power consumption controlled by SPI or Microwire control register
- Most stages can be individually powered down for minimum power consumption

ENHANCED VOICE FEATURES

- One or two-way (full duplex) conversation record (record signal summation)
- One- or two-way (full duplex) message playback (while on a call)
- Voice memo record and playback
- Private call screening
- In-terminal answering machine
- Personalized outgoing message (given caller ID information from host chip set)
- Private call announce while on call (given CIDCW information from host chip set)

EASY-TO-USE AND CONTROL

- No compression algorithm development required
- User-controllable sample rates of 8.0 kHz, 6.4 kHz, 5.3 kHz, or 4.0 kHz providing up to 8 minutes of voice storage.
- Microcontroller SPI or Microwire™ Serial Interface
- Fully addressable to handle multiple messages in 1200 rows

HIGH QUALITY SOLUTION

- High quality voice and music reproduction
- ISD's standard 100-year message retention (typical)
- 100,000 record cycles (typical)

OPTIONS

- Available in die form, PDIP, SOIC, TSOP, and chip scale packaging (CSP)
- Compact µBGA chip scale package available for portable applications
- Extended temperature (-20 to +70°C) and industrial temperature (-40 to +85°C) versions available

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1 DETAILED DESCRIPTION

1.1 SPEECH/SOUND QUALITY

The ISD5008 ChipCorder product can be configured via software to operate at 4.0, 5.3, 6.4, and 8.0 kHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration decreases the sampling frequency and bandwidth, which affects sound quality. Table 1 compares filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state solutions.

1.2 DURATION

To meet end system requirements, the ISD5008 device is a single-chip solution which provides from 4 to 8 minutes of voice record and playback, depending on the sample rates defined by customer software.

Table 1: Input Sample Rate to Duration

Input Sample Rate (kHz)	Duration (Minutes)	Typical Filter Pass Band (kHz)
8.0	4.0	3.4
6.4	5.0	2.7
5.3	6.0	2.3
4.0	8.0	1.7

1.3 FLASH STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, which provides zero-power message storage. The message is retained for up to 100 years (typically) without power. In addition, the device can be re-recorded over 100,000 times (typically).

1.4 MICROCONTROLLER INTERFACE

A four-wire (SCLK, MOSI, MISO, $\overline{SS}$) SPI interface is provided for ISD5008 control, addressing functions, and sample rate selection. The ISD5008 is configured to operate as a peripheral slave device with a microcontroller-based SPI bus interface. Read/Write access to all the internal registers occurs through this SPI interface. An interrupt signal ($\overline{INT}$) and internal read-only Status Register are provided for handshake purposes.

1.5 PROGRAMMING

The ISD5008 series is also ideal for playback-only applications, where single or multiple message Playback is controlled through the SPI port. Once the desired message configuration is created, duplicates can easily be generated via an ISD or third-party programmers. For more information on available application tools and programmers please see the ISD web site at www.isd.com.

2 PIN DESCRIPTIONS

2.1 DIGITAL I/O PINS

SCLK (Serial Clock)

The SCLK is the clock input to the ISD5008. Generated by the master microcontroller, the SCLK synchronizes data transfers in and out of the device through the MISO and MOSI lines. Data is latched into the ISD5008 on the rising edge of SCLK and shifted out on the falling edge.

$\overline{SS}$ (Slave Select)

This input, when LOW, will select the ISD5008 device.

MOSI (Master Out Slave In)

MOSI is the serial data input to the ISD5008 device. The master microcontroller places data to be clocked into the ISD5008 device on the MOSI line one-half cycle before the rising edge of SCLK. Data is clocked into the device LSB (Least Significant Bit) first.

MISO (Master In Slave Out)

MISO is the serial data output of the ISD5008 device. Data is clocked out on the falling edge of SCLK. This output goes into a high-impedance state when the device is not selected. Data is clocked out of the device LSB first.

$\overline{INT}$ (Interrupt)

$\overline{INT}$ is an open drain output pin. The ISD5008 interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. Each operation that ends in an EOM or OVF generates an interrupt, including the message cueing cycles. The interrupt is cleared the next time an SPI cycle is completed. The interrupt status can be read by a RINT instruction that will give one of the two flags out the MISO line.

OVF Flag. The overflow flag indicates that the end of the ISD5008's analog memory has been reached during a record or playback operation.

EOM Flag. The end of message flag is set only during playback, when an EOM is found. There are eight possible EOM markers per row.

RAC (Row Address Clock)

RAC is an open drain output pin that marks the end of a row. At the 8 kHz sample frequency, the duration of this period is 200 ms. There are 1,200 rows of memory in the ISD5008 devices. RAC stays HIGH for 175 ms and stays LOW for the remaining 25 ms before it reaches the end of the row.

The RAC pin remains HIGH for 109.38 µsec and stays LOW for 15.63 µsec under the Message Cueing mode. See Table 15 Timing Parameters for RAC timing information at other sample rates. When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACLO} period, to load sample and hold circuits internal to the device. The RAC pin can be used for message management techniques.

XCLK (External Clock Input)

The external clock input for the ISD5008 product has an internal pull-down device. Normally, the ISD5008 is operated at one of four internal rates selected for its internal oscillator by the Sample Rate Select bits. If greater precision is required, the device can be clocked through the XCLK pin as described in Table 2.

Because the antialiasing and smoothing filters track the Sample Rate Select bits, one must, for optimum performance, change the external clock *AND* the Sample Rate Configuration bits to one of the four values to properly set the filters to the correct cutoff frequency as described in Table 3. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. If the XCLK is not used, this input should be connected to V_{SSD}.

Table 2: External Clock Input Table

Duration (Minutes)	Sample Rate (kHz)	Required Clock (kHz)
4	8.0	1024
5	6.4	819.2
6	5.3	682.7
8	4.0	512

Table 3: Internal Clock Rate/Filter Edge

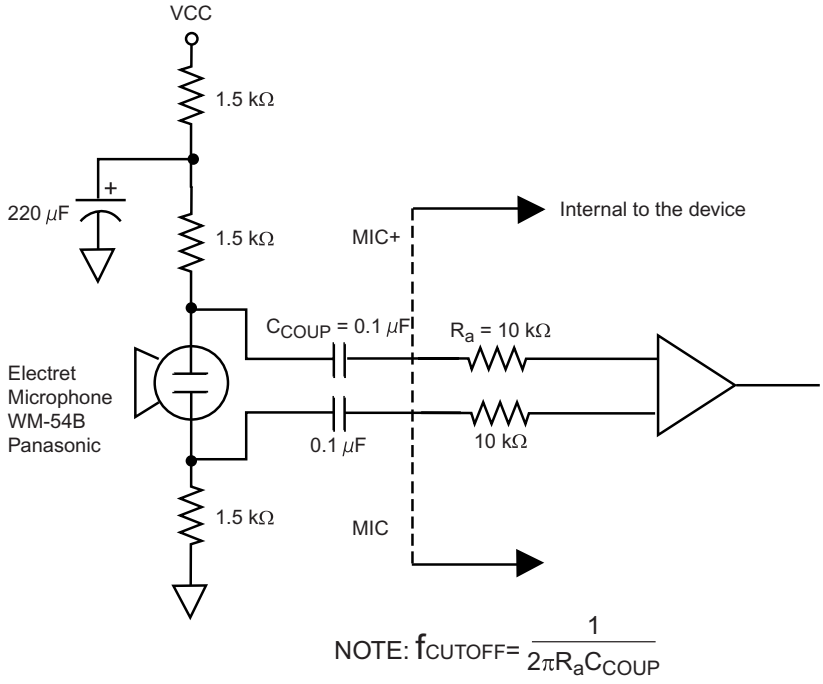
FLD1	FLD0	Sample Rate (kHz)	Filter Pass Band (kHz)
0	0	8	3.4
0	1	6.4	2.7
1	0	5.3	2.3
1	1	4	1.7

2.2 ANALOG I/O PINS

MIC+, MIC – (Microphone Input+/–)

The microphone input transfers the voice signal to the on-chip AGC preamplifier or directly to the ANA OUT MUX, depending on the selected path. The direct path to the ANA OUT MUX has a gain of 6 dB so a 208 mVp-p signal across the differential microphone inputs would give 416 mVp-p across the ANA OUT pins. The AGC circuit has a range of 45 dB in order to deliver a nominal 694 mVp-p into the storage array from a typical electret microphone output of 2 to 20 mVp-p. The input impedance is typically 10 kΩ.

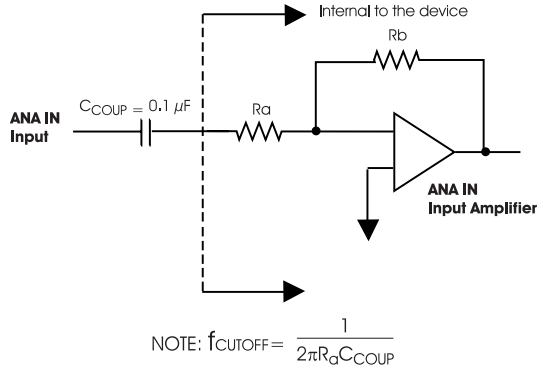
Figure 1: Microphone Input



ANA IN (Analog Input)

The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the SPI bus) to the speaker output, the array input or to various other paths. This pin is designed to accept a nominal 1.11 Vp-p when at its minimum gain (6 dB) setting. There is additional gain available in 3 dB steps controlled from the SPI bus, if required, up to 15 dB.

Figure 2: ANA IN Input Modes



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain[2] (dB)
00	63.9/102	0.625	–4.1
01	77.9/88.1	0.88	–1.1
10	92.3/73.8	1.25	1.9
11	106/60	1.77	4.9

Table 4: ANA IN Amplifier Gain Settings

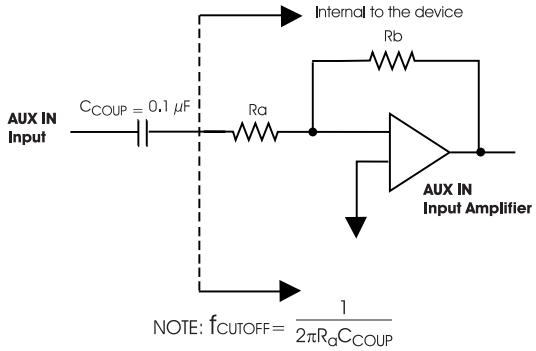
Setting[1]	0TLP Input V_{PP}[3]	CFG0		Gain[2]	Array In/Out V_{PP}	Speaker Out V_{PP}[4]
		AIG1	AIG0			
6 dB	1.11	0	0	.625	.694	2.22
9 dB	.785	0	1	.883	.694	2.22
12 dB	.555	1	0	1.250	.694	2.22
15 dB	.393	1	1	1.767	.694	2.22

1. *Gain from ANA IN to SP+/–*
2. *Gain from ANA IN to ARRAY IN*
3. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping.*
4. *Speaker Out gain set to 1.6 (High). (Differential)*

AUX IN (Auxiliary Input)

The AUX IN is an additional audio input to the ISD5008, such as from the microphone circuit in a mobile phone "car kit." This input has a nominal 700 mVp-p level at its minimum gain setting (0 dB). See Table 5. Additional gain is available in 3 dB steps (controlled by the SPI bus) up to 9 dB.

Figure 3: AUX IN Input Modes



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain (dB)
00	40.1/40.1	1.0	0
01	47.0/33.2	1.414	3
10	53.5/26.7	2.0	6
11	59.2/21	2.82	9

Table 5: AUXIN Amplifier Gain Settings

Setting(1)	0TLP Input V_{PP}(3)	CFG0		Gain(2)	Array In/Out V_{PP}	Ana Out V_{PP}(4)
		AXG1	AXG0			
0 dB	.694	0	0	1.00	.694	.694
3 dB	.491	0	1	1.41	.694	.694
6 dB	.347	1	0	2.00	.694	.694
9 dB	.245	1	1	2.82	.694	.694

1. *Gain from AUX IN to ANA OUT*
2. *Gain from AUX IN to ARRAY IN*
3. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping.*
4. *Differential*

ANAOUT+/– (Analog Outputs)

This differential output is designed to go to the microphone input of the telephone chip set. It is designed to drive a minimum of 5 kΩ between the "+" and "–" pins to a nominal voltage level of 700 mVp-p. Both pins have DC bias of approximately 1.2 VDC. The AC signal is superimposed upon this analog ground voltage. These pins can be used single-ended, getting only half the voltage. Do **NOT** ground the unused pin.

AUX OUT (Auxiliary Output)

The AUXOUT is an additional audio output pin, to be used, for example, to drive the speaker circuit in a "car kit." It drives a minimum load of 5 kΩ and up to a maximum of 1 Vp-p. The AC signal is superimposed on approximately 1.2 VDC bias and must be capacitively coupled to the load.

SP+, SP– (Speaker+/–)

This is the speaker differential output circuit. It is designed to drive an 8 Ω speaker connected across the speaker pins up to a maximum of 23.5 mW power. This stage has two selectable gains, 1.32 and 1.6, which can be chosen through the configuration registers. These pins are biased to approximately 1.2 VDC and, if used single-ended, must be capacitively coupled to their load. Do **NOT** ground the unused pin.

ACAP (AGC Capacitor)

This pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 µF capacitor connected to ground. It cannot be left floating. This is because the capacitor is also used in the playback mode for the AutoMute circuit. This circuit reduces the amount of noise present in the output during quiet pauses. Tying this pin to ground gives maximum gain; to V_{CCA} gives minimum gain for the AGC amplifier but will cancel the AutoMute function.

2.3 POWER AND GROUND PINS

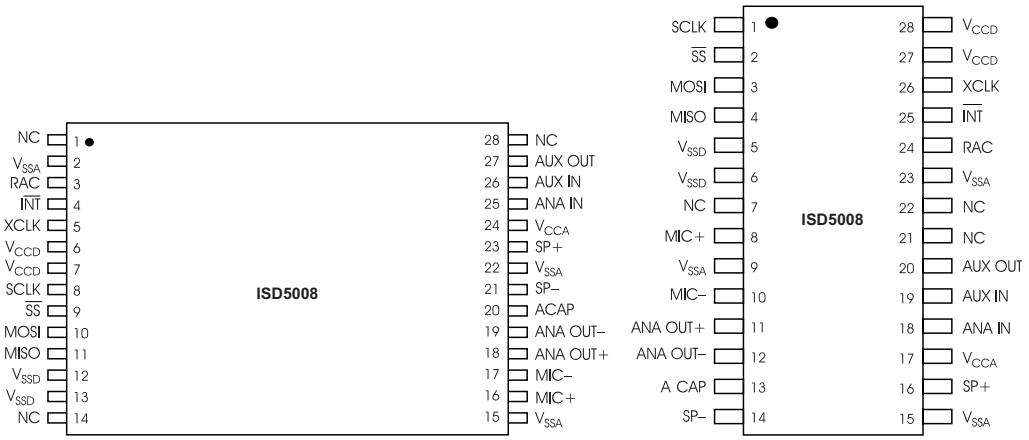
V_{CCA}, V_{CCD} (Voltage Inputs)

To minimize noise, the analog and digital circuits in the ISD5008 device uses separate power busses. These +3 V busses lead to separate pins. Tie the V_{CCD} pins together as close as possible and decouple both supplies as near to the package as possible.

V_{SSA}, V_{SSD} (Ground Inputs)

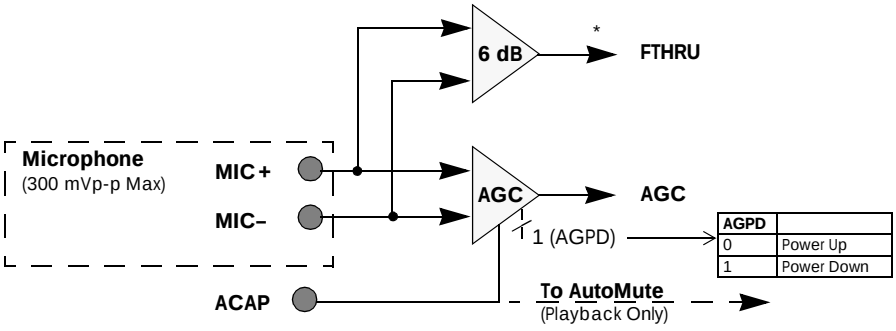
The ISD5008 series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low-impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3 Ω. The backside of the die is connected to V_{SSD} through the substrate resistance. In a chip-on-board design, the die attach area must be connected to V_{SSD}.

Figure 4: ISD5008 Series TSOP and PDIP/SOIC Pinouts



3 INTERNAL FUNCTIONAL BLOCKS

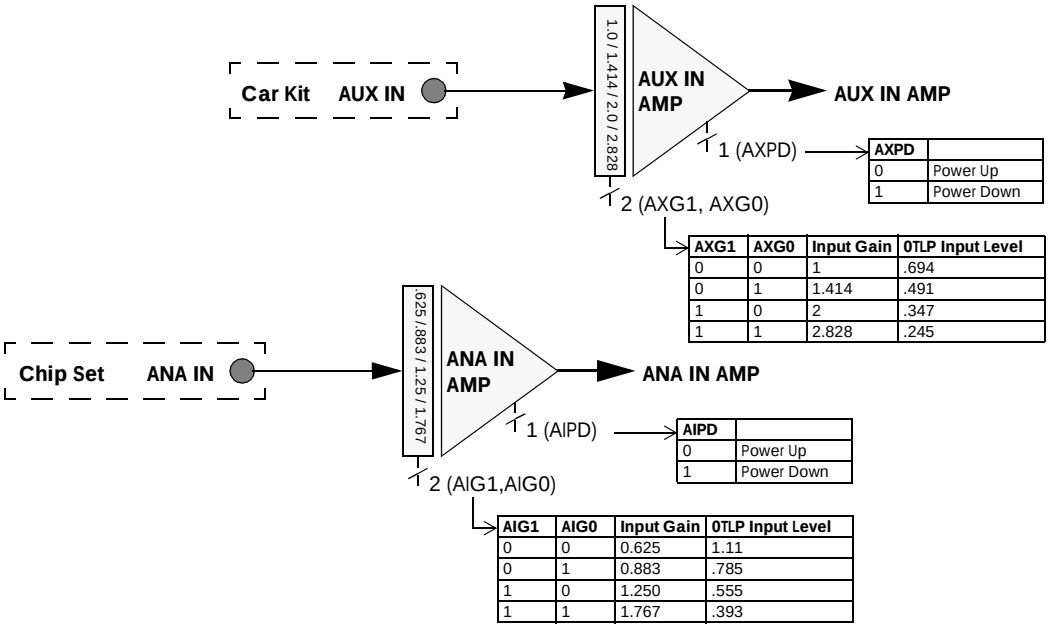
Figure 5: Microphone Amplifier



* Differential Path

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	CFG1

Figure 6: AUX IN and ANA IN



AXPD	
0	Power Up
1	Power Down

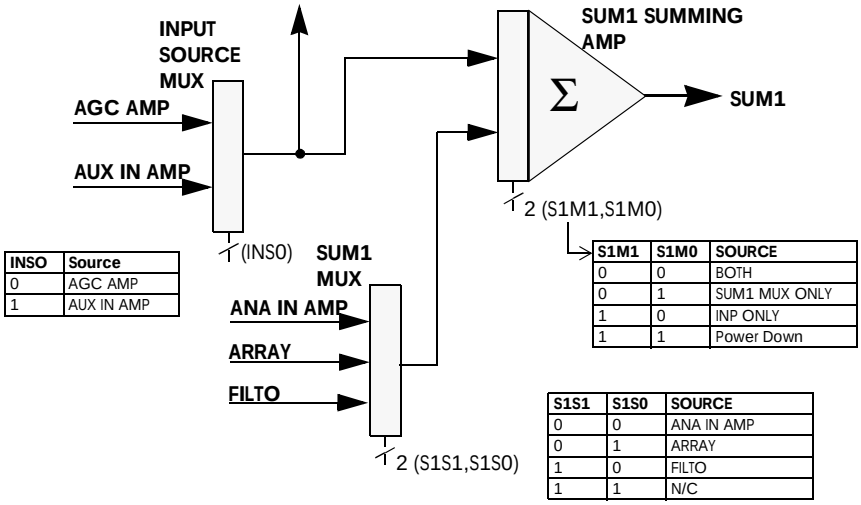
AXG1	AXG0	Input Gain	0TLP Input Level
0	0	1	.694
0	1	1.414	.491
1	0	2	.347
1	1	2.828	.245

AIPD	
0	Power Up
1	Power Down

AIG1	AIG0	Input Gain	0TLP Input Level
0	0	0.625	1.11
0	1	0.883	.785
1	0	1.250	.555
1	1	1.767	.393

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	**AIG0**	**AIPD**	**AXG1**	**AXG0**	**AXPD**	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	**CFG0**

Figure 7: ISD5008 Core (Left Half)



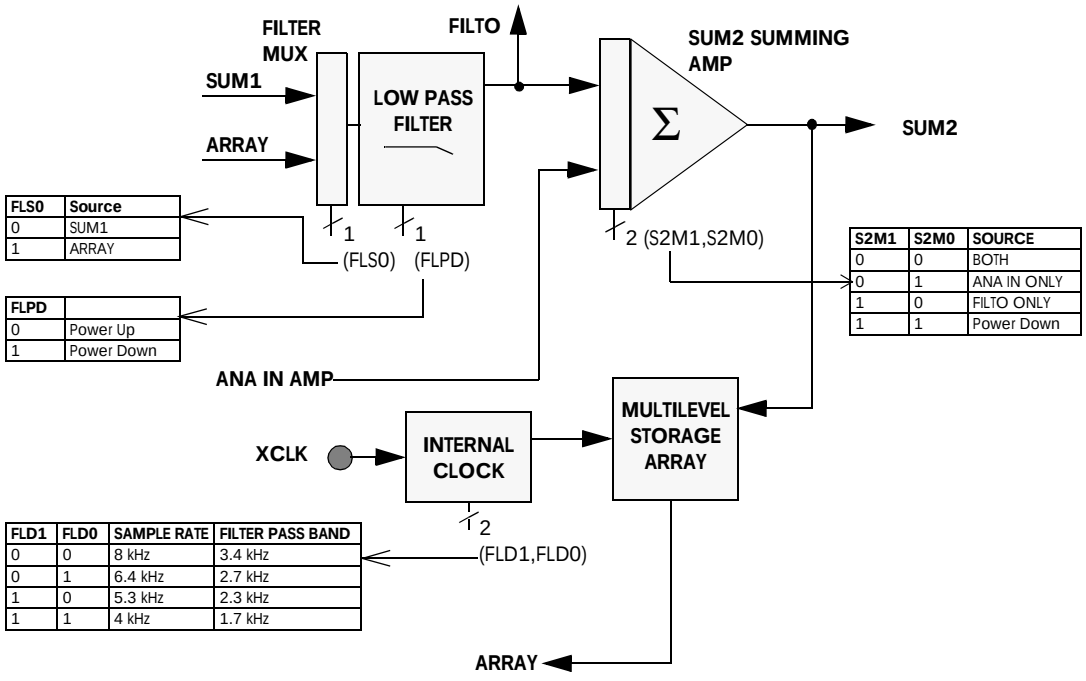
INSO	Source
0	AGC AMP
1	AUX IN AMP

S1M1	S1M0	SOURCE
0	0	BOTH
0	1	SUM1 MUX ONLY
1	0	INP ONLY
1	1	Power Down

S1S1	S1S0	SOURCE
0	0	ANA IN AMP
0	1	ARRAY
1	0	FILTO
1	1	N/C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	**INS0**	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	**CFG0**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	**S1S1**	**S1S0**	**S1M1**	**S1M0**	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	**CFG1**

Figure 8: ISD5008 Core (Right Half)



FLS0	Source
0	SUM1
1	ARRAY

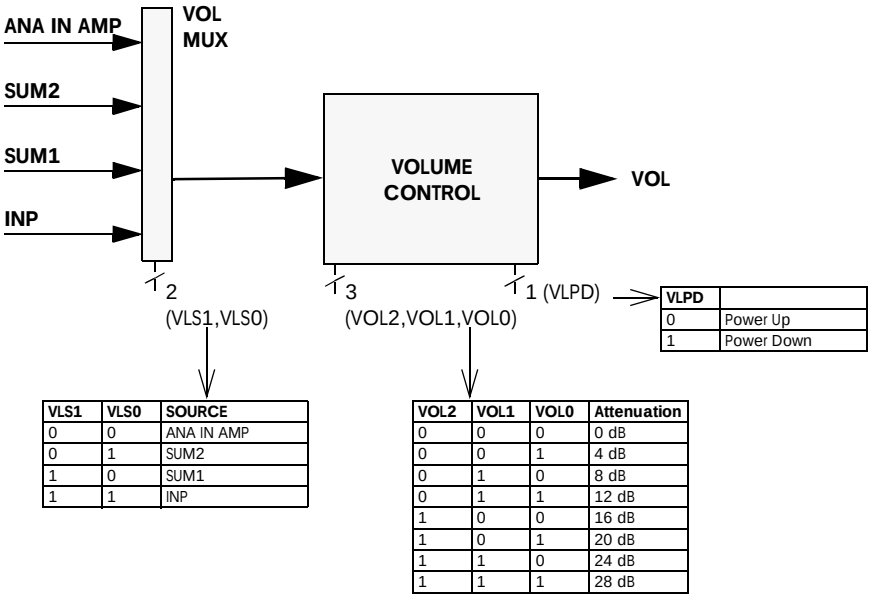
FLPD	
0	Power Up
1	Power Down

S2M1	S2M0	SOURCE
0	0	BOTH
0	1	ANA IN ONLY
1	0	FILTO ONLY
1	1	Power Down

FLD1	FLD0	SAMPLE RATE	FILTER PASS BAND
0	0	8 kHz	3.4 kHz
0	1	6.4 kHz	2.7 kHz
1	0	5.3 kHz	2.3 kHz
1	1	4 kHz	1.7 kHz

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	**S2M1**	**S2M0**	**FLS0**	**FLD1**	**FLD0**	**FLPD**	AGPD	**CFG1**

Figure 9: Volume Control



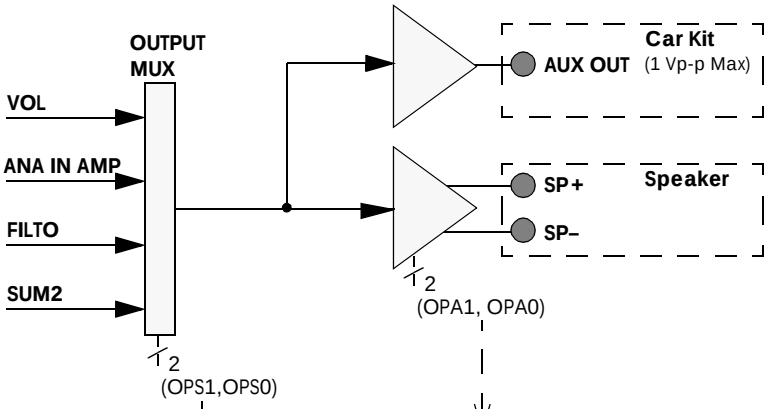
VLPD	
0	Power Up
1	Power Down

VLS1	VLS0	SOURCE
0	0	ANA IN AMP
0	1	SUM2
1	0	SUM1
1	1	INP

VOL2	VOL1	VOL0	Attenuation
0	0	0	0 dB
0	0	1	4 dB
0	1	0	8 dB
0	1	1	12 dB
1	0	0	16 dB
1	0	1	20 dB
1	1	0	24 dB
1	1	1	28 dB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	**VLPD**	**CFG0**
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	**VLS0**	**VOL2**	**VOL1**	**VOL0**	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	**CFG1**

Figure 10: Speaker and AUX OUT

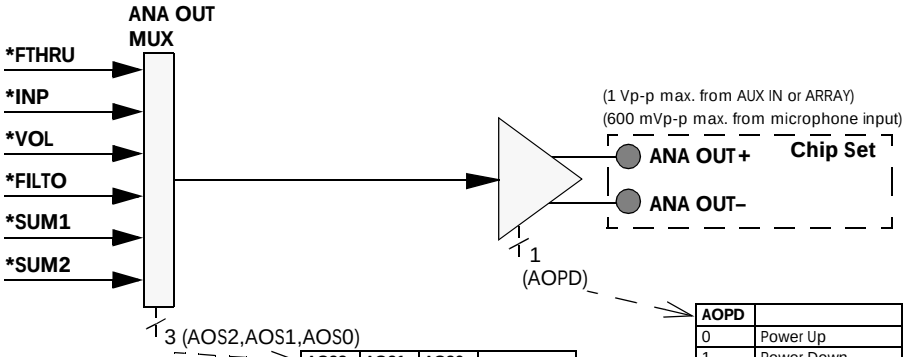


OPS1	OPS0	SOURCE
0	0	VOL
0	1	ANA IN
1	0	FILTO
1	1	SUM2

OPA1	OPA0	SPKR Drive	AUX OP
0	0	Power Down	Power Down
0	1	3.6 Vp-p @ 150 Ω	Power Down
1	0	23 mWatt @ 8 Ω	Power Down
1	1	Power Down	1 Vp-p Max @ 5kΩ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	**OPS1**	**OPS0**	**OPA1**	**OPA0**	VLPD	**CFG0**

Figure 11: ANA OUT Output



AOS2	AOS1	AOS0	
0	0	0	FTHRU
0	0	1	INP
0	1	0	VOL
0	1	1	FILTO
1	0	0	SUM1
1	0	1	SUM2
1	1	0	N/C
1	1	1	N/C

AOPD	
0	Power Up
1	Power Down

*DIFFERENTIAL PATH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	**AOS2**	**AOS1**	**AOS0**	**AOPD**	OPS1	OPS0	OPA1	OPA0	VLPD	**CFG0**

4 SERIAL PERIPHERAL INTERFACE (SPI) DESCRIPTION

The ISD5008 product operates from an SPI serial interface. The SPI interface operates with the following protocol.

The data transfer protocol assumes that the microcontroller's SPI shift registers are clocked on the falling edge of the SCLK. With the ISD5008, data is clocked in on the MOSI pin on the rising clock edge. Data is clocked out on the MISO pin on the falling clock edge.

1. All serial data transfers begin with the falling edge of $\overline{SS}$ pin.
2. $\overline{SS}$ is held LOW during all serial communications and held HIGH between instructions.
3. Data is clocked in on the rising clock edge and data is clocked out on the falling clock edge.
4. Play and Record operations are initiated by enabling the device by asserting the $\overline{SS}$ pin LOW, shifting in an opcode and an address field to the ISD5008 device (refer to the Opcode Summary on the page 14).
5. The opcodes and address fields are as follows: <8 control bits> and <16 address bits>.
6. Each operation that ends in an EOM or Overflow will generate an interrupt, including the Message Cueing cycles. The Interrupt will be cleared the next time an SPI cycle is completed.
7. As Interrupt data is shifted out of the ISD5008 MISO pin, control and address data is simultaneously being shifted into the MOSI pin. Care should be taken such that the data shifted in is compatible with current system operation. It is possible to read interrupt data and start a new operation within the same SPI cycle.
8. A record or playback operation begins with the RUN bit set and the operation ends with the RUN bit reset.
9. All operations begin with the rising edge of $\overline{SS}$.

4.1 MESSAGE CUEING

Message cueing allows the user to skip through messages, without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 1600 times faster than in normal playback mode. It will stop when an EOM marker is reached. Then, the internal address counter will point to the next message.

Table 6: Opcode Summary

Instruction	Opcode <8 bits>[1] Address <16 bits>	Operational Summary
POWERUP	0110 0000	Power-Up: See "Power-Up Sequence"
LOADCFG0[2]	01X0 0010 <D15–D0>	Loads a 16-bit value into Configuration Register 0
LOADCFG1	01X0 0100 <D15–D0>	Loads a 16-bit value into Configuration Register 1
SETPLAY	1110 0000 <A15–A0>	Initiates Playback from address <A15–A0>
PLAY	1111 0000	Playback from current address (until EOM or OVF)
SETREC	1010 0000 <A15–A0>	Initiates Record at address <A15–A0>
REC	1011 0000	Records from current address until OVF is reached
MC	1111 1000	Performs a Message Cue. Proceeds to the end of the current message (EOM) or enters OVF condition if it reaches the end of the array.
STOP	0111 0000	Stops current operation
STOPWRDN	0101 0000	Stops current operation and enters stand-by (power-down) mode.
RINT	0111 0000	Read interrupt status bits: OVF and EOM.

1. *X = Don't Care.*

2. *Changes in CFG0 are not recognized until CFG1 is loaded. The changes will occur at the rising edge of $\overline{SS}$ during the cycle that CFG1 is loaded.*

4.2 POWER-UP SEQUENCE

The ISD5008 will be ready for an operation after T_{PUD} (25 ms approximately for 8 kHz sample rate). The user needs to wait T_{PUD} before issuing an operational command. For example, to play from address 00 the following programing cycle should be used.

Playback Mode

1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Load CFG0 and CFG1 for desired operation.
4. Send SETPLAY command with address 00.

The device will start playback at address 00 and it will generate an interrupt when an EOM is reached. It will then stop playback.

Record Mode

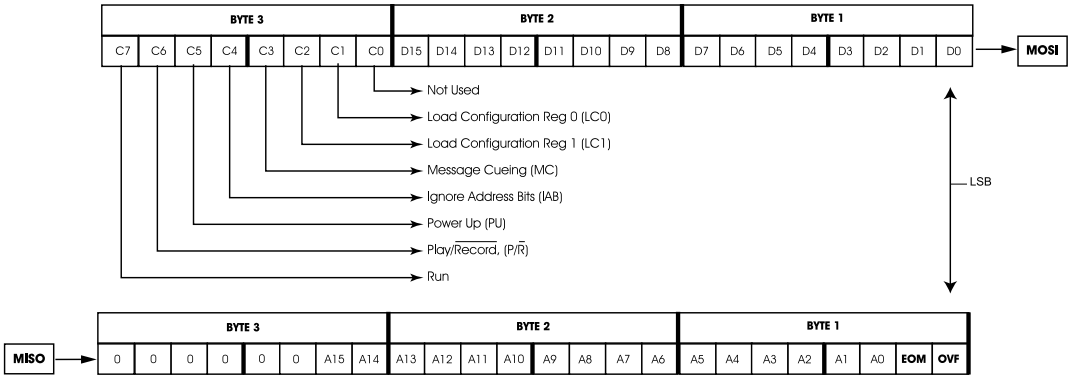
1. Send POWERUP command.
2. Wait T_{PUD} (power-up delay).
3. Load CFG0 and CFG1 for desired operation.
4. Send SETREC command with address 00.

The device will start recording at address 00 and it will generate an interrupt when an overflow is reached (end of memory array) or when it has received a STOP command. It will then stop recording.

4.3 SPI PORT

The following diagram describes the SPI port and the control bits associated with it.

Figure 12: SPI Port



NOTE: *Bytes 1 and 2 of the MOSI input may be address bits or configuration bits, depending on the selected mode in byte 3.*

4.4 SPI CONTROL REGISTER

The SPI control register provides control of individual device functions such as Play, Record, Message Cueing, Power-Up and Power-Down, Start and Stop operations, Ignore Address Pointers and Load Configuration Registers.

Table 7: SPI Control Register

Control Register	Bit	Device Function	Control Register	Bit	Device Function
RUN		Enable or Disable an operation	PU		Master power control
=	1	Start	=	1	Power-Up
=	0	Stop	=	0	Power-Down
P/$\overline{R}$		Selects Play or Record operation	IAB		Ignore address control bit
=	1	Play	=	1	Ignore input address register (A15–A0)
=	0	Record	=	0	Use the input address register contents for an operation (A15–A0)
MC		Enable or Disable Message Cueing	A15–A0		Output of the row pointer register
=	1	Enable Message Cueing	D15–D0		Input control and address register
=	0	Disable Message Cueing			
LC0			LC1		
=	1	Load Configuration Reg 0	=	1	Load Configuration Reg 1
=	0	No Load	=	0	No Load

Table 8: Configuration Register 0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CFG0
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	
ANA IN AMP Gain SET (2 bits)		ANA IN Power Down	AUX IN AMP Gain SET (2 bits)		AUX IN Power Down	INPUT SOURCE MUX Select (1 bit)	ANA OUT MUX Select (3 bits)			ANA OUT Power Down	OUPUT MUX Select (2 bits)		SPKR & AUX OUT Control (2 bits)		Volume Control Power Down	

NOTE: *See details on following pages.*

Table 9: Configuration Register 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CFG1
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLSO	FLD1	FLD0	FLPD	AGPD	
VOLUME CONT. MUX Select (2 bits)		VOLUME CONTROL (3 bits)			SUM 1 MUX Select (2 bits)		SUM 1 SUMMING AMP Control (2 bits)			SUM2 SUMMING AMP Control (2 bits)	FILTER MUX Select		SAMPLE RATE (& Filter) Set Up (2 bits)		Filter Power Down	AGC AMP Power Down

NOTE: *See details on following pages.*

Detail of Configuration Register 0		
Volume Control Power Bit	Bit 0 (VLPD)	0 = Power ON 1 = Power OFF
SPEAKER and AUX OUT Control Bits	Bits 2,1 (OPA1, OPA0)	00 = Power down SPKR and AUX 01 = SPKR ON, HIGH GAIN, AUX Power down 10 = SPKR ON, LOW GAIN, AUX Power down 11 = SPKR Powered down, AUX ON
OUTPUT MUX Control Bits	Bits 4,3 (OPS1, OPS0)	00 = Source is VOL CONTROL (VOL) 01 = Source is ANA IN Input (ANA IN AMP) 10 = Source is LOW PASS FILTER (FILT0) 11 = Source is SUM2 SUMMING AMP (SUM2)
ANA OUT Power Bit	Bit 5 (AOPD)	0 = Power ON 1 = Power OFF
ANA OUT MUX Control Bits	Bits 8,7,6 (AOS2, AOS1, AOS0)	000 = Source is MICROPHONE AMP (FTHRU) 001 = Source is INPUT MUX (INP) 010 = Source is VOLUME CONTROL (VOL) 011 = Source is LOW PASS FILTER (FILT0) 100 = Source is SUM1 SUMMING AMP (SUM1) 101 = Source is SUM2 SUMMING AMP (SUM2) 110 = Unused 111 = Unused
INPUT SOURCE MUX Control Bit	Bit 9 (INS0)	0 = Source is Microphone AGC AMP (AGC) 1 = Source is AUX IN Input (AUX IN AMP)
AUX IN AMP Power Bit	Bit 10 (AXPD)	0 = Power ON 1 = Power OFF
AUX IN AMP Control Bits	Bits 12,11 (AXG1, AXG0)	00 = Input Gain = 1, O_{TLP} input Level = 0.694 01 = Input Gain = 1.414, O_{TLP} input Level = 0.491 10 = Input Gain = 2, O_{TLP} input Level = 0.347 11 = Input Gain = 2.828, O_{TLP} input Level = 0.245
ANA IN AMP Power Bit	Bit 13 (AIPD)	0 = Power ON 1 = Power OFF
ANA IN AMP Control Bits	Bits 15,14 (AIG1, AIG0)	00 = Input Gain = 0.625, O_{TLP} input Level = 1.11 01 = Input Gain = 0.883, O_{TLP} input Level = 0.7l85 10 = Input Gain = 1.250, O_{TLP} input Level = 0.555 11 = Input Gain = 1.767, O_{TLP} input Level = 0.393

Detail of Configuration Register 1		
AGC Power Control Bit	Bit 0 (AGPD)	0 = Power ON 1 = Power OFF
LOW PASS FILTER Power Control Bit	Bit 1 (FLPD)	0 = Power ON 1 = Power OFF
SAMPLE RATE and LOW PASS FILTER Control Bits	Bits 3,2 (FLD1, FLD0)	00 = Sample Rate = 8 KHz, FPB = 3.4 KHz 01 = Sample Rate = 6.4 KHz, FPB = 2.7 KHz 10 = Sample Rate = 5.3 KHz, FPB = 2.3 KHz 11 = Sample Rate = 4 KHz, FPB = 1.7 KHz
FILTER MUX Control bits	Bit 4 (FLS0)	0 = Source is SUM1 SUMMING AMP (SUM1) 1 = Source is Analog Memory Array (ARRAY)
SUM 2 SUMMING AMP Control Bits	Bits 6,5 (S2M1, S2M0)	00 = Source is both ANA IN AMP and FILT0 01 = Source is ANA IN Input (ANA IN AMP) ONLY 10 = Source is LOW PASS FILTER (FILT0) ONLY 11 = Power Down SUM2 SUMMING AMP
SUM1 SUMMING AMP Control Bits	Bit 8,7 (S1M1, S1M0)	00 = Source is both SUM1 and INP 01 = Source is SUM1 SUMMING AMP (SUM1) ONLY 10 = Source is INPUT MUX (INP) ONLY 11 = Power Down SUM1 SUMMING AMP
SUM1MUX Control Bits	Bit 10,9 (S1S1, S1S0)	00 = Source is ANA IN Input (ANA IN AMP) 01 = Source is Analog Memory Array (ARRAY) 10 = Source is LOW PASS FILTER (FILT0) 11 = UNUSED
VOLUME CONTROL Control Bits	Bits 13,12,11 (VOL2, VOL1, VOL0)	000 = Attenuation = 0 dB 001 = Attenuation = 4 dB 010 = Attenuation = 8 dB 011 = Attenuation = 12 dB 100 = Attenuation = 16 dB 101 = Attenuation = 20 dB 110 = Attenuation = 24 dB 111 = Attenuation = 28 dB
VOL MUX Control Bits	Bit 15,14 (VLS1, VLS0)	00 = Source is ANA IN Input (ANA IN AMP) 01 = Source is SUM2 SUMMING AMP (SUM2) 10 = Source is SUM1 SUMMING AMP (SUM1) 11 = Source is INPUT MUX (INP)

Configuration Register Notes

1. ***Important:*** All changes to the internal settings of the ISD5008 are synchronized with the load of Configuration Register 1. A command to load Configuration Register 1 immediately transfers the input data to the internal settings of the device and the changes take place immediately at the end of the command when SS\ goes HIGH. A load to Configuration Register 0 sends the new data to a temporary register in the ISD5008 and does not affect the internal settings of the device. The next time Configuration Register 1 is loaded, data will also transfer from the temporary register to the Configuration 0 Register and effect the desired changes. See Figure Table 13.
2. Configuration Registers may be loaded with data at any time, including when the chip is powered down using the PU bit in the SPI Control Register. The PU bit in the SPI Control Word will have to be set to a “1” before the changes in configuration will be seen.

Figure 13: Configuration Register Programming Sequence

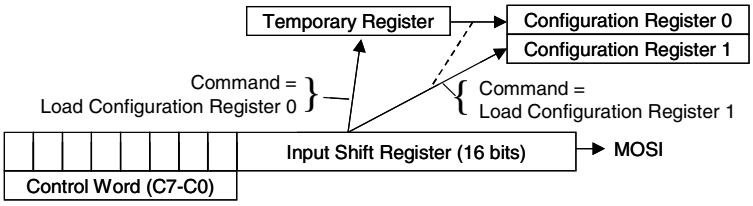
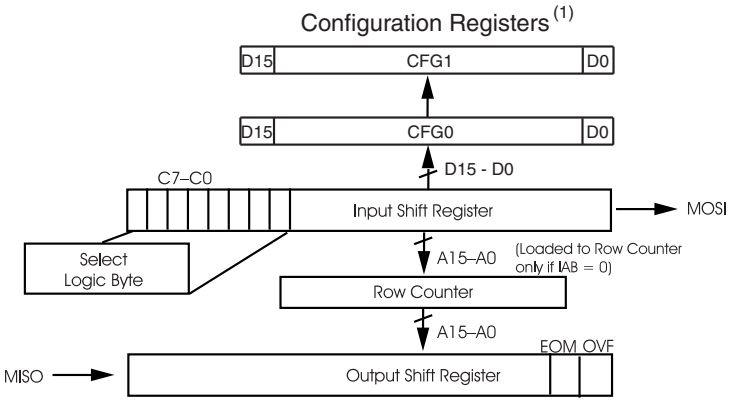
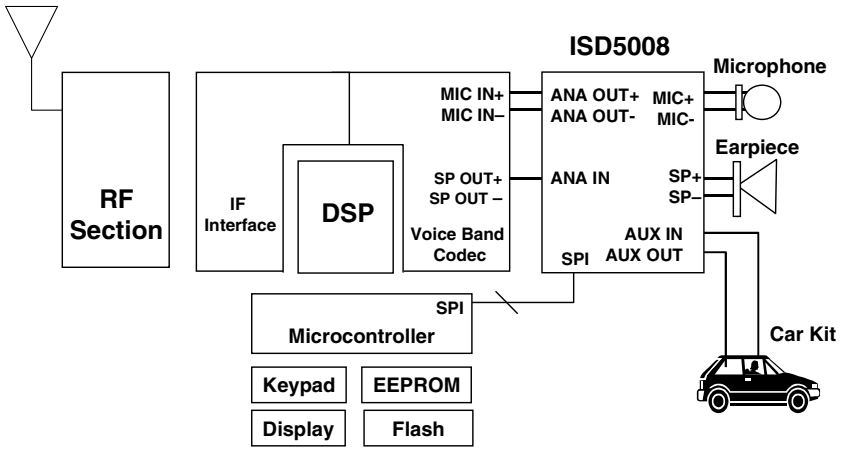


Figure 14: SPI Interface Simplified Block Diagram



1. *See Table 8 for bit details.*

Figure 15: Typical Digital Cellular Phone Integration



5 OPERATIONAL MODES DESCRIPTION

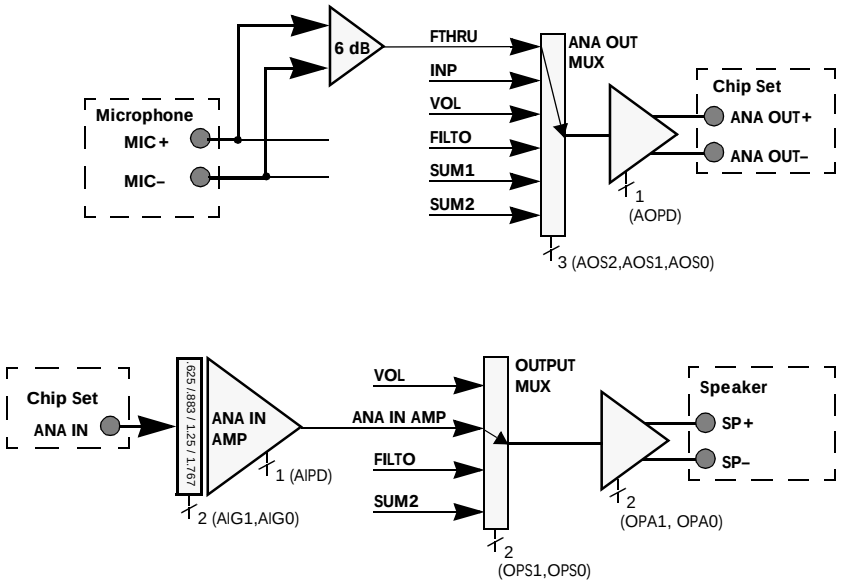
The ISD5008 can operate in many different modes. It's flexibility allows the user to configure the chip such that almost any input can mixed with any other input and then be directed to any output. The variable settings for the ANA and AUX input amplifiers plus the microphone AGC and speaker volume controls make it possible to use the device with most existing cell phone or cordless phone chip sets with no external level adjustment. Several modes will be found in most applications, however. Please refer to the ISD5008 block diagram to better understand the following modes. In all cases, we are assuming that the chip has been powered up with the PU bit in the SPI control register and that a time period of T_{PUD} has elapsed after that bit was set:

5.1 FEED THROUGH MODE

This mode enables the ISD5008 to connect to a base band cell phone or cordless phone chip set without affecting the audio source or destination. There are two paths involved, the transmit path and the receive path. The transmit path connects the ISD chip's microphone source through to the microphone input on the base band chip set. The receive path connects the base band chip set's speaker output through to the speaker driver on the ISD chip. This allows the ISD chip to substitute for those functions and incidentally gain access to the audio to and from the base band chip set. Figure 15 shows one possible connection to such a chip set.

Figure 16 shows the part of the ISD5008 block diagram that is used in Feed Through Mode. The rest of the chip will be powered down to conserve power. The bold lines highlight the audio paths. Note that the Microphone to ANA OUT +/– path is differential.

Figure 16: Basic Feed-Thru Mode



To select this mode, the following control bits must be configured in the ISD5008 configuration registers. To set up the transmit path:

1. *Select the FTHRU path through the ANA OUT MUX*—Bits AOS0, AOS1 and AOS2 control the state of the ANAOUT MUX. These are the D6, D7 and D8 bits respectively of Configuration Register 0 (CFG0) and they should all be ZERO to select the FTHRU path.
2. *Power up the ANA OUT amplifier*—Bit AOPD controls the power up state of ANA OUT. This is bit D5 of CFG0 and it should be a ZERO to power up the amplifier.

To set up the receive path:

1. *Set up the ANA IN amplifier for the correct gain*—Bits AIG0 and AIG1 control the gain settings of this amplifier. These are bits D14 and D15 respectively of CFG0. The input level at this pin determines the setting of this gain stage. Table 4 will help determine this setting. In this example we will assume that the peak signal never goes above 1 volt p-p single ended. That would enable us to use the 9dB attenuation setting, or where D14 is ONE and D15 is ZERO.
2. *Power up the ANA IN amplifier*—Bit AIPD controls the power up state of ANA IN. This is bit D13 of CFG0 and should be a ZERO to power up the amplifier.
3. *Select the ANA IN path through the OUTPUT MUX*—Bits OPS0 and OPS1 control the state of the OUTPUT MUX. These are bits D3 and D4 respectively of CFG0 and they should be set to the state where D3 is ONE and D4 is ZERO to select the ANA IN path.
4. *Power up the Speaker Amplifier*—Bits OPA0 and OPA1 control the state of the Speaker and AUX amplifiers. These are bits D1 and D2 respectively of CFG0. They should be set to the state where D1 is ONE and D2 is ZERO. This powers up the Speaker Amplifier and configures it for it's higher gain setting for use with a piezo speaker element and also powers down the AUX output stage.

The status of the rest of the functions in the ISD5008 chip must be defined before the configuration registers settings are updated:

1. *Power down the Volume Control Element*—Bit VLPD controls the power up state of the Volume Control. This is bit D0 of CFG0 and it should be set to a ONE to power down this stage.
2. *Power down the AUX IN amplifier*—Bit AXPD controls the power up state of the AUX IN input amplifier. This is bit D10 of CFG0 and it should be set to a ONE to power down this stage.
3. *Power down the SUM1 and SUM2 Mixer amplifiers*—Bits S1M0 and S1M1 control the SUM1 mixer and bits S2M0 and S2M1 control the SUM2 mixer. These are bits D7 and D8 in CFG1 and bits D5 and D6 in CFG1 respectively. All 4 bits should be set to a ONE to power down these two amplifiers.
4. *Power down the FILTER stage*—Bit FLPD controls the power up state of the FILTER stage in the device. This is bit D1 in CFG1 and should be set to a ONE to power down the stage.
5. *Power down the AGC amplifier*—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 in CFG1 and should be set to a ONE to power down this stage.
6. *Don't Care bits*—The following stages are not used in Feed Through Mode. Their bits may be set to either level. In this example we will set all the following bits to a ZERO. (a). Bit INS0, bit D9 of CFG0 controls the Input Source Mux. (b). Bits AXG0 and AXG1 are bits D11 and D12 respectively in CFG0. They control the AUX IN amplifier gain setting. (c). Bits FLD0 and FLD1 are bits D2 and D3 respectively in CFG1. They control the sample rate and filter band pass setting. (d). Bit FLS0 is bit D4 in CFG1. It controls the FILTER MUX. (e). Bits S1S0 and S1S1 are bits

D9 and D10 of CFG1. They control the SUM1 MUX. (f). Bits VOL0, VOL1 and VOL2 are bits D11, D12 and D13 of CFG1. They control the setting of the Volume Control. (g). Bits VLS0 and VLS1 are bits D14 and D15 of CFG1. They control the Volume Control MUX.

The end result of the above set up is

CFG0 = 0100 0100 0000 1011 (hex 440B)

and

CFG1 = 0000 0001 1110 0011 (hex 01E3).

Since both registers are being loaded, CFG0 is loaded followed by the loading of CFG1. These two registers must be loaded in this order. The internal set up for both registers will take effect synchronously with the rising edge of $\overline{SS}$.

5.2 CALL RECORD

The call record mode adds the ability to record the incoming phone call. In most applications, the ISD5008 would first be set up for Feed Through Mode as described above. When the user wishes to record the incoming call, the set up of the chip is modified to add that ability. For the purpose of this explanation, we will use the 6.4 kHz sample rate during recording.

The block diagram of the ISD5008 shows that the Multilevel Storage array is always driven from the SUM2 SUMMING amplifier. The path traces back from there through the LOW PASS Filter, THE FILTER MUX, THE SUM1 SUMMING amplifier, the SUM1 MUX, then from the ANA in amplifier. Feed Through Mode has already powered up the ANA IN amp so we only need to power up and enable the path to the Multilevel Storage array from that point:

1. *Select the ANA IN path through the SUM1 MUX*—Bits S1S0 and S1S1 control the state of the SUM1 MUX. These are bits D9 and D10 respectively of CFG1 and they should be set to the state where both D9 and D10 are ZERO to select the ANA IN path.
2. *Select the SUM1 MUX input (only) to the S1 SUMMING amplifier*—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8 respectively of CFG1 and they should be set to the state where D7 is ONE and D8 is ZERO to select the SUM1 MUX (only) path.
3. *Select the SUM1 SUMMING amplifier path through the FILTER MUX*—Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.
4. *Power up the LOWPASS FILTER*—Bit FLPD controls the power up state of the LOWPASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.
5. *Select the 6.4 kHz sample rate*—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 6.4 kHz sample rate, D2 must be set to ONE and D3 set to ZERO.
6. *Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier*—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

In this mode, the elements of the original PASS THROUGH mode do not change. The sections of the chip not required to add the record path remain powered down. In fact, CFG0 does not change and remains

CFG0 = 0100 0100 0000 1011 (hex 440B).

CFG1 changes to

CFG1 = 0000 0000 1100 0101 (hex 00C5).

Since CFG0 is not changed, it is only necessary to load CFG1. Note that if only CFG0 was changed, it would be necessary to load both registers.

5.3 MEMO RECORD

The Memo Record mode sets the chip up to record from the local microphone into the chip's Multilevel Storage Array. A connected cellular telephone or cordless phone chip set may remain powered down and is not active in this mode. The path to be used is microphone input to AGC amplifier, then through the INPUT SOURCE MUX to the SUM1 SUMMING amplifier. From there the path goes through the FILTER MUX, the LOW PASS FILTER, the SUM2 SUMMING amplifier, then to the MULTILEVEL STORAGE ARRAY. In this instance, we will select the 5.3 kHz sample rate. The rest of the chip may be powered down.

1. *Power up the AGC amplifier*—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 of CFG1 and must be set to ZERO to power up this stage.
2. *Select the AGC amplifier through the INPUT SOURCE MUX*—Bit INS0 controls the state of the INPUT SOURCE MUX. This is bit D9 of CFG0 and must be set to a ZERO to select the AGC amplifier.
3. *Select the INPUT SOURCE MUX (only) to the S1 SUMMING amplifier*—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8 respectively of CFG1 and they should be set to the state where D7 is ZERO and D8 is ONE to select the INPUT SOURCE MUX (only) path.
4. *Select the SUM1 SUMMING amplifier path through the FILTER MUX*—Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.
5. *Power up the LOWPASS FILTER*—Bit FLPD controls the power up state of the LOWPASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.
6. *Select the 5.3 kHz sample rate*—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 5.3 kHz sample rate, D2 must be set to ZERO and D3 set to ONE.
7. *Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier*—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

To set up the chip for Memo Record, the configuration registers are set up as follows:

CFG0 = 0010 0100 0010 0001 (hex 2421).

CFG1 = 0000 0001 0100 1000 (hex 0148).

Only those portions necessary for this mode are powered up.

5.4 MEMO AND CALL PLAYBACK

This mode sets the chip up for local playback of messages recorded earlier. The playback path is from the MULTILEVEL STORAGE ARRAY to the FILTER MUX, then to the LOW PASS FILTER stage. From there the audio path goes through the SUM2 SUMMING amplifier to the VOLUME MUX, through the VOLUME CONTROL then to the SPEAKER output stage. We will assume that we are driving a pizeo speaker element. This audio was previously recorded at 8 kHz. All unnecessary stages will be powered down.

1. *Select the MULTILEVEL STORAGE ARRAY path through the FILTER MUX*—Bit FLS0, the state of the FILTER MUX. This is bit D4 of CFG1 and must be set to ONE to select the MULTILEVEL STORAGE ARRAY.
2. *Power up the LOWPASS FILTER*—Bit FLPD controls the power up state of the LOWPASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.
3. *Select the 8.0 kHz sample rate*—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record

and playback. These are bits D2 and D3 of CFG1. To enable the 8.0 kHz sample rate, D2 and D3 must be set to ZERO.

4. *Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier*—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

5. *Select the SUM2 SUMMING amplifier path through the VOLUME MUX*—Bits VLS0 and VLS1 control the state VOLUME MUX. These bits are bits D14 and D15, respectively of CFG1. They should be set to the state where D14 is ONE and D15 is ZERO to select the SUM2 SUMMING amplifier.

6. *Power up the VOLUME CONTROL LEVEL*—Bit VLPD controls the power-up state of the VOLUME CONTROL attenuator. This is Bit D0 of CFG0. This bit must be set to a ZERO to power-up the VOLUME CONTROL.

7. *Select a VOLUME CONTROL LEVEL*—Bits VOL0, VOL1, and VOL2 control the state of the VOLUME CONTROL LEVEL. These are bits D11, D12, and D13, respectively, of CFG1. A binary count of 000 through 111 controls the amount of attenuation through that state. In most cases, the software will select an attenuation level according to the desires of the current users of the product. In this example, we will assume the user wants an attenuation of –12 dB. For that setting, D11 should be set to ONE, D12 should be set to ONE, and D13 should be set to a ZERO.

8. *Select the VOLUME CONTROL path through the OUTPUT MUX*—These are bits D3 and D4, respectively, of CFG0. They should be set to the state where D3 is ZERO and D4 is a ZERO to select the VOLUME CONTROL.

9. *Power up the SPEAKER amplifier and select the HIGH GAIN mode*—Bits OPA0 and OPA1 control the state of the speaker (SP+ and SP–) and AUX OUT outputs. These are bits D1 and D2 of CFG0. They must be set to the state where D1 is ONE and D2 is ZERO to power-up the speaker outputs in the HIGH GAIN mode and to power-down the AUX OUT.

To set up the chip for Memo or Call Playback, the configuration registers are set up as follows:

CFG0 = 0010 0100 0010 0010 (hex 2422).

CFG1 = 0101 1001 1101 0001 (hex 59D1).

Only those portions necessary for this mode are powered up.

Table 10: Absolute Maximum Ratings (Packaged Parts)(1)

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to MOSI, SCLK, $\overline{INT}$, RAC and $\overline{SS}$ pins (Input current limited to ±20mA)	(V_{SS} – 1.0 V) to 5.5V
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 11: Absolute Maximum Ratings (Die)(1)

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to MOSI, SCLK, $\overline{INT}$, RAC and $\overline{SS}$ pins (Input current limited to ±20mA)	(V_{SS} – 0.3 V) to 5.5V
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 12: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range(1)	0°C to +70°C
Extended operating temperature(1)	–20°C to +70°C
Industrial operating temperature(1)	–40°C to +85°C
Supply voltage (V_{CC})(2)	+2.7 V to +3.3 V
Ground voltage (V_{SS})(3)	0 V

1. *Case Temperature*
2. $V_{CC} = V_{CCA} = V_{CCD}$
3. $V_{SS} = V_{SSA} = V_{SSD}$

Table 13: Operating Conditions (Die)

Condition	Value
Commercial operating temperature range	0°C to +50°C
Supply voltage (V_{CC})(1)	+2.7 V to +3.3 V
Ground voltage (V_{SS})(2)	0 V

1. $V_{CC} = V_{CCA} = V_{CCD}$
2. $V_{SS} = V_{SSA} = V_{SSD}$

Table 14: General Parameters

Symbol	Parameters	Min(2)	Typ(1)	Max(2)	Units	Conditions
V_{IL}	Input Low Voltage			V_{CC} x 0.2	V	
V_{IH}	Input High Voltage	V_{CC} x 0.8			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 10 µA
V_{OL1}	RAC, $\overline{INT}$ Output Low Voltage			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
I_{CC}	V_{CC} Current (Operating) — Playback — Record — Feedthru		 15 25 12		 mA mA mA	 No load(3) No load (3) No load (3)
I_{SB}	V_{CC} Current (Standby)		1	10	µA	(3) (4)
I_{IL}	Input Leakage Current			±1	µA	
I_{HZ}	MISO Tristate Current		1	10	µA	

1. *Typical values: T_A = 25°C and Vcc = 3.0 V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} summed together.*
4. *$\overline{SS}$ = V_{CCA} = V_{CCD}, XCLK = MOSI = V_{SSA} = V_{SSD} and all other pins floating.*

Table 15: Timing Parameters

Symbol	Characteristic	Min(2)	Typ(1)	Max(2)	Units	Conditions
F_S	Sampling Frequency		8.0		kHz	(5)
			6.4		kHz	(5)
			5.3		kHz	(5)
			4.0		kHz	(5)
F_{CF}	Filter Pass Band					
	8.0 kHz (sample rate)		3.4		kHz	3-dB Roll-Off Point(3) (7)
	6.4 kHz (sample rate)		2.7		kHz	3-dB Roll-Off Point(3) (7)
	5.3 kHz (sample rate)		2.3		kHz	3-dB Roll-Off Point(3) (7)
	4.0 kHz (sample rate)		1.7		kHz	3-dB Roll-Off Point(3) (7)
T_{REC}	Record Duration					
	8.0 kHz (sample rate)		4		min	(6)
	6.4 kHz (sample rate)		5		min	(6)
	5.3 kHz (sample rate)		6		min	(6)
	4.0 kHz (sample rate)		8		min	(6)
T_{PLAY}	Playback Duration					
	8.0 kHz (sample rate)		4		min	(6)
	6.4 kHz (sample rate)		5		min	(6)
	5.3 kHz (sample rate)		6		min	(6)
	4.0 kHz (sample rate)		8		min	(6)
T_{PUD}	Power-Up Delay					
	8.0 kHz (sample rate)		25		msec	
	6.4 kHz (sample rate)		31.25		msec	
	5.3 kHz (sample rate)		37.5		msec	
	4.0 kHz (sample rate)		50		msec	
T_{STOP} OR $_{PAUSE}$	Stop or Pause Record or Play					
	8.0 kHz (sample rate)		50		msec	
	6.4 kHz (sample rate)		62.5		msec	
	5.3 kHz (sample rate)		75		msec	
	4.0 kHz (sample rate)		100		msec	
T_{RAC}	RAC Clock Period					
	8.0 kHz (sample rate)		200		msec	(9)
	6.4 kHz (sample rate)		250		msec	(9)
	5.3 kHz (sample rate)		300		msec	(9)
	4.0 kHz (sample rate)		400		msec	(9)
T_{RACLO}	RAC Clock Low Time					
	8.0 kHz (sample rate)		25		msec	
	6.4 kHz (sample rate)		31.25		msec	
	5.3 kHz (sample rate)		37.5		msec	
	4.0 kHz (sample rate)		50		msec	

Table 15: Timing Parameters

Symbol	Characteristic	Min(2)	Typ(1)	Max(2)	Units	Conditions
T_{RACM}	RAC Clock Period in Message Cueing Mode 8.0 kHz (sample rate) 6.4 kHz (sample rate) 5.3 kHz (sample rate) 4.0 kHz (sample rate)		 125 156.3 187.5 250		 µsec µsec µsec µsec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode 8.0 kHz (sample rate) 6.4 kHz (sample rate) 5.3 kHz (sample rate) 4.0 kHz (sample rate)		 15.63 19.53 23.44 31.25		 µsec µsec µsec µsec	
THD	Total Harmonic Distortion ANA IN to ARRAY, ARRAY to SPKR		1	2	%	@1 kHz at 0TLP, sample rate = 5.3kHz

Table 16: Analog Parameters

Symbol	Characteristic	Min(2)	Typ(1)	Max(2)	Units	Conditions
MICROPHONE INPUT (14)						
$V_{MIC+/-}$	MIC +/– Input Voltage	3		300	mV	Peak-to-Peak (4)(8)
$V_{MIC\ (0TLP)}$	MIC +/– input reference transmission level point (0TLP)		208		mV	Peak-to-Peak(4)(10)
A_{MIC}	Gain from MIC+/– input to ANA OUT	5.5	6.0	6.5	dB	1 kHz at $V_{MIC\ (0TLP)}$(4)
$A_{MIC\ (GT)}$	MIC +/– Gain Tracking		±0.1		dB	1 kHz, +3 to –40 dB 0TLP Input
R_{MIC}	Microphone input resistance	5	10	15	kΩ	MIC– and MIC+ pins
A_{AGC}	Microphone AGC Amplifier Range	6		40	dB	Over 3–300 mV Input Range
ANA IN (14)						
$V_{ANA\ IN}$	ANA IN Input Voltage			1.6	V	Peak-to-Peak (6dB gain setting)
$V_{ANA\ IN\ (0TLP)}$	ANA IN (0TLP) Input Voltage		1.11		V	Peak-to-Peak (6dB gain setting)(10)
$A_{ANA\ IN\ (SP)}$	Gain from ANA IN to SP+/–		6 to 15		dB	4 Steps of 3 dB

Table 16: Analog Parameters

Symbol	Characteristic	Min[2]	Typ[1]	Max[2]	Units	Conditions
$A_{ANA\ IN\ (AUX\ OUT)}$	Gain from ANA IN to AUX OUT		–4 to +5		dB	4 Steps of 3 dB
$A_{ANA\ IN\ (GA)}$	ANA IN Gain Accuracy	–0.5		+0.5	dB	[11]
$A_{ANA\ IN\ (GT)}$	ANA IN Gain Tracking		±0.1		dB	1000 Hz, +3 to –40 dB 0TLP Input, 6dB setting
$R_{ANA\ IN}$	ANA IN Input Resistance		60 to 102		kΩ	See Ra in Figure 2
AUX IN[14]						
$V_{AUX\ IN}$	AUX IN Input Voltage			1.0	V	Peak-to-Peak (0 dB gain setting)
$V_{AUX\ IN\ (0TLP)}$	AUX IN (0TLP) Input Voltage		694.2		mV	Peak-to-Peak (0 dB gain setting)[10]
$A_{AUX\ IN\ (ANA\ OUT)}$	Gain from AUX IN to ANA OUT		0 to 9		dB	4 Steps of 3dB
$A_{AUX\ IN\ (GA)}$	AUX IN Gain Accuracy	–0.5		+0.5	dB	[11]
$A_{Aux\ IN\ (GT)}$	AUX IN Gain Tracking		±0.1		dB	1000 Hz, +3 to –40 dB 0TLP Input, 0dB setting
$R_{Aux\ IN}$	AUX IN Input Resistance		21 to 40		kΩ	See Ra in Figure 3
SPEAKER OUTPUTS[14]						
V_{SPHG}	SP+/– Output Voltage (High Gain setting)			3.6	V	Peak-to-Peak, differential load = 150Ω, OPA1, OPA0 = 01
R_{SPLG}	SP+/– Output Load Imp. (Low Gain)	8			Ω	OPA1, OPA0 = 10
R_{SPHG}	SP+/– Output Load Imp. (High Gain)	70			Ω	OPA1, OPA0 = 01
C_{SP}	SP+/– Output Load Cap.			100	pF	
V_{SPAG}	SP+/– Output Bias Voltage (analog ground)		1.2		VDC	
V_{SPDCO}	Speaker Output DC Offset	–100		100	mVDC	With ANA IN to Speaker, ANA IN AC coupled to V_{SSA}
$ICN_{ANA\ IN/(SP+/–)}$	ANA IN to SP+/– Idle Channel Noise			–65	dB	Speaker load = 150Ω [12][13]
$C_RT_{(SP+/–)/ANA\ OUT}$	SP+/– to ANA OUT Cross Talk			–65	dB	1kHz 0TLP input to ANA IN, with MIC+/– and AUX IN AC coupled to V_{SSA}, and measured at ANA OUT feedthrough mode [12]
PSRR	Power Supply Rejection Ratio		–50		dB	Measured with a 1kHz,100 mVpp sine wave input at V_{CCA} and V_{CCD} pins

Table 16: Analog Parameters

Symbol	Characteristic	Min[2]	Typ[1]	Max[2]	Units	Conditions
F_R	Frequency Response (300–3400 Hz)	–0.25		+0.25	dB	With 0TLP input to ANA IN, 6dB setting [12]
P_{OUTLG}	Power Output (Low Gain Setting)	23.5			mW RMS	Differential load at 8Ω
SINAD	SINAD ANA IN to SP+/–	62.5			dB	0TLP ANA IN input minimum gain, 150Ω load [12][13]
ANA OUT[14]						
SINAD	SINAD MIC IN to ANA OUT +/-	62.5			dB	Load = 5k Ω [12][13]
SINAD	SINAD AUX IN to ANA OUT (0 to 9 dB)	62.5			dB	Load = 5k Ω [12][13]
$ICN_{MIC/ANA\ OUT}$	Idle Channel Noise—Microphone			–65	dB	Load = 5k Ω [12][13]
$ICN_{AUX\ IN/ANA\ OUT}$	Idle Channel Noise—AUX IN (0 to 9 dB)			–65	dB	Load = 5k Ω [12][13]
$PSRR_{(ANA\ OUT)}$	Power Supply Rejection Ratio		-50		dB	Measured with a 1kHz, 100mVpp sine wave to V_{CCA}, V_{CCD} pins
V_{BIAS}	ANA OUT+ and ANA OUT–		1.2		VDC	Inputs AC coupled to V_{SSA}
V_{OFFSET}	ANA OUT+ to ANA OUT–	–100		+100	mVDC	Inputs AC coupled to V_{SSA}
R_L	Minimum Load Impedence	5			kΩ	Differential Load
F_R	Frequency Response (300–3400 Hz)	–0.25		+0.25	dB	0TLP input to MIC+/- in feedthrough mode. 0TLP input to AUX IN in feedthrough mode[12]
$C_RT_{ANA\ OUT/(SP+/-)}$	ANA OUT to SP+/- Cross Talk			–65	dB	1kHz 0TLP output from ANA OUT, with ANA IN AC coupled to V_{SSA}, and measured at SP+/- [12]
$C_RT_{ANA\ OUT/AUX\ OUT}$	ANA OUT to AUX OUT Cross Talk			–65	dB	1kHz 0TLP output from ANA OUT, with ANA IN AC coupled to V_{SSA}, and measured at AUX OUT(12)
AUX OUT[14]						
$V_{AUX\ OUT}$	AUX OUT—Maximum Output Swing			1.0	Vpp	5 kΩ Load
R_L	Minimum Load Impedence	5			kΩ	
C_L	Maximum Load Capacitance			100	pF	

Table 16: Analog Parameters

Symbol	Characteristic	Min(2)	Typ(1)	Max(2)	Units	Conditions
V_{BIAS}	AUX OUT		1.2		VDC	
SINAD	SINAD—ANA IN to AUX OUT	62.5			dB	0TLP ANA IN input, minimum gain, 5k load (12)(13)
$ICN_{(AUX\ OUT)}$	Idle Channel Noise—ANA IN to AUX OUT			–65	dB	Load = 5kΩ (12)(13)
$C_RT_{AUX\ OUT/ANA\ OUT}$	AUX OUT to ANA OUT cross Talk			–65	dB	1 kHz 0TLP input to ANA IN, with MIC +/- and AUX IN AC coupled to V_{SSA}, and measured at SP+/-, load = 5kΩ Referenced to nominal 0TLP @ output
VOLUME CONTROL (14)						
A_{OUT}	Output Gain		–28 to 0		dB	8 Steps of 4 dB, referenced to output
	Gain Accuracy	-0.5		0.5	dB	ANA IN = 1 kHz 0TLP, 6dB Gain setting, measured differentially at SP+/–

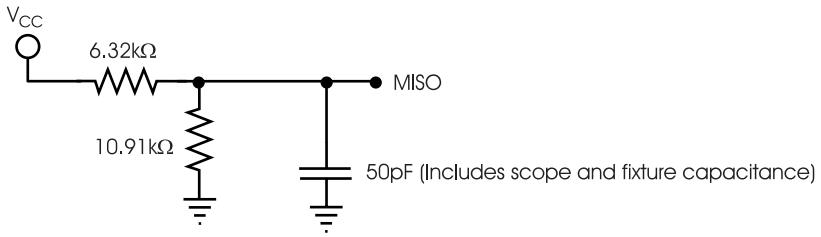
1. *Typical values: T_A = 25°C and Vcc = 3.0V.*
2. *All min/max limits are guaranteed by ISD via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Differential input mode. Nominal differential input is 208 mVp-p. (0 dBm0)*
5. *Sampling frequency can vary as much as –6/+4 percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions). Sampling frequency will be accurate within ±1% for 5.3kHz, and ±5% for 4.0, 6.4 and 8.0 kHz sampling rates at room temperature.*
6. *Playback and Record Duration can vary as much as –6/+4 percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (See Pin Descriptions). Playback and record durations are accurate within ±1% for 5.3kHz, and ±5% for 4.0, 6.4 and 8.0kHz sampling rates at room temperature.*
7. *Filter specification applies to the low pass filter. Therefore, from input to output, expect a 6 dB drop by nature of passing through the filter twice.*
8. *For optimal signal quality, this maximum limit is recommended.*
9. *When a record command is sent, T_{RAC} = T_{RAC} + T_{RACLO} on the first row addressed.*
10. *The maximum signal level at any input is defined as 3.17dB higher than the reference transmission level point. (0TLP) This is the point where signal clipping may begin.*
11. *Measured at 0TLP point for each gain setting. See Table 4 and Table 5.*
12. *0TLP is the reference test level through inputs and outputs. See Table 4 and Table 5.*
13. *Referenced to 0TLP input at 1kHz, measured over 300 to 3,400 Hz bandwidth.*
14. *For die, only typical values from Analog Parameters are applicable.*

Table 17: SPI AC Parameters(1)

Symbol	Characteristics	Min	Max	Units	Conditions
T_{SSS}	$\overline{SS}$ Setup Time	500		nsec	
T_{SSH}	$\overline{SS}$ Hold Time	500		nsec	
T_{DIS}	Data in Setup Time	200		nsec	
T_{DIH}	Data in Hold Time	200		nsec	
T_{PD}	Output Delay		500	nsec	
T_{DF}	Output Delay to hiZ		500	nsec	(2)
T_{SSmin}	$\overline{SS}$ HIGH	1		µsec	
T_{SCKhi}	SCLK High Time	400		nsec	
T_{SCKlow}	SCLK Low Time	400		nsec	
F_0	CLK Frequency		1,000	kHz	

1. *Typical values: T_A = 25°C and V_{cc} = 3.0 V. Timing measured at 50 percent of the V_{CC} level.*

2. *Tristate test condition*



6 TIMING DIAGRAMS

Figure 17: SPI Timing Diagram

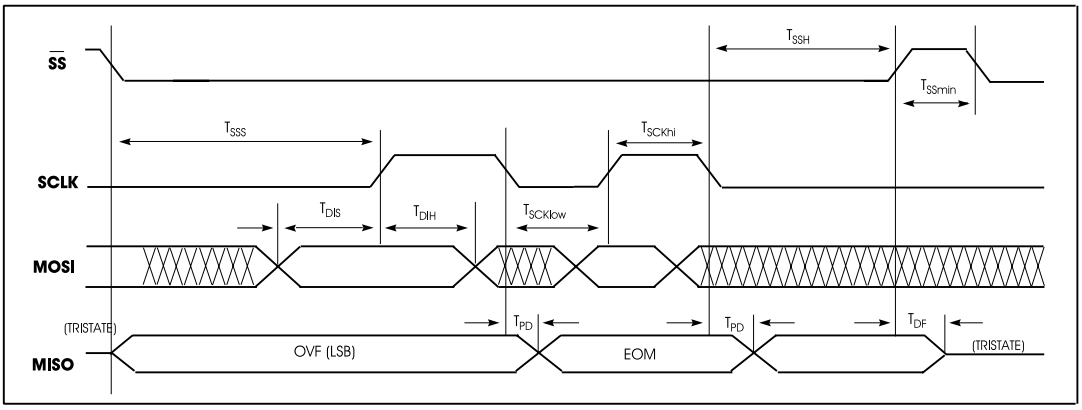


Figure 18: 8-Bit SPI Command Format

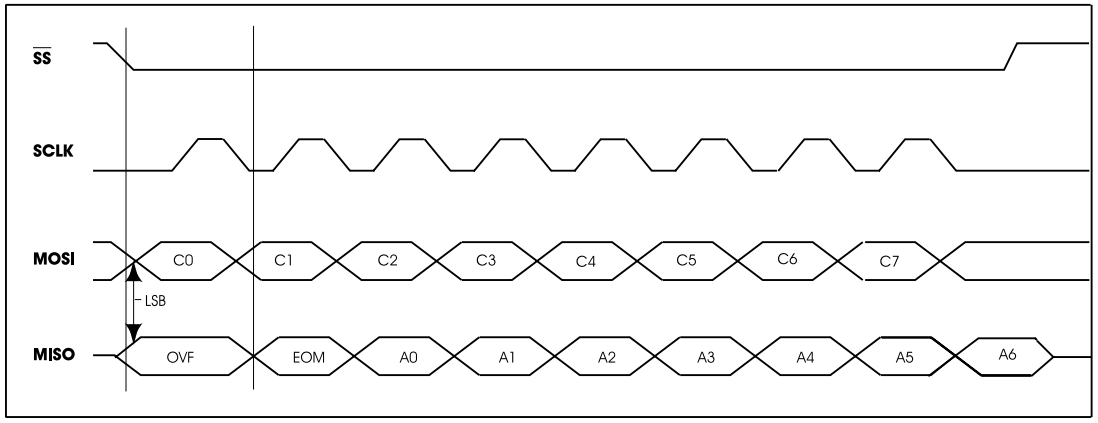


Figure 19: 24-Bit SPI Command Format

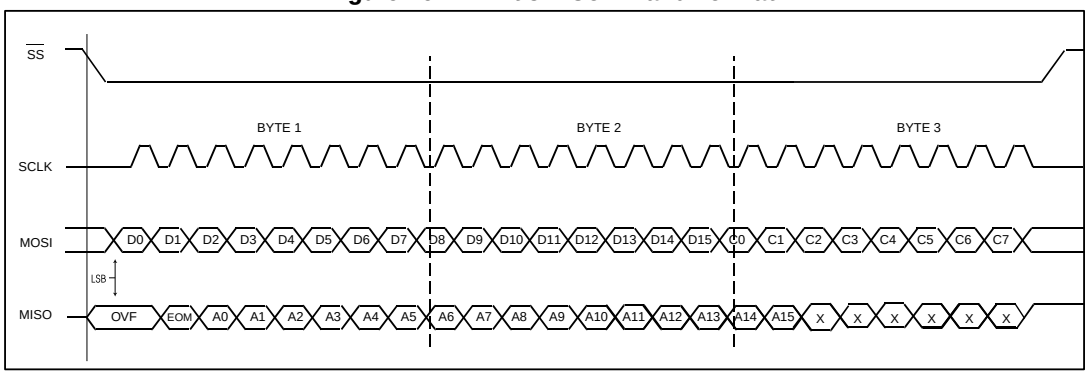
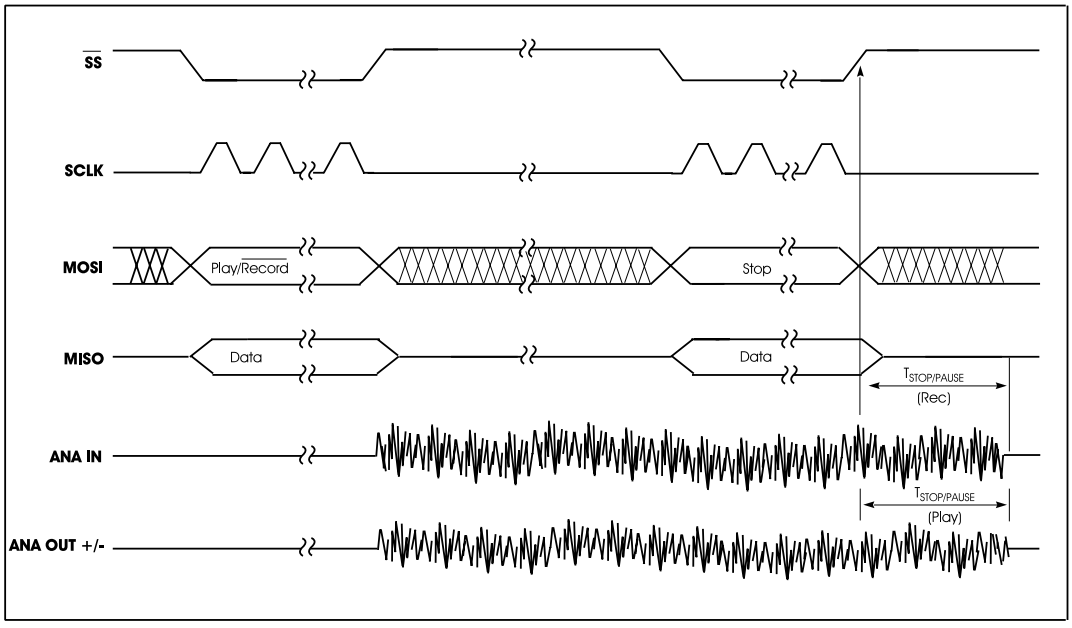


Figure 20: Playback/Record and Stop Cycle



7 DEVICE PHYSICAL DIMENSIONS

Figure 21: 28-Lead 8x13.4 mm Plastic Thin Small Outline Package (TSOP) Type I (E)

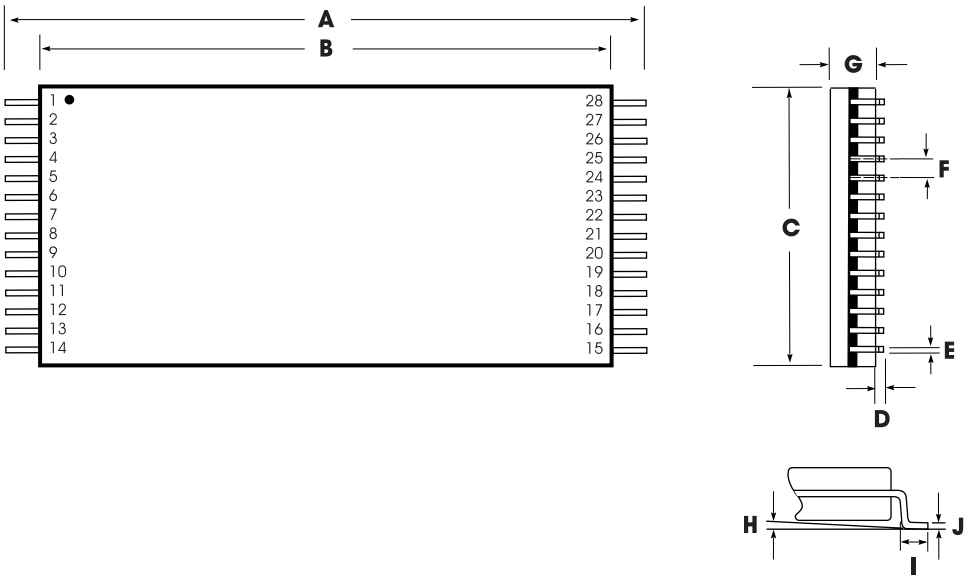


Table 18: Plastic Thin Small Outline Package (TSOP) Type I (E) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0°	3°	6°	0°	3°	6°
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 22: 28-Lead 0.600-Inch Plastic Dual Inline Package (PDIP) (P)

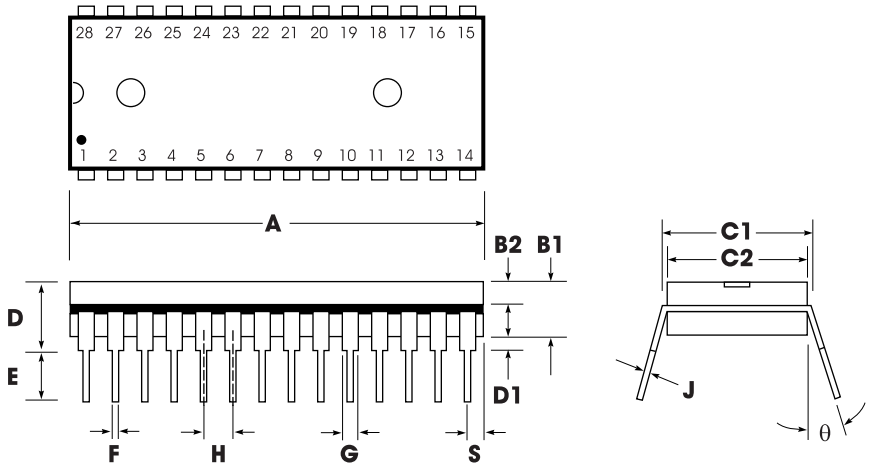


Table 19: Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
θ	0°		15°	0°		15°

Figure 23: 28-Lead 0.300-Inch Plastic Small Outline Integrated Circuit (SOIC) (S)

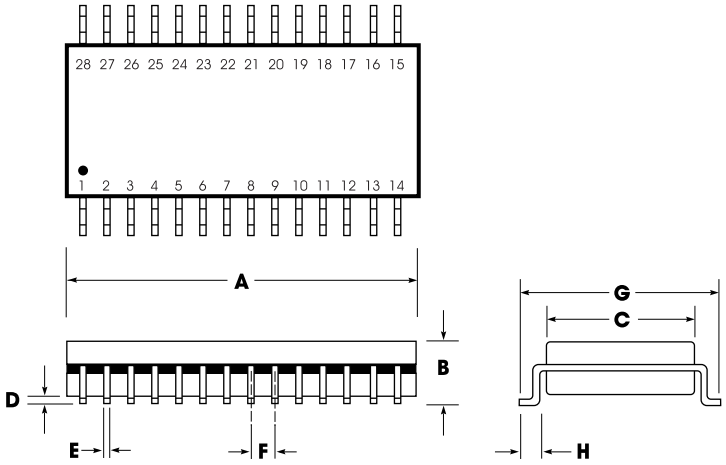
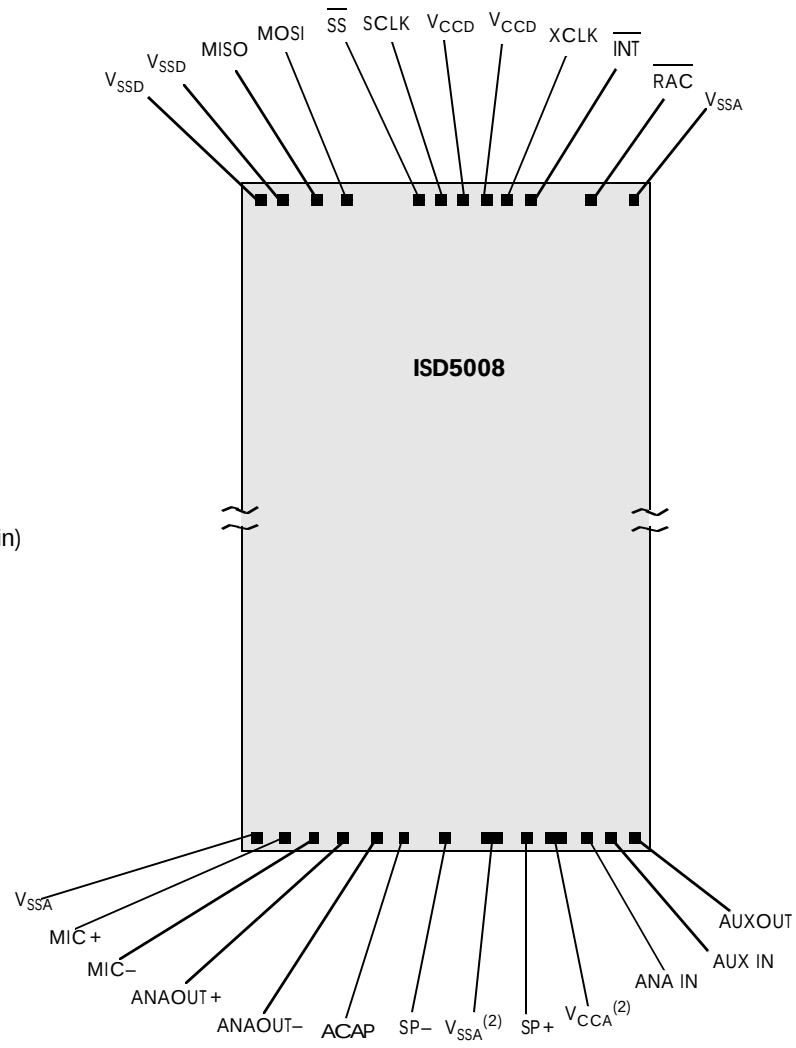


Table 20: Plastic Small Outline Integrated Circuit (SOIC) (S) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

NOTE: *Lead coplanarity to be within 0.004 inches.*

Figure 24: ISD5008 Series Bonding Physical Layout[1] (Unpackaged Die)



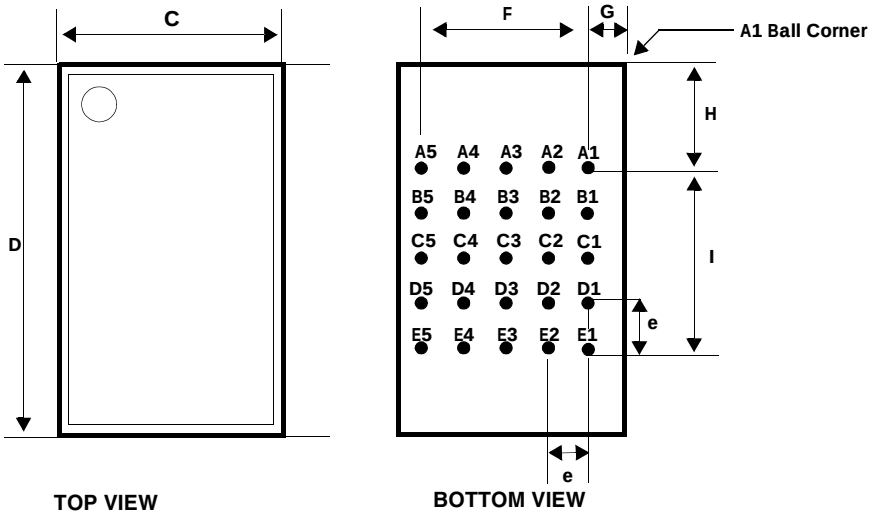
1. *The backside of die is internally connected to V_{SS}. It **MUST NOT** be connected to any other potential or damage may occur.*
2. *Double bond recommended.*
3. *This figure reflects the current die thickness. Please contact ISD as this thickness may change in the future.*

Table 21: ISD5008 Series Device Pin/Pad Designations, with Respect to Die Center (µm)

Pin	Pin Name	X Axis	Y Axis
V_{SSD}	V_{SS} Digital Power Supply	–1837.0	3623.7
V_{SSD}	V_{SS} Digital Power Supply	–1665.4	3623.7
MISO	Master In Slave Out	–1325.7	3623.7
MOSI	Master Out Slave In	–1063.8	3623.7
$\overline{SS}$	Slave Select	–198.2	3623.7
SCLK	Slave Clock	–14.8	3623.7
V_{CCD}	V_{CC} Digital Power Supply	169.4	3623.7
V_{CCD}	V_{CC} Digital Power Supply	384.8	3623.7
XCLK	External Clock Input	564.7	3623.7
$\overline{INT}$	Interrupt	794.7	3623.7
RAC	Row Address Clock	1483.7	3623.7
V_{SSA}	V_{SS} Analog Power Supply	1885.1	3623.7
V_{SSA}	V_{SS} Analog Power Supply	–1943.2	–3615.9
MIC+	Noninverting Microphone Input	–1735.4	–3615.9
MIC–	Inverting Microphone Input	–1502.9	–3615.9
ANA OUT+	Noninverting Analog Output	—1251.2	–3615.9
ANA OUT–	Inverting Analog Output	–917.0	–3615.9
ACAP	AGC/AutoMute Cap	–632.6	–3615.9
SP–	Inverting Speaker Output	–138.4	–3615.9
V_{SSA}(1)	V_{SS} Analog Power Supply	240.2	–3615.9
SP+	Noninverting Speaker Output	618.8	–3615.9
V_{CCA}(1)	V_{CC} Analog Power Supply	997.4	–3615.9
ANA IN	Analog Input	1249.9	–3615.9
AUX IN	Auxiliary Input	1515.5	–3615.9
AUX OUT	Auxiliary Output	1758.4	–3615.9

1. *Double bond recommended.*

Figure 25: SD5008 Chip Scale Package (CSP) (Z)



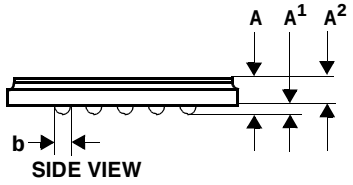


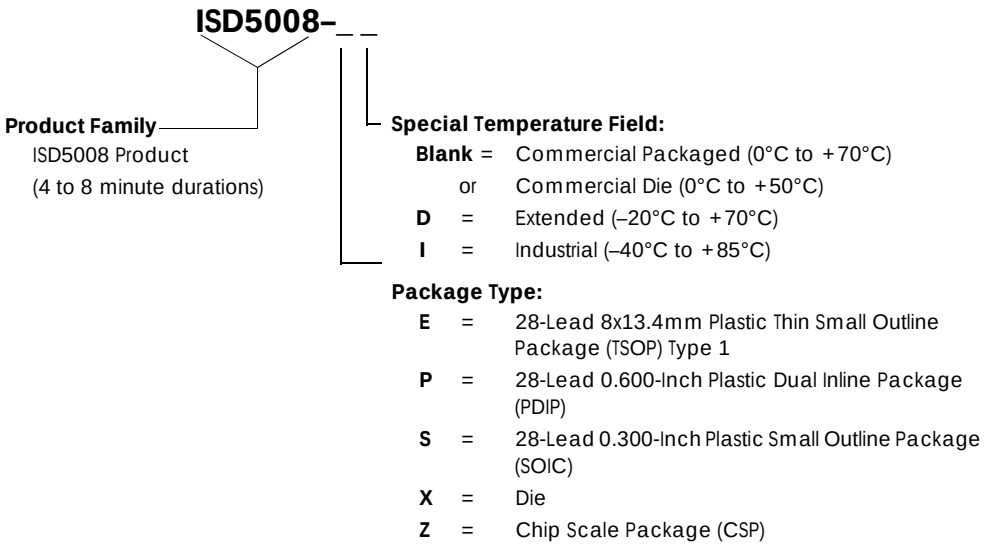
Table 22: CSP Dimensions (mm)

Symbol	Min.	Nom.	Max.
A	—	—	0.86
A^1	0.18	—	—
A^2	—	0.55	—
b	0.30	0.35	0.40
C	—	4.68	—
D	—	8.13	—
e		0.75	
F	—	3.00	—
G	—	0.84	—
H	—	2.57	—
I	—	3.00	—

PIN Name	Ball Location
MIC-	A1
ACAP	A2
V_{SSA}	A3
V_{CCA}	A4
AUX IN	A5
MIC +	B1
ANA OUT-	B2
SP-	B3
ANA IN	B4
AUX OUT	B5
V_{SSA}	C1
ANA OUT +	C2
SP +	C3
V_{CCD}	C4
V_{SSA}	C5
V_{SSD}	D1
MISO	D2
$\overline{SS}$	D3
XCLK	D4
RAC	D5
VSSD	E1
MOSI	E2
SCLK	E3
VCCD	E4
$\overline{INT}$	E5

8 ORDERING INFORMATION

ISD Part Number Description



When ordering ISD5008 series devices, please refer to the following valid part numbers.

Part Number
ISD5008E
ISD5008ED
ISD5008EI
ISD5008P
ISD5008S
ISD5008SD
ISD5008SI
ISD5008X
ISD5008Z
ISD5008ZD
ISD5008ZI

For the latest product information, access ISD's worldwide website at http://www.isd.com.

9. VERSION HISTORY

VERSION	DATE	DESCRIPTION
0	Before 2005	Initial issue
0.1	May 2005	Add revision history Update the disclaim section.

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