



# PCA9554B; PCA9554C

Low-voltage 8-bit I<sup>2</sup>C-bus and SMBus low power I/O port with interrupt, weak pull-up

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Product data sheet

## 1. General description

The PCA9554B and PCA9554C are low-voltage 8-bit General Purpose Input/Output (GPIO) expanders with interrupt and weak pull-up resistors for I<sup>2</sup>C-bus/SMBus applications. The only difference between the PCA9554B and PCA9554C is their I<sup>2</sup>C fixed address allowing a larger number of the same device on the I<sup>2</sup>C-bus with no chance of address conflict. NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs, fan control, etc.

In addition to providing a flexible set of GPIOs, the wide  $V_{DD}$  range of 1.65 V to 5.5 V allow the PCA9554B/PCA9554C to interface with next-generation microprocessors and microcontrollers where supply levels are dropping down to conserve power.

The PCA9554B/PCA9554C contain a register set of 8-bit Configuration, Input, Output, and Polarity Inversion registers.

The PCA9554B is a pin-to-pin replacement for the PCA9554, while the PCA9554C replaces the PCA9554A. Both of these devices replace other industry-standard part numbers. More fully-featured parts PCAL9554B and PCAL9554C are also available with Agile I/O features. See the respective data sheet for more details.

The PCA9554B/PCA9554C open-drain interrupt ( $\overline{INT}$ ) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$  can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C-bus. Thus, the PCA9554B/PCA9554C can remain a simple slave device.

The device outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

The power-on reset sets the registers to their default values and initializes the device state machine.

All input/output pins have weak pull-up resistors connected to them to eliminate external components.

Three hardware pins (A0, A1, A2) select the fixed I<sup>2</sup>C-bus address and allow up to eight devices to share the same I<sup>2</sup>C-bus/SMBus. The PCA9554B and PCA9554C differ only in their base I<sup>2</sup>C-bus addresses permitting a total of 16 devices on the I<sup>2</sup>C-bus, minimizing the chance for address conflict, even in the most complex system.



## 2. Features and benefits

- I<sup>2</sup>C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - ◆ 1.5  $\mu$ A (typical at 5 V  $V_{DD}$ )
  - ◆ 1.0  $\mu$ A (typical at 3.3 V  $V_{DD}$ )
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - ◆  $V_{hys} = 0.10 \times V_{DD}$  (typical)
- 5 V tolerant I/Os
- Open-drain active LOW interrupt output ( $\overline{INT}$ )
- 400 kHz Fast-mode I<sup>2</sup>C-bus
- Input/output configuration register
- Polarity inversion register
- Internal power-on reset
- Power-up with all channels configured as inputs with weak pull-up resistors
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection exceeds JESD22
  - ◆ 2000 V Human Body Model (A114-A)
  - ◆ 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP16 and HVQFN16

### 3. Ordering information

Table 1. Ordering information

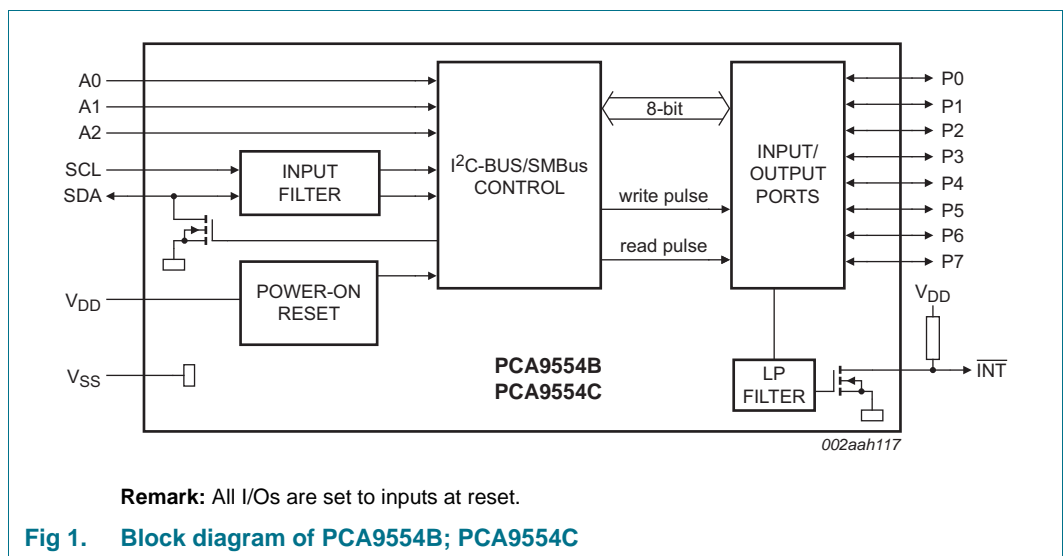
Type number	Topside mark	Package		
		Name	Description	Version
PCA9554BBS	P4B	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9554BPW	PA9554B	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9554CBS	P4C	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCA9554CPW	PA9554C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

#### 3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9554BBS	PCA9554BBSHP	HVQFN16	Reel pack, SMD, 13-inch, Turned	6000	T <sub>amb</sub> = -40 °C to +85 °C
PCA9554BPW	PCA9554BPWJ	TSSOP16	Reel pack, SMD, 13-inch	2500	T <sub>amb</sub> = -40 °C to +85 °C
PCA9554CBS	PCA9554CBSHP	HVQFN16	Reel pack, SMD, 13-inch, Turned	6000	T <sub>amb</sub> = -40 °C to +85 °C
PCA9554CPW	PCA9554CPWJ	TSSOP16	Reel pack, SMD, 13-inch	2500	T <sub>amb</sub> = -40 °C to +85 °C

### 4. Block diagram



## 5. Pinning information

### 5.1 Pinning

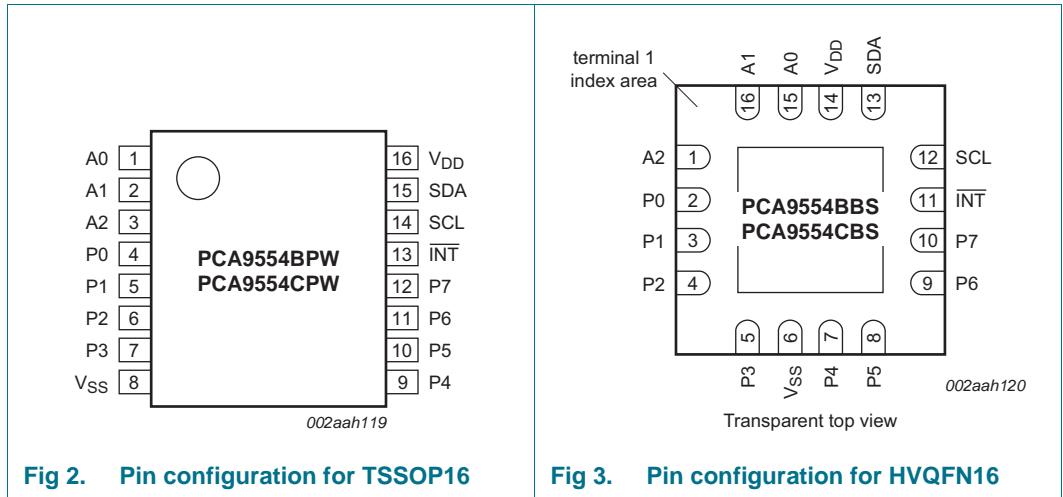


Fig 2. Pin configuration for TSSOP16

Fig 3. Pin configuration for HVQFN16

### 5.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP16	HVQFN16	
A0	1	15	address input 0
A1	2	16	address input 1
A2	3	1	address input 2
P0 <sup>[1]</sup>	4	2	Port P input/output 0
P1 <sup>[1]</sup>	5	3	Port P input/output 1
P2 <sup>[1]</sup>	6	4	Port P input/output 2
P3 <sup>[1]</sup>	7	5	Port P input/output 3
V <sub>SS</sub>	8	6 <sup>[2]</sup>	supply ground
P4 <sup>[1]</sup>	9	7	Port P input/output 4
P5 <sup>[1]</sup>	10	8	Port P input/output 5
P6 <sup>[1]</sup>	11	9	Port P input/output 6
P7 <sup>[1]</sup>	12	10	Port P input/output 7
$\overline{\text{INT}}$	13	11	interrupt output (open-drain)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V <sub>DD</sub>	16	14	supply voltage

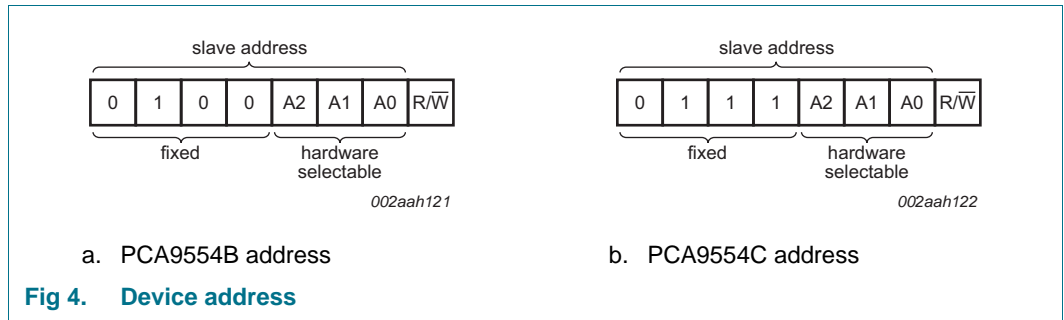
[1] All I/O are configured as input at power-on.

[2] HVQFN16 package die supply ground is connected to both the V<sub>SS</sub> pin and the exposed center pad. The V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9554B; PCA9554C”](#).

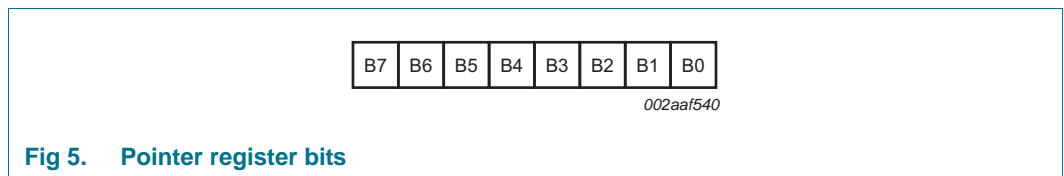
### 6.1 Device address



A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the eight possible slave addresses. The last bit of the slave address (R/W) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

### 6.2 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCA9554B/PCA9554C. The lower two bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.



**Table 4. Command byte**

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port	read byte	xxxx xxxx <sup>[1]</sup>
0	0	0	0	0	0	0	1	01h	Output port	read/write byte	1111 1111
0	0	0	0	0	0	1	0	02h	Polarity Inversion	read/write byte	0000 0000
0	0	0	0	0	0	1	1	03h	Configuration	read/write byte	1111 1111

[1] Undefined.

## 6.3 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
PCA9554B I <sup>2</sup> C-bus slave address	L	H	L	L	A2	A1	A0	R/ $\overline{W}$
PCA9554C I <sup>2</sup> C-bus slave address	L	H	H	H	A2	A1	A0	R/ $\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

## 6.4 Register descriptions

### 6.4.1 Input port register (00h)

The Input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port register is read only; writes to this register have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in [Section 7.2 "Read commands"](#).

Table 6. Input port register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

### 6.4.2 Output port register (01h)

The Output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from this register reflect the value that was written to this register, **not** the actual pin value.

Table 7. Output port register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

### 6.4.3 Polarity inversion register (02h)

The Polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with '1'), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a '0'), the corresponding port pin's original polarity is retained.

Table 8. Polarity inversion register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

6.4.4 Configuration register (03h)

The Configuration register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

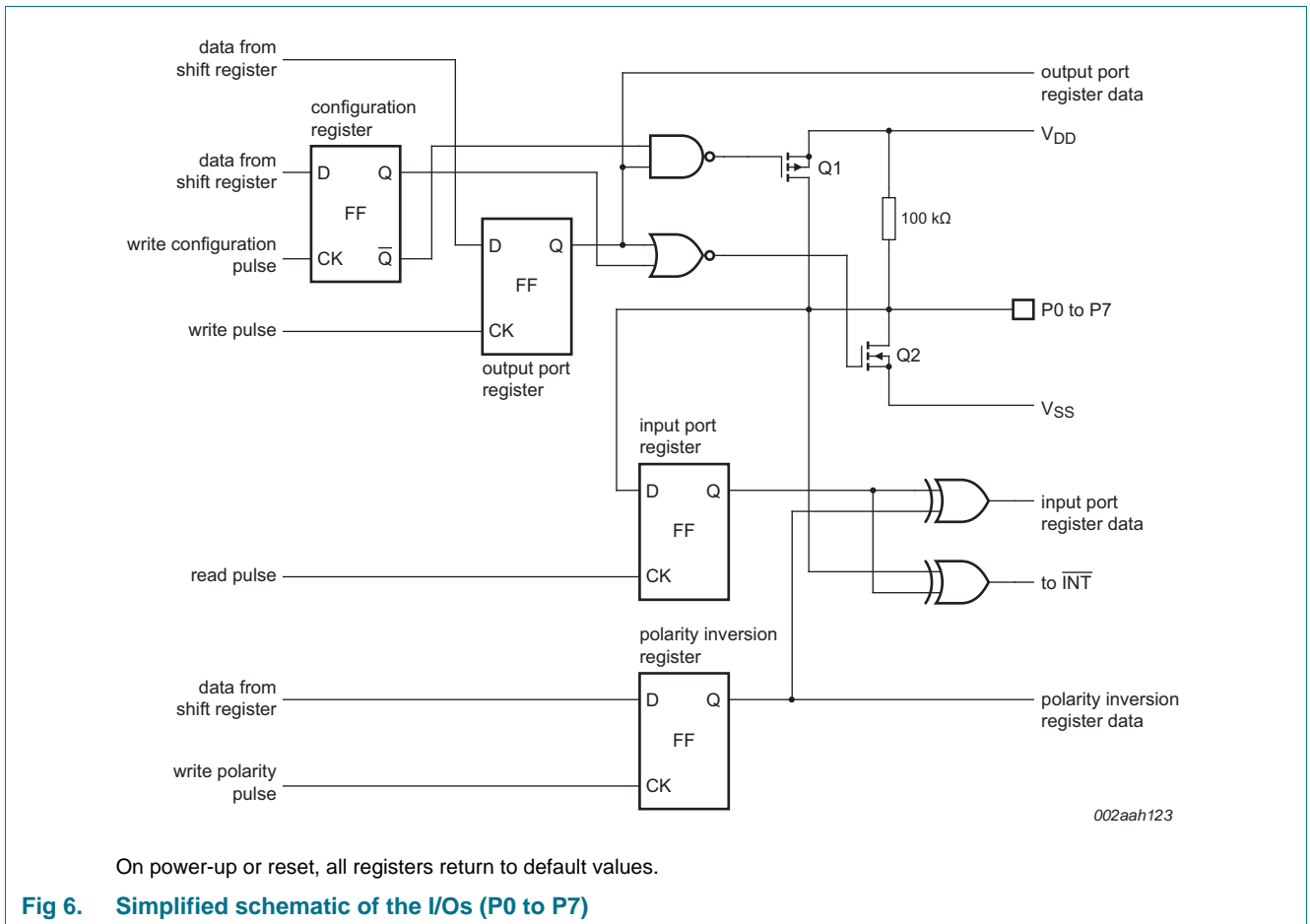
Table 9. Configuration register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

6.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V<sub>DD</sub> to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V<sub>DD</sub> or V<sub>SS</sub>. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values.

Fig 6. Simplified schematic of the I/Os (P0 to P7)

## 6.6 Power-on reset

When power (from 0 V) is applied to  $V_{DD}$ , an internal power-on reset holds the PCA9554B/PCA9554C in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that time, the reset condition is released and the PCA9554B/PCA9554C registers and I<sup>2</sup>C-bus/SMBus state machine initialize to their default states. After that,  $V_{DD}$  must be lowered to below  $V_{PORF}$  and back up to the operating voltage for a power-reset cycle. See [Section 8.2](#) “Power-on reset requirements”.

## 6.7 Interrupt output ( $\overline{INT}$ )

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time  $t_{V(INT)}$ , the signal  $\overline{INT}$  is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt (see [Figure 10](#)). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the reset of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{INT}$ .

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input port register.

The  $\overline{INT}$  output has an open-drain structure and requires a pull-up resistor to  $V_{DD}$ .  $\overline{INT}$  should be connected to the voltage source of the device that requires the interrupt information. When using the input latch feature, the input pin state is latched. The interrupt is reset only when data is read from the port that generated the interrupt. The reset occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

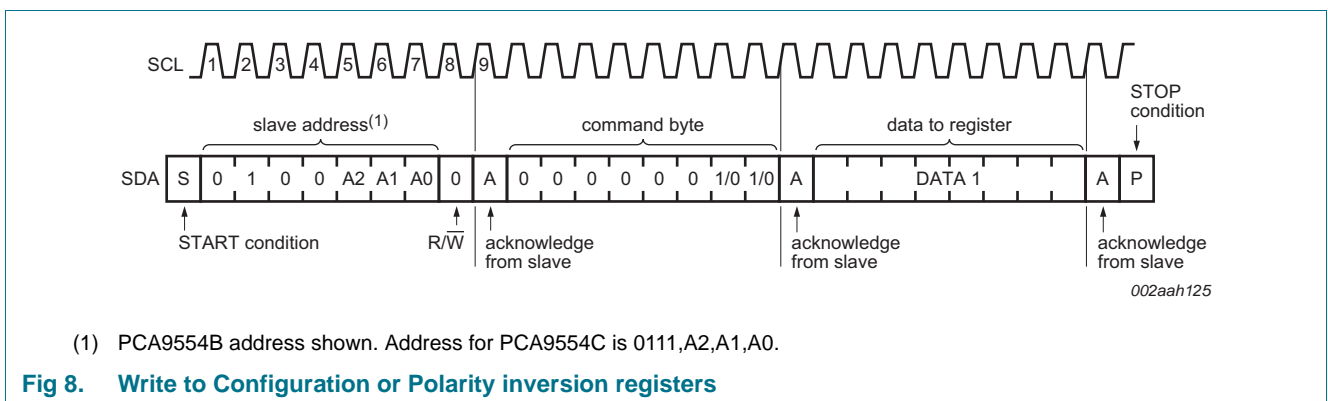
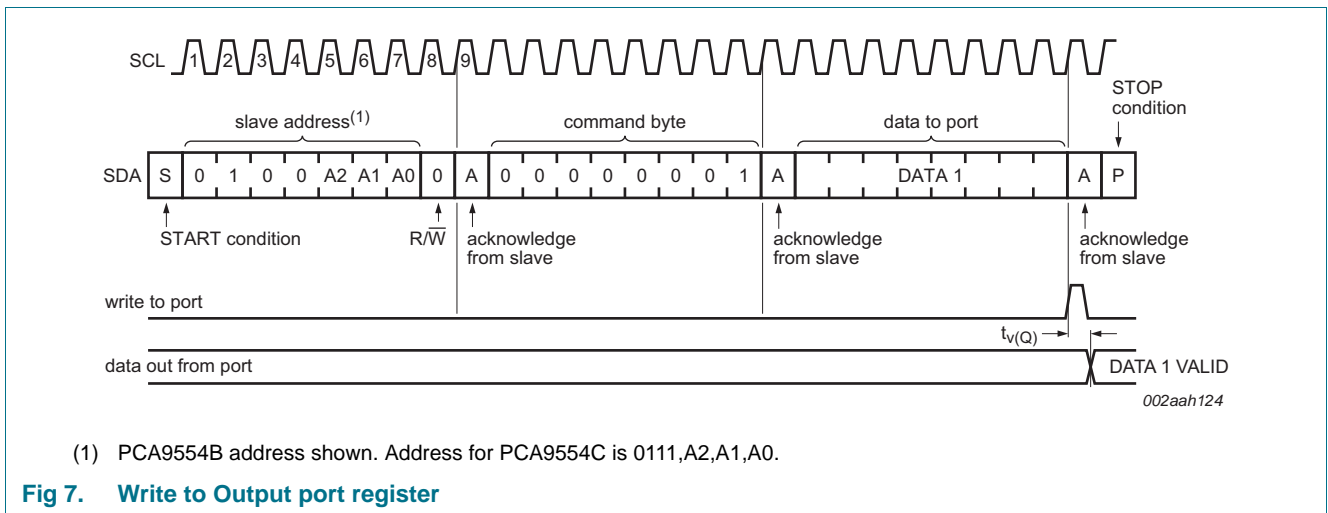


## 7. Bus transactions

The PCA9554B/PCA9554C is an I<sup>2</sup>C-bus slave device. Data is exchanged between the master and PCA9554B/PCA9554C through write and read commands using I<sup>2</sup>C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 7.1 Write commands

Data is transmitted to the PCA9554B/PCA9554C by sending the device address and setting the Least Significant Bit (LSB) to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

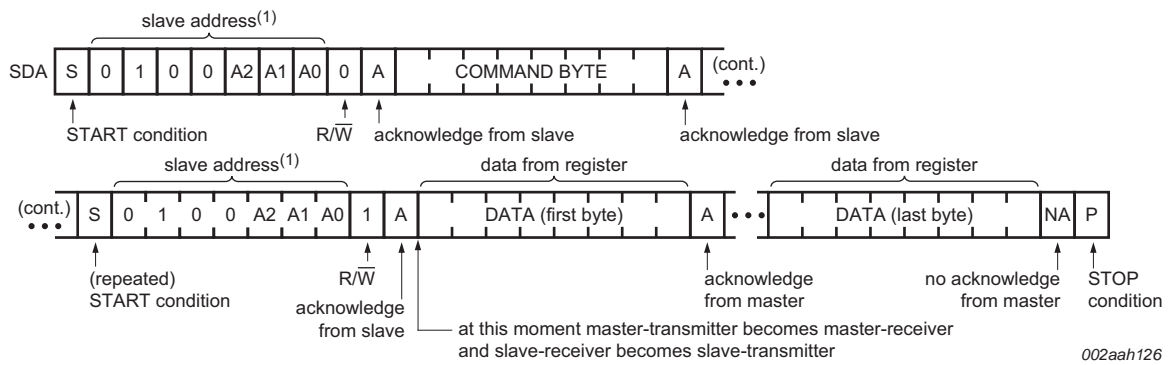


7.2 Read commands

To read data from the PCA9554B/PCA9554C, the bus master must first send the PCA9554B/PCA9554C address with the least significant bit set to a logic 0 (see Figure 4 for device address). The command byte is sent after the address and determines which register is to be accessed.

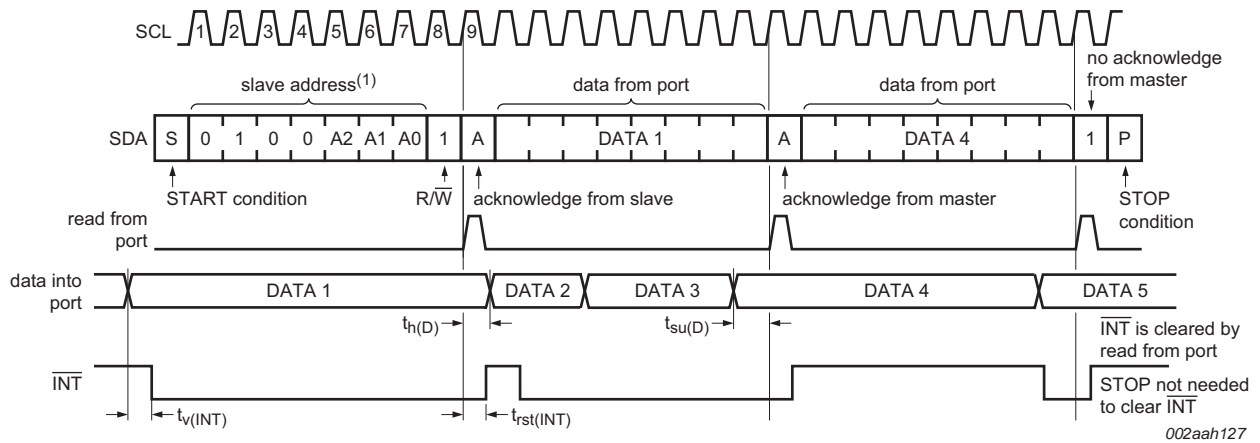
After a restart the device address is sent again, but this time the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9554B/PCA9554C (see Figure 9 and Figure 10).

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.



(1) PCA9554B address shown. Address for PCA9554C is 0111,A2,A1,A0.

Fig 9. Read from register



Transfer of data can be stopped at any time by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been programmed with 00h (read Input port register).

This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P port (see Figure 9).

(1) PCA9554B address shown. Address for PCA9554C is 0111,A2,A1,A0.

Fig 10. Read Input port register

8. Application design-in information

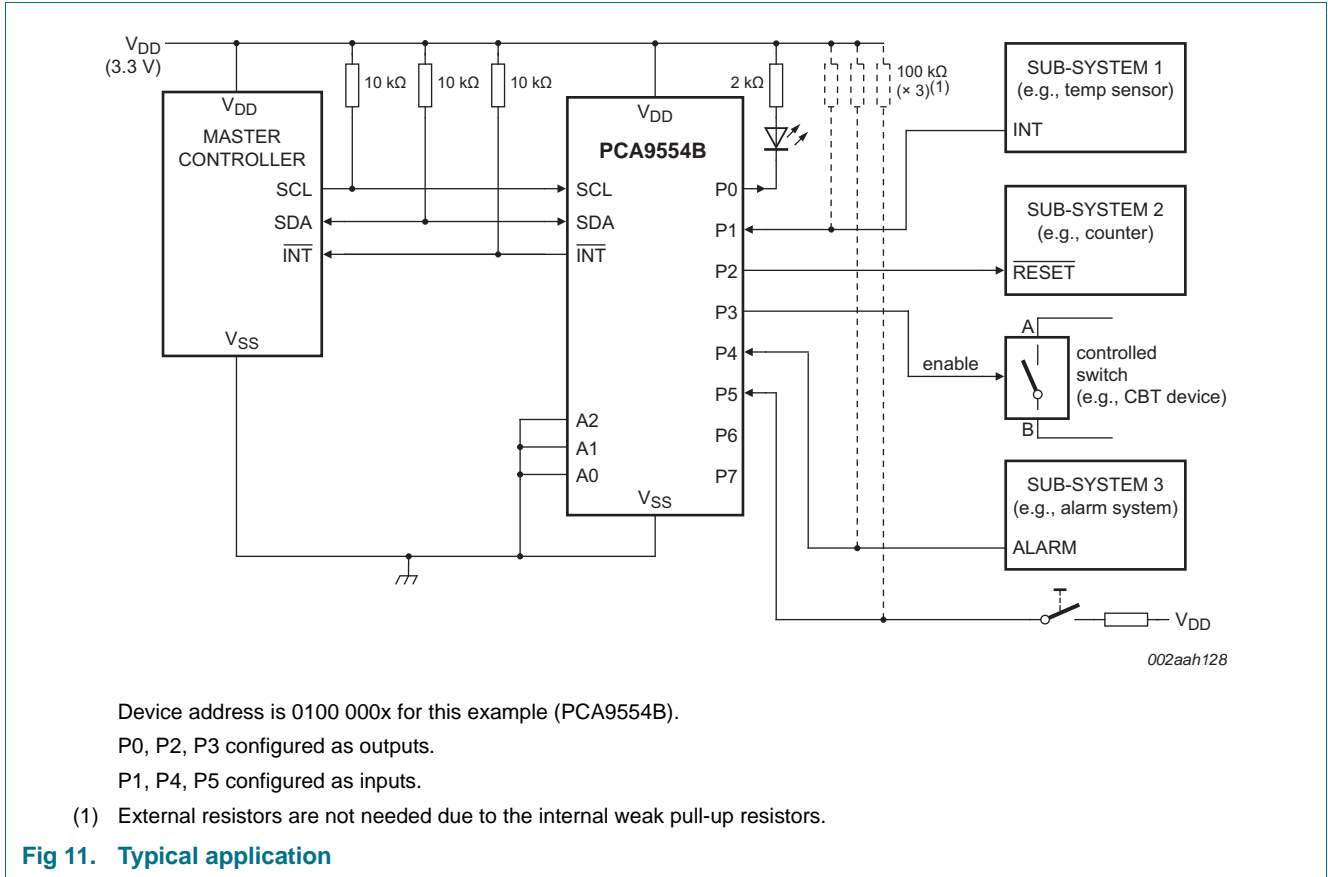
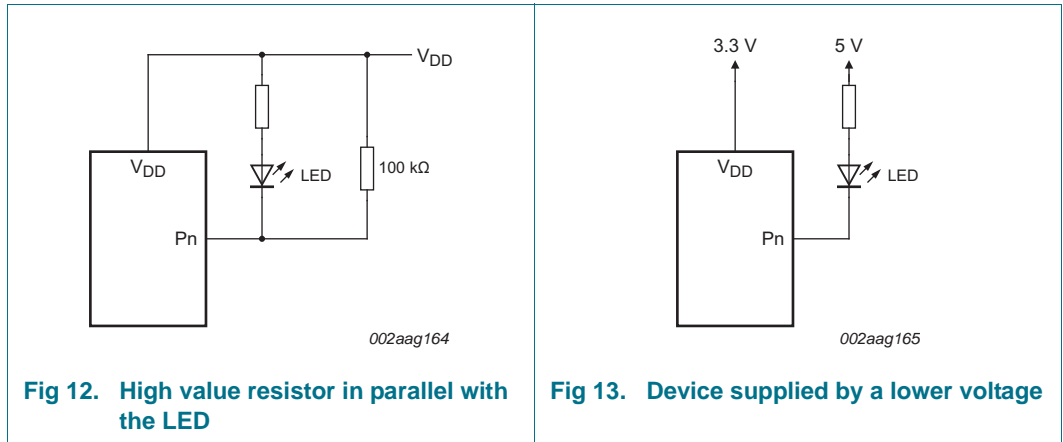


Fig 11. Typical application

8.1 Minimizing I<sub>DD</sub> when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>DD</sub> through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V<sub>I</sub> is about 1.2 V less than V<sub>DD</sub>. The supply current, I<sub>DD</sub>, increases as V<sub>I</sub> becomes lower than V<sub>DD</sub>.

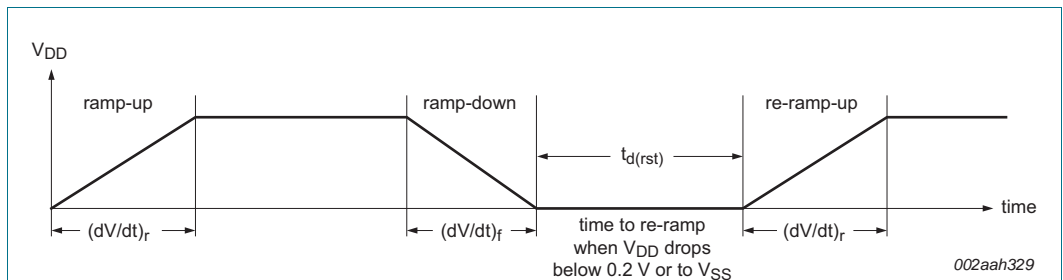
Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V<sub>DD</sub> when the LED is off. Figure 12 and Figure 13 show typical solutions to minimizing current consumption. Figure 12 shows a high value resistor in parallel with the LED. Figure 13 shows V<sub>DD</sub> less than the LED supply voltage by at least 1.2 V. However, the PCA9554B/PCA9554C needs no external resistors due to the integrated 100 kΩ pull-up resistors.



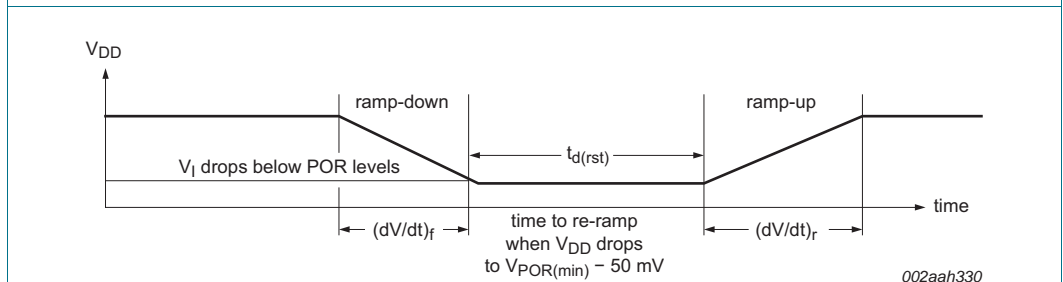
### 8.2 Power-on reset requirements

In the event of a glitch or data corruption, PCA9554B/PCA9554C can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 14](#) and [Figure 15](#).



**Fig 14. V<sub>DD</sub> is lowered below 0.2 V or 0 V and then ramped up to V<sub>DD</sub>**



**Fig 15. V<sub>DD</sub> is lowered below the POR threshold, then ramped back up to V<sub>DD</sub>**

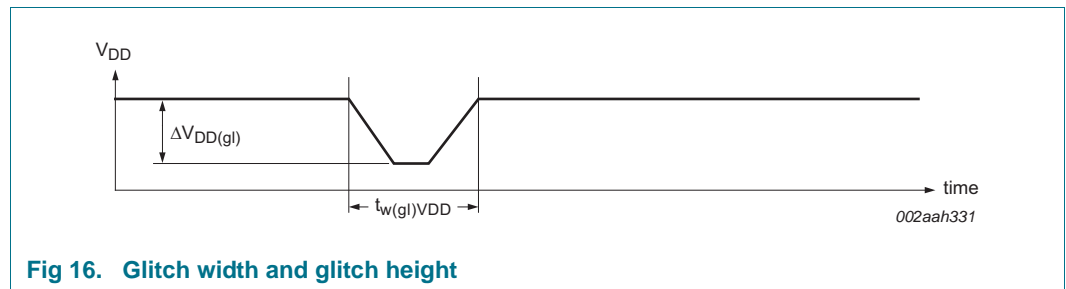
[Table 10](#) specifies the performance of the power-on reset feature for PCA9554B/PCA9554C for both types of power-on reset.

**Table 10. Recommended supply sequencing and ramp rates**  
*T<sub>amb</sub> = 25 °C (unless otherwise noted). Not tested; specified by design.*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
(dV/dt) <sub>f</sub>	fall rate of change of voltage	<a href="#">Figure 14</a>	0.1	-	2000	ms
(dV/dt) <sub>r</sub>	rise rate of change of voltage	<a href="#">Figure 14</a>	0.1	-	2000	ms
t <sub>d(rst)</sub>	reset delay time	<a href="#">Figure 14</a> ; re-ramp time when V <sub>DD</sub> drops to V <sub>SS</sub>	1	-	-	μs
		<a href="#">Figure 15</a> ; re-ramp time when V <sub>DD</sub> drops to V <sub>POR(min)</sub> - 50 mV	1	-	-	μs
ΔV <sub>DD(gl)</sub>	glitch supply voltage difference	<a href="#">Figure 16</a>	[1]	-	1.0	V
t <sub>w(gl)VDD</sub>	supply voltage glitch pulse width	<a href="#">Figure 16</a>	[2]	-	10	μs
V <sub>POR(trip)</sub>	power-on reset trip voltage	falling V <sub>DD</sub>	0.7	-	-	V
		rising V <sub>DD</sub>	-	-	1.4	V

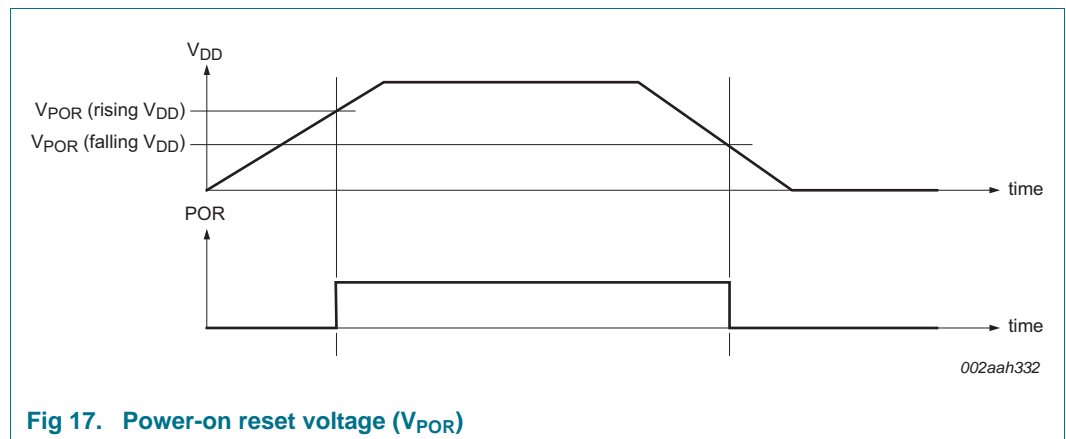
- [1] Level that V<sub>DD</sub> can glitch down to with a ramp rate of 0.4 μs/V, but not cause a functional disruption when t<sub>w(gl)VDD</sub> < 1 μs.
- [2] Glitch width that will not cause a functional disruption when ΔV<sub>DD(gl)</sub> = 0.5 × V<sub>DD</sub>.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t<sub>w(gl)VDD</sub>) and glitch height (ΔV<sub>DD(gl)</sub>) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 16](#) and [Table 10](#) provide more information on how to measure these specifications.



**Fig 16. Glitch width and glitch height**

V<sub>POR</sub> is critical to the power-on reset. V<sub>POR</sub> is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C-bus/SMBus state machine are initialized to their default states. The value of V<sub>POR</sub> differs based on the V<sub>DD</sub> being lowered to or from 0 V. [Figure 17](#) and [Table 10](#) provide more details on this specification.



**Fig 17. Power-on reset voltage (V<sub>POR</sub>)**

### 8.3 Device current consumption with internal pull-up resistors

The PCA9554B/PCA9554C integrates pull-up resistors to eliminate external components when pins are configured as inputs and pull-up resistors are required (for example, nothing is driving the inputs to the power supply rails). Since these pull-up resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The internal pull-up resistor is connected to  $V_{DD}$ , a current will flow from the  $V_{DD}$  pin through the resistor to ground when the pin is held LOW. This current will appear as additional  $I_{DD}$  upsetting any current consumption measurements.

The pull-up resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 k $\Omega$  with a nominal 100 k $\Omega$  value. Any current flow through these resistors is additive by the number of pins held LOW and the current can be calculated by Ohm's law. See [Figure 21](#) for a graph of supply current versus the number of pull-up resistors.

## 9. Limiting values

**Table 11. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+6.5	V
V <sub>I</sub>	input voltage		[1] -0.5	+6.5	V
V <sub>O</sub>	output voltage		[1] -0.5	+6.5	V
I <sub>IK</sub>	input clamping current	A0, A1, A2, SCL; V <sub>I</sub> < 0 V	-	±20	mA
I <sub>OK</sub>	output clamping current	$\overline{\text{INT}}$ ; V <sub>O</sub> < 0 V	-	±20	mA
I <sub>IOK</sub>	input/output clamping current	P port; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>DD</sub>	-	±20	mA
		SDA; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>DD</sub>	-	±20	mA
I <sub>OL</sub>	LOW-level output current	continuous; I/O port	-	50	mA
		continuous; SDA, $\overline{\text{INT}}$	-	25	mA
I <sub>OH</sub>	HIGH-level output current	continuous; P port	-	25	mA
I <sub>DD</sub>	supply current		-	160	mA
I <sub>SS</sub>	ground supply current		-	200	mA
P <sub>tot</sub>	total power dissipation		-	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j(max)</sub>	maximum junction temperature		-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 10. Recommended operating conditions

**Table 12. Operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		1.65	5.5	V
V <sub>IH</sub>	HIGH-level input voltage	SCL, SDA	0.7 × V <sub>DD</sub>	5.5	V
		A0, A1, A2, P port	0.7 × V <sub>DD</sub>	5.5	V
V <sub>IL</sub>	LOW-level input voltage	SCL, SDA	-0.5	0.3 × V <sub>DD</sub>	V
		A0, A1, A2, P port	-0.5	0.3 × V <sub>DD</sub>	V
I <sub>OH</sub>	HIGH-level output current	P port	-	10	mA
I <sub>OL</sub>	LOW-level output current	P port	-	25	mA
T <sub>amb</sub>	ambient temperature	operating in free air	-40	+85	°C

## 11. Thermal characteristics

**Table 13. Thermal characteristics**

Symbol	Parameter	Conditions	Max	Unit
Z <sub>th(j-a)</sub>	transient thermal impedance from junction to ambient	HVQFN16 package	[1] 53	K/W
		TSSOP16 package	[1] 108	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

## 12. Static characteristics

**Table 14. Static characteristics**
 $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}; V_{DD} = 1.65\text{ V to }5.5\text{ V}; \text{ unless otherwise specified.}$ 

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{IK}$	input clamping voltage	$I_I = -18\text{ mA}$	-1.2	-	-	V
$V_{POR}$	power-on reset voltage	$V_I = V_{DD}$ or $V_{SS}$ ; $I_O = 0\text{ mA}$	-	1.1	1.4	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}; V_{DD} = 1.65\text{ V to }5.5\text{ V}$				
		SDA	3	-	-	mA
		$\overline{\text{INT}}$	3	15 <sup>[2]</sup>	-	mA
		P port				
		$V_{OL} = 0.5\text{ V}; V_{DD} = 1.65\text{ V}$	<sup>[3]</sup> 8	10	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 1.65\text{ V}$	<sup>[3]</sup> 10	13	-	mA
		$V_{OL} = 0.5\text{ V}; V_{DD} = 2.3\text{ V}$	<sup>[3]</sup> 8	10	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 2.3\text{ V}$	<sup>[3]</sup> 10	13	-	mA
		$V_{OL} = 0.5\text{ V}; V_{DD} = 3.0\text{ V}$	<sup>[3]</sup> 8	14	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 3.0\text{ V}$	<sup>[3]</sup> 10	19	-	mA
$V_{OH}$	HIGH-level output voltage	P port				
		$I_{OH} = -8\text{ mA}; V_{DD} = 1.65\text{ V}$	<sup>[4]</sup> 1.2	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 1.65\text{ V}$	<sup>[4]</sup> 1.1	-	-	V
		$I_{OH} = -8\text{ mA}; V_{DD} = 2.3\text{ V}$	<sup>[4]</sup> 1.8	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 2.3\text{ V}$	<sup>[4]</sup> 1.7	-	-	V
		$I_{OH} = -8\text{ mA}; V_{DD} = 3.0\text{ V}$	<sup>[4]</sup> 2.6	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 3.0\text{ V}$	<sup>[4]</sup> 2.5	-	-	V
		$I_{OH} = -8\text{ mA}; V_{DD} = 4.75\text{ V}$	<sup>[4]</sup> 4.1	-	-	V
$I_{OH} = -10\text{ mA}; V_{DD} = 4.75\text{ V}$	<sup>[4]</sup> 4.0	-	-	V		
$I_I$	input current	$V_{DD} = 1.65\text{ V to }5.5\text{ V}$				
		SCL, SDA; $V_I = V_{DD}$ or $V_{SS}$	-	-	0.1	$\mu\text{A}$
		A0, A1, A2; $V_I = V_{DD}$ or $V_{SS}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{IH}$	HIGH-level input current	P port; $V_I = V_{DD}$ ; $V_{DD} = 1.65\text{ V to }5.5\text{ V}$	-	-	1	$\mu\text{A}$
$I_{IL}$	LOW-level input current	P port; $V_I = V_{SS}$ ; $V_{DD} = 1.65\text{ V to }5.5\text{ V}$	-	-	-100	$\mu\text{A}$



**Table 14. Static characteristics ...continued**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{DD} = 1.65\text{ V}$  to  $5.5\text{ V}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
I <sub>DD</sub>	supply current	SDA, P port, A0, A1, A2; V <sub>I</sub> on SCL, SDA = V <sub>DD</sub> or V <sub>SS</sub> ; V <sub>I</sub> on P port and A0, A1, A2 = V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 400 kHz					
		V <sub>DD</sub> = 3.6 V to 5.5 V	-	10	25	μA	
		V <sub>DD</sub> = 2.3 V to 3.6 V	-	6.5	15	μA	
		V <sub>DD</sub> = 1.65 V to 2.3 V	-	4	9	μA	
		SCL, SDA, P port, A0, A1, A2; V <sub>I</sub> on SCL, SDA = V <sub>DD</sub> or V <sub>SS</sub> ; V <sub>I</sub> on P port and A0, A1, A2 = V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 0 kHz					
		V <sub>DD</sub> = 3.6 V to 5.5 V	-	1.5	7	μA	
		V <sub>DD</sub> = 2.3 V to 3.6 V	-	1	3.2	μA	
		V <sub>DD</sub> = 1.65 V to 2.3 V	-	0.5	1.7	μA	
		Active mode; P port, A0, A1, A2; V <sub>I</sub> on P port and A0, A1, A2 = V <sub>DD</sub> ; I <sub>O</sub> = 0 mA; I/O = inputs; f <sub>SCL</sub> = 400 kHz, continuous register read					
		V <sub>DD</sub> = 3.6 V to 5.5 V	-	60	125	μA	
		V <sub>DD</sub> = 2.3 V to 3.6 V	-	40	75	μA	
		V <sub>DD</sub> = 1.65 V to 2.3 V	-	20	45	μA	
ΔI <sub>DD</sub>	additional quiescent supply current	SCL, SDA; one input at V <sub>DD</sub> - 0.6 V, other inputs at V <sub>DD</sub> or V <sub>SS</sub> ; V <sub>DD</sub> = 1.65 V to 5.5 V	-	-	25	μA	
		P port, A0, A1, A2; one input at V <sub>DD</sub> - 0.6 V, other inputs at V <sub>DD</sub> or V <sub>SS</sub> ; V <sub>DD</sub> = 1.65 V to 5.5 V	-	-	80	μA	
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; V <sub>DD</sub> = 1.65 V to 5.5 V	-	6	7	pF	
C <sub>io</sub>	input/output capacitance	V <sub>I/O</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; V <sub>DD</sub> = 1.65 V to 5.5 V	-	7	8	pF	
		V <sub>I/O</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; V <sub>DD</sub> = 1.65 V to 5.5 V	-	7.5	8.5	pF	
R <sub>pu(int)</sub>	internal pull-up resistance	input/output	50	100	150	kΩ	

- [1] For I<sub>DD</sub>, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V V<sub>DD</sub>) and T<sub>amb</sub> = 25 °C. Except for I<sub>DD</sub>, the typical values are at V<sub>DD</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
- [2] Typical value for T<sub>amb</sub> = 25 °C. V<sub>OL</sub> = 0.4 V and V<sub>DD</sub> = 3.3 V. Typical value for V<sub>DD</sub> < 2.5 V, V<sub>OL</sub> = 0.6 V.
- [3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.
- [4] The total current sourced by all I/Os must be limited to 85 mA.

12.1 Typical characteristics

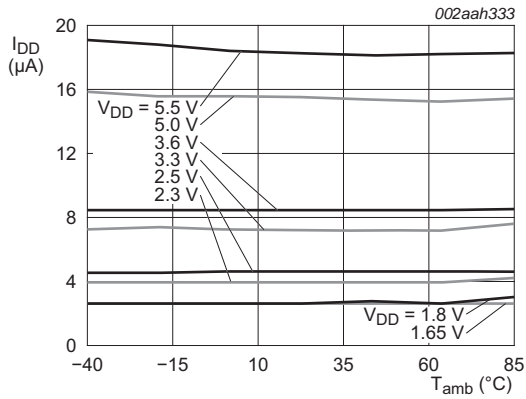


Fig 18. Supply current versus ambient temperature

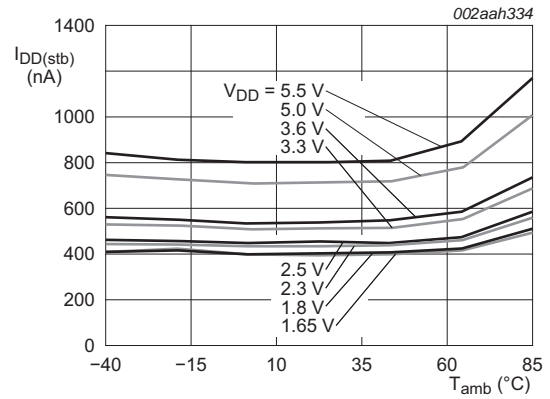


Fig 19. Standby supply current versus ambient temperature

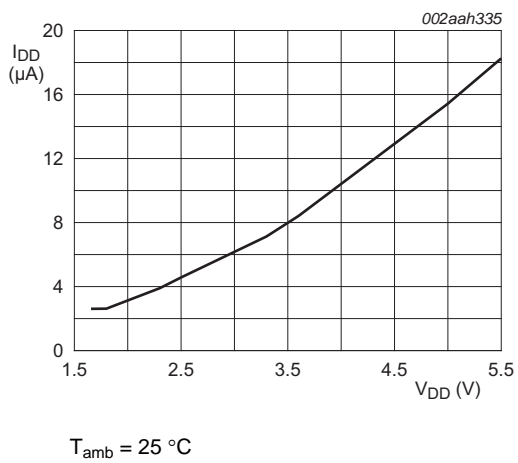


Fig 20. Supply current versus supply voltage

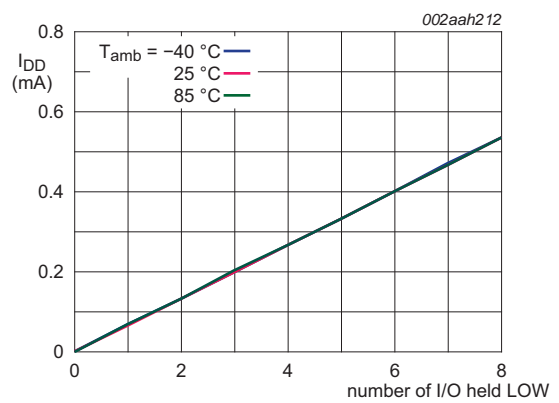
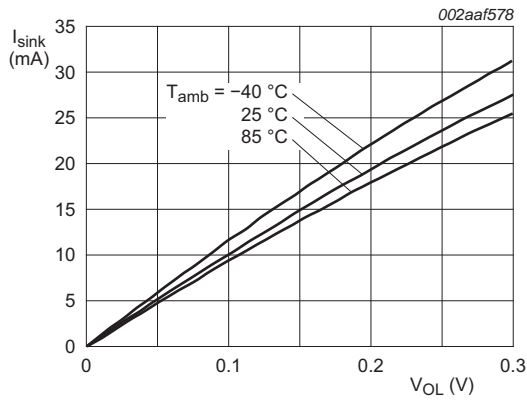
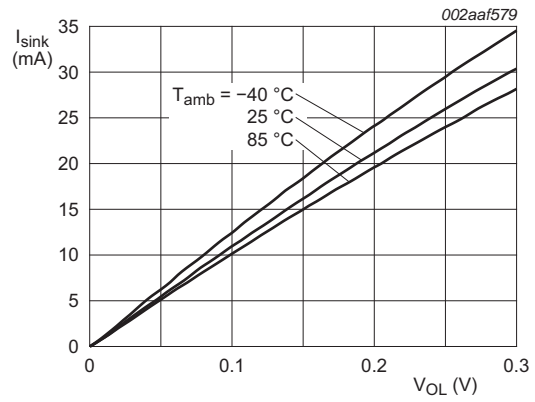


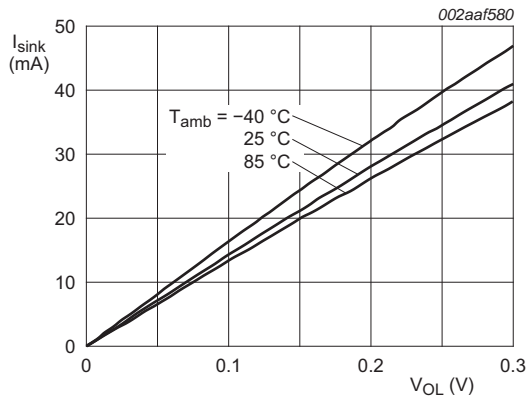
Fig 21. Supply current versus number of I/O held LOW



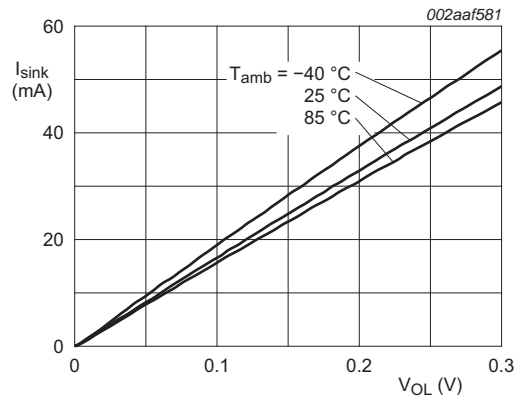
a.  $V_{DD} = 1.65\text{ V}$



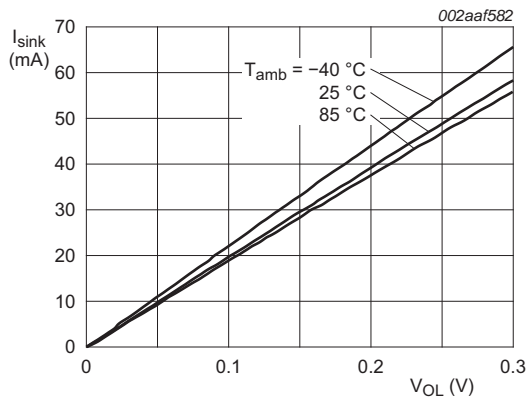
b.  $V_{DD} = 1.8\text{ V}$



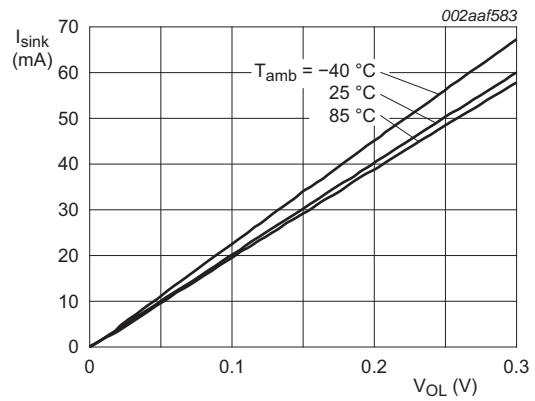
c.  $V_{DD} = 2.5\text{ V}$



d.  $V_{DD} = 3.3\text{ V}$

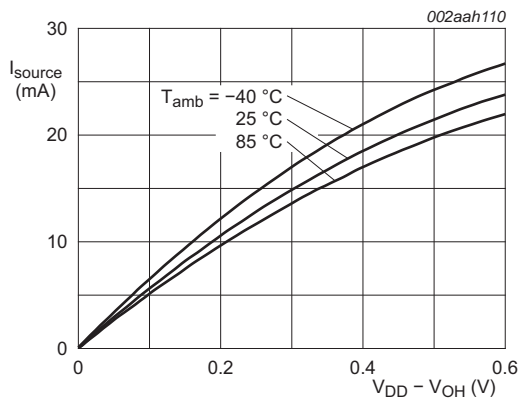


e.  $V_{DD} = 5.0\text{ V}$

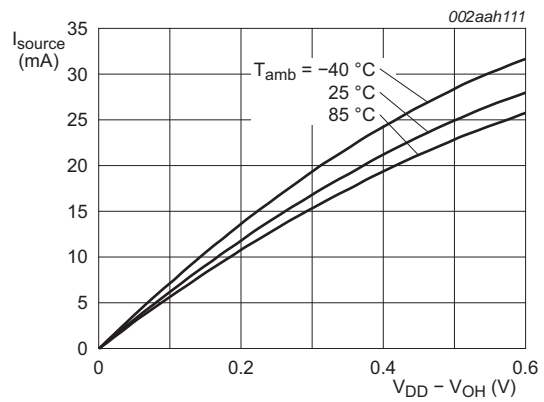


f.  $V_{DD} = 5.5\text{ V}$

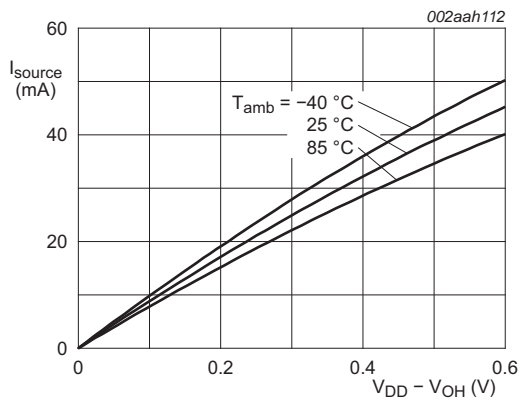
Fig 22. I/O sink current versus LOW-level output voltage



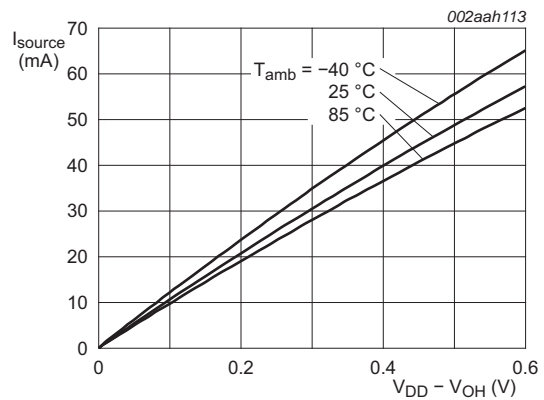
a.  $V_{DD} = 1.65\text{ V}$



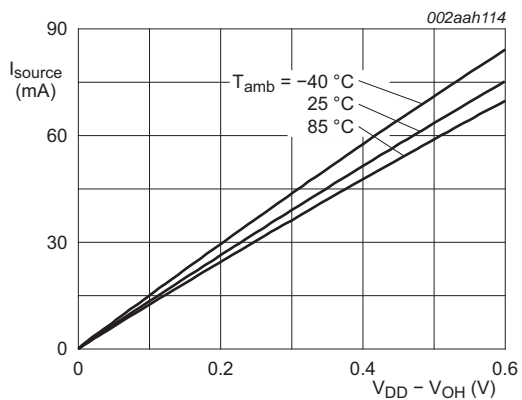
b.  $V_{DD} = 1.8\text{ V}$



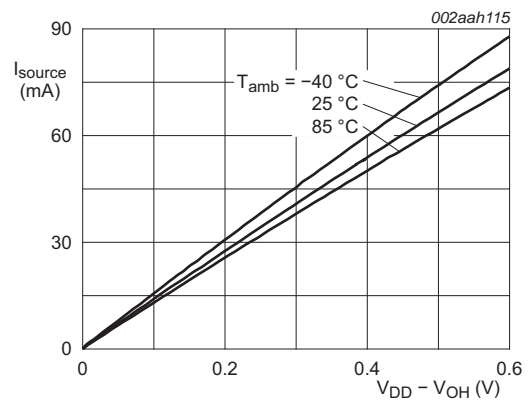
c.  $V_{DD} = 2.5\text{ V}$



d.  $V_{DD} = 3.3\text{ V}$

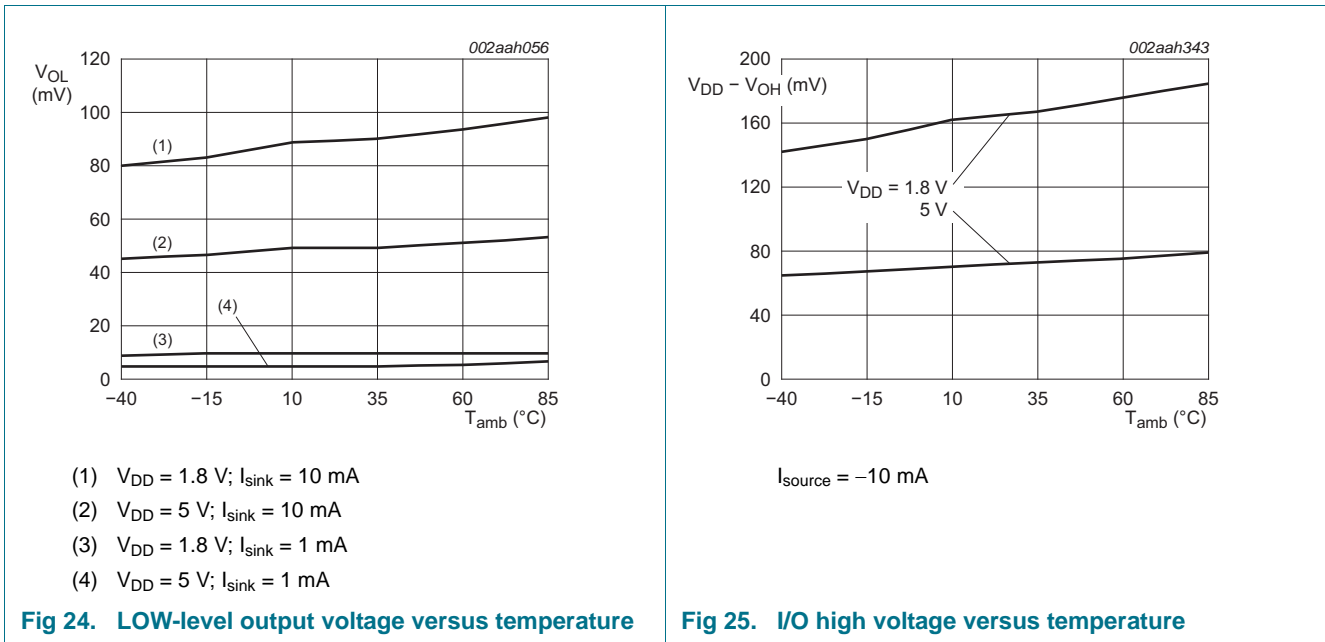


e.  $V_{DD} = 5.0\text{ V}$



f.  $V_{DD} = 5.5\text{ V}$

Fig 23. I/O source current versus HIGH-level output voltage



### 13. Dynamic characteristics

**Table 15. I<sup>2</sup>C-bus interface timing requirements**

Over recommended operating free air temperature range, unless otherwise specified. See [Figure 26](#).

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	kHz
t <sub>HIGH</sub>	HIGH period of the SCL clock		4	-	0.6	-	μs
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	μs
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	ns
t <sub>HD;DAT</sub>	data hold time		0	-	0	-	ns
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	20	300	ns
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	20 × (V <sub>DD</sub> / 5.5 V)	300	ns
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		4	-	0.6	-	μs
t <sub>SU;STO</sub>	set-up time for STOP condition		4	-	0.6	-	μs
t <sub>VD;DAT</sub>	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	μs
t <sub>VD;ACK</sub>	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	μs

**Table 16. Switching characteristics**

Over recommended operating free air temperature range; C<sub>L</sub> ≤ 100 pF; unless otherwise specified. See [Figure 26](#).

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
t <sub>v(INT)</sub>	valid time on pin $\overline{\text{INT}}$	from P port to $\overline{\text{INT}}$	-	1	-	1	μs
t <sub>rst(INT)</sub>	reset time on pin $\overline{\text{INT}}$	from SCL to $\overline{\text{INT}}$	-	1	-	1	μs
t <sub>v(Q)</sub>	data output valid time	from SCL to P port	-	400	-	400	ns
t <sub>su(D)</sub>	data input set-up time	from P port to SCL	0	-	0	-	ns
t <sub>h(D)</sub>	data input hold time	from P port to SCL	300	-	300	-	ns

14. Parameter measurement information

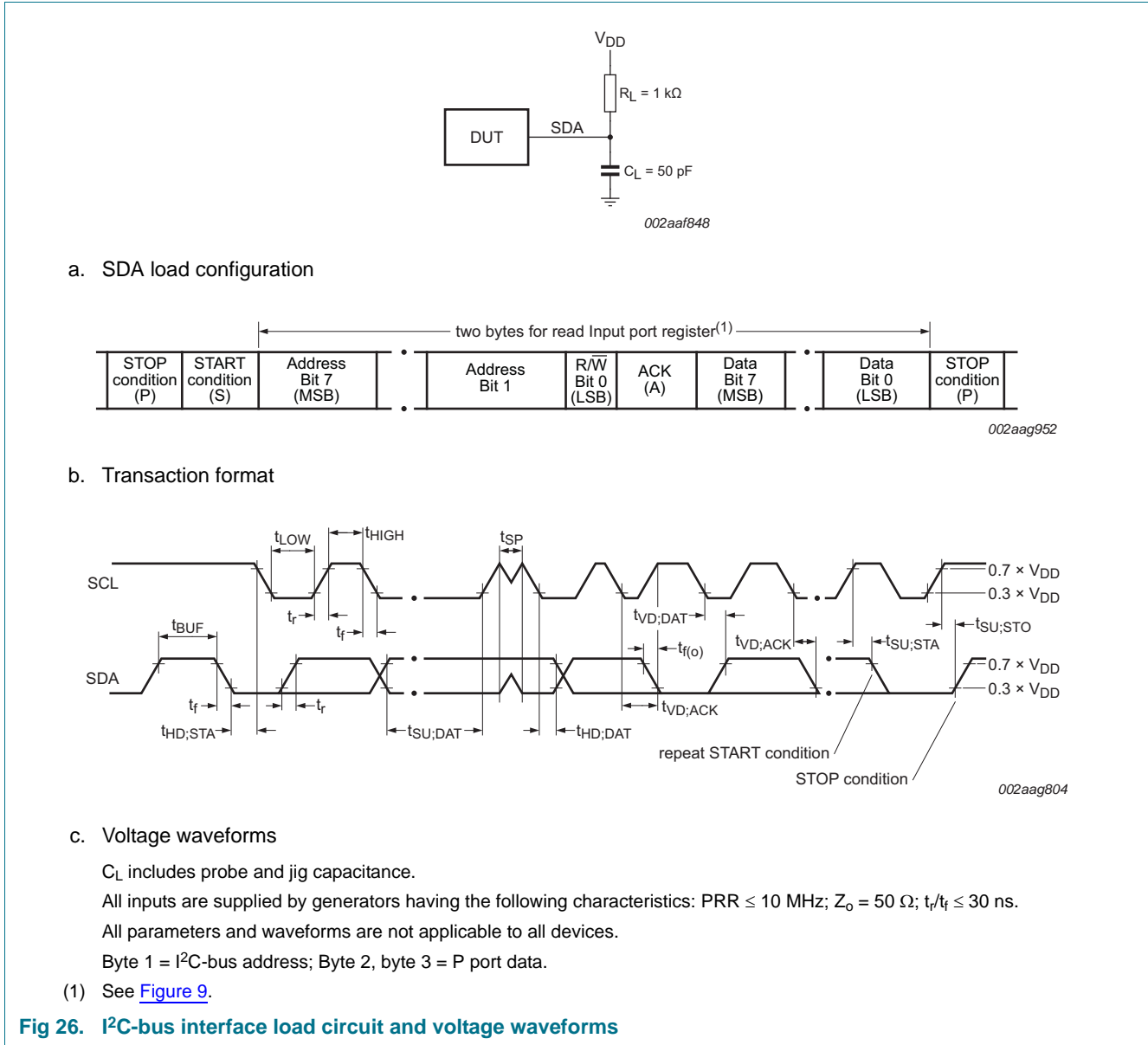
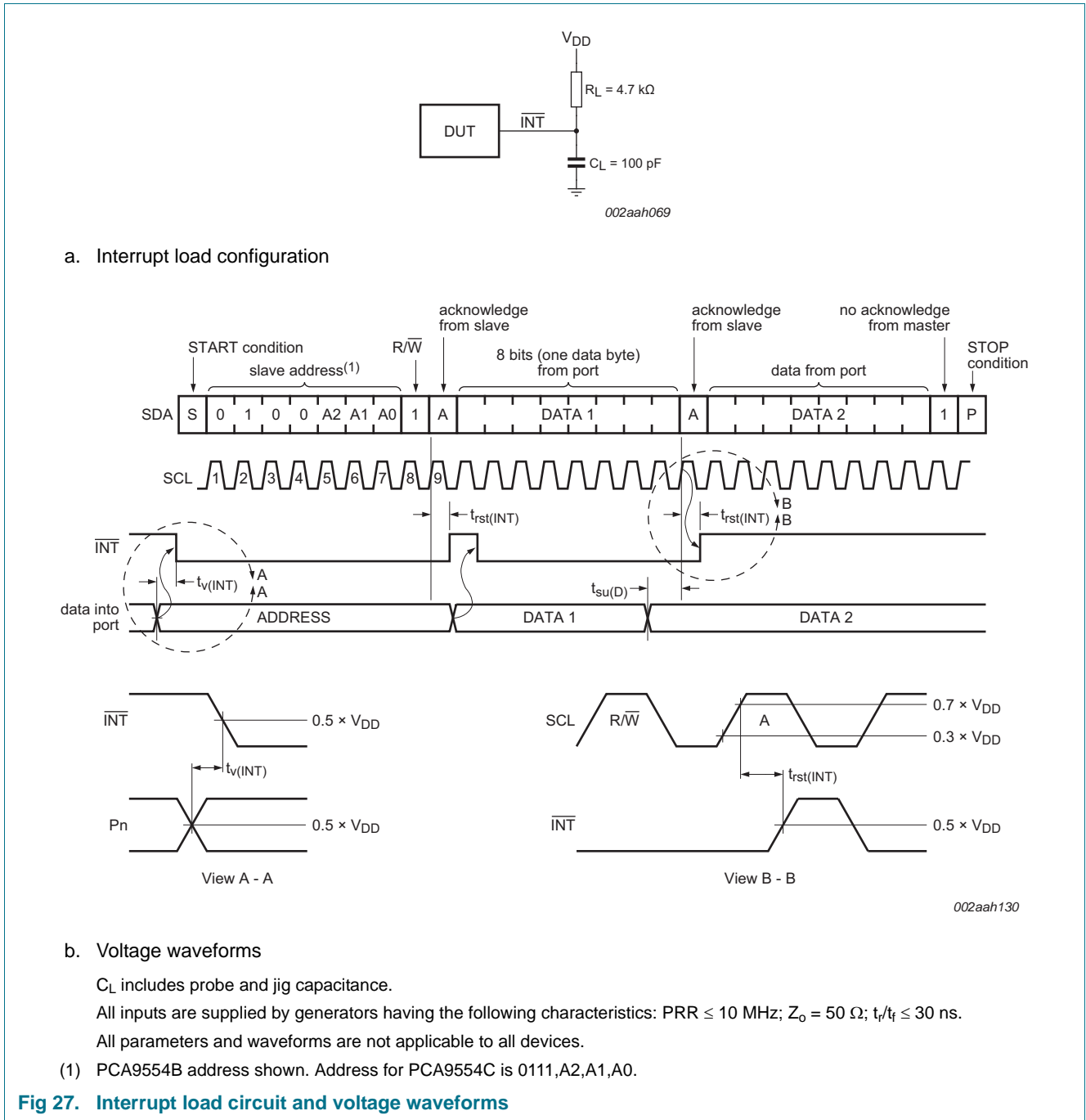
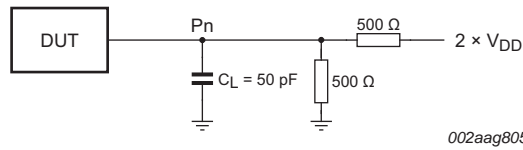


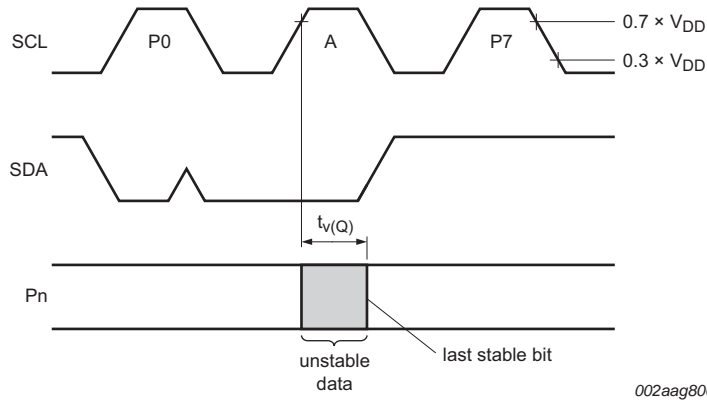
Fig 26. I<sup>2</sup>C-bus interface load circuit and voltage waveforms



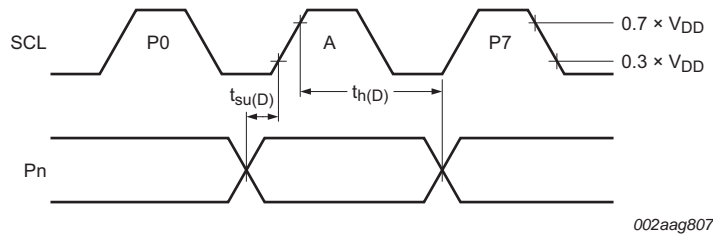




a. P port load configuration



b. Write mode ( $\overline{R/\overline{W}} = 0$ )



c. Read mode ( $\overline{R/\overline{W}} = 1$ )

$C_L$  includes probe and jig capacitance.

$t_{V(Q)}$  is measured from  $0.7 \times V_{DD}$  on SCL to 50 % I/O ( $P_n$ ) output.

All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz;  $Z_o = 50 \Omega$ ;  $t_r/t_f \leq 30$  ns.

The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig 28. P port load circuit and voltage waveforms

15. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

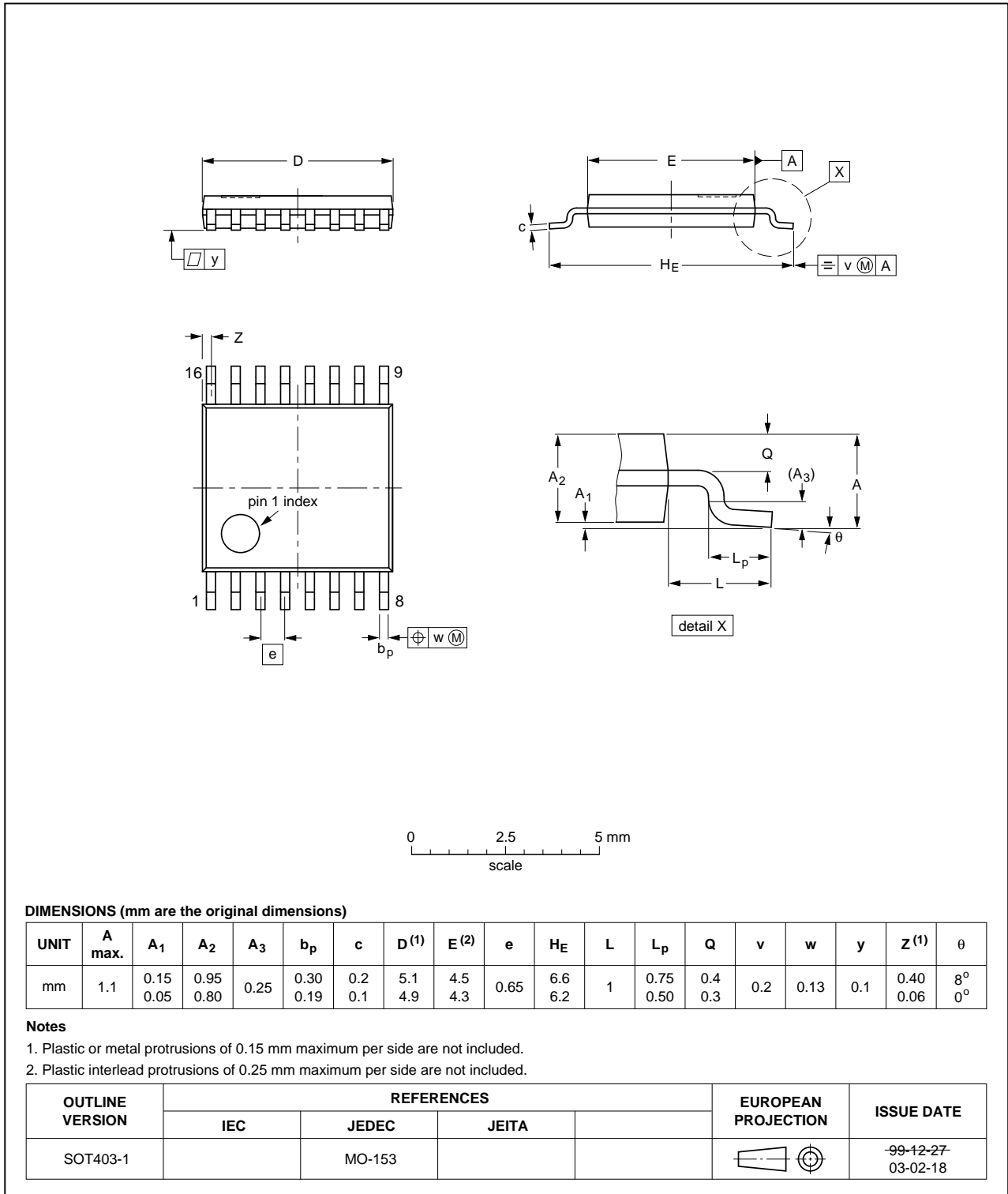


Fig 29. Package outline SOT403-1 (TSSOP16)

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm

SOT758-1

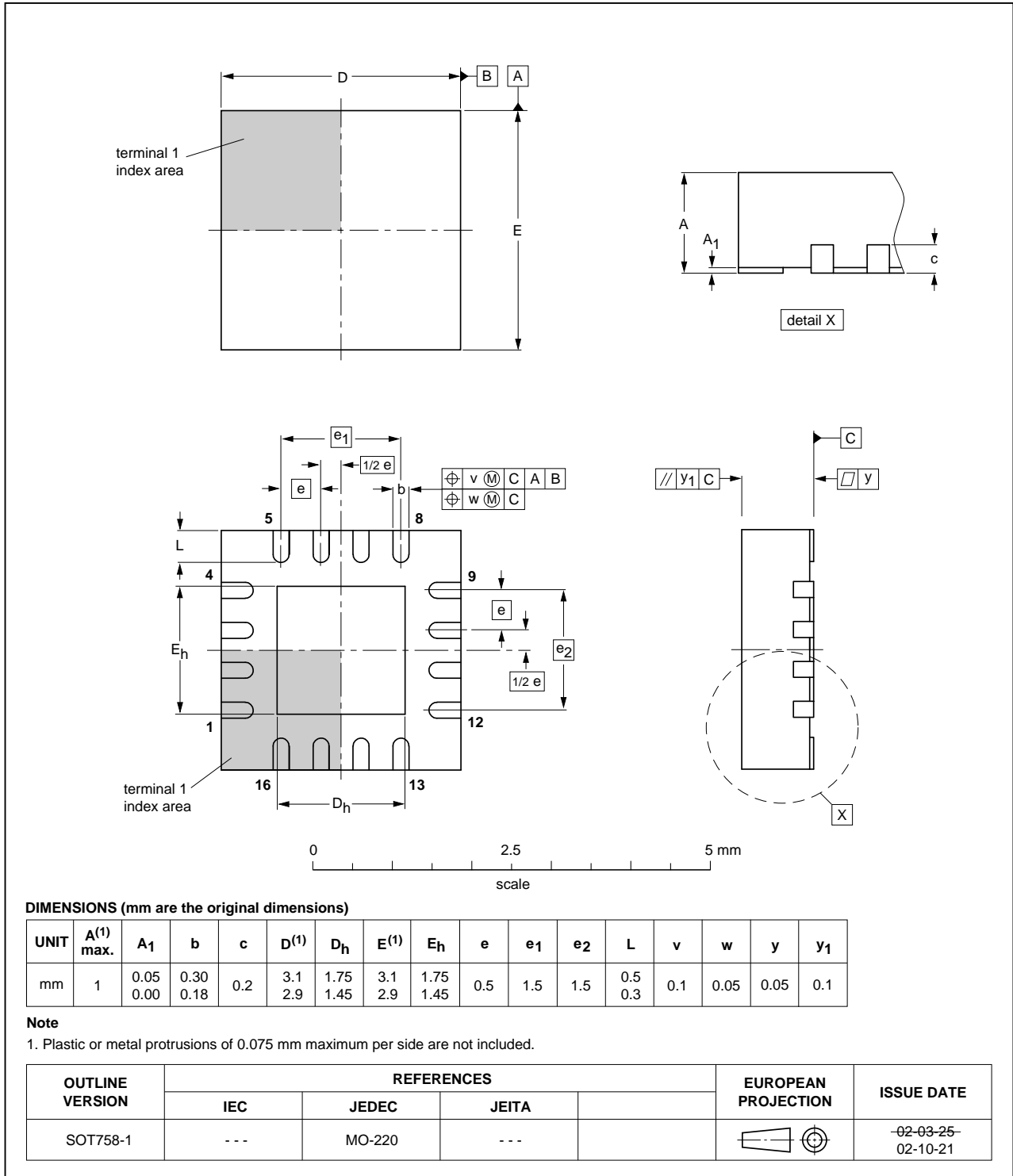


Fig 30. Package outline SOT758-1 (HVQFN16)

## 16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 31](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 17](#) and [18](#)

**Table 17. SnPb eutectic process (from J-STD-020D)**

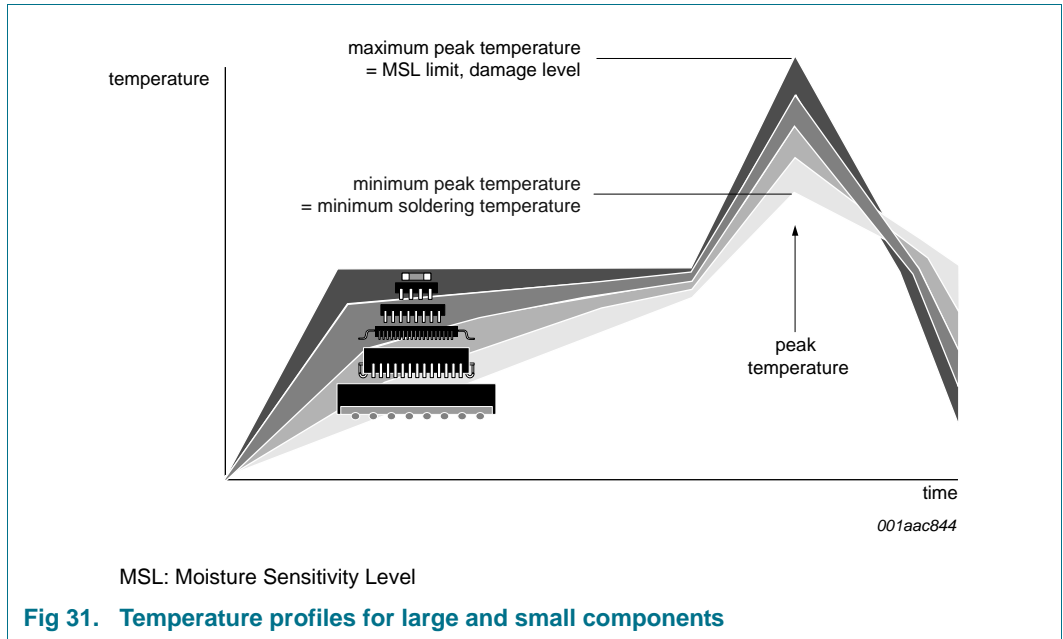
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 18. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 31](#).

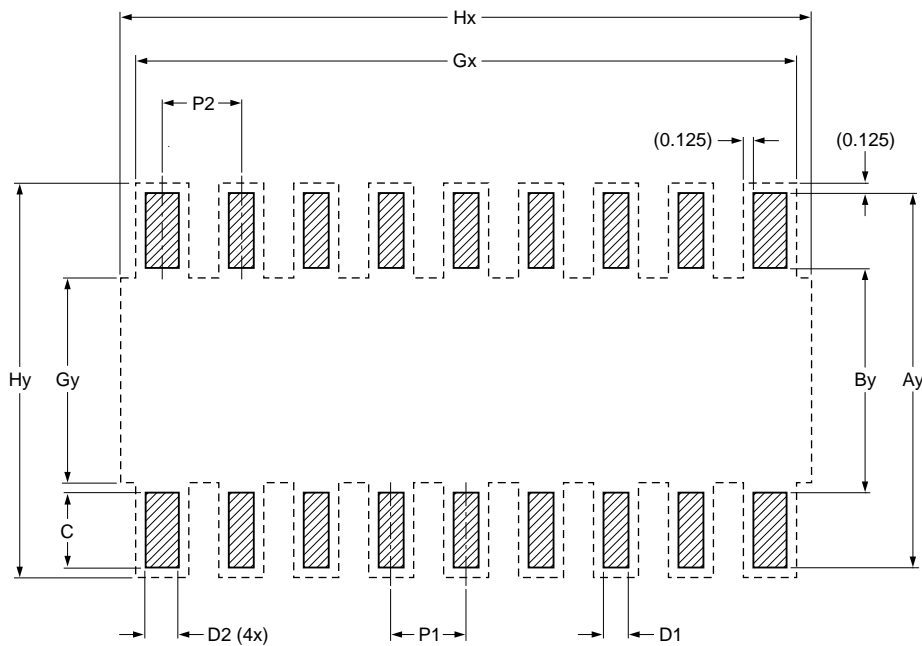


For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.


18. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP16 package

SOT403-1



Generic footprint pattern  
Refer to the package outline drawing for actual layout

 solder land  
- - - - occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1\_fr

Fig 32. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

Footprint information for reflow soldering of HVQFN16 package

SOT758-1

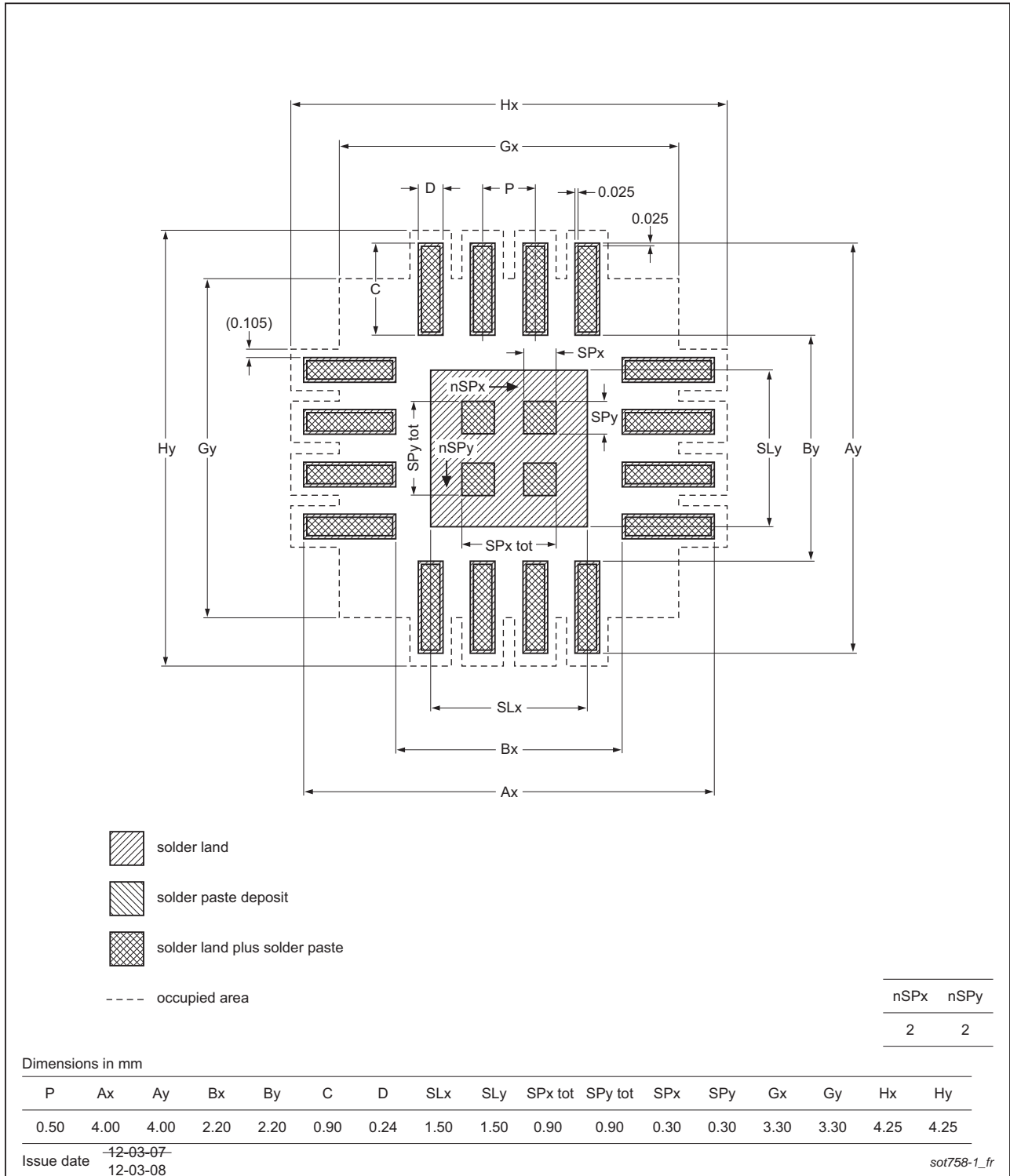


Fig 33. PCB footprint for SOT758-1 (HVQFN16); reflow soldering



## 19. Abbreviations

Table 19. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General Purpose Input/Output
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
LP	Low-Pass
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
SCR	Silicon Controlled Rectifier
SMBus	System Management Bus

## 20. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9554B_PCA9554C v.2	20150804	Product data sheet	-	PCA9554B_PCA9554C v.1
Modifications:	<ul style="list-style-type: none"> <li>Clarified pull-up information throughout document.</li> </ul>			
PCA9554B_PCA9554C v.1	20120919	Product data sheet	-	-

## 21. Legal information

### 21.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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