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June 2016

FDG6306P

P-Channel 2.5V Specified PowerTrench^o MOSFET

General Description

This PChannel 2.5V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V - 12V).

Applications

- Battery management
- · Load switch

Features

- -0.6 A, -20 V. $R_{DS(ON)} = 420$ m Ω @ $V_{GS} = -4.5$ V $R_{DS(ON)} = 630 \text{ m}\Omega$ @ $V_{GS} = -2.5 \text{ V}$
- · Low gate charge

S 1 or 4

G 2 or 5

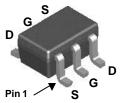
D 3 or 6

- High performance trench technology for extremely low R_{DS(ON)}
- Compact industry standard SC70-6 surface mount package

6 or 3 D

5 or 2 G

4 or 1 S





The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		± 12	V
I _D	Drain Current - Continuous	(Note 1)	-0.6	А
	- Pulsed		-2.0	
P _D	Power Dissipation for Single Operation	(Note 1)	0.3	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

R _{θJA} Therm	nal Resistance, Junction-to-Ambient	(Note 1)	415	°C/W
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Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.06	FDG6306P	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics					
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_D = -250 \mu\text{A}$	-20			V
<u>ΔBV dss</u> ΔT _J	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu A$, Referenced to 25°C		-14		mV/°C
l _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = -12 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = 12 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
On Char	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	-0.6	-1.2	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$, Referenced to 25°C		3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = -4.5 V, I _D = -0.6 A V _{GS} = -2.5 V, I _D = -0.5 A V _{GS} = -4.5 V, I _D = -0.6 A, T _J =125°C		300 470 400	420 630 700	МΩ
I _{D(on)}	On–State Drain Current	$V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$	-2			Α
g FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_D = -0.6 \text{ A}$		1.8		S
Dynamic	Characteristics					
Ciss	Input Capacitance	$V_{DS} = -10 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$		114		pF
Coss	Output Capacitance	f = 1.0 MHz		24		pF
C _{rss}	Reverse Transfer Capacitance			9		pF
Switchir	ng Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -10 \text{ V}, I_D = 1 \text{ A},$		5.5	11	ns
t _r	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		14	25	ns
t _{d(off)}	Turn-Off Delay Time			6	12	ns
t _f	Turn-Off Fall Time			1.7	3.4	ns
Qg	Total Gate Charge	$V_{DS} = -10 \text{ V}, I_{D} = -0.6 \text{ A},$		1.4	2.0	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 \text{ V}$		0.3		nC
Q _{gd}	Gate-Drain Charge			0.4		nC
Drain-S	ource Diode Characteristic					
ls	Maximum Continuous Drain-Source				-0.25	Α
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \qquad I_S = -0.25 \text{ A(Note 2)}$		-0.77	-1.2	V

Notes

^{1.} R_{RJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{RJC} is guaranteed by design while R_{RLA} is determined by the user's board design. $R_{RLA} = 415^{\circ}$ C/W when mounted on a minimum pad.

^{2.} Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%

Typical Characteristics

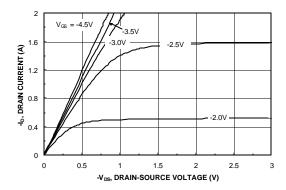
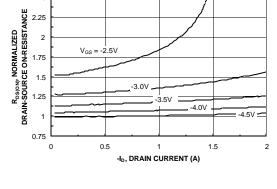


Figure 1. On-Region Characteristics.



2.5

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

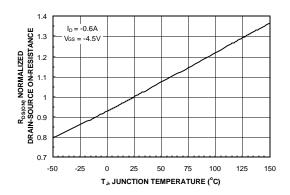


Figure 3. On-Resistance Variation with Temperature.

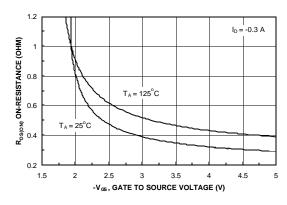


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

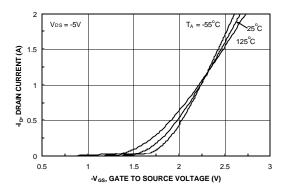


Figure 5. Transfer Characteristics.

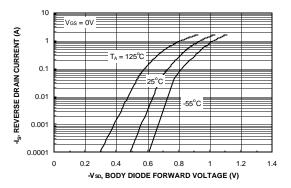
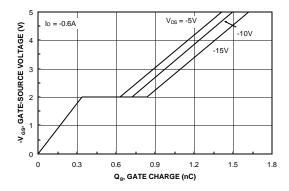


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



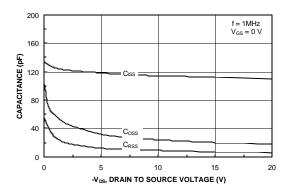
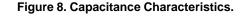
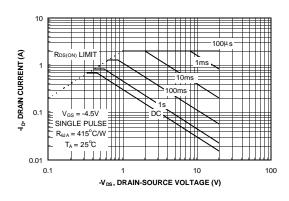


Figure 7. Gate Charge Characteristics.





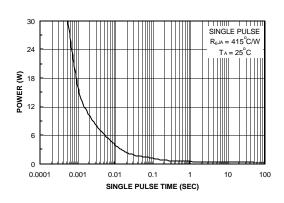


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

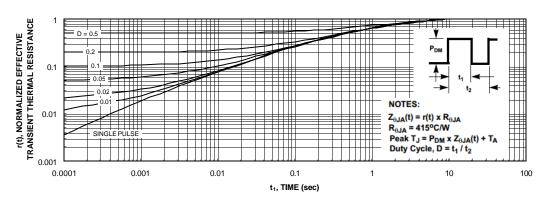


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1. Transient thermal response will change depending on the circuit board design.





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