ISL78235

5A Automotive Synchronous Buck Regulator

FN8713
Rev 7.00
Sep 28, 2018

The ISL78235 is a highly efficient, monolithic, synchronous step-down DC/DC converter that can deliver 5A of continuous output current from a 2.7V to 5.5V input supply. The device uses peak current mode control architecture to achieve very low duty cycle operation at high frequency with fast transient response and excellent loop stability.

The ISL78235 integrates a low ON-resistance P-channel (35mΩ, typical) high-side FET and N-channel (11mΩ, typical) low-side FET to maximize efficiency and minimize external component count. The 100% duty cycle operation allows less than 250mV dropout voltage at 5A output current. The operating frequency of the Pulse-Width Modulator (PWM) is adjustable from 500kHz to 4MHz. The default switching frequency of 2MHz is set by connecting the FS pin high.

The ISL78235 can be configured for discontinuous (PFM) or forced continuous (PWM) operation at light load. Forced continuous operation reduces noise and RF interference; discontinuous mode provides higher efficiency by reducing switching losses at light loads.

Fault protection is provided by internal hiccup mode current limiting during short-circuit and overcurrent conditions. The device also integrates output overvoltage and over-temperature protections. A power-good monitor indicates when the output is in regulation. The ISL78235 features a 1ms Power-Good (PG) timer at power-up.

When in shutdown, the ISL78235 discharges the output capacitor through an internal 100Ω soft-stop switch. Other features include internal fixed or adjustable soft-start and internal/external compensation.

The ISL78235 is available in a 3mmx3mm 16 Ld Thin Quad Flat No-lead (TQFN) Pb-free package and in a 5mmx5mm 16 Ld Wettable Flank Quad Flat No-Lead (WFQFN) package with an exposed pad for improved thermal performance. The ISL78235 is rated to operate across the temperature range of -40°C to +105°C in the 3mmx3mm package and -40°C to +125°C in the 5mmx5mm package.

Features

- 2.7V to 5.5V input voltage range
- 2MHz default switching frequency
- 100ns guaranteed phase minimum on time for wide output regulation
- Adjustable switching frequency from 500kHz to 4MHz
- External synchronization from 1MHz to 4MHz
- Optional PFM mode for light-load efficiency improvement
- Very low ON-resistance HS/LS switches: 35mΩ/11mΩ
- Internal 1ms or adjustable external soft-start
- Soft-stop output discharge during disable
- OTP, OCP, output OVP, and input UVLO protections
- 1% reference accuracy over-temperature
- Up to 95% efficiency
- AEC-Q100 qualified
- Common pinout family allows migration from 3A to 5A without PCB change:
  - ISL78233 . . . . . 3A
  - ISL78234 . . . . . 4A
  - ISL78235 . . . . . 5A

Applications

- DC/DC POL modules
- µC/µP, FPGA, and DSP power
- Video processor/SOC power
- Automotive infotainment power

Related Literature

For a full list of related documents, visit our website

- ISL78235 product page

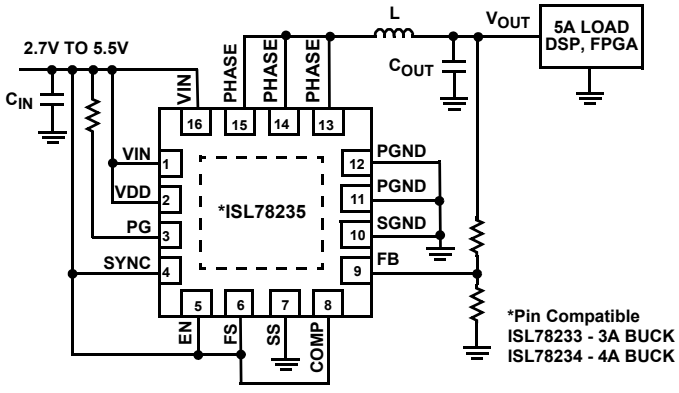

FIGURE 1. TYPICAL APPLICATION: 5A BUCK REGULATOR

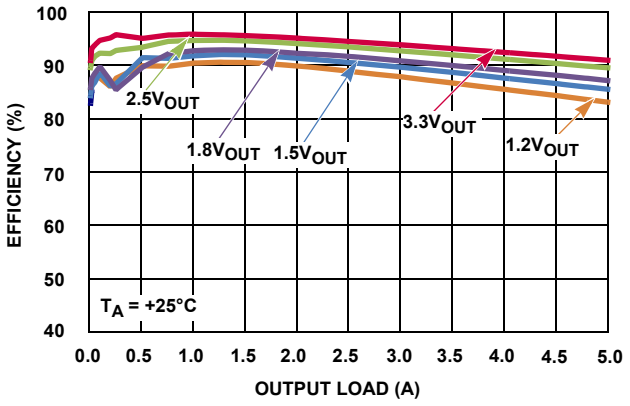

FIGURE 2. EFFICIENCY vs LOAD (V_{IN} = 5V; f_{sw} = 2MHz; SYNC = GND)

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Functional Block Diagram

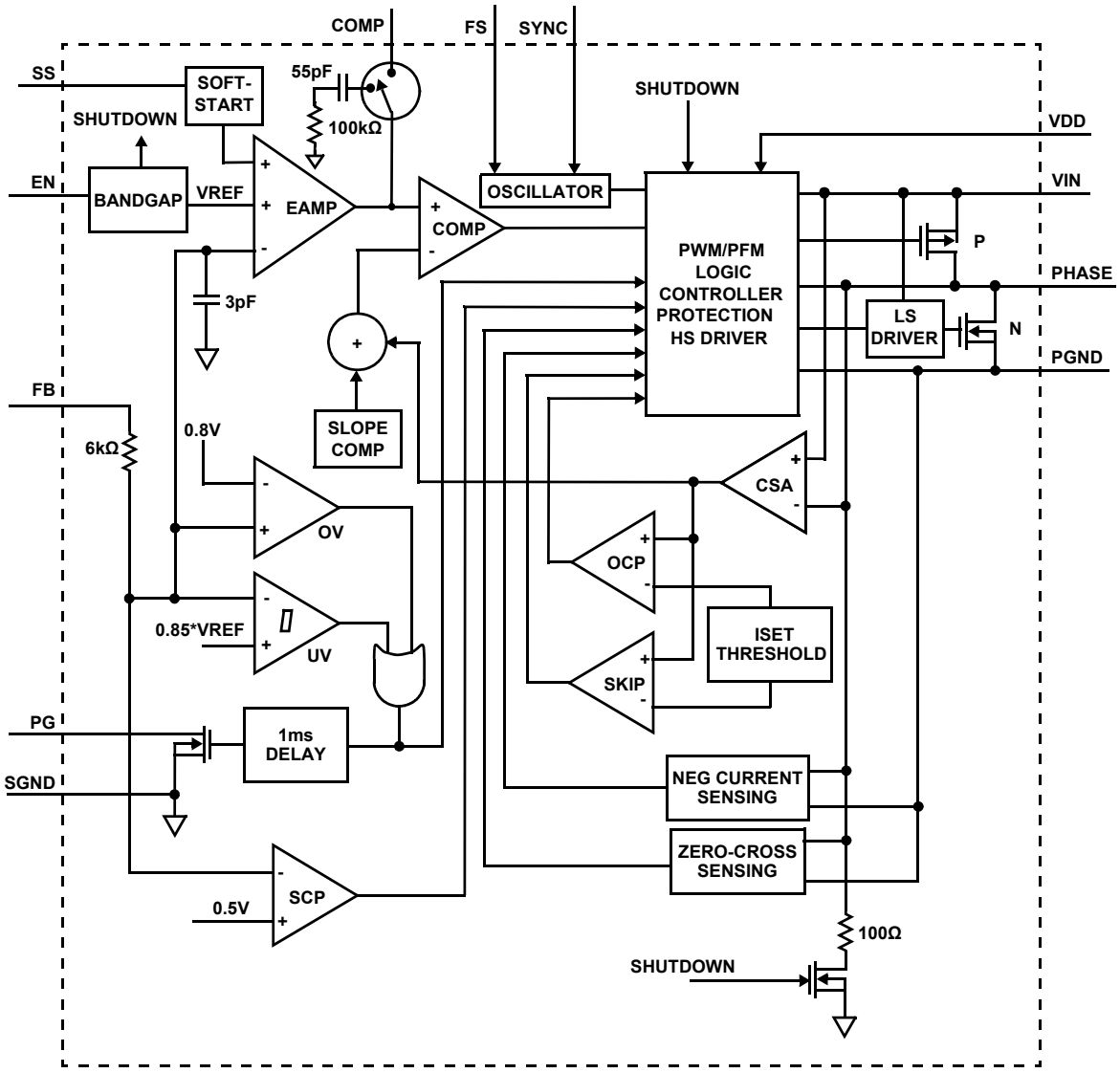
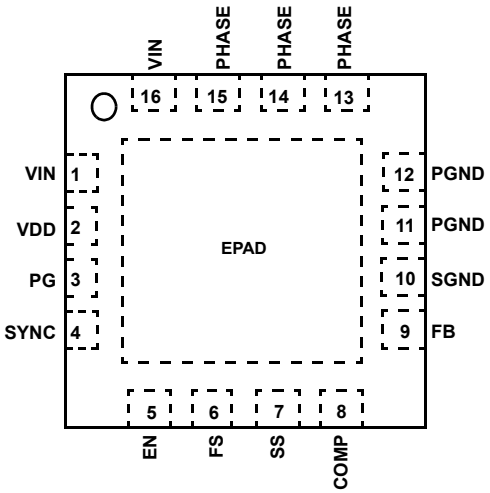


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Pin Configuration

ISL78235
(16 LD TQFN, WFQFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 16	VIN	Input supply voltage. Place a minimum of two 22µF low ESR ceramic capacitors from VIN to PGND as close as possible to the IC for decoupling.
2	VDD	Input supply voltage for the logic circuitry. A 0.1µF high frequency decoupling ceramic capacitor should also be placed close to the VDD and SGND pin. Connect to the VIN pin.
3	PG	PG is an open-drain output for power-good indication. Use a 10kΩ to 100kΩ pull-up resistor connected from PG to VIN. At power-up or EN high, the PG rising edge is delayed by 1ms upon output voltage within regulation.
4	SYNC	Mode selection pin. Connect to logic high or input voltage VIN for forced PWM mode. Connect to logic low or ground for PFM mode. Connect to an external function generator for synchronization with a positive edge trigger. In external synchronization the ISL78235 operates in forced PWM mode. The transition to and from the internal oscillator to external synchronization is seamless and does not require disabling the ISL78235. An internal 1MΩ pull-down resistor to SGND prevents an undefined logic state if the SYNC pin is floating.
5	EN	Regulator enable pin. The regulator is enabled when driven logic high. The regulator is shut down and the PHASE pin discharges the output capacitor when the enable pin is driven low.
6	FS	This pin sets the internal oscillator switching frequency using a resistor, R_{FS}, from the FS pin to GND. The frequency of operation may be programmed between 500kHz to 4MHz. The switching frequency is 2MHz if FS is connected to VIN.
7	SS	SS is used to adjust the soft-start time. Connect the SS pin to SGND for an internal 1ms soft-start time. Connect a capacitor from SS to SGND to adjust the soft-start time. Do not use more than 33nF on the SS pin.
8	COMP	COMP is the output of the error amplifier if COMP is not connected to VDD. An external compensation network must be used if COMP is not tied to VDD. If COMP is tied to VDD, the error amplifier output is internally compensated. External compensation network across COMP and SGND may be required to improve the loop compensation of the amplifier.
9	FB	The feedback network of the regulator, FB, is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. In addition, the regulator power-good and undervoltage protection circuitry use FB to monitor the regulator output voltage.
10	SGND	Signal ground. Connect to PGND.
11, 12	PGND	Power ground.
13, 14, 15	PHASE	Switching node connections. Connect to one terminal of the inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See "Functional Block Diagram" on page 3 for more detail.
Exposed Pad	EPAD	The exposed pad must be connected to the SGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to SGND plane for optimal thermal performance.

Ordering Information

PART NUMBER (Note 4)	PART MARKING	OUTPUT VOLTAGE (V)	TEMP. RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL78235ARZ (Note 2)	8235	Adjustable	-40°C to +105°C	-	16 Ld 3x3mm TQFN	L16.3x3D
ISL78235ARZ-T (Notes 1, 2)	8235	Adjustable	-40°C to +105°C	6k	16 Ld 3x3mm TQFN	L16.3x3D
ISL78235ARZ-T7A (Notes 1, 2)	8235	Adjustable	-40°C to +105°C	250	16 Ld 3x3mm TQFN	L16.3x3D
ISL78235AARZ (Note 3)	78235A ARZ	Adjustable	-40°C to +125°C	-	16 Ld 5x5mm WFQFN	L16.5x5D
ISL78235AARZ-T (Notes 1, 3)	78235A ARZ	Adjustable	-40°C to +125°C	6k	16 Ld 5x5mm WFQFN	L16.5x5D
ISL78235AARZ-T7A (Notes 1, 3)	78235A ARZ	Adjustable	-40°C to +125°C	250	16 Ld 5x5mm WFQFN	L16.5x5D
ISL78235EVAL1Z	3x3mm TQFN Evaluation Board					
ISL78235EVAL2Z	5x5mm WFQFN Evaluation Board					

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
4. For Moisture Sensitivity Level (MSL), refer to the ISL78235 product information page. For more information about MSL, refer to TB363.

TABLE 1. KEY DIFFERENCE BETWEEN FAMILY OF PARTS

PART NUMBER	I_{OUT} MAX (A)
ISL78235	5
ISL78234	4
ISL78233	3

Typical Application Diagram

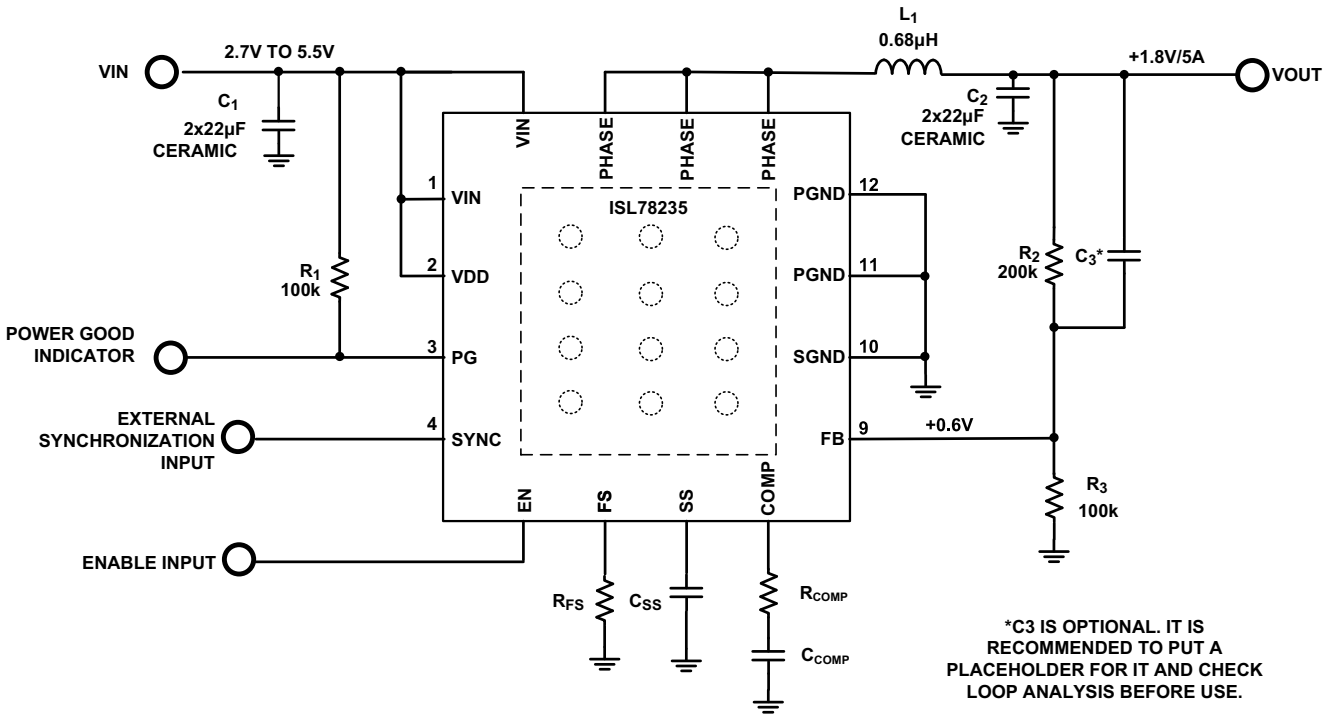


FIGURE 4. TYPICAL APPLICATION DIAGRAM

TABLE 2. COMPONENT SELECTION TABLE WITH INTERNAL COMPENSATION

V_{OUT}	1.2V	1.5V	1.8V	2.5V	3.3V
C_1	2 x 22µF	2 x 22µF	2 x 22µF	2x22µF	2 x 22µF
C_2 (Note 5)	3 x 22µF	3 x 22µF	2 x 22µF	2 x 22µF	2 x 22µF
C_3	22pF	10pF	10pF	10pF	10pF
L_1	0.33µH-0.68µH	0.33µH-0.68µH	0.33µH-0.68µH	0.47µH-0.78µH	0.47µH-0.78µH
R_2	100kΩ	150kΩ	200kΩ	316kΩ	450kΩ
R_3	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ

NOTE:

5. C_2 values are minimum recommended values for ceramic capacitors. Higher capacitance may be needed based on system requirements.

Absolute Maximum Ratings (Reference to GND)

VIN ..... -0.3V to 5.8V (DC) or 7V (20ms)
EN, FS, PG, SYNC, VFB ..... -0.3V to VIN + 0.3V
PHASE ..... -1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
COMP, SS ..... -0.3V to 2.7V
ESD Rating
Human Body Model (Tested per AEC-Q100-002) 5kV
Machine Model (Tested per AEC-Q100-003) 300V
Charge Device Model (Tested per AEC-Q100-011) 2kV
Latch-Up (Tested per AEC-Q100-004, Class II, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld TQFN Package (Notes 6, 7)	43	3.5
16 Ld WFQFN Package (Notes 6, 7)	33	3.5

Operating Junction Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range ..... 2.7V to 5.5V
Load Current Range ..... 0A to 5A
Ambient Temperature Range
3x3mm TQFN ..... -40°C to +105°C
5x5mm WFQFN ..... -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. Refer to TB379.
7. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside.

Electrical Specifications

Specification limits are established at the following conditions: T_A = -40°C to +105°C or T_A = -40°C to +125°C depending on package, V_{IN} = 3.6V, EN = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range specified in the Recommended Operating Conditions table for the specified package.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load		2.5	**2.7**	V
		Falling, no load	**2.20**	2.45		V
Quiescent Supply Current	I_{VIN}	SYNC = GND, no load at the output		47		µA
		SYNC = GND, no load at the output and no switches switching		47	**60**	µA
		SYNC = V_{IN}, f_{SW} = 2MHz, no load at the output		19	**25**	mA
Shutdown Supply Current	I_{SD}	SYNC = GND, V_{IN} = 5.5V, EN = low		4	**10**	µA
OUTPUT REGULATION						
Reference Voltage	V_{REF}		**0.594**	0.600	**0.606**	V
VFB Bias Current	I_{VFB}	VFB = 0.75V		0.1		µA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.7V)		0.2		%/V
Soft-Start Ramp Time Cycle		SS = SGND		1		ms
Soft-Start Charging Current	I_{SS}	V_{SS} = 0.1V	**1.7**	2.1	**2.5**	µA
OVERCURRENT PROTECTION						
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Current Limit	I_{PLIMIT}	T_A = +25°C	6.2	7.8	9.4	A
		T_A = -40°C to +105°C	**6.1**		**11.0**	A
		5x5 mm WFQFN package T_A = +105°C to +125°C			**12.5**	A
Peak Skip Limit	I_{SKIP}	T_A = +25°C	0.85	1.10	1.40	A
		T_A = -40°C to +105°C	**0.83**		**1.60**	A
		5x5 mm WFQFN package T_A = +105°C to +125°C			**1.65**	A

Electrical Specifications Specification limits are established at the following conditions: T_A = -40°C to +105°C or T_A = -40°C to +125°C depending on package, V_{IN} = 3.6V, EN = V_{IN}, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range specified in the Recommended Operating Conditions table for the specified package. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Zero Cross Threshold			**-275**		**375**	mA
Negative Current Limit	I_{NLIMIT}	T_A = +25°C	-5.1	-2.8	-1.3	A
			-6.0		**-0.6**	A
COMPENSATION						
Error Amplifier Transconductance		COMP = V_{DD}, internal compensation		125		µA/V
		External compensation		130		µA/V
Transresistance	RT	T_A = -40°C to +105°C	**0.11**	0.17	**0.22**	Ω
		5x5 mm WFQFN package T_A = +105°C to +125°C	**0.1**			Ω
MOSFET						
P-Channel ON-Resistance		V_{IN} = 5V, I_O = 200mA	**26**	35	**50**	mΩ
		V_{IN} = 2.7V, I_O = 200mA	**38**	52	**78**	mΩ
N-Channel ON-Resistance		V_{IN} = 5V, I_O = 200mA	**5**	11	**20**	mΩ
		V_{IN} = 2.7V, I_O = 200mA	**8**	15	**31**	mΩ
PHASE						
PHASE Maximum Duty Cycle				100		%
PHASE Minimum On-Time		SYNC = High			**100**	ns
OSCILLATOR						
Nominal Switching Frequency	f_{SW}	FS = V_{IN}	**1730**	2000	**2350**	kHz
		FS with RS = 402kΩ		420		kHz
		FS with RS = 42.2kΩ		4200		kHz
SYNC Logic LOW to HIGH Threshold			**0.67**	0.75	**0.84**	V
SYNC Logic Hysteresis			**0.10**	0.17	**0.20**	V
SYNC Logic Input Leakage Current		SYNC = 3.6V		3.7	**5.0**	µA
POWER-GOOD (PG)						
Output Low Voltage		I_{PG} = 1mA			**0.3**	V
PG Delay Time (Rising Edge)		Time from V_{OUT} reached regulation	**0.5**	1.0	**2.0**	ms
PG Delay Time (Falling Edge)				6.5		µs
PG Pin Leakage Current		PG = V_{IN}		0.01	**0.10**	µA
OVP PG Rising Threshold				0.80		V
UVP PG Rising Threshold			**80**	85	**90**	%
UVP PG Hysteresis				5.5		%
EN						
Logic Input Low (Note 9)	EN_VIL				**0.4**	V
Logic Input High	EN_VIH		**0.9**			V
EN Logic Input Leakage Current		EN = 3.6V		0.1	**1.0**	µA
OVER-TEMPERATURE PROTECTION						
Thermal Shutdown		Temperature rising		150		°C
Thermal Shutdown Hysteresis		Temperature falling		25		°C

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
9. EN should be held below the EN_VIL until V_{IN} exceeds V_{UVLO} rising.

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = V_{DD} = 5V, V_{OUT} = 1.8V, EN = V_{DD}, SYNC = V_{DD}, L = 0.68µH, f_{SW} = 2MHz, C_{IN} = 2 x 22µF, C_{OUT} = 2 x 22µF, I_{OUT} = 0A to 5A.

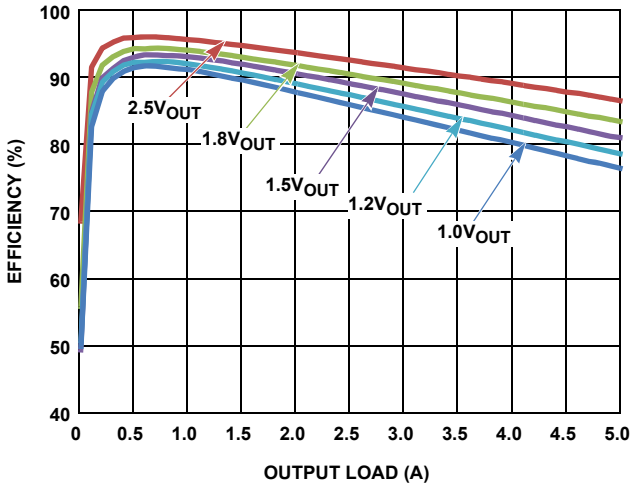


FIGURE 5. EFFICIENCY vs LOAD ($3.3V_{IN}$; SYNC = V_{DD})

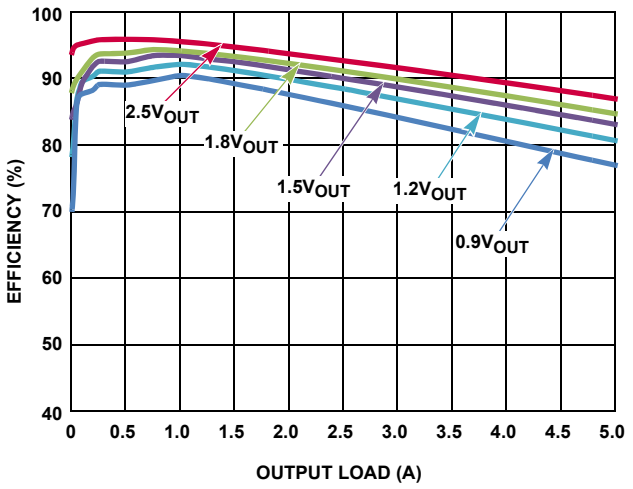


FIGURE 6. EFFICIENCY vs LOAD ($3.3V_{IN}$; SYNC = GND)

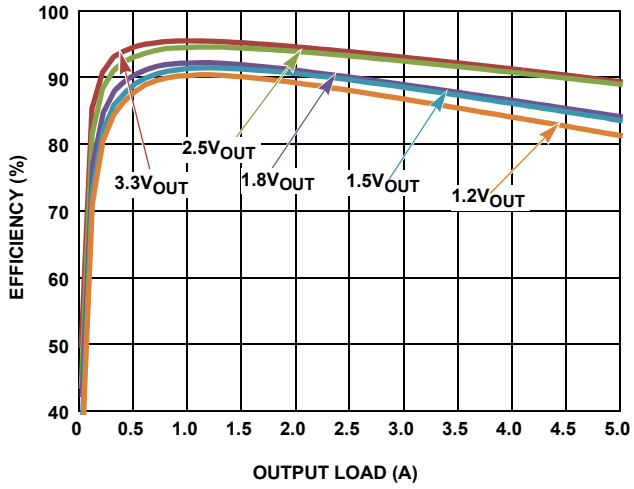


FIGURE 7. EFFICIENCY vs LOAD ($5V_{IN}$; SYNC = V_{DD})

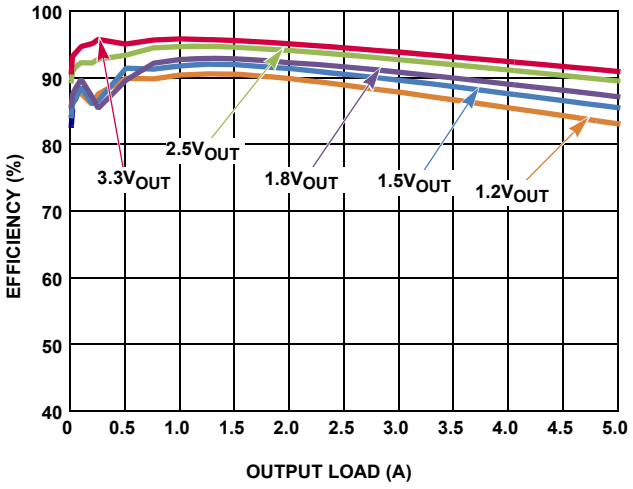


FIGURE 8. EFFICIENCY vs LOAD ($5V_{IN}$; SYNC = GND)

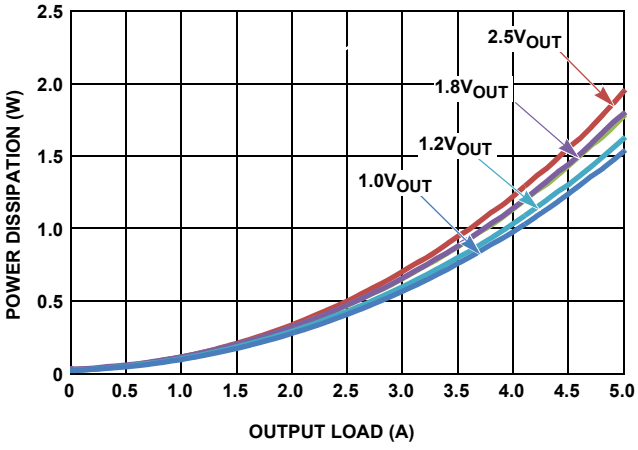


FIGURE 9. POWER DISSIPATION vs LOAD ($3.3V_{IN}$; SYNC = V_{DD})

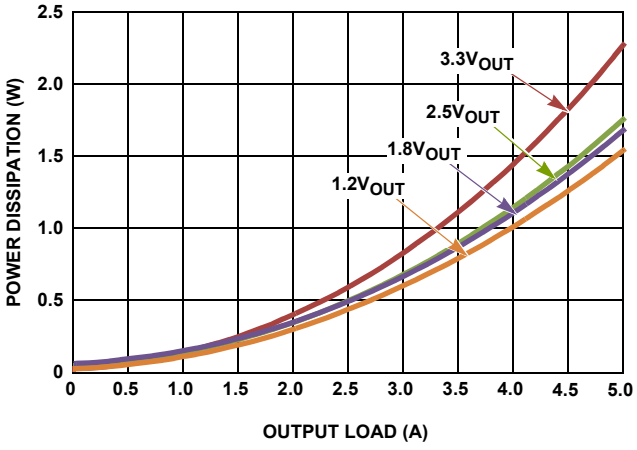


FIGURE 10. POWER DISSIPATION vs LOAD ($5V_{IN}$; SYNC = V_{DD})

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = V_{DD} = 5V, V_{OUT} = 1.8V, EN = V_{DD}, SYNC = V_{DD}, L = 0.68µH, f_{SW} = 2MHz, C_{IN} = 2 x 22µF, C_{OUT} = 2 x 22µF, I_{OUT} = 0A to 5A. **(Continued)**

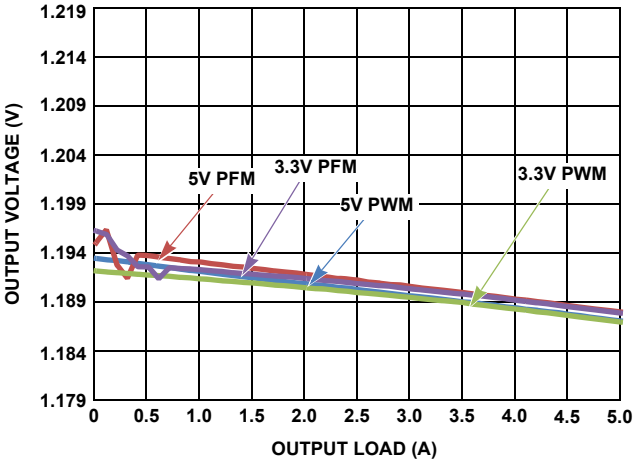


FIGURE 11. V_{OUT} REGULATION vs LOAD (V_{OUT} = 1.2V)

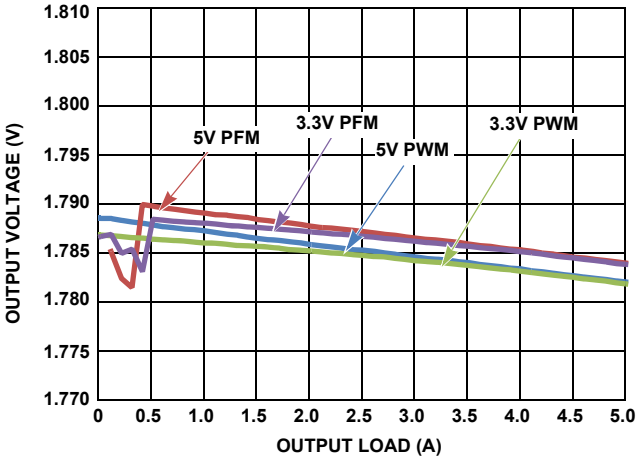


FIGURE 12. V_{OUT} REGULATION vs LOAD (V_{OUT} = 1.8V)

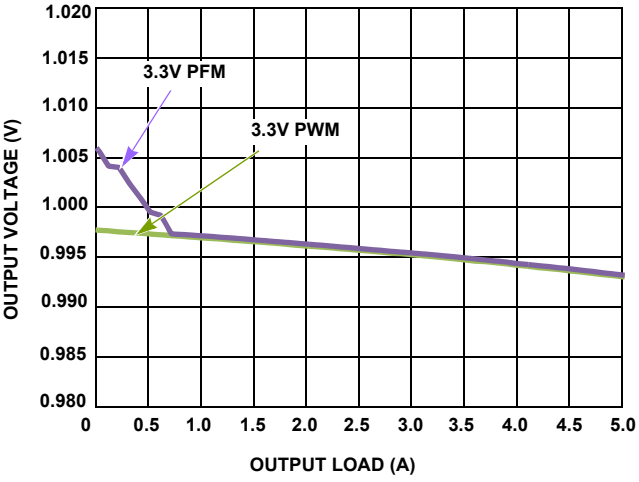


FIGURE 13. V_{OUT} REGULATION vs LOAD (V_{OUT} = 1.0V)

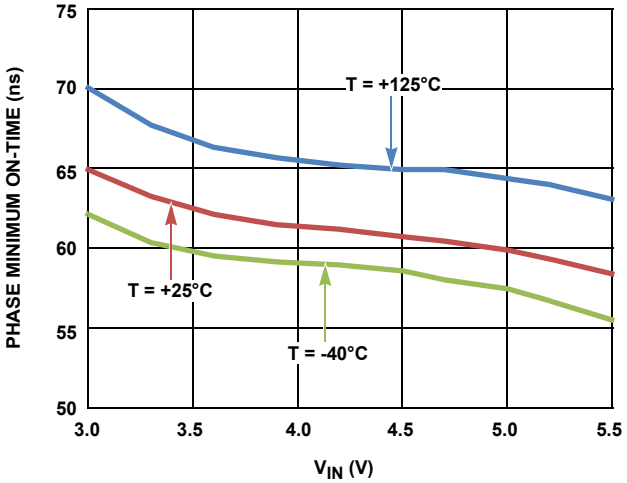


FIGURE 14. PHASE MINIMUM ON-TIME vs V_{IN}

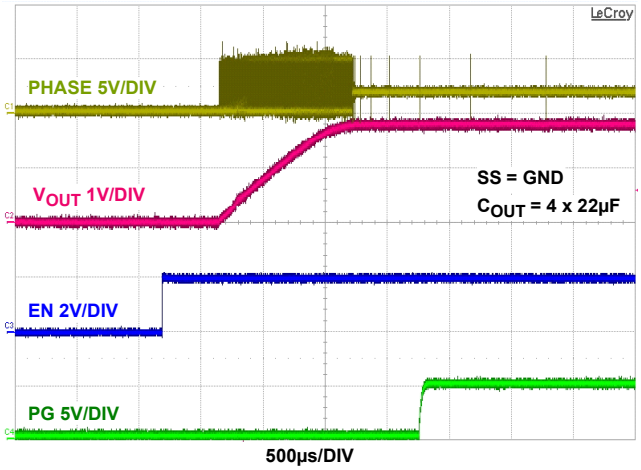


FIGURE 15. EN START-UP AT NO LOAD (SYNC = GND)

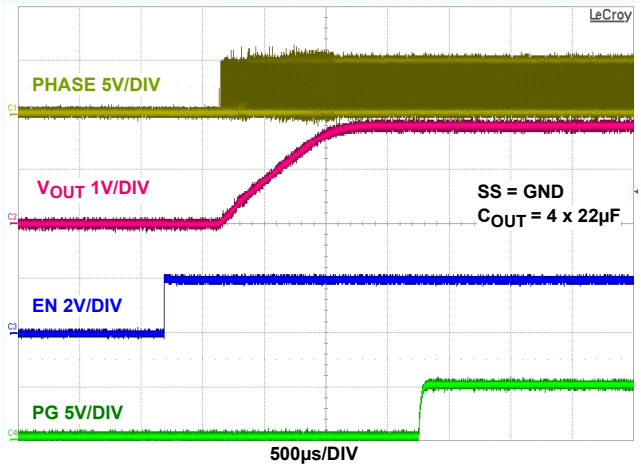


FIGURE 16. EN START-UP AT NO LOAD (SYNC = V_{DD})

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = V_{DD} = 5V, V_{OUT} = 1.8V, EN = V_{DD}, SYNC = V_{DD}, L = 0.68µH, f_{SW} = 2MHz, C_{IN} = 2 x 22µF, C_{OUT} = 2 x 22µF, I_{OUT} = 0A to 5A. **(Continued)**

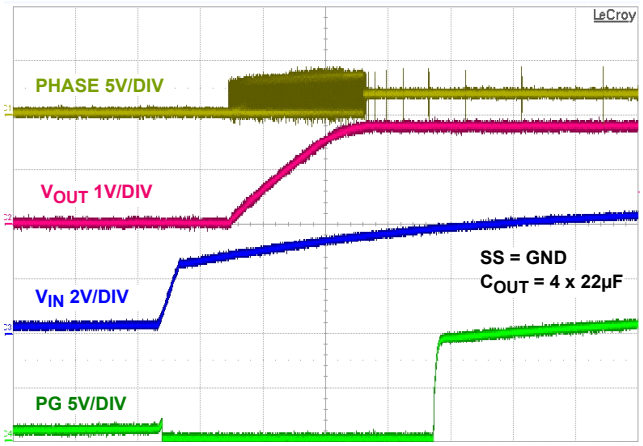


FIGURE 17. V_{IN} START-UP AT NO LOAD (SYNC = GND)

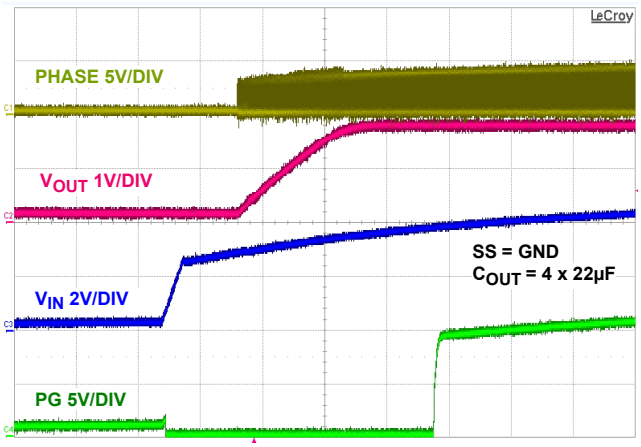


FIGURE 18. V_{IN} START-UP AT NO LOAD (SYNC = V_{DD})

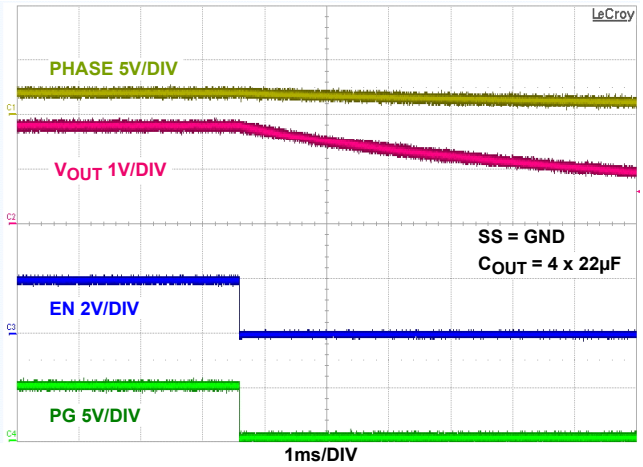


FIGURE 19. EN SHUTDOWN AT NO LOAD (SYNC = GND)

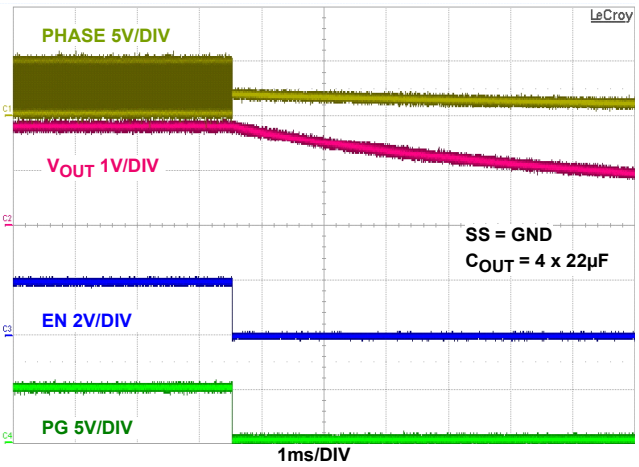


FIGURE 20. EN SHUTDOWN AT NO LOAD (SYNC = V_{DD})

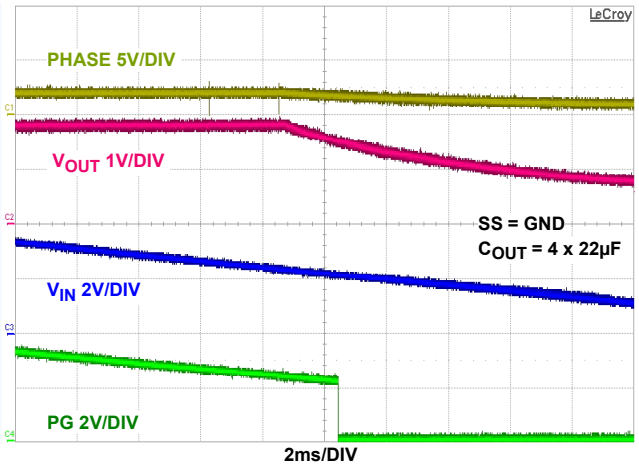


FIGURE 21. V_{IN} SHUTDOWN AT NO LOAD (SYNC = GND)

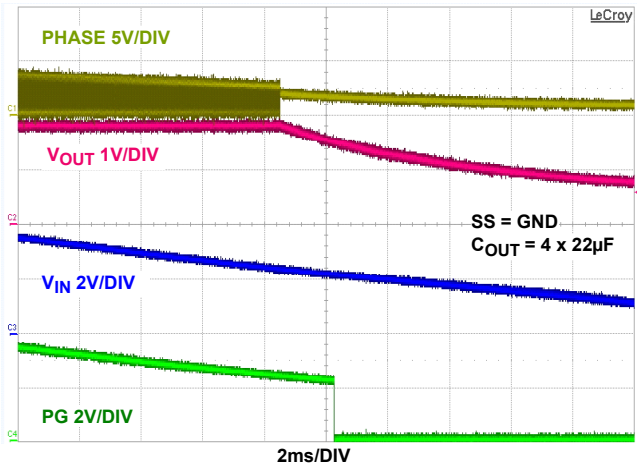


FIGURE 22. V_{IN} SHUTDOWN AT NO LOAD (SYNC = V_{DD})

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = V_{DD} = 5V, V_{OUT} = 1.8V, EN = V_{DD}, SYNC = V_{DD}, L = 0.68µH, f_{SW} = 2MHz, C_{IN} = 2 x 22µF, C_{OUT} = 2 x 22µF, I_{OUT} = 0A to 5A. **(Continued)**

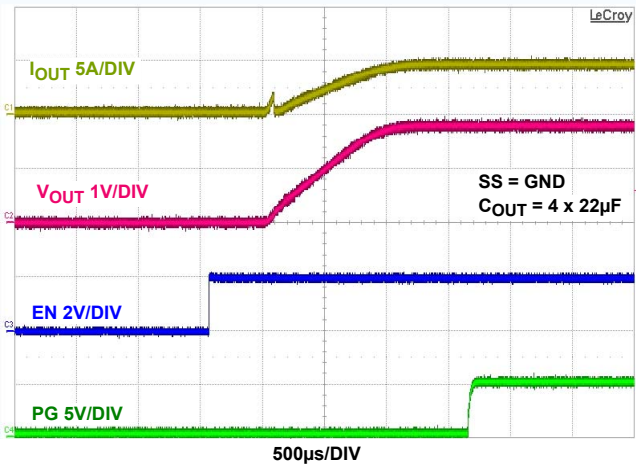


FIGURE 23. EN START-UP AT 5A LOAD (SYNC = GND)

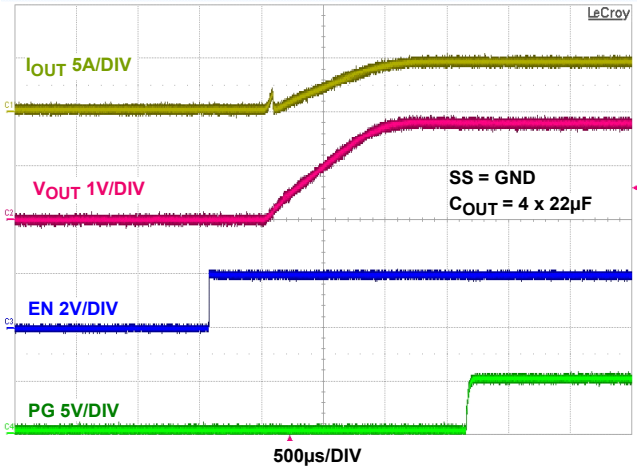


FIGURE 24. EN START-UP AT 5A LOAD (SYNC = V_{DD})

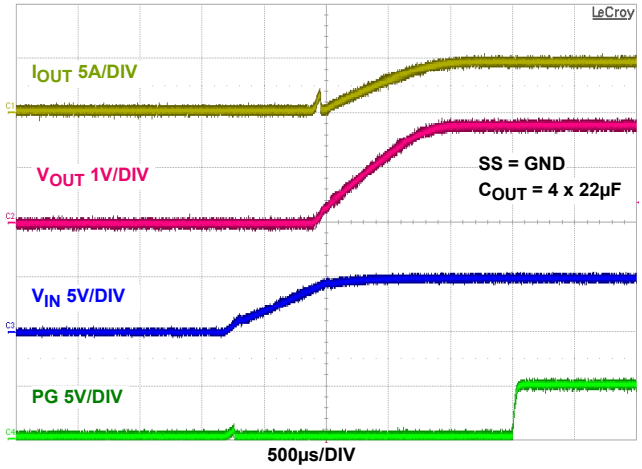


FIGURE 25. V_{IN} START-UP AT 5A LOAD (SYNC = GND)

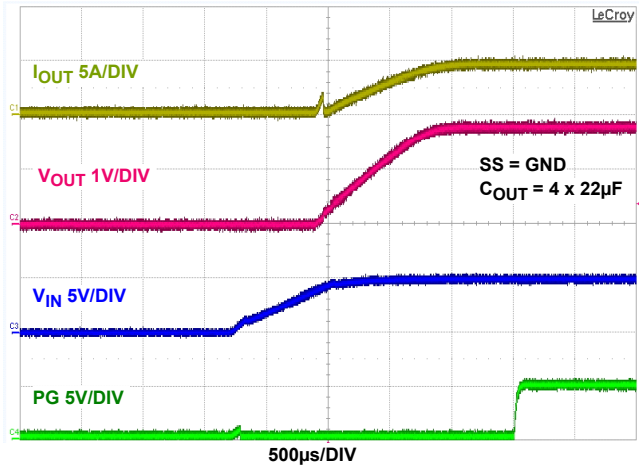


FIGURE 26. V_{IN} START-UP AT 5A LOAD (SYNC = V_{DD})

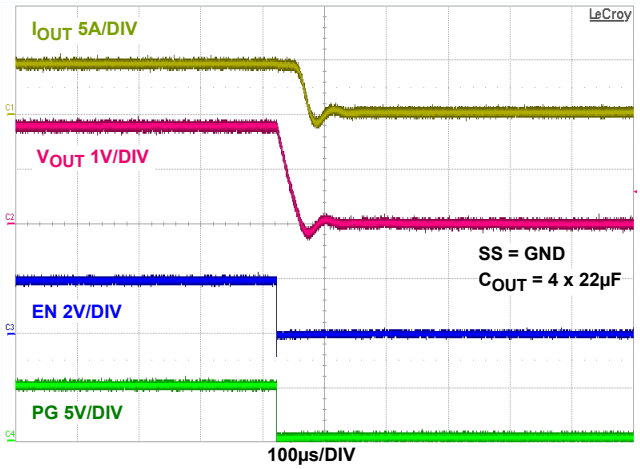


FIGURE 27. EN SHUTDOWN AT 5A LOAD (SYNC = GND)

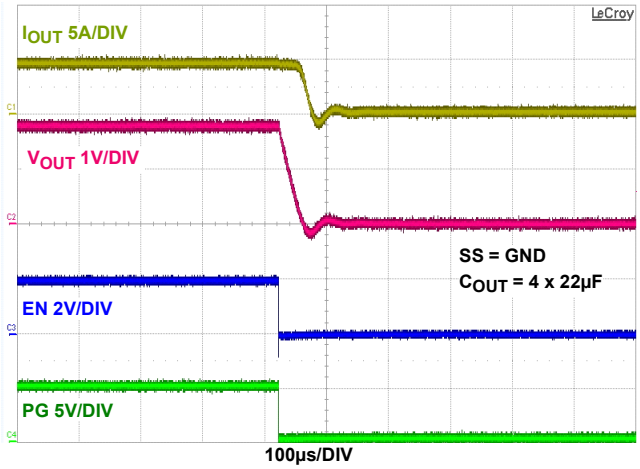


FIGURE 28. EN SHUTDOWN AT 5A LOAD (SYNC = V_{DD})

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = V_{DD} = 5V, V_{OUT} = 1.8V, EN = V_{DD}, SYNC = V_{DD}, L = 0.68µH, f_{SW} = 2MHz, C_{IN} = 2 x 22µF, C_{OUT} = 2 x 22µF, I_{OUT} = 0A to 5A. **(Continued)**

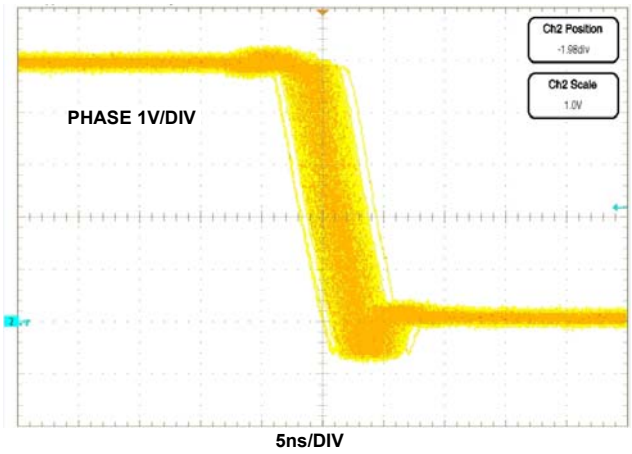


FIGURE 29. JITTER AT NO LOAD (SYNC = V_{DD})

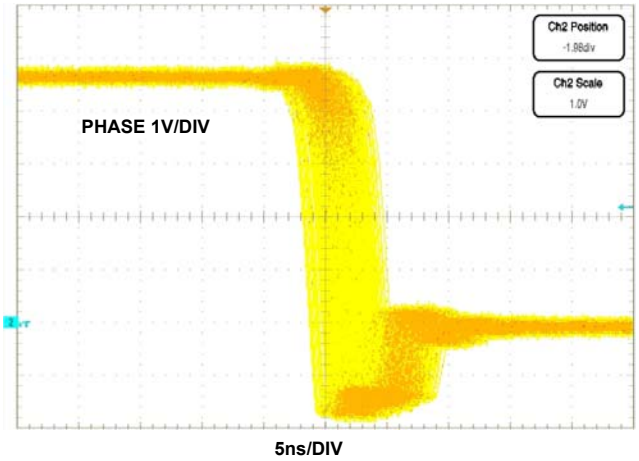


FIGURE 30. JITTER AT 5A LOAD (SYNC = V_{DD})

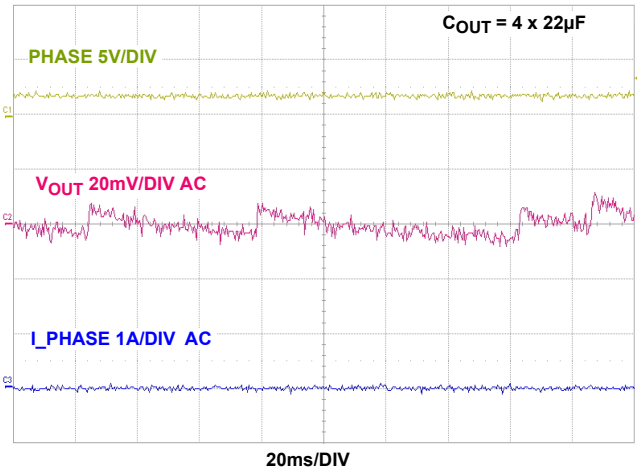


FIGURE 31. STEADY STATE AT NO LOAD (SYNC = GND)

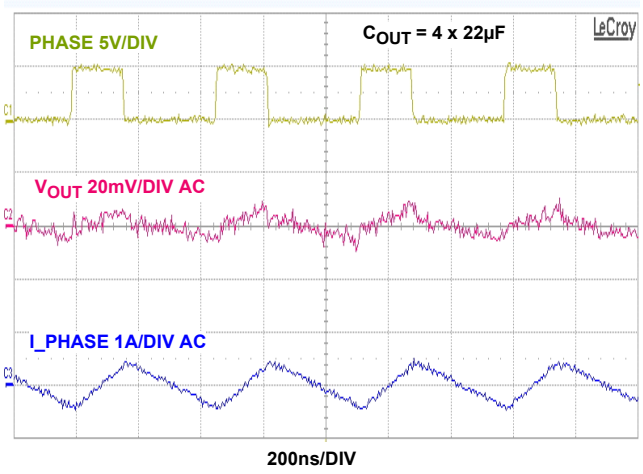


FIGURE 32. STEADY STATE AT NO LOAD (SYNC = V_{DD})

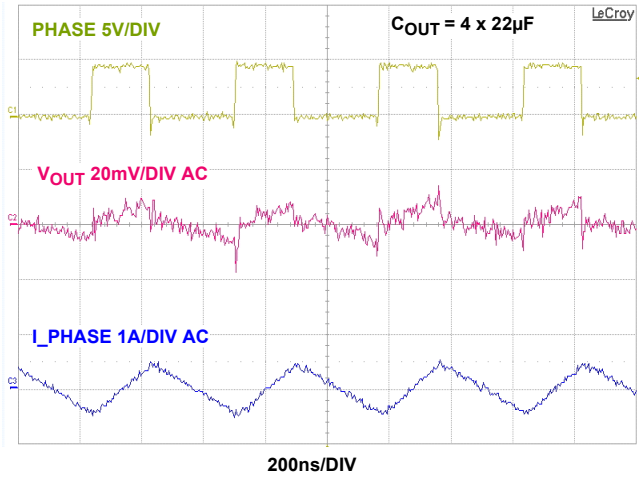


FIGURE 33. STEADY STATE AT 5A (SYNC = V_{DD})

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = V_{DD} = 5V, V_{OUT} = 1.8V, EN = V_{DD}, SYNC = V_{DD}, L = 0.68µH, f_{SW} = 2MHz, C_{IN} = 2 x 22µF, C_{OUT} = 2 x 22µF, I_{OUT} = 0A to 5A. **(Continued)**

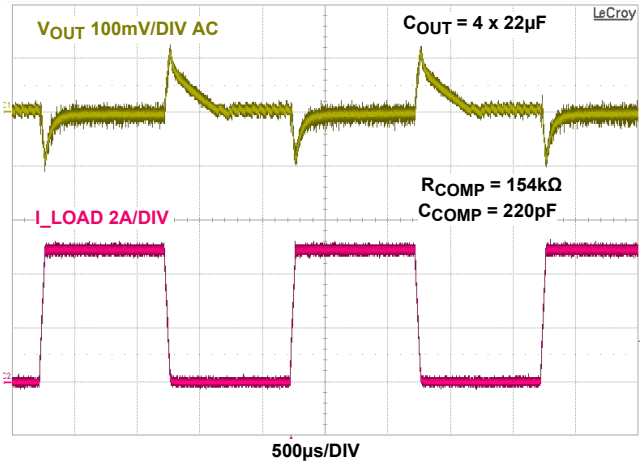


FIGURE 34. LOAD TRANSIENT 0A TO 5A; 0.5A/µs (SYNC = GND)

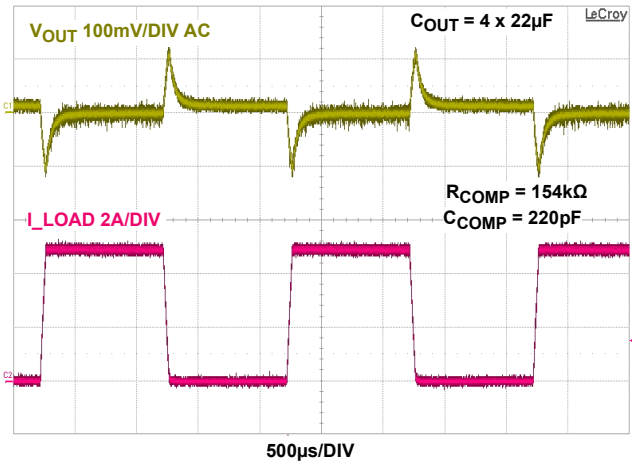


FIGURE 35. LOAD TRANSIENT 0A TO 5A; 0.5A/µs (SYNC = V_{DD})

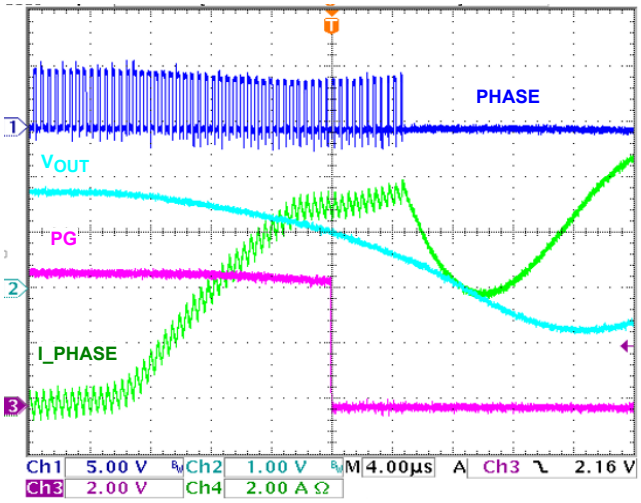


FIGURE 36. OUTPUT SHORT-CIRCUIT

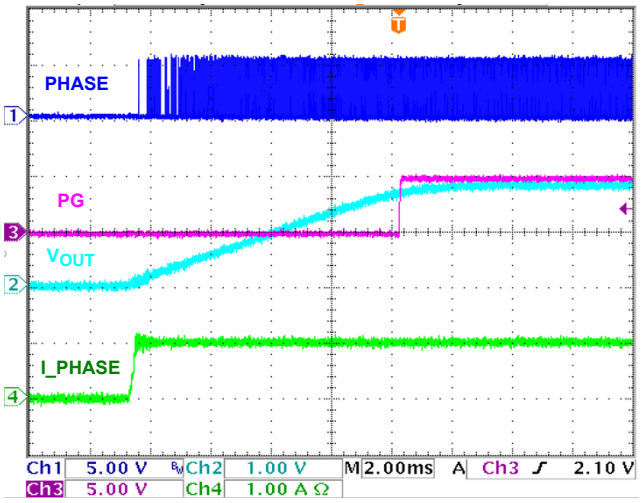


FIGURE 37. OUTPUT SHORT-CIRCUIT RECOVERY TO 1A LOAD

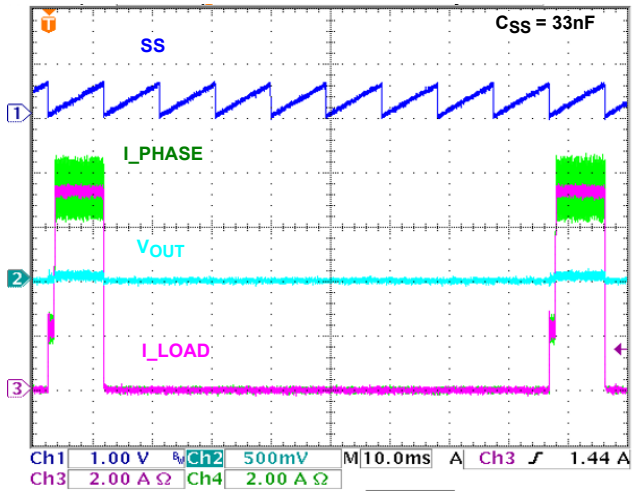


FIGURE 38. SHORT-CIRCUIT HICCUP WAVEFORM

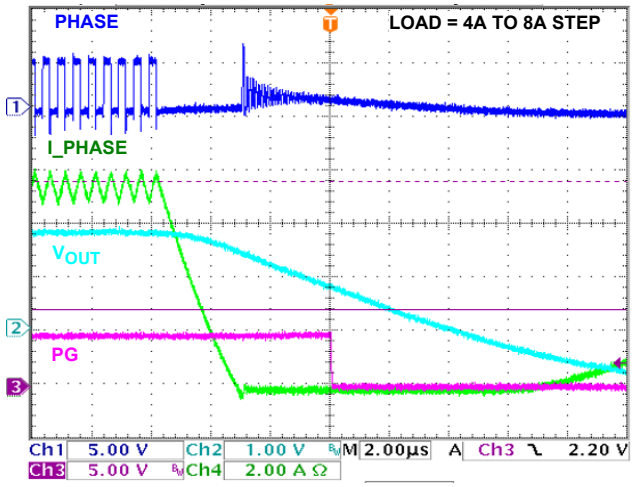


FIGURE 39. OVERCURRENT PROTECTION

Typical Operating Performance

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = V_{DD} = 5V, V_{OUT} = 1.8V, EN = V_{DD}, SYNC = V_{DD}, L = 0.68µH, f_{SW} = 2MHz, C_{IN} = 2 x 22µF, C_{OUT} = 2 x 22µF, I_{OUT} = 0A to 5A. **(Continued)**

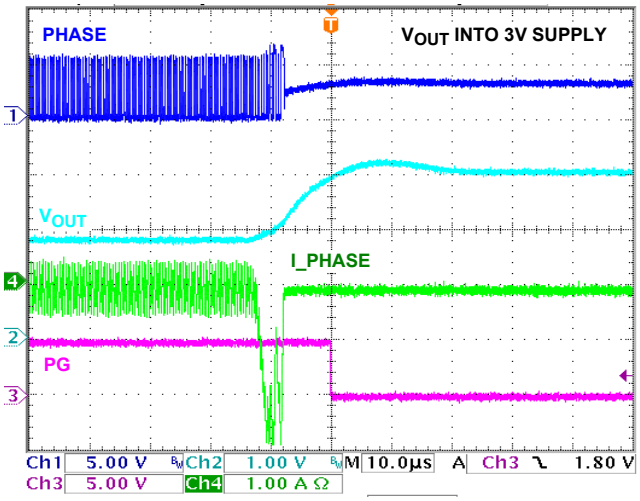


FIGURE 40. OVERVOLTAGE PROTECTION

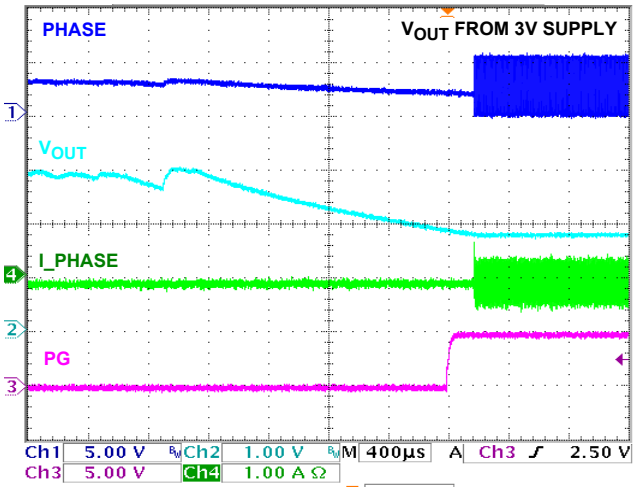


FIGURE 41. OVERVOLTAGE RECOVERY

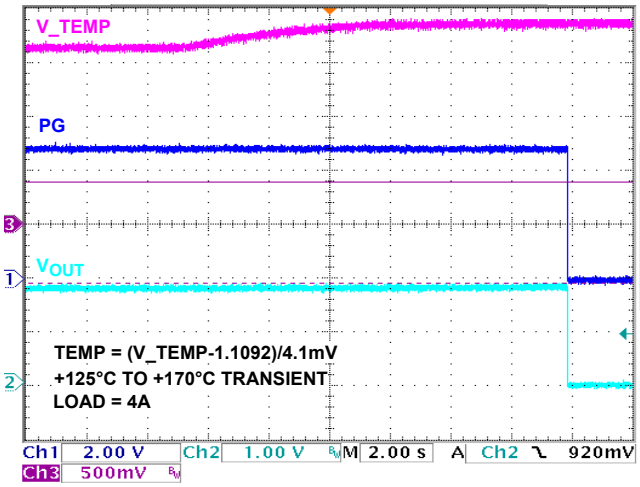


FIGURE 42. OVER-TEMPERATURE PROTECTION

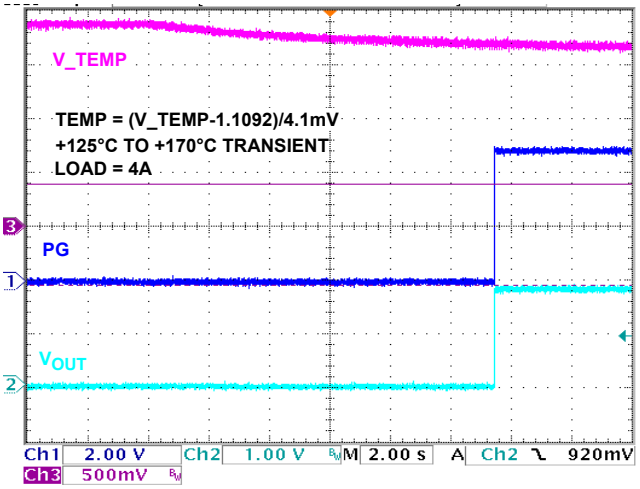


FIGURE 43. OVER-TEMPERATURE RECOVERY

Theory of Operation

The ISL78235 is a step-down switching regulator optimized for automotive point-of-load powered applications. The regulator operates at a 2MHz default switching frequency for high efficiency and smaller form factor while staying out of the AM frequency band. By connecting a resistor from FS to SGND, the operational frequency is adjustable in the range of 500kHz to 4MHz. At light load, the regulator reduces the switching frequency by operating in Pulse Frequency Modulation (PFM) mode, unless forced to operate in fixed frequency PWM mode, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 45µA. The supply current is typically only 3.8µA when the regulator is shut down.

PWM Control Scheme

Pulling the SYNC pin HI (>0.8V) forces the converter into PWM mode, regardless of output current, bypassing the PFM operation at light load. The ISL78235 uses the current-mode Pulse-Width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting (see Figure 3 on page 3). The current loop consists of the oscillator, the PWM comparator, current-sensing circuit, and the slope compensation for the current loop stability. The slope compensation is 440mV/Ts (Ts is the switching period), which changes proportionally with frequency. The gain for the current-sensing circuit is typically 170mV/A. The control reference for the current loops comes from the Error Amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the PFET and turn on the N-channel MOSFET. The NFET stays on until the end of the PWM cycle. Figure 44 shows the typical operating waveforms during the PWM operation. The dotted lines on V_{CSA} illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and is discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 55pF and 100kΩ RC network. The maximum EAMP voltage output is precisely clamped to 2.5V.

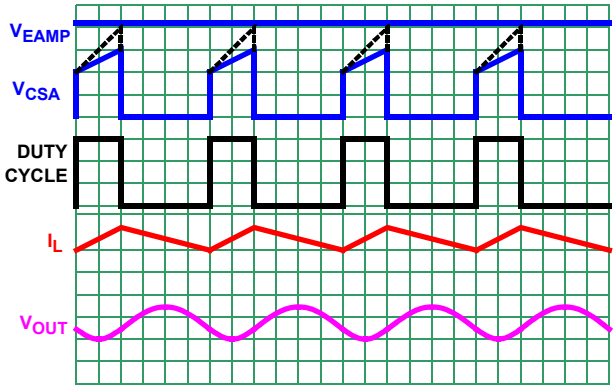


FIGURE 44. PWM OPERATION WAVEFORMS

Skip Mode (PFM)

Pulling the SYNC pin low (<0.4V), forces the converter into PFM mode. The ISL78235 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 45 on page 17 illustrates Skip mode operation. A zero-cross sensing circuit shown in Figure 3 on page 3 monitors the NFET current for zero crossing. When 16 consecutive cycles are detected, the regulator enters Skip mode. During the 16 detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

When Skip mode is entered, the pulse modulation starts being controlled by the Skip comparator shown in Figure 3 on page 3. Each pulse cycle is still synchronized by the PWM clock. The PFET is turned on at the clock's rising edge and turned off when the output is higher than 1.2% of the nominal regulation or when its current reaches the peak skip current limit value. Then, the inductor current discharges to 0A and stays at zero (the internal clock is disabled), and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the PFET is turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.2% below the nominal voltage.

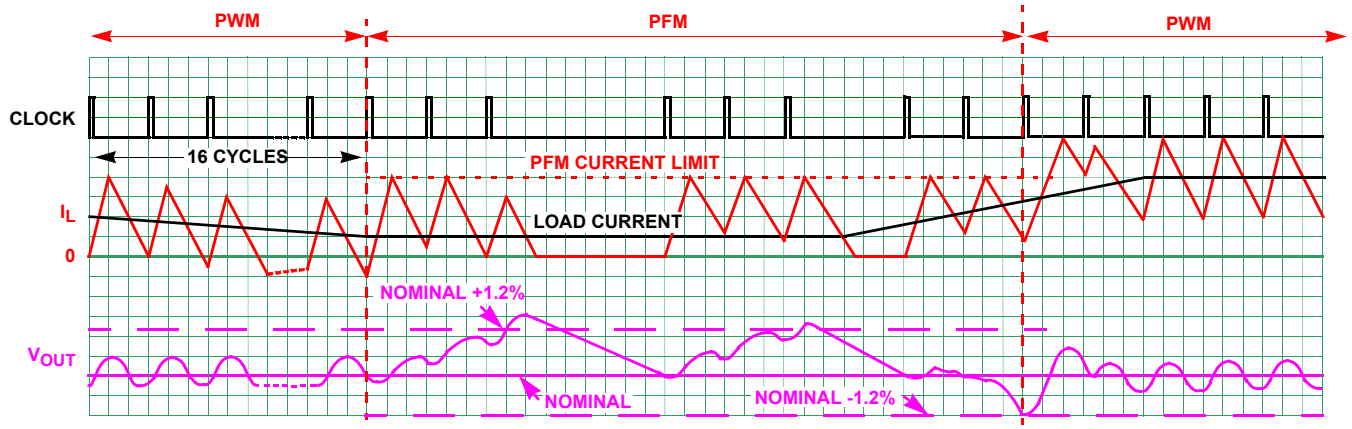


FIGURE 45. SKIP MODE OPERATION WAVEFORMS

Frequency Adjust

The frequency of operation is fixed at 2MHz when FS is tied to VIN. The switching frequency is adjustable in the range from 500kHz to 4MHz with a resistor from FS to SGND according to Equation 1:

$$R_{FS}[k\Omega] = \frac{220 \cdot 10^3}{f_{OSC}[kHz]} - 14 \quad \text{(EQ. 1)}$$

Connect the SYNC pin to an external square pulse waveform to enable the ISL78235's frequency synchronization capability. The frequency synchronization feature synchronizes the positive edge trigger and its switching frequency up to 4MHz. The synchronization positive pulse width should be 100ns or greater for proper operation. The minimum external SYNC frequency is half of the free running oscillator frequency (either the default 2MHz when FS is tied to VIN or determined by the resistor from FS to SGND).

Overcurrent Protection

The overcurrent protection is enabled by monitoring the CSA output with the OCP comparator, as shown in Figure 3 on page 3. The current-sensing circuit has a gain of 170mV/A typical, from the PFET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripped to turn off the PFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

When an overcurrent condition is detected, the upper MOSFET is immediately turned off and is not turned on again until the next switching cycle. When the initial overcurrent condition is detected, the overcurrent fault counter is set to 1. The OC fault counter is incremented if another overcurrent condition is detected on the subsequent cycle. If 17 sequential OC fault detections occur, the regulator is shut down under an overcurrent fault condition. An overcurrent fault condition causes the regulator to attempt to restart in hiccup mode within the delay of eight soft-start periods. At the end of the eighth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition stops during the delay of eight soft-start periods, the output will resume back into the regulation point after hiccup mode expires.

Negative Current Protection

Similar to overcurrent, the negative current protection is enabled by monitoring the current across the low-side NFET, as shown in Figure 3 on page 3. When the valley point of the inductor current reaches -3A for four consecutive cycles, both PFET and NFET are off. A 100Ω discharge circuit in parallel to the NFET activates to discharge the output into regulation. The regulator resumes switching operation when the output is within regulation. The regulator will be in PFM for 20µs before switching to PWM if necessary.

PG

PG is an open-drain output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. PG is a 1ms delay after the soft-start period that becomes high impedance as long as the output voltage is within the nominal regulation voltage set by VFB. When the voltage at the FB pin drops 15% below 0.6V or rises above 0.8V, the ISL78235 pulls PG low. Any fault condition forces PG low until the fault condition is cleared and after soft-start completes. For logic level output voltages, connect an external pull-up resistor between PG and VIN. A 100kΩ resistor works well in most applications.

UVLO

When the input voltage is below the Undervoltage Lockout (UVLO) threshold (2.5V typical), the regulator is disabled.

Soft Start-Up

The soft start-up circuit reduces the inrush current during power- up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the slew rate of inductor current as well as the output voltage, so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz, so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in Skip mode to support prebiased output conditions.

Tie SS to SGND for internal soft-start (1ms typical). Connect a capacitor from SS to SGND to adjust the soft-start time. This capacitor, along with an internal 2.1µA current source, sets the soft-start interval of the converter, t_{SS}, as shown by Equation 2.

$$C_{SS}[\mu F] = 3.1 \cdot t_{SS}[s] \quad \text{(EQ. 2)}$$

C_{SS} must be less than 33nF to ensure proper soft-start reset after fault condition.

Enable

The Enable (EN) input allows the user to turn the regulator on or off for purposes such as power-up sequencing or minimizing power dissipation when the output is not needed. When the regulator is enabled, a typical 600µs delay occurs for waking up the bandgap reference, then the soft start-up begins. EN should be held below the EN_VIL until V_{IN} exceeds V_{UVLO} rising.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs, (EN low or fault condition) or the V_{IN} UVLO is set, the output is discharged to GND through an internal 100Ω switch on the PHASE pin.

Power MOSFETs

The power MOSFETs are optimized for highest efficiency. The ON-resistance for the PFET is typically 35mΩ and the ON-resistance for the NFET is typically 11mΩ.

100% Duty Cycle

The ISL78235 features a 100% duty cycle operation to maximize the battery operation life and provide very low dropout down to the minimum operating voltage. When the battery voltage drops to a level that the ISL78235 can no longer maintain the regulation at the output, the regulator completely turns on the PFET. The maximum dropout voltage under the 100% duty cycle operation is the product of the load current and the ON-resistance of the PFET.

Thermal Shutdown

The ISL78235 has built-in over-temperature thermal protection. When the internal temperature reaches +150°C, the regulator completely shuts down. As the temperature drops to +125°C, the ISL78235 resumes operation after a soft-start cycle.

Applications Information

Output Inductor and Capacitor Selection

The ISL78235 typically uses a 0.33µH to 0.78µH output inductor for steady state and transient operation. Higher or lower inductor values can be used to optimize the total converter system performance. For example, the output inductor value can be increased for a higher output voltage 3.3V application in order to decrease the inductor current ripple and output voltage ripple. Set the ripple inductor current to approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 3:

$$\Delta I = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \bullet f_{SW}} \quad \text{(EQ. 3)}$$

The inductor's saturation current rating must be larger than the positive peak current limit specified on page 7 of the Electrical Specifications table. The ISL78235 has a typical peak current limit of 7.5A. The inductor saturation current must be over 7.5A for proper operation.

The ISL78235 uses an internal compensation network for regulator stability and the output capacitor value is dependent on the output voltage. The recommended ceramic capacitors are low ESR X7R rated or better. The recommended minimum output capacitor values are shown in Table 2 on page 6.

Table 2 shows that the minimum output capacitor value is given for the different output voltages to ensure that the whole converter system is stable. Additional output capacitance should be added for better performance in applications in which high load transient or low output ripple is required. Renesas recommends checking the system level performance along with the simulation model.

Output Voltage Selection

The output voltage of the regulator is programmed with an external resistor divider that scales the output voltage relative to the internal reference voltage (0.6V) and is fed back to the inverting input of the error amplifier FB pin (see Figure 46).

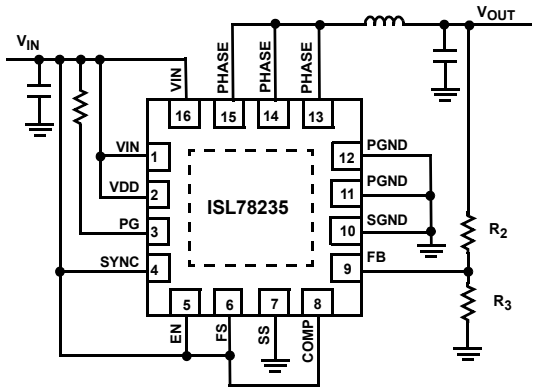


FIGURE 46. PROGRAMMING OUTPUT VOLTAGE WITH R_2 AND R_3

The output voltage programming resistor R_2 (from VOUT to FB) depends on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor, R_3 (from FB to GND), is typically between 10kΩ and 100kΩ. R_2 is chosen as shown in Equation 4, where VFB = 0.6V and V_{OUT} is the output voltage.

$$R_2 = R_3\left(\frac{V_{OUT}}{VFB} - 1\right) \quad \text{(EQ. 4)}$$

There is a leakage current from VIN to PHASE. Renesas recommends preloading the output with 10µA minimum for accurate output voltage. For improved loop stability performance, add 10pF to 22pF in parallel with R_2. Check loop analysis before use in an application. See "Loop Compensation Design" for more information.

Input Capacitor Selection

The main functions for the input capacitor are decoupling the parasitic inductance and providing a filtering function to prevent the switching current flowing back to the input rail. Place two 22µF low ESR X7R rated ceramic capacitors in parallel with a 0.1µF high frequency decoupling capacitor very close to the VIN/VDD and SGND/PGND pins.

Loop Compensation Design

When COMP is not connected to VDD, the COMP pin is active for external loop compensation. The ISL78235 uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current-sensing circuit in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered a state variable because its peak current is constant and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 47 shows the small signal model of the synchronous buck regulator.

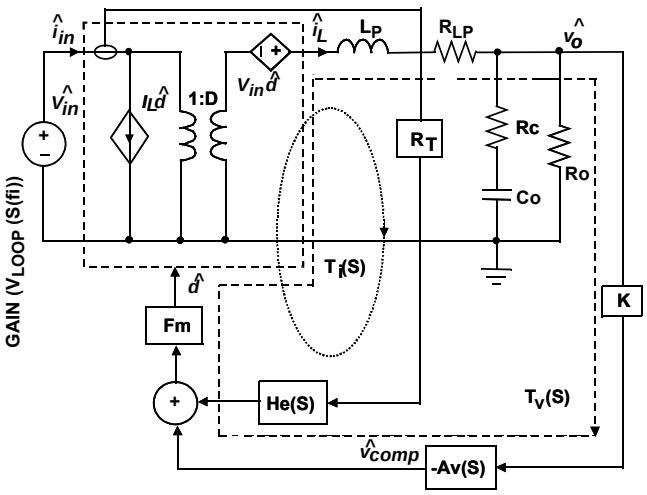


FIGURE 47. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

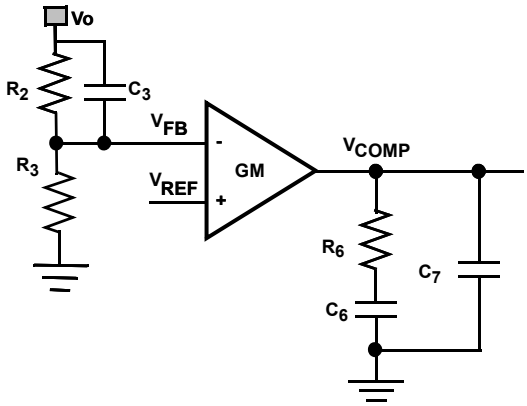


FIGURE 48. TYPE II COMPENSATOR

Figure 48 shows the type II compensator and its transfer function is expressed as Equation 5:

$$A_V(S) = \frac{\hat{v}_{comp}}{\hat{v}_{FB}} = \frac{GM \cdot R_3}{(C_6 + C_7) \cdot (R_2 + R_3)} \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp1}}\right)\left(1 + \frac{S}{\omega_{cp2}}\right)} \quad \text{(EQ. 5)}$$

where

$$\omega_{cz1} = \frac{1}{R_6 C_6},\ \omega_{cz2} = \frac{1}{R_2 C_3},\ \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7},\ \omega_{cp2} = \frac{R_2 + R_3}{C_3 R_2 R_3}$$

Compensator design goal:

High DC gain
Choose Loop bandwidth f_c ~100kHz or less
Gain margin: >10dB
Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has a unity gain. Therefore, the compensator resistance R_6 is determined by Equation 6.

$$R_6 = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} = 13.7 \times 10^3 \cdot f_c V_o C_o \quad \text{(EQ. 6)}$$

where GM is the transconductance, g_m, of the voltage error amplifier and R_t is the gain of the current sense amplifier. Compensator capacitors C_6 and C_7 are given by Equation 7.

$$C_6 = \frac{R_o C_o}{R_6} = \frac{V_o C_o}{I_o R_6}, C_7 = \max\left(\frac{R_c C_o}{R_6}, \frac{1}{\pi f_s R_6}\right) \quad \text{(EQ. 7)}$$

Set one compensator pole at zero frequency to achieve high DC gain, and set another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower in Equation 7. An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_2 and C_3.

Set compensator zero 2 to 5 times f_c:

$$C_3 = \frac{1}{\pi f_c R_2} \quad \text{(EQ. 8)}$$

Example: V_{IN} = 5V, V_O = 1.8V, I_O = 5A, f_{SW} = 2MHz, R_2 = 200kΩ, R_3 = 100kΩ, C_o = 2 x 22µF/10mΩ, L = 0.68µH, f_c = 100kHz, then compensator resistance R_6:

$$R_6 = 13.7\times10^3 \cdot 100kHz \cdot 1.8V \cdot 44\mu F = 108k\Omega \quad \text{(EQ. 9)}$$

It is acceptable to use 107kΩ as the closest standard value for R_6.

$$C_6 = \frac{1.8V \cdot 44\mu F}{5A \cdot 107k\Omega} = 148pF \quad \text{(EQ. 10)}$$

$$C_7 = \max\left(\frac{10m\Omega \cdot 44\mu F}{107k\Omega}, \frac{1}{\pi \cdot 2MHz(107k\Omega)}\right) = (4.1pF, 1.5pF) \quad \text{(EQ. 11)}$$

It is also acceptable to use the closest standard values for C_6 and C_7. There is approximately 3pF parasitic capacitance from V_{COMP} to GND. Therefore, C_7 is optional. Use C_6 = 150pF and C_7 = OPEN.

$$C_3 = \frac{1}{\pi 100kHz \cdot 200k\Omega} = 16pF \quad \text{(EQ. 12)}$$

Use C_3 = 10pF. Note that C_3 may increase the loop bandwidth from the previous estimated value. Figure 49 shows the simulated voltage loop gain. It has a 120kHz loop bandwidth with a 58° phase margin and 8dB gain margin. It may be more desirable to achieve an increased phase and gain margin. This can be accomplished by lowering R_6 by 10% to 20%.

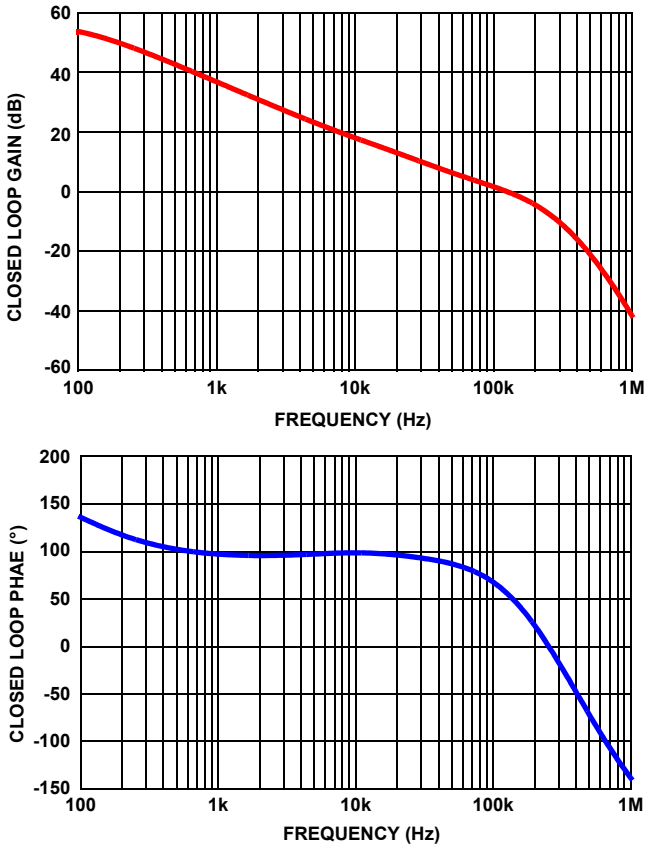


FIGURE 49. SIMULATED LOOP GAIN AND PHASE

PCB Layout Recommendation

Proper PCB layout is a very important converter design step to ensure the designed converter works well. The ISL78235 power loop is composed of the output inductor L_O, the output capacitor C_O, the PHASE pins, and the PGND pin. Make the power loop as small as possible. The connecting traces among them should be direct, short, and wide. The switching node of the converter, the PHASE pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. Place the input capacitor as close as possible to the VIN pin. The ground of the input and output capacitors should be connected as close as possible. The IC heat is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. Refer to TB389 for information about via placement on the copper area of the PCB underneath the thermal pad for optimum thermal performance.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Sep 28, 2018	FN8713.7	Updated Related Literature Section Updated the Ordering Information table on page 5. Added Note 9 on page 8. Added specification symbols for the Logic Input Low and Logic Input High specifications on page 8. Added information about EN_VIL to the “Enable” section on page 18. Removed About Intersil section and updated disclaimer.
Sep 22, 2016	FN8713.6	Corrected shifted connection in Block Diagram on page 3.
Apr 1, 2016	FN8713.5	Updated Figure 10 title on page 9.
Dec 11, 2015	FN8713.4	Added a new User Guide to Related Literature section on page 1. Added ISL78235EVAL2Z to the ordering information table on page 5. Added table1 on page 5.
Nov 10, 2015	FN8713.3	Added 5x5mmWFQFN information throughout datasheet. Removed “Li-Ion Battery Powered devices” application bullet from page 1. Updated Note 1 on page 5 from “Add “-T*” suffix for tape and reel.” to “Add “-T” suffix for 6k unit or “-T7A” suffix for 250 unit tape and reel options.” On page 8, removed the test condition “T_A = -40°C to +105°C” for the I_{NLIMIT} specifications. On page 8, added “T_A = -40°C to +105°C to the test conditions of the Transresistance specification.” In “PWM Control Scheme” on page 16 (last sentence) corrected a typo by changing “1.6V to “2.5V”. Updated the “PCB Layout Recommendation” section.
Jul 1, 2015	FN8713.2	Figures 15 through 28 changed “CSS = 33nF” to “SS = GND”.
Feb 20, 2015	FN8713.1	Electrical Spec table, Oscillator section on page 8: Changed nominal switching frequency minimum from 1700kHz to 1730kHz.
Feb 3, 2015	FN8713.0	Initial Release

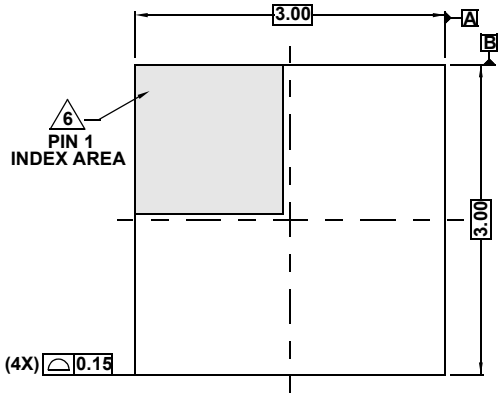
Package Outline Drawing

For the most recent package outline drawing, see L16.3x3D.

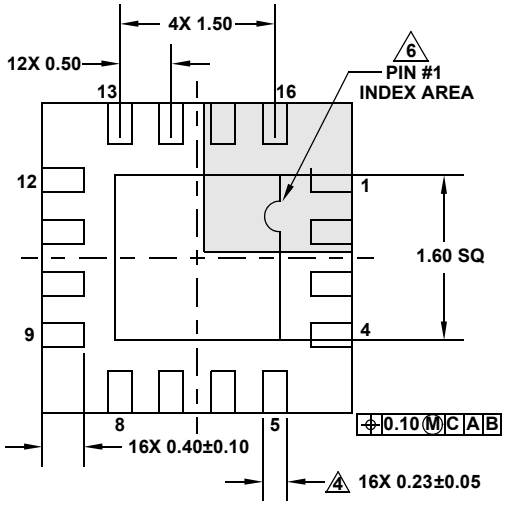
L16.3x3D

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

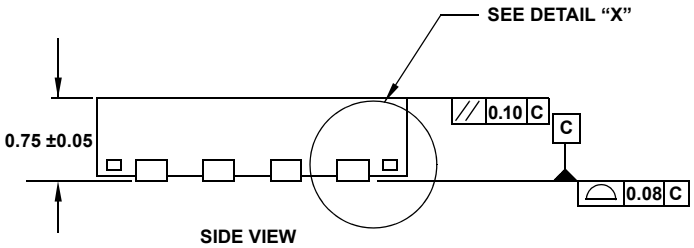
Rev 0, 3/10



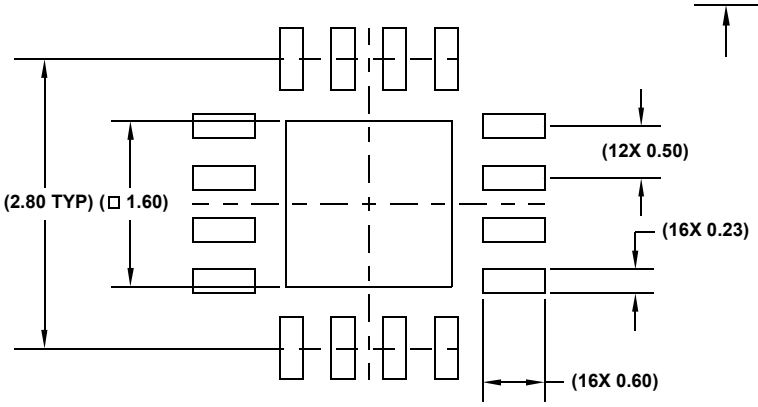
TOP VIEW



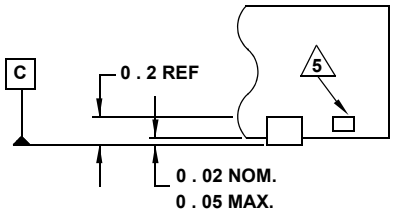
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.

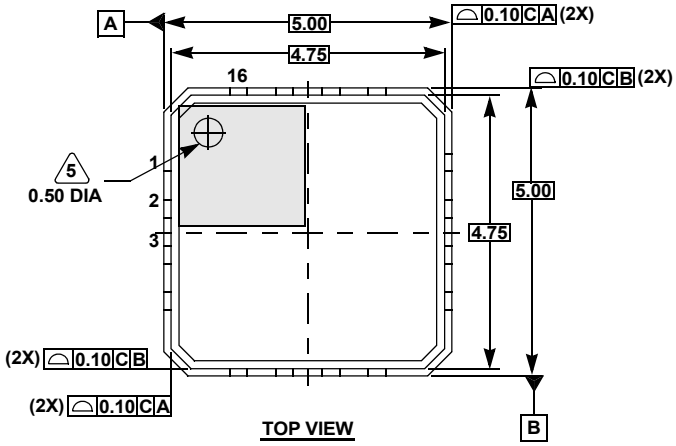
Package Outline Drawing

For the most recent package outline drawing, see L16.5x5D.

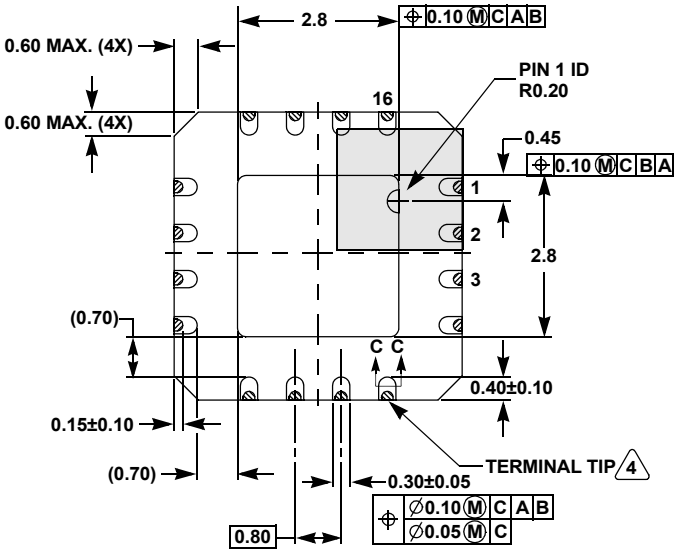
L16.5x5D

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN WITH WETTABLE FLANK)

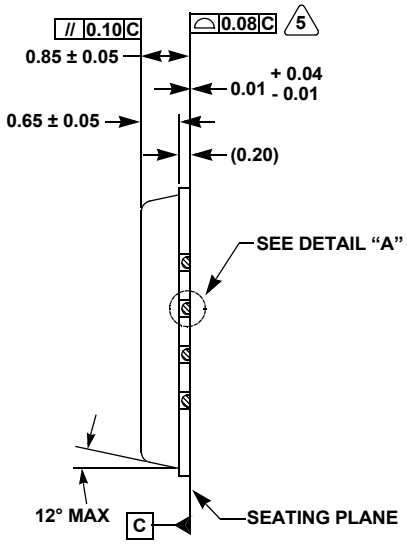
Rev 2, 5/14



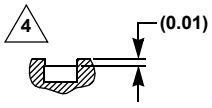
TOP VIEW



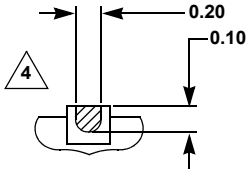
BOTTOM VIEW



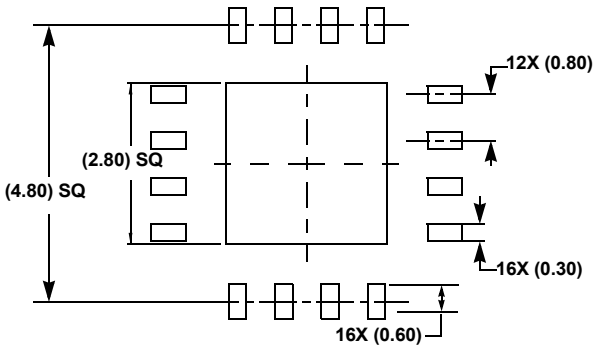
SIDE VIEW



SECTION "C-C"
SCALE: NONE



DETAIL "A" (DIMPLE DEPTH)
SCALE: NONE



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) are for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Reference document: JEDEC M0220.

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Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

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Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
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