SM840004-11

62.5/125MHz Gigabit Ethernet, 4 Output, Ultra-Low Jitter Clock Synthesizer

General Description

The SM840004-11 clock synthesizer was designed for Gigabit Ethernet applications. The device design is optimized for 62.5MHz and 125MHz using a standard 25MHz fundamental parallel resonant crystal, with unparalleled stability and accuracy over the full operating range, and provides an easy fit for Jitter and Phase Noise standards for these high performance interfaces.

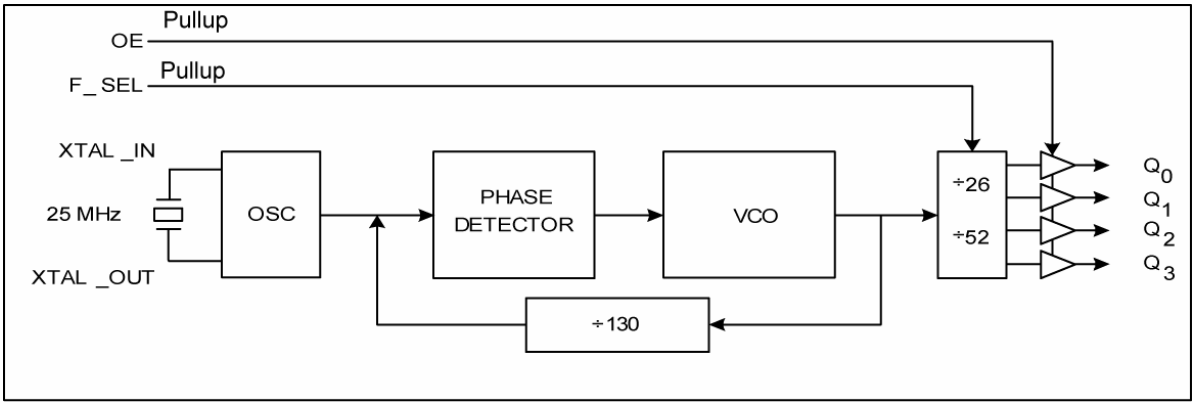
The SM840004-11 design includes a unique power reduction methodology, along with a patented RotaryWave™ architecture, that provides a stable clock with very low noise for optimized performance. This yields an overall improved Bit Error Rate (BER) and improved waveform integrity.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Generates 4 optimized LVCMOS clock outputs
- RMS phase jitter @ 125MHz: ~55 fs (typ)
- Integrated loop filter components
- Operates with either a 3.3V or 2.5V supply
- Power consumption 65mA (typ @ 2.5V)
- Selectable output frequency: 125MHz or 62.5MHz
- Input frequency of 25MHz
- Fundamental parallel resonant crystal interface
- Pin compatible with the ICS/IDT840004-11
- Industrial temperature range: –40°C to +85°C
- Green, RoHS-compliant and PFOS-compliant

Block Diagram



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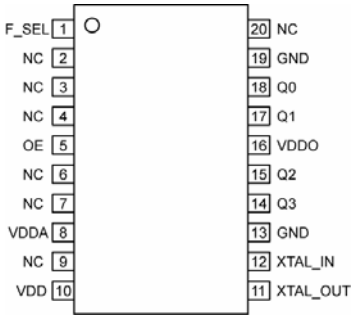
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking
SM840004-11KA	K-20	Industrial	840004-11
SM840004-11KA TR	K-20	Industrial	840004-11

Note:

1. Devices are Green, RoHS-compliant and PFOS-compliant.

Pin Configuration



20-Pin TSSOP (K-20)

Pin Description

Pin Number	Pin Name	Type	Level	Pin Function
1	F_SEL	I	Pull-up	Frequency Select Pin.
2,3,4,6,7,9,20	NC		NC	No Connect. Do Not Use.
5	OE	I	Pull-up	Output Enable: (1=Active, 0=High-Z)
8	V_{DDA}	P		Analog Power.
10	V_{DD}	P		Core Power.
11	XTAL_OUT	O		Crystal Out.
12	XTAL_IN	I		Crystal In.
13,19	GND	P		Ground.
14	Q3	O		Single Ended LVCMOS Clock Out-3.
15	Q2	O		Single Ended LVCMOS Clock Out-2.
16	V_{DDO}	P		Output Power Supply.
17	Q1	O		Single Ended LVCMOS Clock Out-1.
18	Q0	O		Single Ended LVCMOS Clock Out-0.

Configuration Table

F_SEL	M/N Ratio	M Divider	N Divider	Output Frequency (MHz)
0	2.5	130	52	62.5
1	5	130	26	125

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to V_{DD}+0.5V
Output Voltage (V_{OUT}) ..... –0.50V to V_{DD}+0.5V
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
TSSOP (θ_{JA}) ..... 113°C/W

DC Electrical Characteristics

V_{DD} = 2.5V ±5%; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		2.375	2.50	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.50	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.50	2.625	V
I_{DD}	Power Supply Current			0.1	1	mA
I_{DDA}	Analog Supply Current			50	60	mA
I_{DD0}	Output Supply Current	No Load		15	23	mA

DC Electrical Characteristics

V_{DD} = 3.3V ±5%; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		3.135	3.30	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.30	3.465	V
VDDO	Output Supply Voltage		3.135	3.30	3.465	V
I_{DD}	Power Supply Current			0.1	1	mA
I_{DDA}	Analog Supply Current			50	60	mA
I_{DDO}	Output Supply Current	No Load		25	32	mA

LVCMOS DC Electrical Characteristics

T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	V_{DD} = 3.3V ±5%	2		V_{DD} +0.3	V
		V_{DD} = 2.5V ±5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	V_{DD} = 3.3V ±5%	-0.30		0.80	V
		V_{DD} = 2.5V ±5%	-0.30		0.70	V
V_{OH}	Output HIGH Voltage	V_{DD} = 3.3V ±5%	2.6			V
		V_{DD} = 2.5V ±5%	1.8			V
V_{OL}	Output LOW Voltage				0.5	V
I_{IH}	Input HIGH Current	Output Enable input			5	µA
I_{IL}	Input LOW Current	Output Enable input	-150			µA
I_{IH}	Input HIGH Current	FSEL input			150	µA
I_{IL}	Input LOW Current	FSEL input	-5			µA

Notes:

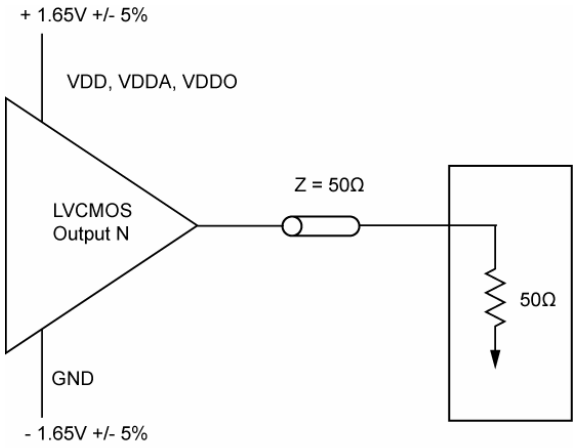
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.

AC Electrical Characteristics

V_{DD} = 2.5V and 3.3V ±5%; T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{OUT}	Output Frequency	F_SEL = 1		125		MHz
		F_SEL = 0		62.5		
t_{SKEW}	Output to Output Skew				12	ps
t_{JITTER}	RMS Phase Jitter(random)	125MHz @ 1.875MHz-20MHz		55		fs
		62.5MHz @ 1.875MHz-20MHz		356		fs
t_R / t_F	Output Rise/Fall Time	20% to 80%		300		ps
ODC	Output Duty Cycle	62.5MHz & 125MHz	48	50	52	%

Test Circuit



3.3V Output Load AC Test Circuit

3.3V Carrier Frequency, 62.5MHz

Offset from Carrier	Measured Phase Noise	Unit
100Hz	-103	dBc/Hz
1kHz	-124	dBc/Hz
10kHz	-137	dBc/Hz
100kHz	-135	dBc/Hz
1MHz	-145	dBc/Hz
1.825MHz	-151	dBc/Hz
10MHz	-169	dBc/Hz
20MHz	-169	dBc/Hz

3.3V Carrier Frequency, 125MHz

Offset from Carrier	Measured Phase Noise	Unit
100Hz	-103	dBc/Hz
1kHz	-125	dBc/Hz
10kHz	-134	dBc/Hz
100kHz	-132	dBc/Hz
1MHz	-143	dBc/Hz
1.825	-152	dBc/Hz
10MHz	-166	dBc/Hz
20MHz	-167	dBc/Hz

Crystal Characteristics

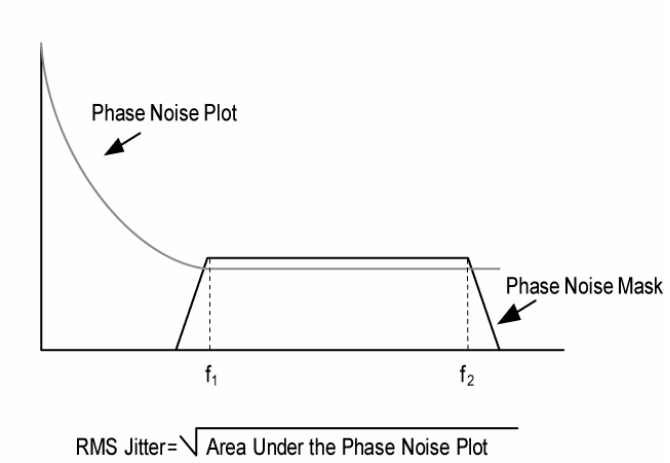
Parameter	Min	Typ	Max	Units
Mode of Oscillation		Fundamental Parallel Resonant		
Frequency		25		MHz
Equivalent Series Resistance (ESR)			50	Ω
Shunt Capacitor			7	pF
Drive Level			1	mW

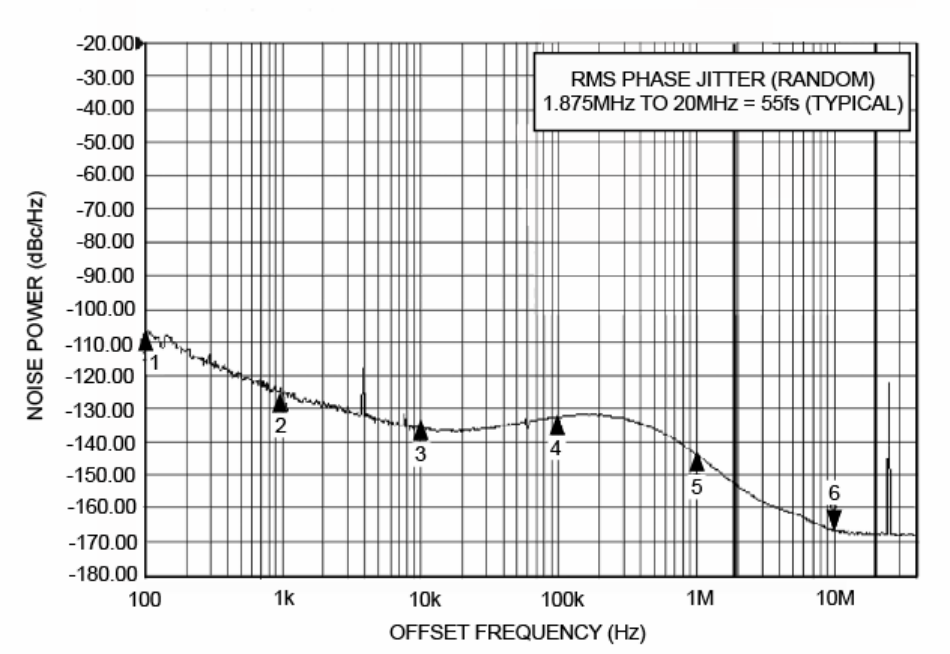
Functional Description

The SM840004-11 provides a high performance and high accuracy solution for a precision clock source at either 62.5MHz or 125MHz derived from a low cost 25MHz Xtal. Four synchronous low skew 12mA capable LVCMOS outputs are provided with tri state controlled via an external pin (OE).

The design of the SM840004-11 consumes very low power in the PLL due to a patented technology in the VCO and the associated dividers. The VCO range is ~3.2GHz to 3.5GHz providing high resolution and easy integer divide ratios. Output divider ratios are fixed at either ÷26 or ÷52 via the F_SEL pin, and the feedback divider is fixed at ÷130. Duty Cycle is inherently improved and provides tight control and stability on this critical specification. This provides improved specifications for Duty Cycle, Jitter, Phase Noise, Power Consumption, and noise sensitivity. Additionally, the SM840004-11 will operate at either 3.3V or 2.5V supplies.

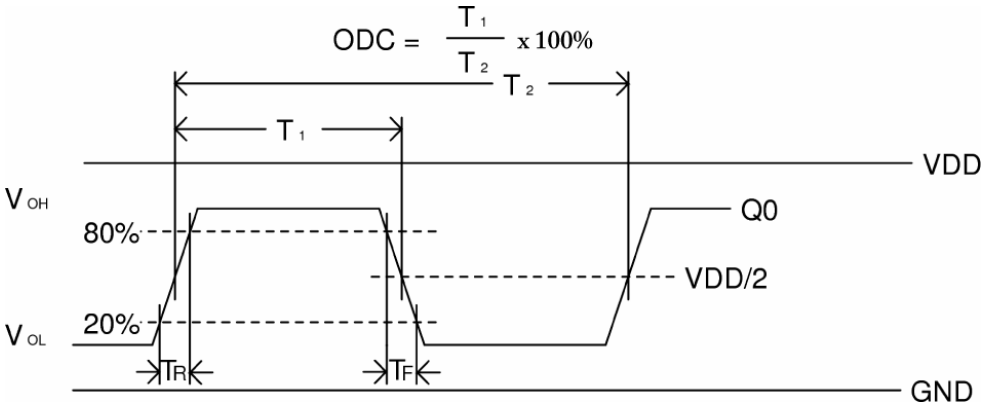
RMS Phase Noise/Jitter



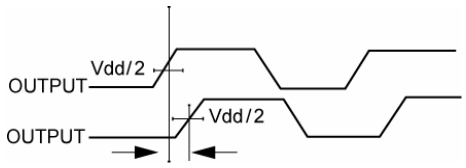


Phase Noise Plot 125MHz @ 3.3V

Switching Waveforms



Output Rise/Fall Time



Output-Output Skew

Power Supply Filtering

The SM840004-11 provides separate power supply pins to isolate any high switching noise from outputs to internal core blocks. VDD and VDDA should be individually connected to the power plane through vias. Bypass capacitors should be used for each pin. Figure 2, illustrates how the power supply filter for 3.3V and 2.5V is configured.

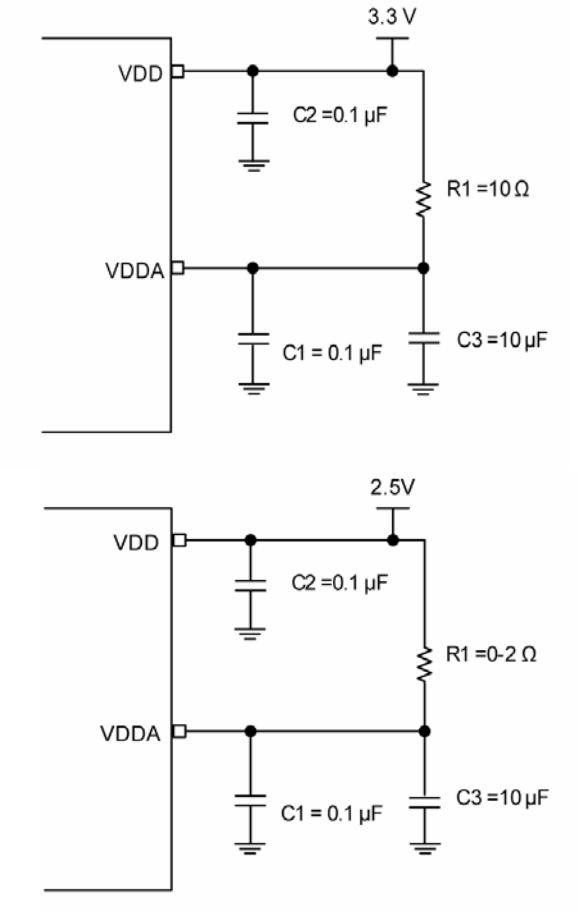
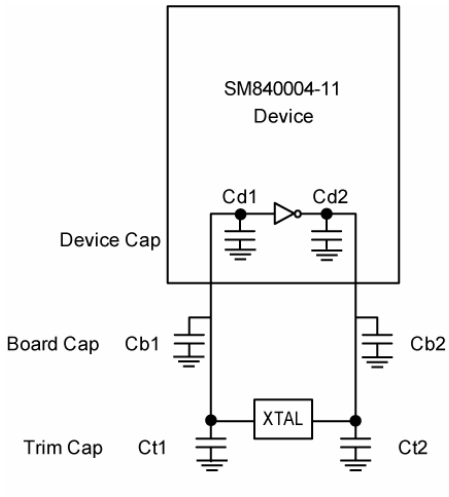


Figure 2. Power Supply Filter

Crystal Loading



Crystal Recommendations

This device requires a parallel resonance crystal. Substituting a series resonance crystal will cause this device to operate at the wrong frequency and violate the ppm specifications.

To achieve low ppm error, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Load Capacitance at each side: Trim Capacitance = Ct = (2*CL-(Cb + Cd))

CL: Crystal load capacitance. Defined by manufacturer

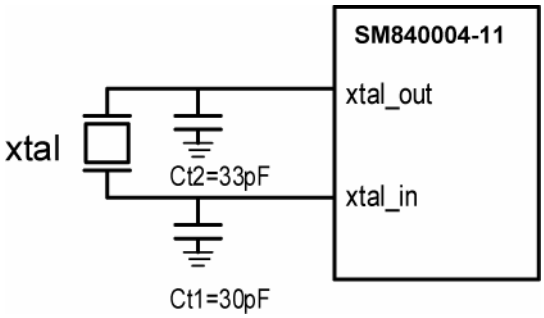
Ct: External trim capacitors. (Trimmed CL Load capacitance to get the right ppm)

Cb: Board capacitance (vias, traces, etc.)

Cd: Internal capacitance of the device (lead frame, bond wires, pin, etc.)

Equivalent Series Resistance (ESR) Max.	Cut	Load Cap.	Shunt Cap. Max.	Drive Max.
50Ω	AT	18pF	7pF	0.1mW

Crystal Input Interface



hbwhelp@micrel.com or (408) 955-1690

Total capacitance seen by crystal = CL =

$$\frac{1}{\frac{1}{(Ct1 + Cb1 + Cd1)} + \frac{1}{(Ct2 + Cb2 + Cd2)}}$$

Example:

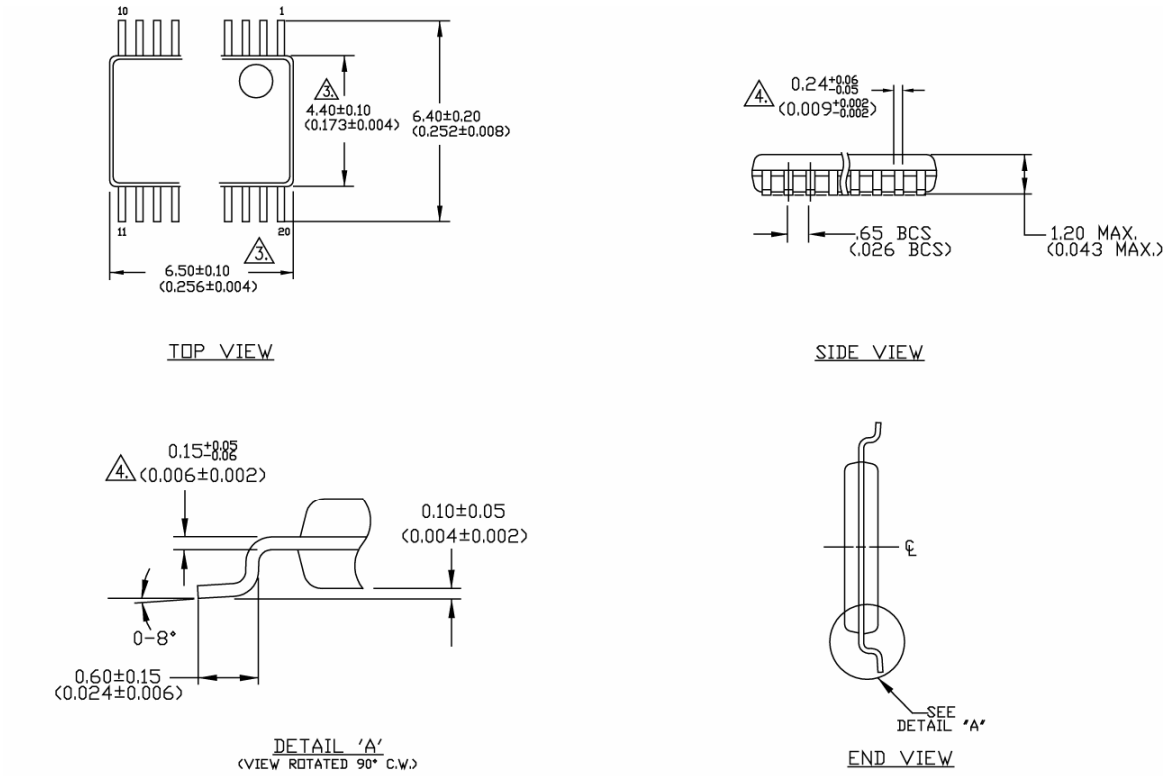
CL = 18pF, Cb = 2pF, Cd = 4pF

Trim Cap = Ct = 2 (18pF) - (2pF +4pF) = 30pF

The SM840004-11has been characterized with 19.44MHz, 18pF parallel resonant crystal. The trim capacitors Ct1 and Ct2 were optimized to minimize the ppm error.

To minimize the board capacitance, a short trace from pin to crystal footprint without vias is desirable. It is preferable to have ground shielding or distance between the crystal traces and noisy signals on the board.

Package Information



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

20-Pin TSSOP (K-20)

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