Si53112-A03A

DB1200ZL 12-Output PCIe Gen 3 Buffer

Features

- Twelve 0.7 V low-power, push-pull, HCSL-compatible PCIe Gen 3 outputs
- Individual OE HW pins for each output clock
- 100 MHz /133 MHz PLL operation, supports PCIe and QPI
- PLL bandwidth SW SMBUS programming overrides the latch value from HW pin
- 9 selectable SMBUS addresses
- SMBus address configurable to allow multiple buffers in a single control network 3.3 V supply voltage operation
- Integrated termination resistors supporting 85 Ω transmission lines
- PLL or bypass mode
- Spread spectrum tolerable
- 1.05 to 3.3 V I/O supply voltage
- 50 ps output-to-output skew
- 50 ps cyc-cyc jitter (PLL mode)
- Low phase jitter (Intel QPI, PCIe Gen 1/2/3/4 common clock compliant)
- Gen 3 SRNS Compliant
- 100 ps input-to-output delay
- Extended Temperature: –40 to 85 °C
- Package: 64-pin QFN
- For higher output devices or variations of this device, contact Silicon Labs

Ordering Information:
See page 30.

Patents pending

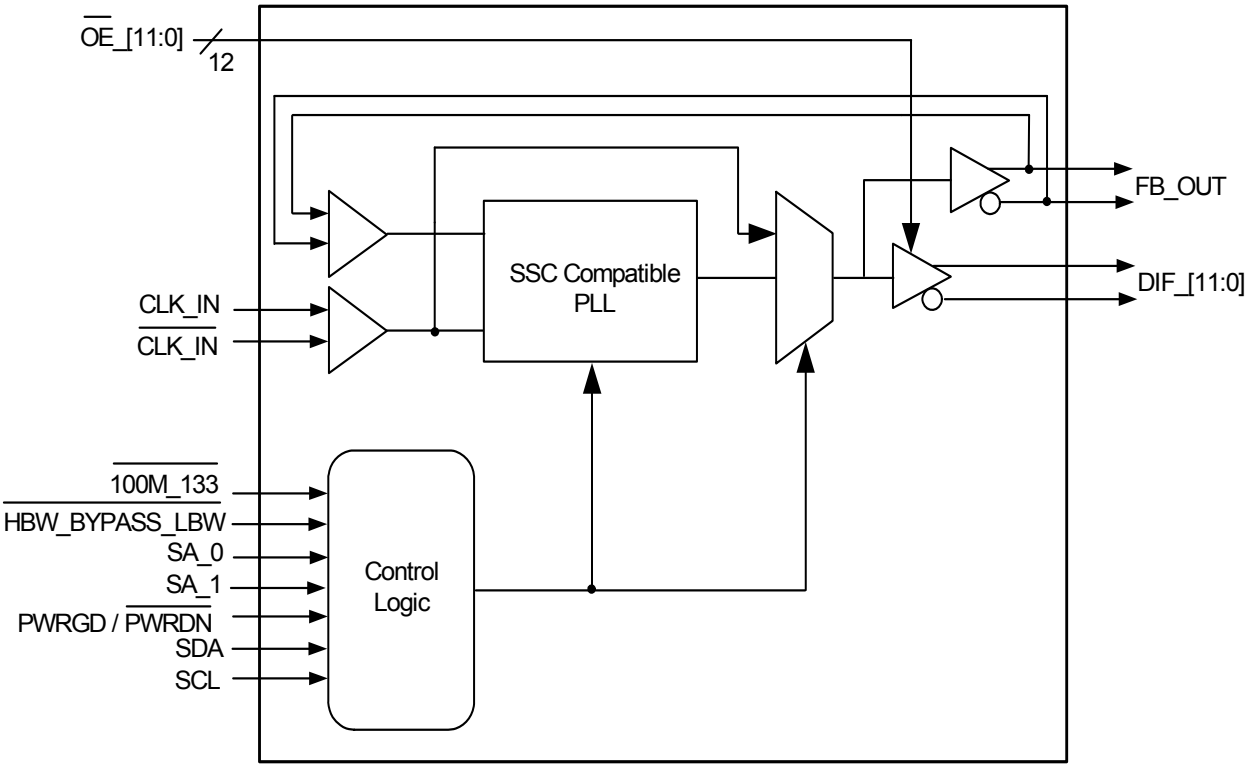
Applications

- Server
- Storage
- Data center
- Enterprise Switches and Routers

Description

The Si53112-A03A is a low-power, 12-output, differential clock buffer that meets all of the performance requirements of the Intel DB1200ZL specification. To reduce board space and bill of material cost, the device fully integrates all external resistors, supporting 85 Ω transmission lines. The device is optimized for distributing reference clocks for Intel® QuickPath Interconnect (Intel QPI), PCIe Gen 1/Gen 2/Gen 3/Gen 4, SAS, SATA, and Intel Scalable Memory Interconnect (Intel SMI) applications. The VCO of the device is optimized to support 100 MHz and 133 MHz operation. Each differential output has a dedicated hardware output enable pin for maximum flexibility and power savings. Measuring PCIe clock jitter is quick and easy with the Silicon Labs PCIe Clock Jitter Tool. Download it for free at www.silabs.com/pcie-learningcenter.

Functional Block Diagram



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1. Electrical Specifications

Table 1. DC Operating Characteristics

V_{DD_A} = 3.3 V±5%, V_{DD} = 3.3 V±5%

Parameter	Symbol	Test Condition	Min	Max	Unit
3.3 V Core Supply Voltage	VDD/VDD_A	3.3 V ±5%	3.135	3.465	V
3.3 V I/O Supply Voltage[1]	VDD_IO	1.05 V to 3.3 V ±5%	0.9975	3.465	V
3.3 V Input High Voltage	V_{IH}	VDD	2.0	VDD+0.3	V
3.3 V Input Low Voltage	V_{IL}		VSS-0.3	0.8	V
Input Leakage Current[2]	I_{IL}	0 < VIN < VDD	–5	+5	µA
3.3 V Input High Voltage[3]	V_{IH_FS}	VDD	0.7	VDD+0.3	V
3.3 V Input Low Voltage[3]	V_{IL_FS}		VSS–0.3	0.35	V
3.3 V Input Low Voltage	V_{IL_Tri}		0	0.8	V
3.3 V Input Med Voltage	V_{IM_Tri}		1.2	1.8	V
3.3 V Input High Voltage	V_{IH_Tri}		2.2	VDD	V
3.3 V Output High Voltage[4]	V_{OH}	I_{OH} = –1 mA	2.4	—	V
3.3 V Output Low Voltage[4]	V_{OL}	I_{OL} = 1 mA	—	0.4	V
Input Capacitance[5]	C_{IN}		2.5	4.5	pF
Output Capacitance[5]	C_{OUT}		2.5	4.5	pF
Pin Inductance	L_{PIN}		—	7	nH
Ambient Temperature	T_A	No Airflow	–40	85	°C

Notes:

1. VDD_IO applies to the low-power NMOS push-pull HCSL compatible outputs.
2. Input Leakage Current does not include inputs with pull-up or pull-down resistors. Inputs with resistors should state current requirements.
3. Internal voltage reference is to be used to guarantee V_{IH}_FS and V_{IL}_FS thresholds levels over full operating range.
4. Signal edge is required to be monotonic when transitioning through this region.
5. Ccomp capacitance based on pad metallization and silicon device capacitance. Not including pin capacitance.

Table 2. Current Consumption

T_A = –40 to 85 °C; supply voltage V_{DD} = 3.3 V ±5%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Current	IDD_{VDD}	133 MHz, VDD Rail, Zo=85 Ω	—	18	25	mA
	IDD_{VDDA}	133 MHz, VDDA + VDDR, PLL Mode, Zo=85 Ω	—	17	20	mA
	IDD_{VDDIO}	133 MHz, CL = Full Load, VDD IO Rail, Zo=85 Ω	—	85	110	mA
Power Down Current	IDD_{VDDPD}	Power Down, VDD Rail	—	0.4	1	mA
	IDD_{VDDAPD}	Power Down, VDDA Rail	—	2	5	mA
	$IDD_{VDDIOPD}$	Power Down, VDD_IO Rail	—	0.2	0.5	mA

Table 3. Output Skew, PLL Bandwidth and Peaking

T_A = –40 to 85 °C; supply voltage V_{DD} = 3.3 V ±5%

Parameter	Test Condition	Min	TYP	Max	Unit
CLK_IN, DIF[x:0]	Input-to-Output Delay in PLL Mode Nominal Value[1,2,3,4]	–100	27	100	ps
CLK_IN, DIF[x:0]	Input-to-Output Delay in Bypass Mode \Nominal Value[2,4,5]	2.5	3.3	4.5	ns
CLK_IN, DIF[x:0]	Input-to-Output Delay Variation in PLL mode Over voltage and temperature[2,4,5]	–100	39	100	ps
CLK_IN, DIF[x:0]	Input-to-Output Delay Variation in Bypass Mode Over voltage and temperature[2,4,5]	–250	3.7	250	ps
DIF[11:0]	Output-to-Output Skew across all 12 Outputs (Common to Bypass and PLL Mode)[1,2,3,4,5]	0	20	50	ps
PLL Jitter Peaking	($\overline{HBW\_BYPASS\_LBW}$ = 0)[6]	—	0.4	2.0	dB
PLL Jitter Peaking	($\overline{HBW\_BYPASS\_LBW}$ = 1)[6]	—	0.1	2.5	dB
PLL Bandwidth	($\overline{HBW\_BYPASS\_LBW}$ = 0)[7]	—	0.7	1.4	MHz
PLL Bandwidth	($\overline{HBW\_BYPASS\_LBW}$ = 1)[7]	—	2	4	MHz

Notes:

1. Measured into fixed 2 pF load cap. Input-to-output skew is measured at the first output edge following the corresponding input.
2. Measured from differential cross-point to differential cross-point.
3. This parameter is deterministic for a given device.
4. Measured with scope averaging on to find mean value.
5. All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
6. Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
7. Measured at 3 db down or half power point.

Table 4. Phase Jitter

Parameter	Test Condition	Min	Typ	Max	Unit
Phase Jitter PLL Mode	PCIe Gen 1, Common Clock[1,2,3]	—	29	86	ps
	PCIe Gen 2 Low Band, Common Clock F < 1.5 MHz[1,3,4,5]	—	2.0	3.0	ps (RMS)
	PCIe Gen 2 High Band, Common Clock 1.5 MHz < F < Nyquist[1,3,4,5]	—	1.9	3.1	ps (RMS)
	PCIe Gen 3, Common Clock (PLL BW 2–4 MHz, CDR = 10 MHz)[1,3,4,5]	—	0.45	1.0	ps (RMS)
	PCIe Gen 3 Separate Reference No Spread, SRNS (PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz)[1,3,4,5]	—	0.32	0.71	ps (RMS)
	PCIe Gen 4, Common Clock (PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz)[1,4,5,8]	—	0.45	1.0	ps (RMS)
	Intel® QPI & Intel SMI (4.8 Gbps or 6.4 Gb/s, 100 or 133 MHz, 12 UI)[1,6,7]	—	0.21	0.5	ps (RMS)
	Intel QPI & Intel SMI (8 Gb/s, 100 MHz, 12 UI)[1,6]	—	0.13	0.3	ps (RMS)
	Intel QPI & Intel SMI (9.6 Gb/s, 100 MHz, 12 UI)[1,6]	—	0.11	0.2	ps (RMS)

Notes:

1. Post processed evaluation through Intel supplied Matlab* scripts. Defined for a BER of 1E-12. Measured values at a smaller sample size have to be extrapolated to this BER target.
2. ζ = 0.54 implies a jitter peaking of 3 dB.
3. PCIe* Gen3 filter characteristics are subject to final ratification by PCISIG. Check the PCI-SIG for the latest specification.
4. Measured on 100 MHz PCIe output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
5. Measured on 100 MHz output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
6. Measured on 100 MHz, 133 MHz output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
7. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.
8. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
9. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 4. Phase Jitter (Continued)

Additive Phase Jitter Bypass Mode	PCIe Gen 1[1,2,3]	—	10	—	ps
	PCIe Gen2 Low Band F < 1.5 MHz[1,3,4,5]	—	1.2	—	ps (RMS)
	PCIe Gen2 High Band 1.5 MHz < F < Nyquist[1,3,4,5]	—	1.3	—	ps (RMS)
	PCIe Gen3 (PLL BW 2–4 MHz, CDR = 10 MHz)[1,3,4,5]	—	0.25	—	ps (RMS)
	PCIe Gen 4, Common Clock (PLL BW of 2–4 or 2–5 MHz, CDR = 10 MHz)[1,4,5,8]	—	0.25	—	ps (RMS)
	Intel QPI & Intel® SMI (4.8 Gbps or 6.4 Gb/s, 100 or 133 MHz, 12 UI)[1,6,7]	—	0.12	—	ps (RMS)
	Intel QPI & Intel® SMI (8 Gb/s, 100 MHz, 12 UI)[1,6]	—	0.1	—	ps (RMS)
	Intel QPI & Intel® SMI (9.6 Gb/s, 100 MHz, 12 UI)[1,6]	—	0.09	—	ps (RMS)

Notes:

1. Post processed evaluation through Intel supplied Matlab* scripts. Defined for a BER of 1E-12. Measured values at a smaller sample size have to be extrapolated to this BER target.
2. ζ = 0.54 implies a jitter peaking of 3 dB.
3. PCIe* Gen3 filter characteristics are subject to final ratification by PCISIG. Check the PCI-SIG for the latest specification.
4. Measured on 100 MHz PCIe output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
5. Measured on 100 MHz output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
6. Measured on 100 MHz, 133 MHz output using the template file in the Intel-supplied Clock Jitter Tool V1.6.3.
7. These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.
8. Gen 4 specifications based on the PCI-Express Base Specification 4.0 rev. 0.5.
9. Download the Silicon Labs PCIe Clock Jitter Tool at www.silabs.com/pcie-learningcenter.

Table 5. DIF 0.7 V AC Timing Characteristics (Non-Spread Spectrum Mode)[1]

Parameter	Symbol	CLK 100 MHz, 133 MHz			Unit
		Min	Typ	Max	
Clock Stabilization Time[2]	T_{STAB}	—	1.5	1.8	ms
Long Term Accuracy[2,3,4]	L_{ACC}	—		100	ppm
Absolute Host CLK Period (100 MHz)[2,3,5]	T_{ABS}	9.94900		10.05100	ns
Absolute Host CLK Period (133 MHz)[2,3,5]	T_{ABS}	7.44925		7.55075	ns
Edge Rate[2,3,6]	Edge_rate	1.0		4.0	V/ns
Rise Time Variation[2,7,8]	Δ Trise	—		125	ps
Fall Time Variation[2,7,8]	Δ Tfall	—		125	ps
Rise/Fall Matching[2,7,9,10]	T_{RISE_MAT}/ T_{FALL_MAT}	—		20	%
Voltage High (typ 0.7 V)[2,7,11]	V_{HIGH}	660		850	mV
Voltage Low (typ 0.7 V)[2,7,12]	V_{LOW}	–150		150	mV
Maximum Voltage[2,7,13,14,15]	V_{MAX}	—		1150	mV
Absolute Crossing Point Voltages[2,7,15,16]	Vox_{ABS}	250		550	mV
Relative Crossing Point Voltages	Vox_{REL}				
Total Variation of Vcross Over All Edges[2,7,17]	Total Δ Vox	—		140	mV
Duty Cycle[2,3]	DC	45		55	%
Maximum Voltage (Overshoot)[2,7,18]	V_{ovs}	—		V_{High} + 0.3	V
Maximum Voltage (Undershoot)[2,7,19]	V_{uds}	—		V_{Low} – 0.3	V

Table 5. DIF 0.7 V AC Timing Characteristics (Non-Spread Spectrum Mode)[1] (Continued)

Parameter	Symbol	CLK 100 MHz, 133 MHz			Unit
		Min	Typ	Max	
Ringback Voltage[2,7]	V_{rb}	0.2		N/A	V

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. This is the time from the valid CLK_IN input clocks and the assertion of the PWRGD signal level at 1.8–2.0 V to the time that stable clocks are output from the buffer chip (PLL locked).
3. Measurement taken from differential waveform.
4. Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz.
5. The average period over any 1 µs period of time must be greater than the minimum and less than the maximum specified period.
6. Measure taken from differential waveform on a component test board. The edge (slew) rate is measured from –150 mV to +150 mV on the differential waveform . Scope is set to average because the scope sample clock is making most of the dynamic wiggles along the clock edge Only valid for Rising clock and Falling $\overline{\text{CLOCK}}$. Signal must be monotonic through the Vol to Voh region for Trise and Tfall.
7. Measurement taken from single-ended waveform.
8. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
9. Measured with oscilloscope, averaging on, The difference between the rising edge rate (average) of clock verses the falling edge rate (average) of $\overline{\text{CLOCK}}$.
10. Rise/Fall matching is derived using the following, 2*(Trise - Tfall) / (Trise + Tfall).
11. VHigh is defined as the statistical average High value as obtained by using the Oscilloscope VHigh Math function.
12. VLow is defined as the statistical average Low value as obtained by using the Oscilloscope VLow Math function.
13. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of $\overline{\text{CLK}}$.
14. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
15. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
16. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg – 0.700), Vcross(rel) Max = 0.550 – 0.5 (0.700 – Vhavg), (see Figures 3-4 for further clarification).
17. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling $\overline{\text{CLOCK}}$. This is the maximum allowed variance in Vcross for any particular system.
18. Overshoot is defined as the absolute value of the maximum voltage.
19. Undershoot is defined as the absolute value of the minimum voltage.

Table 6. Clock Periods Differential Clock Outputs with SSC Disabled

SSC ON Center Freq, MHz	Measurement Window							Units
	1 Clock	1 µs	0.1 s	0.1 s	0.1 s	1 µs	1 Clock	
	-C-C Jitter AbsPer Min	-SSC Short Term AVG Min	-ppm Long Term AVG Min	0 ppm Period Nominal	+ppm Long Term AVG Max	+SSC Short Term AVG Max	+C-C Jitter AbsPer Max	
100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns
133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns

Table 7. Clock Periods Differential Clock Outputs with SSC Enabled

SSC ON Center Freq, MHz	Measurement Window							Units
	1 Clock	1 µs	0.1 s	0.1 s	0.1 s	1 µs	1 Clock	
	-C-C Jitter AbsPer Min	-SSC Short Term AVG Min	-ppm Long Term AVG Min	0 ppm Period Nominal	+ppm Long Term AVG Max	+SSC Short Term AVG Max	+C-C Jitter AbsPer Max	
99.75	9.94900	9.99900	10.02406	10.02506	10.02607	10.05126	10.10126	ns
133.33	7.44925	7.49925	7.51805	7.51880	7.51955	7.53845	7.58845	ns

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3 V Core Supply Voltage[1]	VDD/VDD_A	—	4.6	V
3.3 V I/O Supply Voltage[1]	VDD_IO	—	4.6	V
3.3 V Input High Voltage[1,2]	VIH	—	4.6	V
3.3 V Input Low Voltage[1]	VIL	−0.5	—	V
Storage Temperature[1]	t_s	–65	150	°C
Input ESD protection[3]	ESD	2000	—	V

Notes:
1. Consult manufacturer regarding extended operation in excess of normal dc operating parameters.
2. Maximum VIH is not to exceed maximum V_{DD}.
3. Human body model.

2. Functional Description

2.1. CLK_IN, $\overline{\text{CLK\_IN}}$

The differential input clock is expected to be sourced from a clock synthesizer, e.g. CK420BQ, CK509B, or CK410B+.

2.2. $\overline{\text{OE}}$ and Output Enables (Control Registers)

Each output can be individually enabled or disabled by SMBus control register bits. Additionally, each output of the DIF[11:0] has a dedicated $\overline{\text{OE}}$ pin. The $\overline{\text{OE}}$ pins are asynchronous, asserted-low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default. The disabled state for the DB1200ZL NMOS push-pull output is Low/Low. Note that the logic level for assertion or deassertion is different in software than it is on hardware. This follows hardware default nomenclature for communication channels (e.g., output is enabled if the OE# pin is pulled low) and still maintains software programming logic (e.g., output is enabled if OE register is true). Table 9 is a truth table depicting enabling and disabling of outputs via hardware and software. Note that, for the output to be active, the control register bit must be a 1 *and* the $\overline{\text{OE}}$ pin must be a 0.

Note: The assertion and deassertion of this signal is absolutely asynchronous.

Table 9. si53112-A03A-A03A Output Management

Inputs		$\overline{\text{OE}}$ Hardware Pins and Control Register Bits			Outputs	PLL State
PWRGD/ PWRDN	CLK_IN/ CLK_IN	SMBUS Enable Bit	$\overline{\text{OE}}$ Pin	DIF/$\overline{\text{DIF}}$[11:0]	FB_OUT/ FB_OUT	
0	x	x	x	Low/Low	Low/Low	OFF
1	Running	0	x	Low/Low	Running	ON
		1	0	Running	Running	ON
		1	1	Low/Low	Running	ON

2.2.1. $\overline{\text{OE}}$ Assertion (Transition from 1 to 0)

All differential outputs that were disabled are to resume normal operation in a glitch-free manner. The latency from the assertion to active outputs is 4 to 12 DIF clock periods.

2.2.2. $\overline{\text{OE}}$ De-Assertion (Transition from 0 to 1)

The impact of deasserting $\overline{\text{OE}}$ is that each corresponding output will transition from normal operation to disabled in a glitch-free manner. A minimum of four valid clocks will be provided after the deassertion of $\overline{\text{OE}}$. The maximum latency from the deassertion to disabled outputs is 12 DIF clock periods.

2.3. $\overline{\text{100M\_133M}}$—Frequency Selection

The Si53112-A03A is optimized for lowest phase jitter performance at operating frequencies of 100 and 133 MHz. $\overline{\text{100M\_133M}}$ is a hardware input pin, which programs the appropriate output frequency of the differential outputs. Note that the CLK_IN frequency must be equal to the CLK_OUT frequency; meaning Si53112-A03A is operated in 1:1 mode only. Frequency selection can be enabled by the $\overline{\text{100M\_133M}}$ hardware pin. An external pull-up or pull-down resistor is attached to this pin to select the input/output frequency. The functionality is summarized in Table 10.

Table 10. Frequency Program Table

$\overline{\text{100M\_133M}}$	Optimized Frequency (CLK_IN = CLK_OUT)
0	133.33 MHz
1	100.00 MHz

Note: All differential outputs transition from 100 to 133 MHz or from 133 to 100 MHz in a glitch free manner.

2.4. SA_0, SA_1—Address Selection

SA_0 and SA_1 are tri-level hardware pins, which program the appropriate address for the si53112-A03A-A03Asi53112-A03A-A03A. The two tri-level input pins that can configure the device to nine different addresses.

Table 11. SMBUS Address Table

SA_1	SA_0	SMBUS Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

2.5. PWRGD/$\overline{\text{PWRDN}}$

PWRGD is asserted high and deasserted low. Deassertion of PWRGD (pulling the signal low) is equivalent to indicating a power down condition. PWRGD (assertion) is used by the si53112-A03A to sample initial configurations, such as frequency select condition and SA selections. After PWRGD has been asserted high for the first time, the pin becomes a $\overline{\text{PWRDN}}$ (power down) pin that can be used to shut off all clocks cleanly and instruct the device to invoke power-saving mode. $\overline{\text{PWRDN}}$ is a completely asynchronous active low input. When entering power-saving mode, $\overline{\text{PWRDN}}$ should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When $\overline{\text{PWRDN}}$ is asserted low, all clocks will be disabled prior to turning off the VCO. When $\overline{\text{PWRDN}}$ is deasserted high, all clocks will start and stop without any abnormal behavior and will meet all ac and dc parameters.

Note: The assertion and deassertion of $\overline{\text{PWRDN}}$ is absolutely asynchronous.

Warning: Disabling of the CLK_IN input clock prior to assertion of $\overline{\text{PWRDN}}$ is an undefined mode and not recommended. Operation in this mode may result in glitches, excessive frequency shifting, etc.

Table 12. PWRGD/PWRDN Functionality

PWRGD/$\overline{\text{PWRDN}}$	DIF	$\overline{\text{DIF}}$
0	Low	Low
1	Normal	Normal

2.5.1. $\overline{\text{PWRDN}}$ Assertion

When $\overline{\text{PWRDN}}$ is sampled low by two consecutive rising edges of $\overline{\text{DIF}}$, all differential outputs must be held LOW/LOW on the next $\overline{\text{DIF}}$ high-to-low transition.

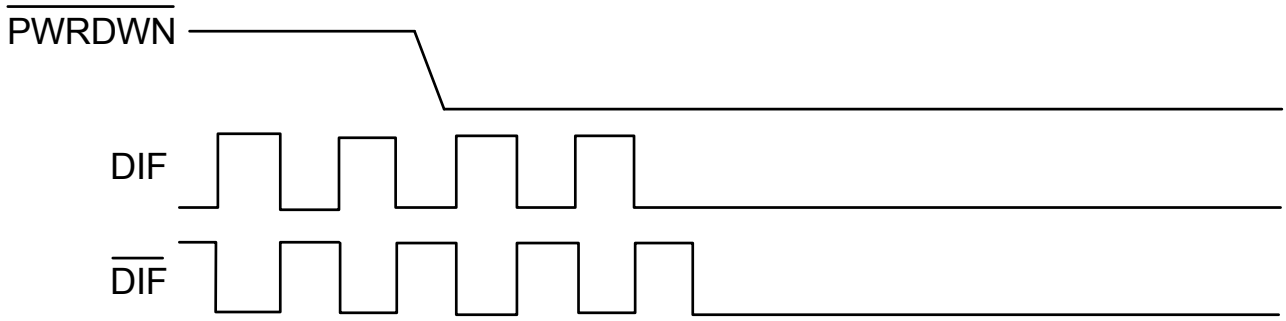


Figure 1. $\overline{\text{PWRDN}}$ Assertion

2.5.2. PWRGD Assertion

The power-up latency is to be less than 1.8 ms. This is the time from a valid CLK_IN input clock and the assertion of the PWRGD signal to the time that stable clocks are output from the device (PLL locked). All differential outputs stopped in a LOW/LOW condition resulting from power down must be driven high in less than 300 µs of $\overline{\text{PWRDN}}$ deassertion to a voltage greater than 200 mV.

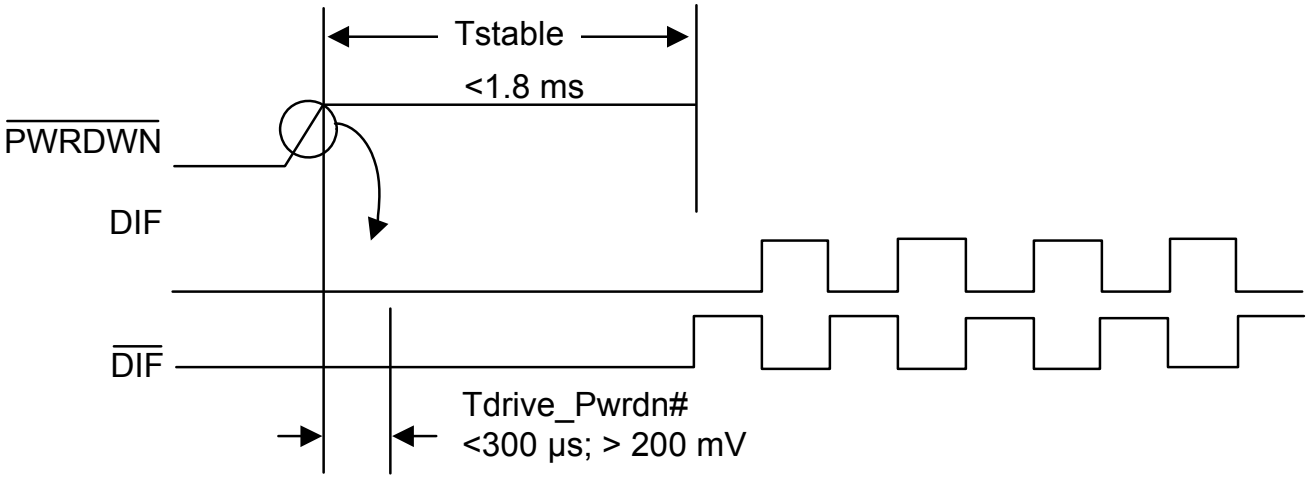


Figure 2. PWRDG Assertion (Pwrdown—Deassertion)

2.6. HBW_BYPASS_LBW

The $\overline{\text{HBW\_BYPASS\_LBW}}$ pin is a tri-level function input pin (refer to Table 13 for VIL_Tri, VIM_Tri, and VIH_Tri signal levels). It is used to select between PLL high-bandwidth, PLL bypass mode, or PLL low-bandwidth mode. In PLL bypass mode, the input clock is passed directly to the output stage, which may result in up to 50 ps of additive cycle-to-cycle jitter (50 ps + input jitter) on the differential outputs. In the case of PLL mode, the input clock is passed through a PLL to reduce high-frequency jitter. The PLL HBW, BYPASS, and PLL LBW modes may be selected by asserting the $\overline{\text{HBW\_BYPASS\_LBW}}$ input pin to the appropriate level described in Table 13.

Table 13. PLL Bandwidth and Readback Table

$\overline{\text{HBW\_BYPASS\_LBW}}$ Pin	Mode	Byte 0, Bit 7	Byte 0, Bit 6
L	LBW	0	0
M	BYPASS	0	1
H	HBW	1	1

The Si53112-A03A has the ability to override the latch value of the PLL operating mode from hardware strap pin 5 via the use of Byte 0 and bits 2 and 1. Byte 0 bit 3 must be set to 1 to allow the user to change Bits 2 and 1, affecting the PLL. Bits 7 and 6 will always read back the original latched value. A warm reset of the system will have to be accomplished if the user changes these bits.

2.7. Miscellaneous Requirements

Data Transfer Rate: 100 kbps (standard mode) is the base functionality required. Fast mode (400 kbps) functionality is optional.

Logic Levels: SMBus logic levels are based on a percentage of V_{DD} for the controller and other devices on the bus. Assume all devices are based on a 3.3 V supply.

Clock Stretching: The clock buffer must not hold/stretch the SCL or SDA lines low for more than 10 ms. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.

General Call: It is assumed that the clock buffer will not have to respond to the “general call.”

Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in Section 3 of the SMBus 2.0 specification.

Pull-Up Resistors: Any internal resistor pull-ups on the SDATA and SCLK inputs must be stated in the individual data sheet. The use of internal pull-ups on these pins of below 100 K is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5–6 kΩ range. Assume one SMBus device per DIMM (serial presence detect), one SMBus controller, one clock buffer, one clock driver plus one/two more SMBus devices on the platform for capacitive loading purposes.

Input Glitch Filters: Only fast mode SMBus devices require input glitch filters to suppress bus noise. The clock buffer is specified as a standard mode device and is not required to support this feature. However, it is considered a good design practice to include the filters.

$\overline{\text{PWRDN}}$: If a clock buffer is placed in $\overline{\text{PWRDN}}$ mode, the SDATA and SCLK inputs must be Tri-stated and the device must retain all programming information. IDD current due to the SMBus circuitry must be characterized and in the data sheet.

2.8. Buffer Power-Up State Machine

Table 14. Buffer Power-Up State Machine

State	Description
0	3.3 V buffer power is off.
1	After 3.3 V supply is detected to rise above 1.8–2.0 V, the buffer enters State 1 and initiates a 0.1–0.3 ms delay.
2	Buffer waits for a valid clock on the CLK input and $\overline{\text{PWRDN}}$ de-assertion.
3	Once the PLL is locked to the CLK_IN input clock, the buffer enters state 3 and enables outputs for normal operation.

Notes:
1. The total power-up latency from power-on to all outputs active must be less than 1.8 ms (assuming a valid clock is present on CLK_IN input).
2. If power is valid and power-down is deasserted but no input clocks are present on the CLK_IN input, DIF clocks must remain disabled. Only after valid input clocks are detected, valid power, $\overline{\text{PWRDN}}$ deasserted with the PLL locked/stable are the DIF outputs enabled.

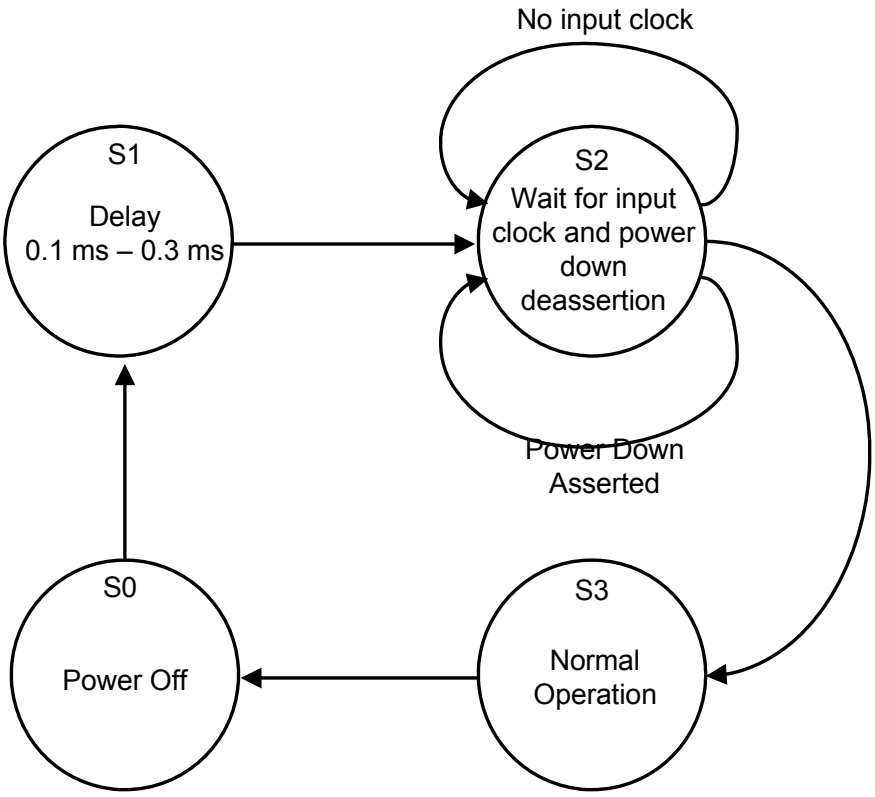


Figure 3. Buffer Power-Up State Diagram

3. Test and Measurement Setup

3.1. Input Edge

Input edge rate is based on single-ended measurement. This is the minimum input edge rate at which the Si53112-A03A is guaranteed to meet all performance specifications.

Table 15. Input Edge Rate

Frequency	Min	Max	Unit
100 MHz	0.35	N/A	V/ns
133 MHz	0.35	N/A	V/ns

3.1.1. Measurement Points for Differential

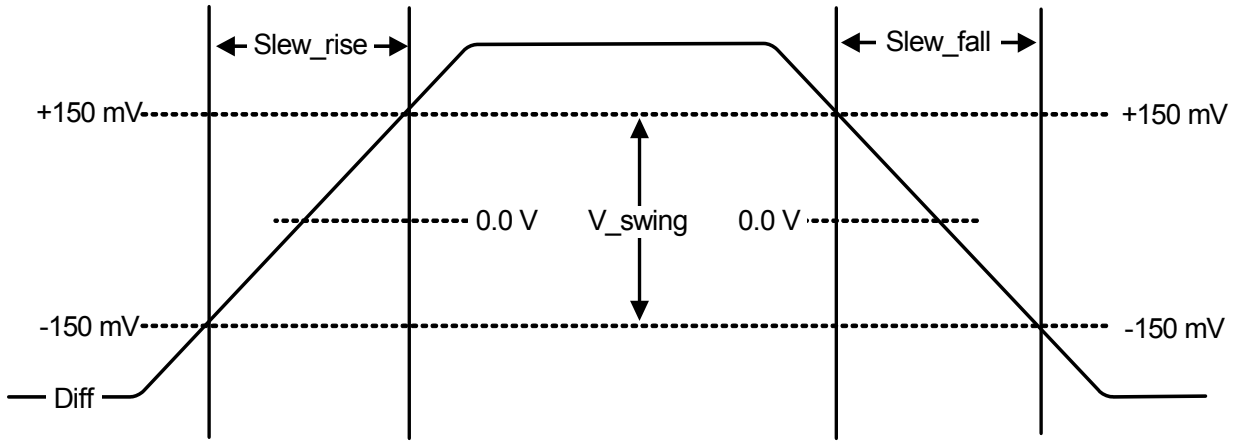


Figure 4. Measurement Points for Rise Time and Fall Time

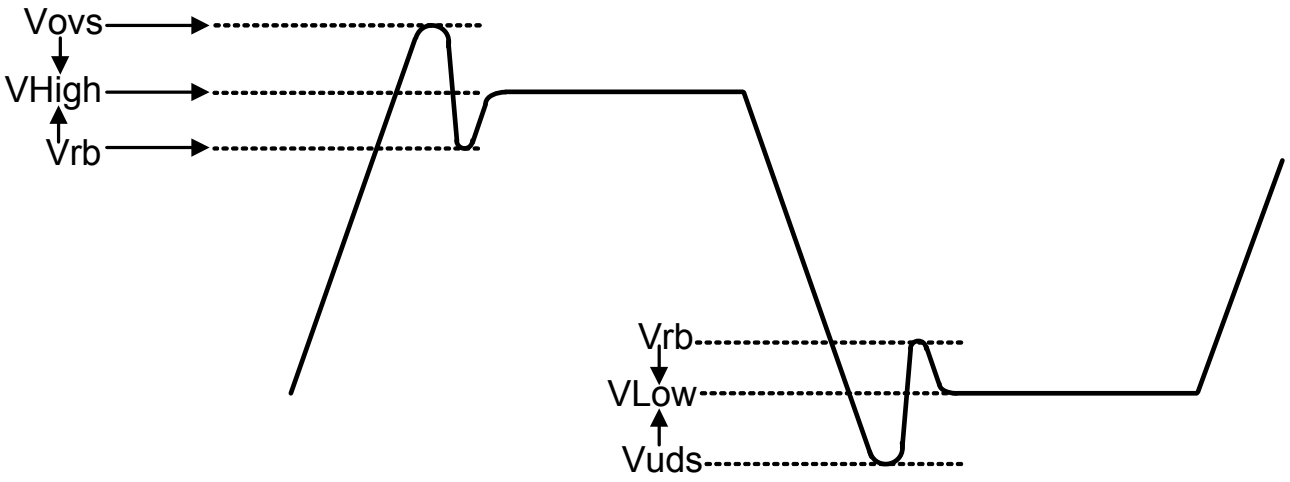


Figure 5. Single-Ended Measurement Points for V_{ovs}, V_{uds}, V_{rb}

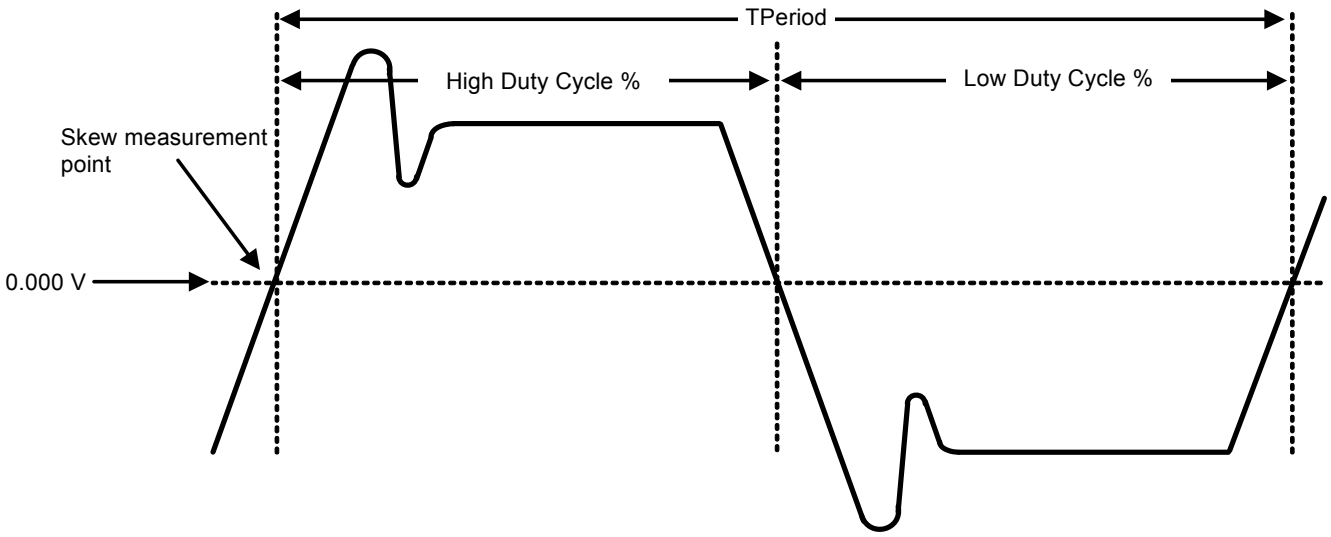


Figure 6. Differential (CLOCK–$\overline{\text{CLOCK}}$) Measurement Points (T_{period}, Duty Cycle, Jitter)

3.2. Termination of Differential Outputs

All differential outputs are to be tested into an 85 Ω differential impedance transmission line. All output termination resistors are fully integrated into the Si53119-A03A, no external components are required. Contact Silicon Labs Support if 100 Ω differential impedance support is needed.

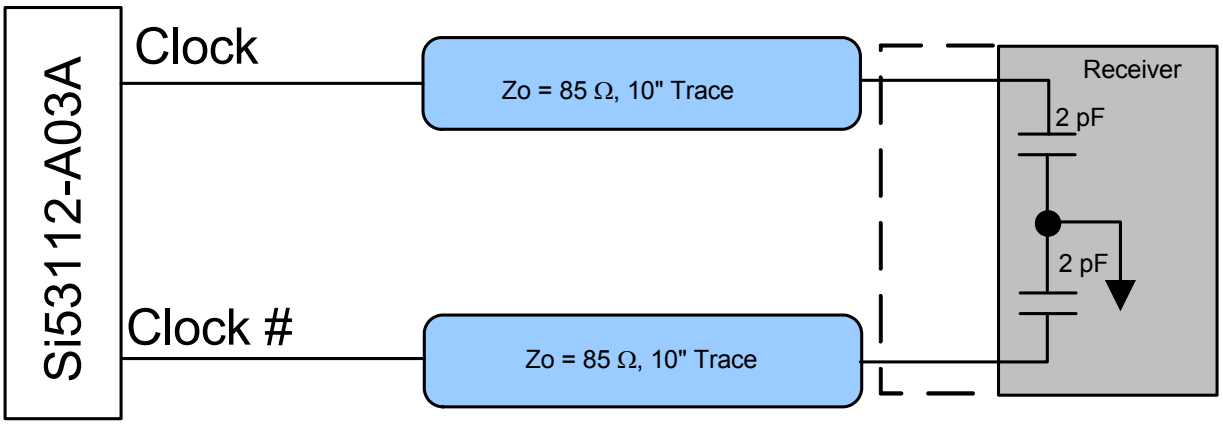


Figure 7. 0.7 V Configuration Test Load Board Termination for NMOS Push-Pull

4. Control Registers

4.1. Byte Read/Write

Reading or writing a register in an SMBus slave device in byte mode always involves specifying the register number.

4.1.1. Byte Read

The standard byte read is as shown in Figure 8. It is an extension of the byte write. The write start condition is repeated, then the slave device starts sending data, and the master acknowledges it until the last byte is sent. The master terminates the transfer with a NAK, then a stop condition. For byte operation, the 2 x 7th bit of the command byte must be set. For block operations, the 2 x 7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

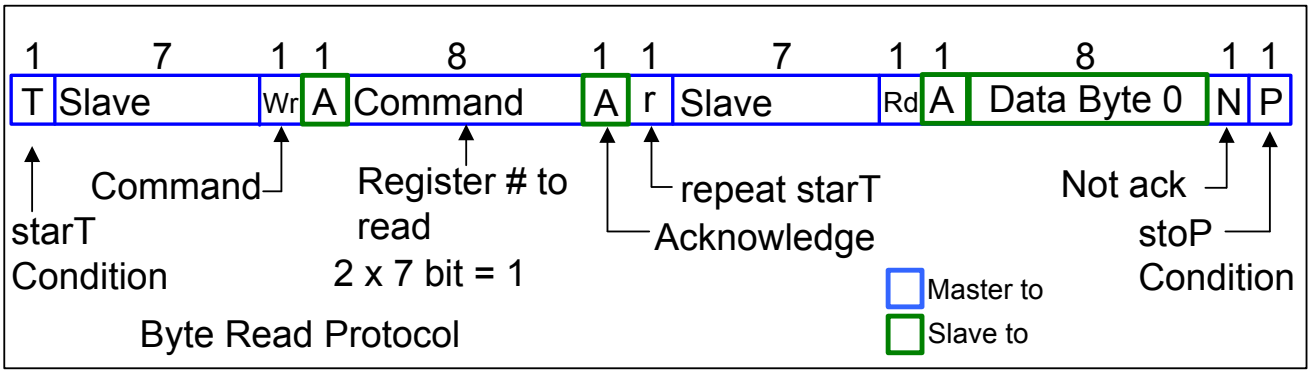


Figure 8. Byte Read Protocol

4.1.2. Byte Write

Figure 9 illustrates a simple, typical byte write. For byte operation, the 2 x 7th bit of the command byte must be set. For block operations, the 2 x 7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count. The count can be between 1 and 32. It is not allowed to be 0 or to exceed 32.

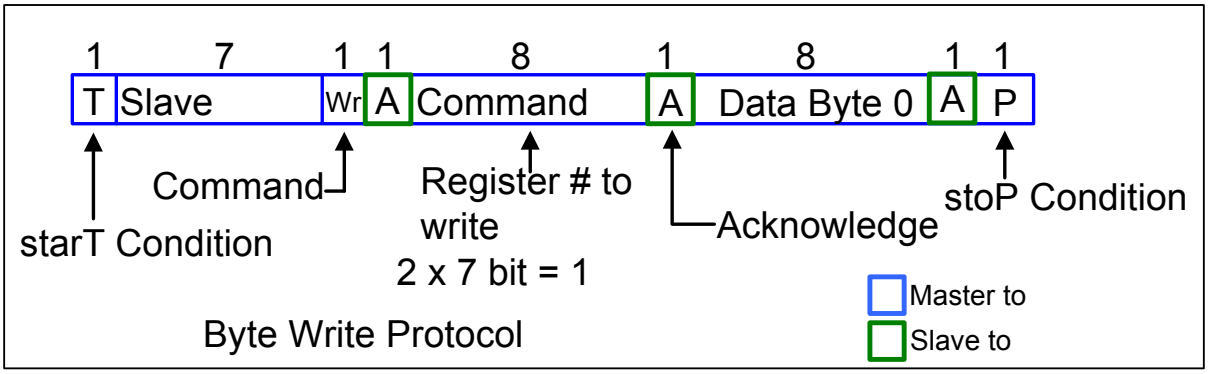


Figure 9. Byte Write Protocol

4.2. Block Read/Write

4.2.1. Block Read

After the slave address is sent with the R/W condition bit set, the command byte is sent with the MSB = 0. The slave acknowledges the register index in the command byte. The master sends a repeat start function. After the slave acknowledges this, the slave sends the number of bytes it wants to transfer (>0 and <33). The master acknowledges each byte except the last and sends a stop function.

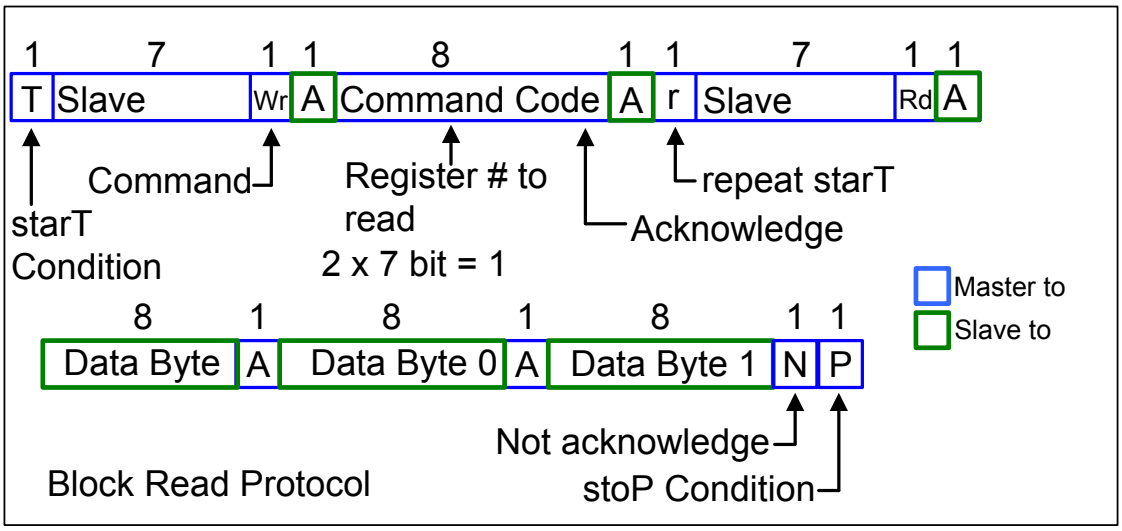


Figure 10. Block Read Protocol

4.2.2. Block Write

After the slave address is sent with the R/W condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate the register at which to start the transfer. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than 0 and less than 33. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

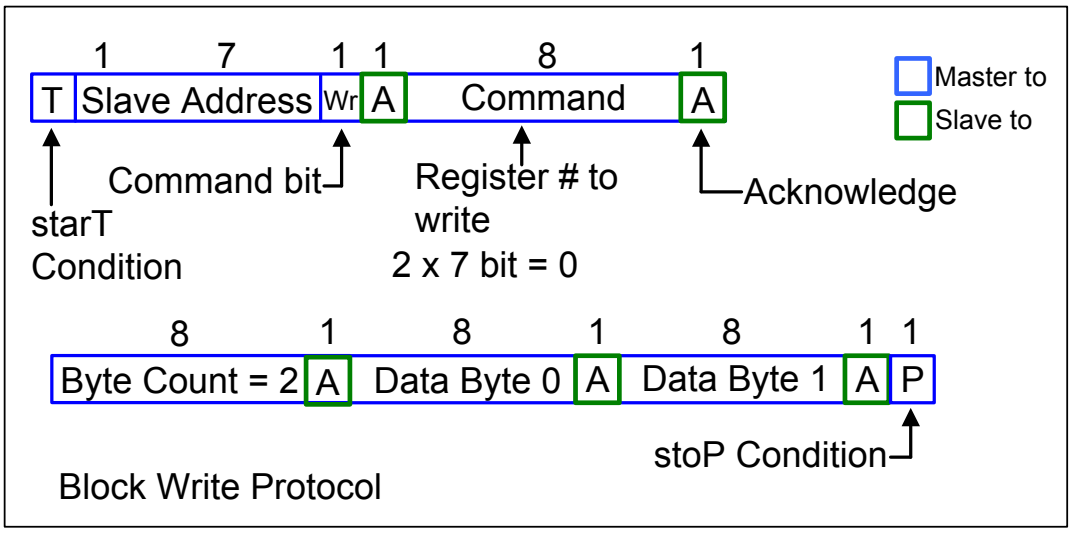


Figure 11. Block Write Protocol

4.3. Control Registers

Table 16. Byte 0: Frequency Select, Output Enable, PLL Mode Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	100M_133M# Frequency Select	133 MHz	100 MHz	R	Latched at power up	DIF[11:0]
1	PLL Mode 0	See PLL Operating Mode Readback Table		RW	1	
2	PLL Mode 1			RW	1	
3	PLL Software Enable	HW Latch	SMBUS Control	RW	0	
4	Reserved				0	
5	Reserved				0	
6	PLL Mode 0	See PLL Operating Mode Readback Table		R	Latched at power up	
7	PLL Mode 1	See PLL Operating Mode Readback Table		R	Latched at power up	

Note: Byte 0, bit_[3:1] are BW PLL SW enable for the DB1200ZL. Setting bit 3 to 1 allows the user to override the Latch value from pin 5 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. A warm reset of the system will have to be accomplished if the user changes these bits.

Table 17. Byte 1: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable DIF 0	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[0]
1	Output Enable DIF 1	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[1]
2	Output Enable DIF 2	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[2]
3	Output Enable DIF 3	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[3]
4	Output Enable DIF 4	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[4]
5	Output Enable DIF 5	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[5]
6	Output Enable DIF 6	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[6]
7	Output Enable DIF 7	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[7]

Table 18. Byte 2: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable DIF 8	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[8]
1	Output Enable DIF 9	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[9]
2	Output Enable DIF 10	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[10]
3	Output Enable DIF 11	Low/Low for Si53112-A03A	Enabled	RW	1	DIF[11]
4	Reserved				0	
5	Reserved				0	
6	Reserved				0	
7	Reserved				0	

Table 19. Byte 3: Reserved Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Reserved				0	
1	Reserved				0	
2	Reserved				0	
3	Reserved				0	
4	Reserved				0	
5	Reserved				0	
6	Reserved				0	
7	Reserved				0	

Table 20. Byte 4: Reserved Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Reserved				0	
1	Reserved				0	
2	Reserved				0	
3	Reserved				0	
4	Reserved				0	
5	Reserved				0	
6	Reserved				0	
7	Reserved				0	

Table 21. Byte 5: Vendor/Revision Identification Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Default
0	Vendor ID Bit 0			R	Vendor Specific	0
1	Vendor ID Bit 1			R	Vendor Specific	0
2	Vendor ID Bit 2			R	Vendor Specific	0
3	Vendor ID Bit 3			R	Vendor Specific	1
4	Revision Code Bit 0			R	Vendor Specific	0
5	Revision Code Bit 1			R	Vendor Specific	0
6	Revision Code Bit 2			R	Vendor Specific	0
7	Revision Code Bit 3			R	Vendor Specific	0

Table 22. Byte 6: Device ID Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Default
0	Device ID 0			R		0
1	Device ID 1			R		0
2	Device ID 2			R		0
3	Device ID 3			R		0
4	Device ID 4			R		0
5	Device ID 5			R		0
6	Device ID 6			R		0
7	Device ID 7 (MSB)			R		0

Table 23. Byte 7: Byte Count Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	BC0 - Writing to this register configures how many bytes will be read back			RW	0	
1	BC1 - Writing to this register configures how many bytes will be read back			RW	0	
2	BC2 - Writing to this register configures how many bytes will be read back			RW	0	
3	BC3 - Writing to this register configures how many bytes will be read back			RW	1	
4	BC4 - Writing to this register configures how many bytes will be read back			RW	0	
5	Reserved				0	
6	Reserved				0	
7	Reserved				0	

5. Power Filtering Example

5.1. Ferrite Bead Power Filtering

Recommended ferrite bead filtering equivalent to the following: 600 Ω impedance at 100 MHz, ≤ 0.1 Ω DCR max., ≥ 400 mA current rating.

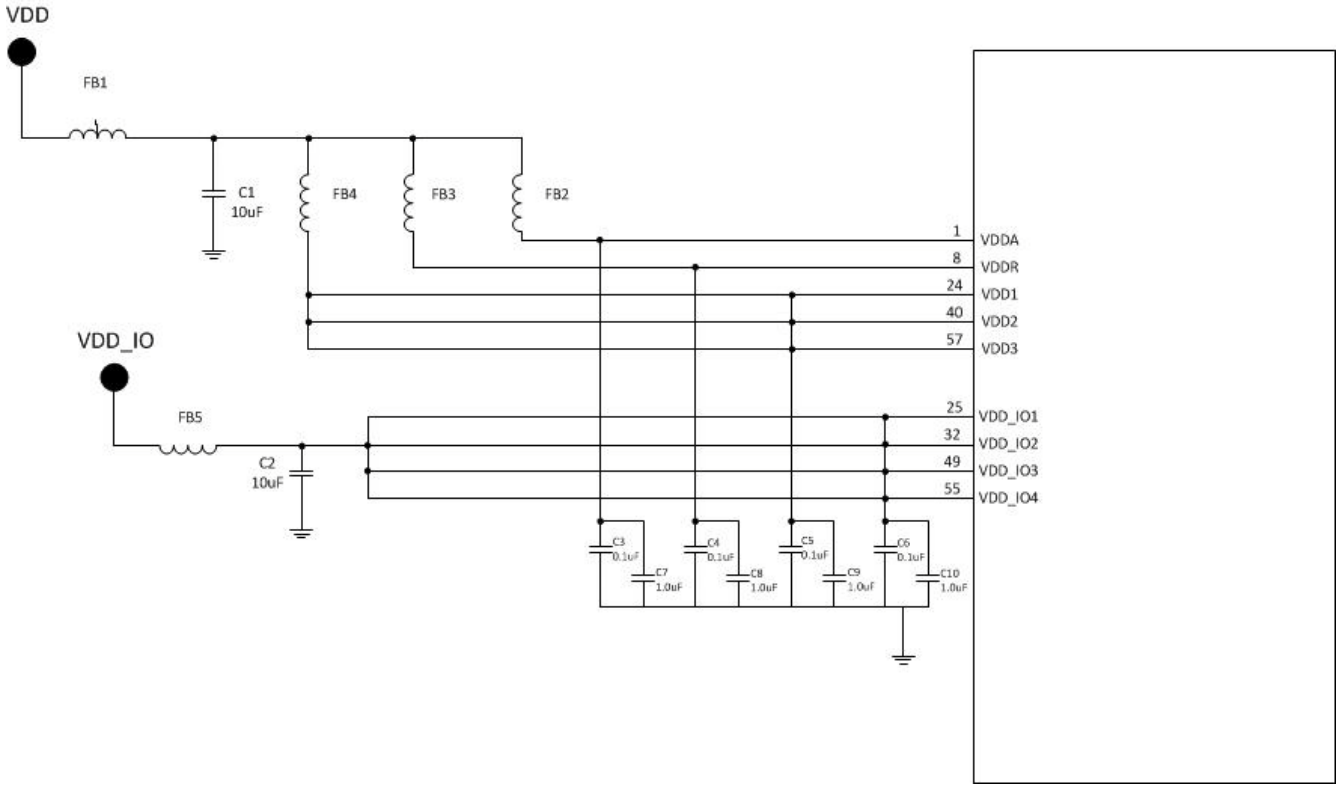
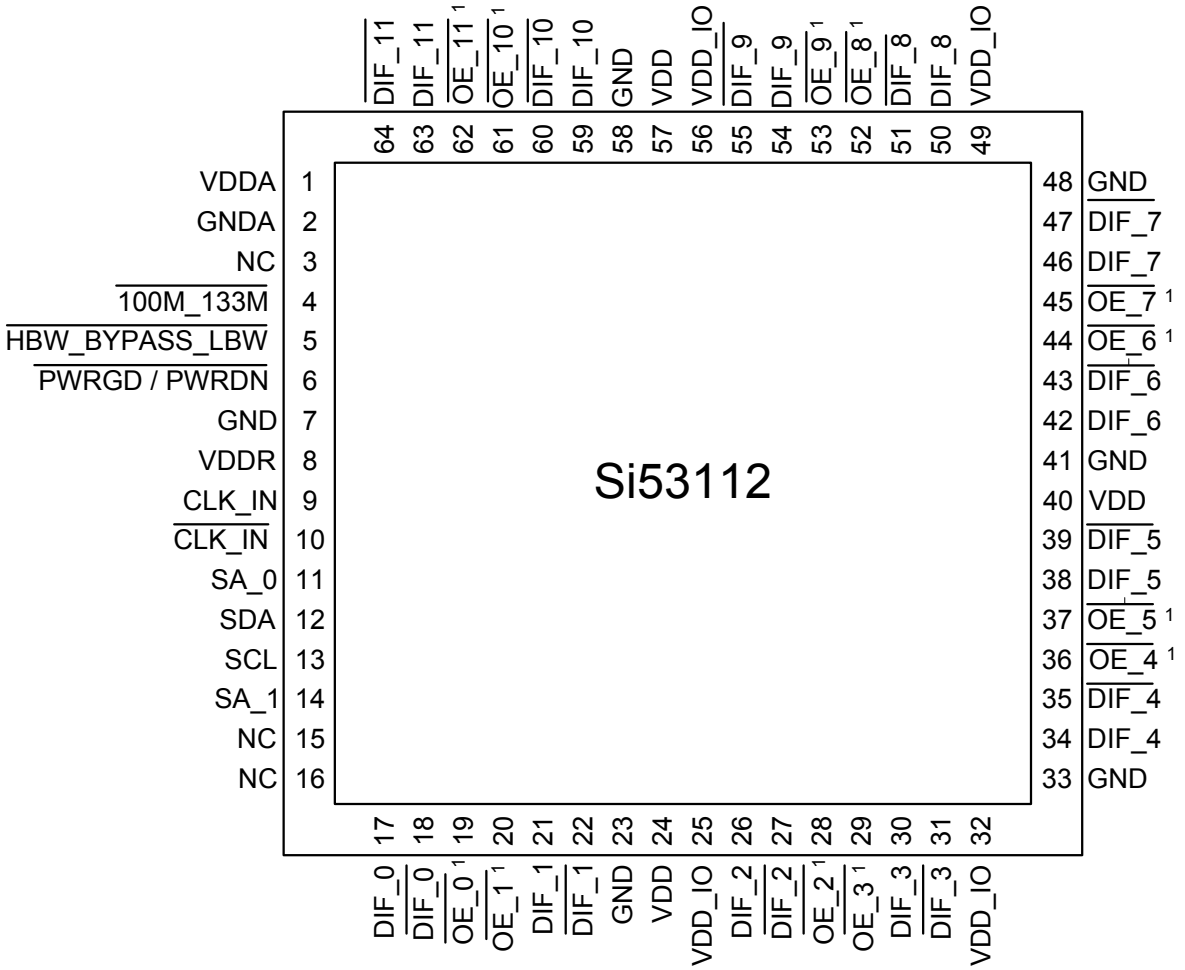


Figure 12. Schematic Example of Si53112-A03A Power Filtering

6. Pin Descriptions: 64-Pin QFN



Notes:
1) Internal 100K pull-down

Table 24. si53112-A03A 64-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDDA	3.3 V	3.3 V power supply for PLL.
2	GNDA	GND	Ground for PLL.
3	NC	I/O	No connect.
4	$\overline{100M\_133M}$	I,SE	3.3 V tolerant inputs for input/output frequency selection. An external pull-up or pull-down resistor is attached to this pin to select the input/output frequency. High = 100 MHz output Low = 133 MHz output
5	$\overline{HBW\_BYPASS\_LBW}$	I, SE	Tri-Level input for selecting the PLL bandwidth or bypass mode. High = High BW mode Med = Bypass mode Low = Low BW mode
6	$\overline{PWRGD/PWRDN}$	I	3.3 V LVTTL input to power up or power down the device.
7	GND	GND	Ground for outputs.
8	VDDR	VDD	3.3 V power supply for differential input receiver. This VDDR should be treated as an analog power rail and filtered appropriately.
9	CLK_IN	I, DIF	0.7 V Differential input.
10	$\overline{CLK\_IN}$	I, DIF	0.7 V Differential input.
11	SA_0	I	3.3 V LVTTL input selecting the address. Tri-level input.
12	SDA	I/O	Open collector SMBus data.
13	SCL	I/O	SMBus slave clock input.
14	SA_1	I	3.3 V LVTTL input selecting the address. Tri-level input.
15	NC	I/O	No connect. There are active signals on pin 15 and 16, do not connect anything to these pins.
16	NC	I/O	No connect. There are active signals on pin 15 and 16, do not connect anything to these pins.
17	DIF_0	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
18	$\overline{DIF\_0}$	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
19	$\overline{OE\_0}$	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
20	$\overline{OE\_1}$	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
21	DIF_1	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
22	$\overline{DIF\_1}$	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
23	GND	GND	Ground for outputs.

Table 24. si53112-A03A 64-Pin QFN Descriptions

Pin #	Name	Type	Description
24	VDD	3.3 V	3.3 V power supply for outputs.
25	VDD_IO	VDD	Power supply for differential outputs.
26	DIF_2	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
27	$\overline{\text{DIF}}$_2	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
28	$\overline{\text{OE}}$_2	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
29	$\overline{\text{OE}}$_3	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
30	DIF_3	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
31	$\overline{\text{DIF}}$_3	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
32	VDD_IO	VDD	Power supply for differential outputs.
33	GND	GND	Ground for outputs.
34	DIF_4	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
35	$\overline{\text{DIF}}$_4	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
36	$\overline{\text{OE}}$_4	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
37	$\overline{\text{OE}}$_5	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
38	DIF_5	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
39	$\overline{\text{DIF}}$_5	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
40	VDD	3.3 V	3.3 V power supply for outputs.
41	GND	GND	Ground for outputs.
42	DIF_6	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
43	$\overline{\text{DIF}}$_6	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
44	$\overline{\text{OE}}$_6	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
45	$\overline{\text{OE}}$_7	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
46	DIF_7	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
47	$\overline{\text{DIF}}$_7	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
48	GND	GND	Ground for outputs.
49	VDD_IO	VDD	Power supply for differential outputs.
50	DIF_8	O, DIF	0.7 V Differential clock outputs. Default is 1:1.

Table 24. si53112-A03A 64-Pin QFN Descriptions

Pin #	Name	Type	Description
51	$\overline{\text{DIF}}$_8	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
52	$\overline{\text{OE}}$_8	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
53	$\overline{\text{OE}}$_9	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
54	DIF_9	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
55	$\overline{\text{DIF}}$_9	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
56	VDD_IO	VDD	Power supply for differential outputs.
57	VDD	3.3 V	3.3 V power supply for outputs.
58	GND	GND	Ground for outputs.
59	DIF_10	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
60	$\overline{\text{DIF}}$_10	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
61	$\overline{\text{OE}}$_10	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
62	$\overline{\text{OE}}$_11	I, SE	3.3 V LVTTL active low input for enabling differential outputs (default). Controls the corresponding output pair. Internal pull-down.
63	DIF_11	O, DIF	0.7 V Differential clock outputs. Default is 1:1.
64	$\overline{\text{DIF}}$_11	O, DIF	0.7 V Differential clock outputs. Default is 1:1.

7. Ordering Guide

Part Number	Package Type	Temperature
Lead-free		
Si53112-A03AGM	64-pin QFN	Extended, –40 to 85 °C
Si53112-A03AGMR	64-pin QFN—Tape and Reel	Extended, –40 to 85 °C

8. Package Outline

Figure 13 illustrates the package details for the Si53112-A03A. Table 25 lists the values for the dimensions shown in the illustration.

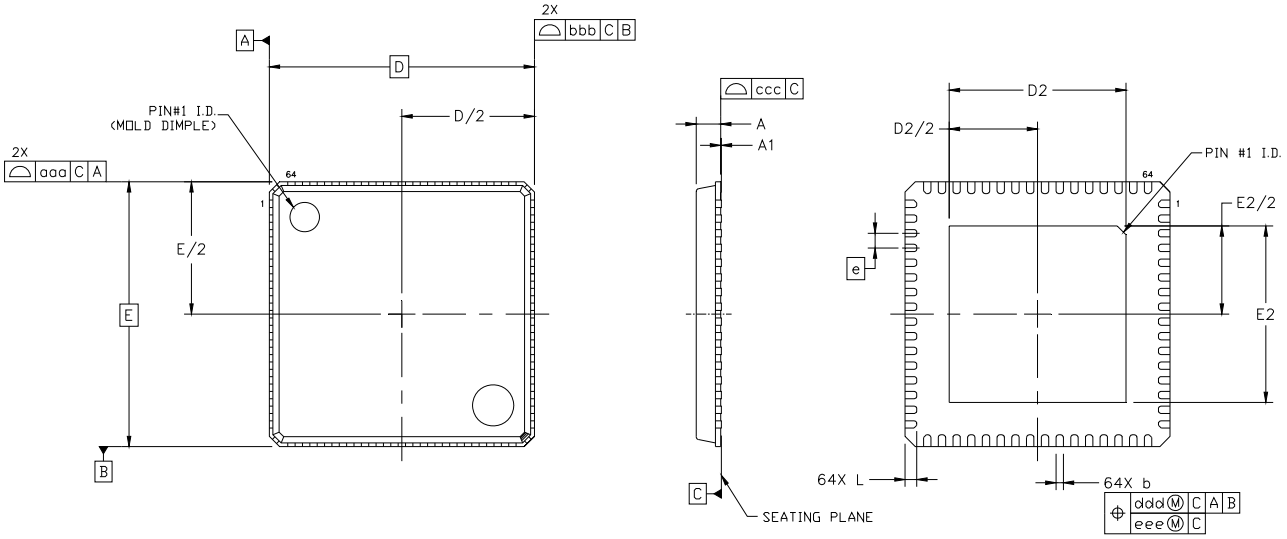


Figure 13. 64-Pin Quad Flat No Lead (QFN) Package

Table 25. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC.	
D2	6.00	6.10	6.20
e		0.50 BSC.	
E		9.00 BSC.	
E2	6.00	6.10	6.20
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Land Pattern

Figure 14 illustrates the recommended land pattern details for the Si53112-A03A in a 64-pin QFN package. Table 26 lists the values for the dimensions shown in the illustration.

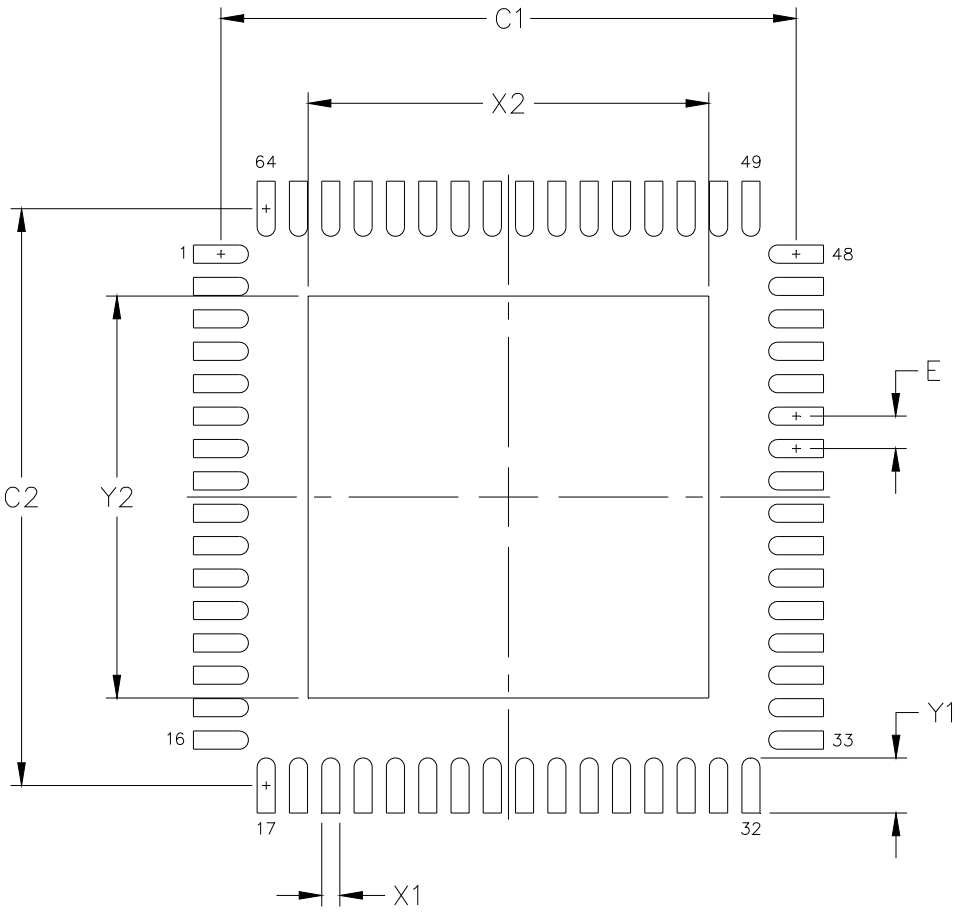


Figure 14. Land Pattern

Table 26. PCB Land Pattern Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	6.20
Y2	6.20

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 m minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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