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Kind regards,

Team Nexperia

DATA SHEET

PDTA124T series

PNP resistor-equipped transistors;
R1 = 22 k Ω , R2 = open

Product data sheet
Supersedes data of 2004 May 05

2004 Aug 04

PNP resistor-equipped transistors; R1 = 22 k Ω , R2 = open

PDTA124T series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	–50	V
I _O	output current (DC)	–	–100	mA
R1	bias resistor	22	–	k Ω
R2	open	–	–	–

DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA124TE	SOT416	SC-75	3R	PDTC124TE
PDTA124TEF	SOT490	SC-89	24	PDTC124TEF
PDTA124TK	SOT346	SC-59	59	PDTC124TK
PDTA124TM	SOT883	SC-101	DJ	PDTC124TM
PDTA124TS	SOT54 (TO-92)	SC-43	TA124T	PDTC124TS
PDTA124TT	SOT23	–	*AE ⁽¹⁾	PDTC124TT
PDTA124TU	SOT323	SC-70	*7B ⁽¹⁾	PDTC124TU

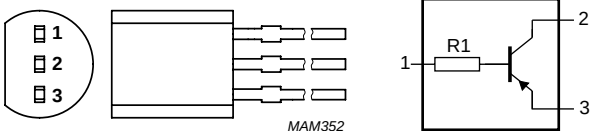
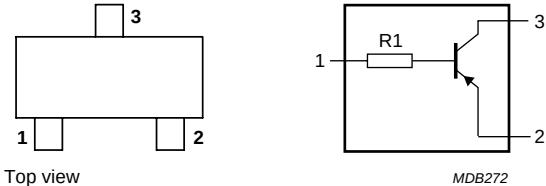
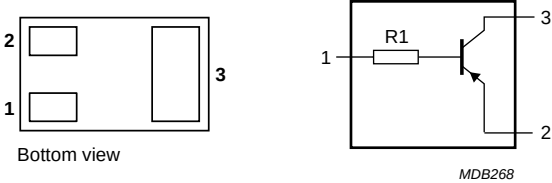
Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

PNP resistor-equipped transistors;
R1 = 22 kΩ, R2 = open

PDTA124T series

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA124TS		1 2 3	base collector emitter
PDTA124TE PDTA124TEF PDTA124TK PDTA124TT PDTA124TU		1 2 3	base emitter collector
PDTA124TM		1 2 3	base emitter collector

PNP resistor-equipped transistors;
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PDTA124T series

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTA124TE	–	plastic surface mounted package; 3 leads	SOT416
PDTA124TEF	–	plastic surface mounted package; 3 leads	SOT490
PDTA124TK	–	plastic surface mounted package; 3 leads	SOT346
PDTA124TM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTA124TS	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA124TT	–	plastic surface mounted package; 3 leads	SOT23
PDTA124TU	–	plastic surface mounted package; 3 leads	SOT323

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	–50	V
V _{CEO}	collector-emitter voltage	open base	–	–50	V
V _{EBO}	emitter-base voltage	open collector	–	–5	V
I _O	output current (DC)		–	–100	mA
I _{CM}	peak collector current		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT23	note 1	–	250	mW
	SOT54	note 1	–	500	mW
	SOT323	note 1	–	200	mW
	SOT346	note 1	–	250	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	SOT23	note 1	500	K/W
	SOT54	note 1	250	K/W
	SOT323	note 1	625	K/W
	SOT346	note 1	500	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = -50 V; I _E = 0 A	–	–	-100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = -30 V; I _B = 0 A	–	–	-1	μ A
		V _{CE} = -30 V; I _B = 0 A; T _j = 150 °C	–	–	-50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A	–	–	-100	nA
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -1 mA	100	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = -10 mA; I _B = -0.5 mA	–	–	-150	mV
R1	input resistor		15.4	22	28.6	k Ω
C _c	collector capacitance	I _E = I _e = 0 A; V _{CB} = -10 V; f = 1 MHz	–	–	3	pF

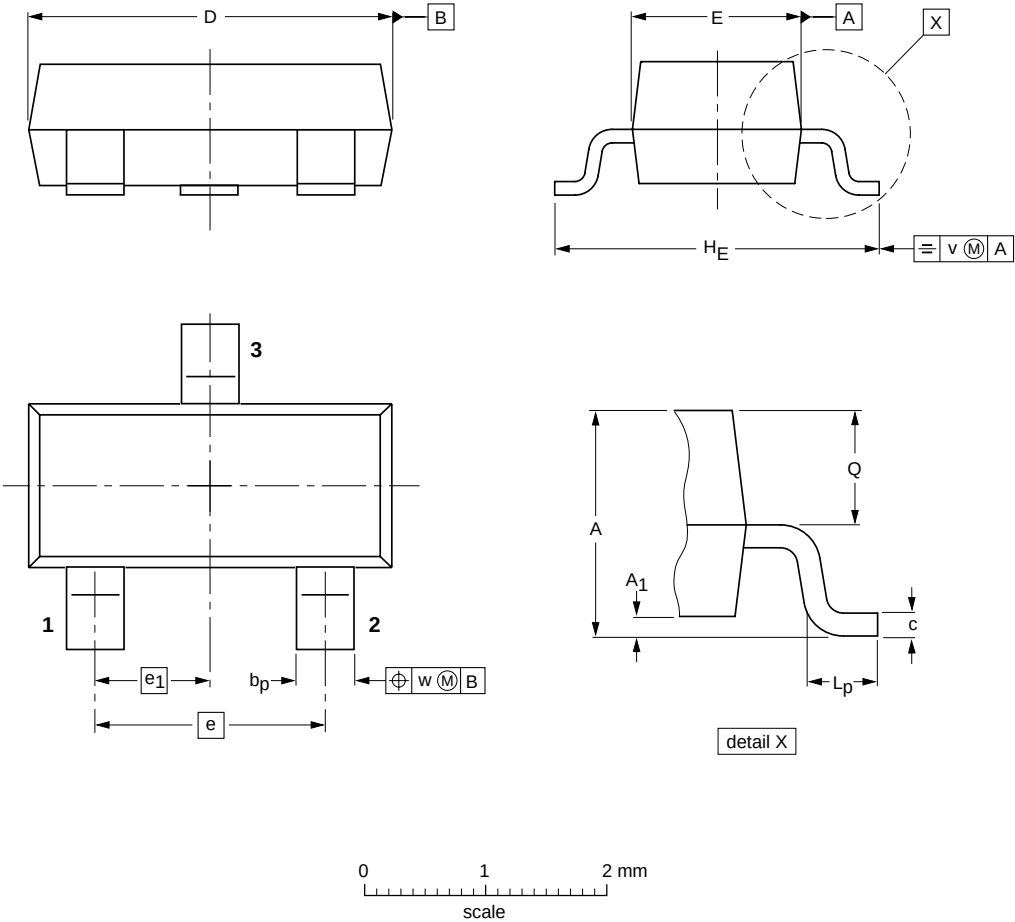
PNP resistor-equipped transistors;
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PDTA124T series

PACKAGE OUTLINES

Plastic surface-mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				04-11-04 06-03-16

PNP resistor-equipped transistors;
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PDTA124T series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

Technical drawing of the SOT54 package showing top, side, and lead detail views with dimension labels A, b, b₁, c, D, d, E, e, e₁, L, L₁.

0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

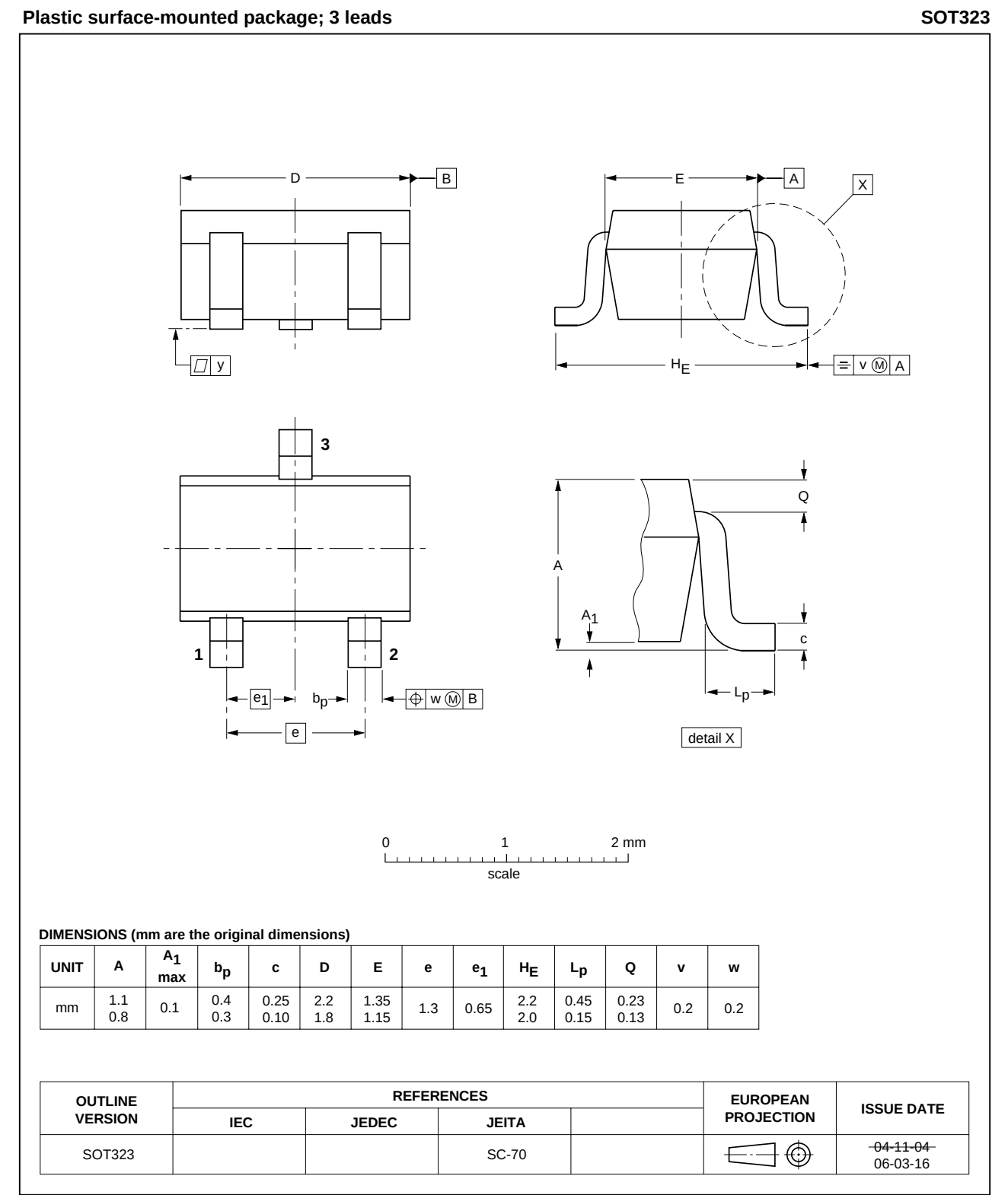
Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			04-06-28 04-11-16

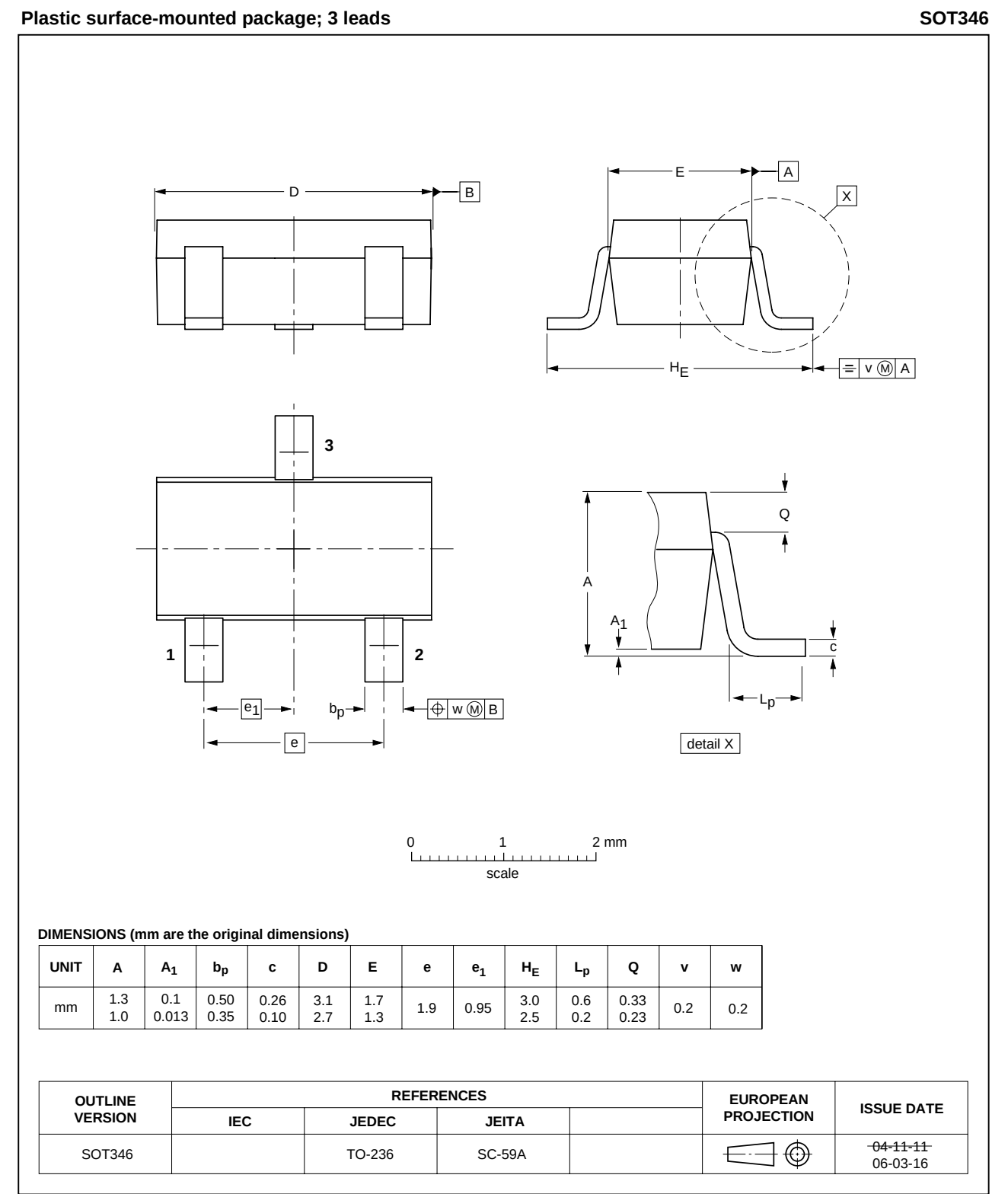
PNP resistor-equipped transistors;
R1 = 22 kΩ, R2 = open

PDTA124T series



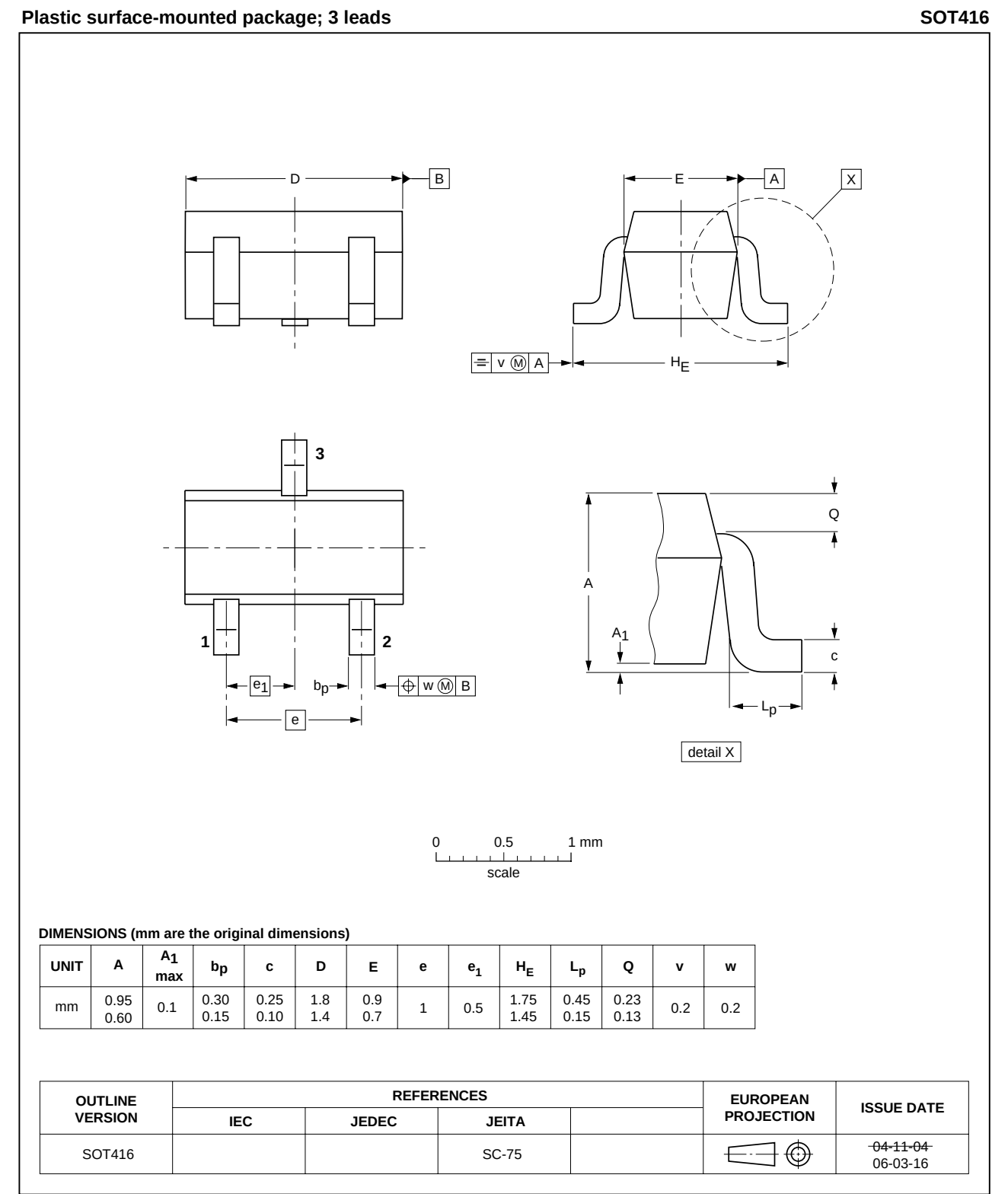
PNP resistor-equipped transistors;
R1 = 22 kΩ, R2 = open

PDTA124T series



PNP resistor-equipped transistors;
R1 = 22 kΩ, R2 = open

PDTA124T series

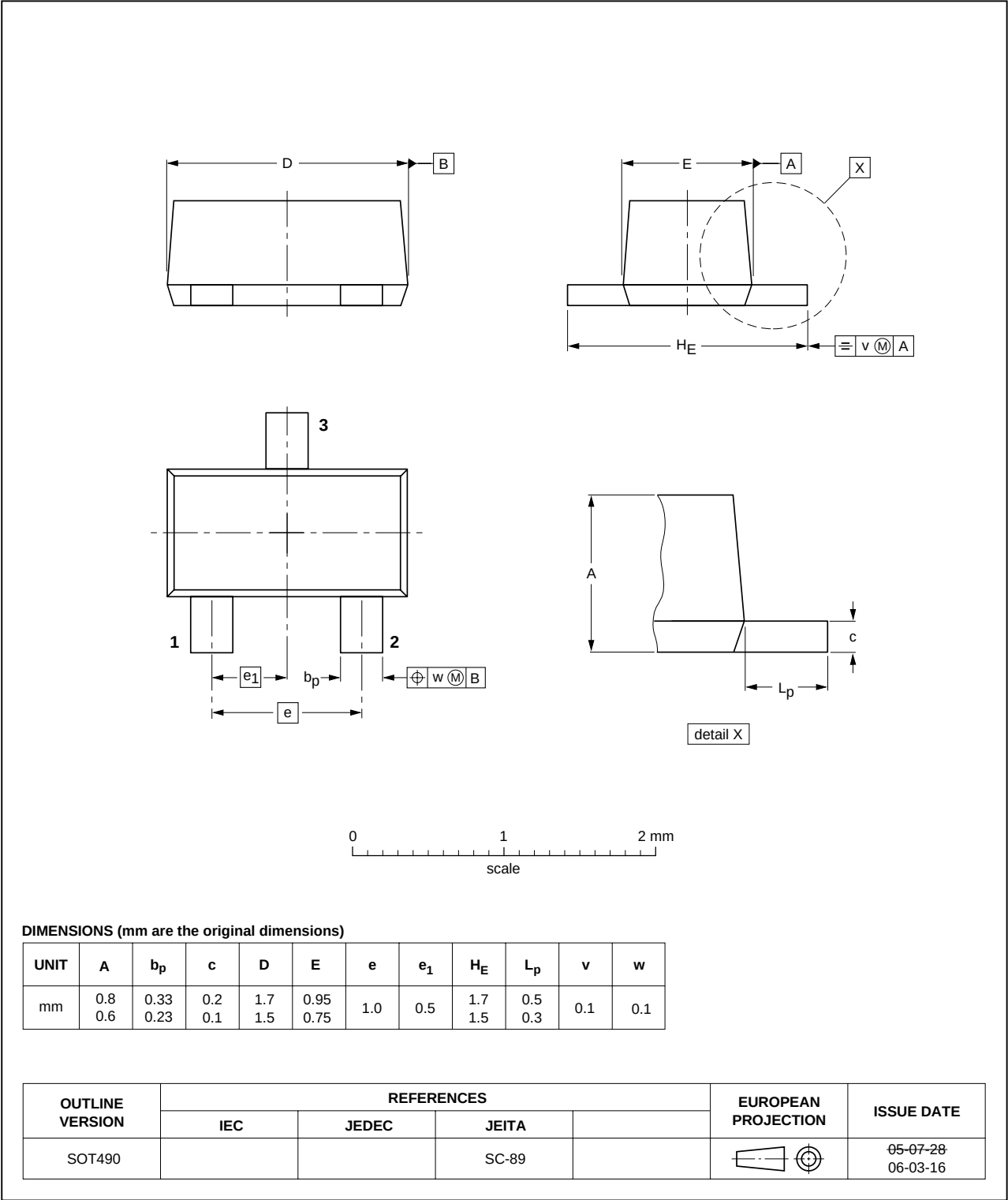


PNP resistor-equipped transistors;
R1 = 22 kΩ, R2 = open

PDTA124T series

Plastic surface-mounted package; 3 leads

SOT490

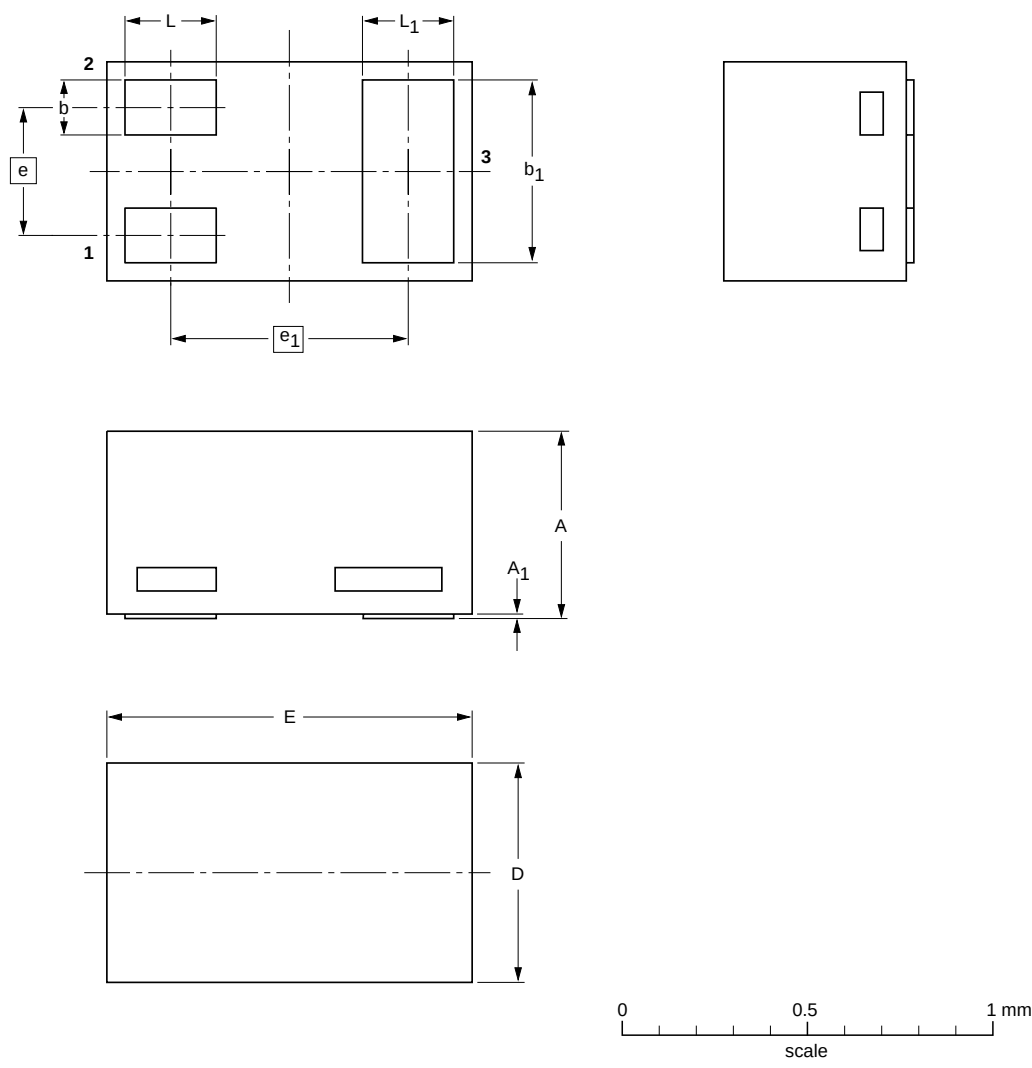


PNP resistor-equipped transistors;
R1 = 22 kΩ, R2 = open

PDTA124T series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note
1. Including plating thickness

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			03-02-05 03-04-03

PNP resistor-equipped transistors;
R1 = 22 kΩ, R2 = open

PDTA124T series

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

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