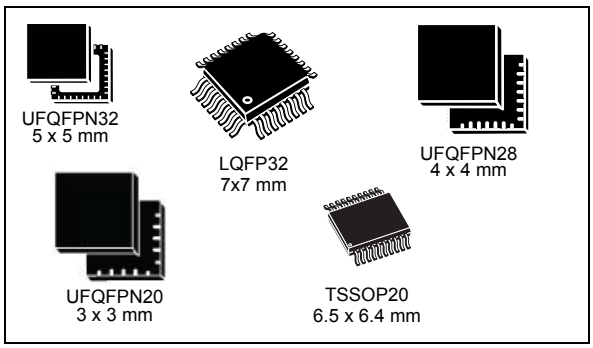
# STM8L101x1 STM8L101x2 STM8L101x3

## 8-bit ultra-low power microcontroller with up to 8 Kbytes Flash, multifunction timers, comparators, USART, SPI, I2C

**Datasheet - production data**

## Features

- Main microcontroller features
  - Supply voltage range 1.65 V to 3.6 V
  - Low power consumption (Halt: 0.3 µA, Active-halt: 0.8 µA, Dynamic Run: 150 µA/MHz)
  - STM8 Core with up to 16 CISC MIPS throughput
  - Temp. range: -40 to 85 °C and 125 °C
- Memories
  - Up to 8 Kbytes of Flash program including up to 2 Kbytes of data EEPROM
  - Error correction code (ECC)
  - Flexible write and read protection modes
  - In-application and in-circuit programming
  - Data EEPROM capability
  - 1.5 Kbytes of static RAM
- Clock management
  - Internal 16 MHz RC with fast wakeup time (typ. 4 µs)
  - Internal low consumption 38 kHz RC driving both the IWDG and the AWU
- Reset and supply management
  - Ultra-low power POR/PDR
  - Three low-power modes: Wait, Active-halt, Halt
- Interrupt management
  - Nested interrupt controller with software priority control
  - Up to 29 external interrupt sources
- I/Os
  - Up to 30 I/Os, all mappable on external interrupt vectors
  - I/Os with programmable input pull-ups, high sink/source capability and one LED driver infrared output




- Peripherals
  - Two 16-bit general purpose timers (TIM2 and TIM3) with up and down counter and 2 channels (used as IC, OC, PWM)
  - One 8-bit timer (TIM4) with 7-bit prescaler
  - Infrared remote control (IR)
  - Independent watchdog
  - Auto-wakeup unit
  - Beeper timer with 1, 2 or 4 kHz frequencies
  - SPI synchronous serial interface
  - Fast I2C Multimaster/slave 400 kHz
  - USART with fractional baud rate generator
  - 2 comparators with 4 inputs each
- Development support
  - Hardware single wire interface module (SWIM) for fast on-chip programming and non intrusive debugging
  - In-circuit emulation (ICE)
- 96-bit unique ID

**Table 1. Device summary**

| Reference | Part numbers |
|---|---|
| STM8L101x1 | STM8L101F1 |
| STM8L101x2 | STM8L101F2, STM8L101G2 |
| STM8L101x3 | STM8L101F3, STM8L101G3, STM8L101K3 |



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# 1 Introduction

This datasheet provides the STM8L101x1 STM8L101x2 STM8L101x3 pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller memory, registers and peripherals, please refer to the STM8L reference manual.

The STM8L101x1 STM8L101x2 STM8L101x3devices are members of the STM8L low-power 8-bit family. They are
referred to as low-density devices in the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller family reference manual (RM0013) and in the STM8L Flash programming manual (PM0054).

All devices of the SM8L product line provide the following benefits:

- Reduced system cost
  - Up to 8 Kbytes of low-density embedded Flash program memory including up to 2 Kbytes of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs.
  - Smaller battery and cheaper power supplies.
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MH, 0.8 µA in Active-halt mode, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Product family operating from 1.65 V to 3.6 V supply.

# 2 Description

The STM8L101x1 STM8L101x2 STM8L101x3 low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All STM8L101xx microcontrollers feature low power low-voltage single-supply program Flash memory. The 8-Kbyte devices embed data EEPROM.

The STM8L101xx low power family is based on a generic set of state-of-the-art peripherals. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

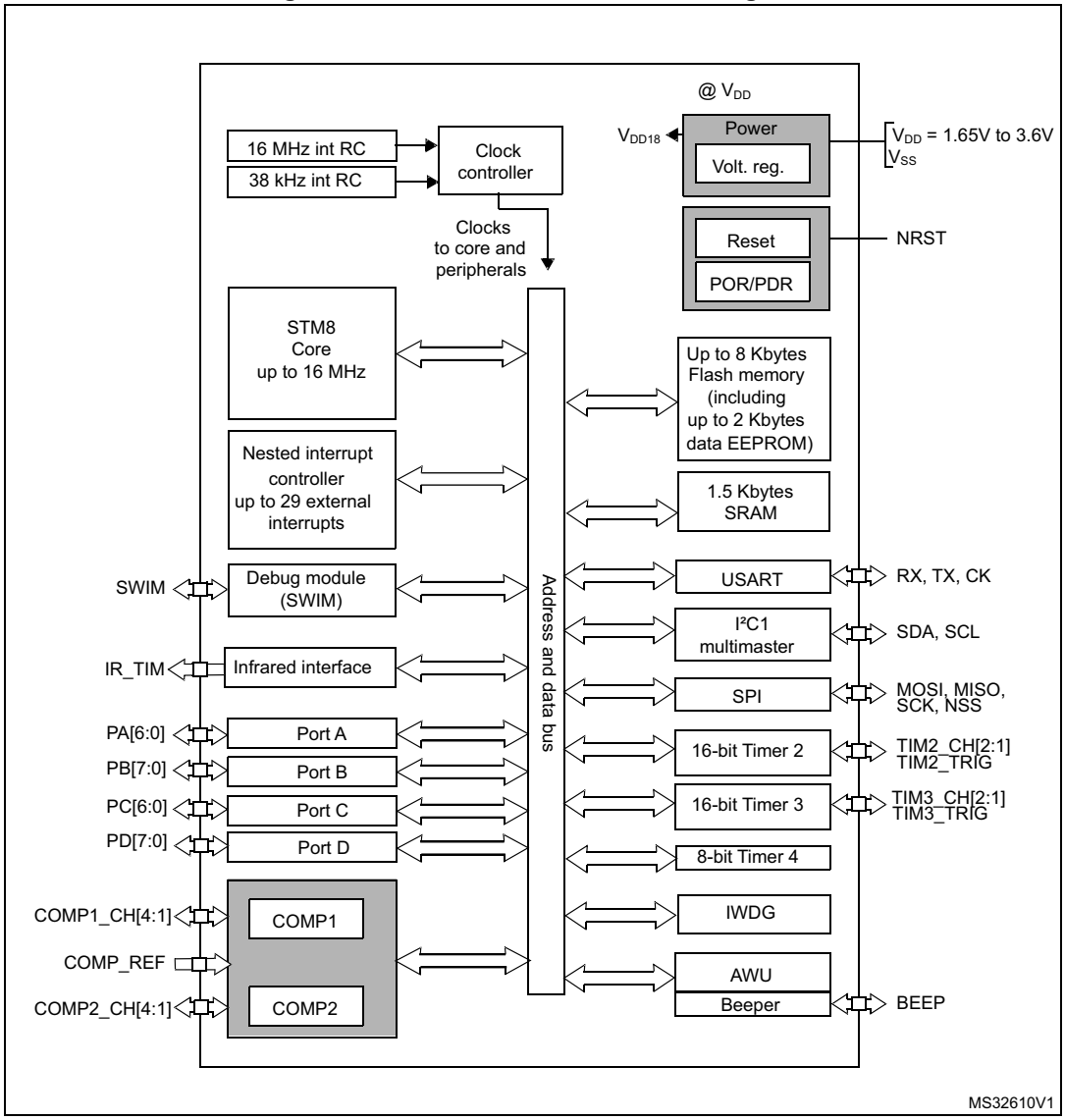
All STM8L low power products are based on the same architecture with the same memory mapping and a coherent pinout.

**Table 2. STM8L101xx device feature summary**

| Features | STM8L101xx | | |
|---|---|---|---|
| Flash | 2 Kbytes of Flash program memory | 4 Kbytes of Flash program memory | 8 Kbytes of Flash program memory including up to 2 Kbytes of Data EEPROM |
| RAM | 1.5 Kbytes | | |
| Peripheral functions | Independent watchdog (IWDG), Auto-wakeup unit (AWU), Beep, Serial peripheral interface (SPI), Inter-integrated circuit (I²C), Universal synchronous / asynchronous receiver / transmitter (USART), 2 comparators, Infrared (IR) interface | | |
| Timers | Two 16-bit timers, one 8-bit timer | | |
| Operating voltage | 1.65 to 3.6 V | | |
| Operating temperature | -40 to +85 °C | | -40 to +85 °C or -40 to +125 °C |
| Packages | UFQFPN20 3x3 | UFQFPN28 4x 4<br>UFQFPN20 3x3<br>TSSOP20 4.4 x 6.4 | UFQFPN28 4x4<br>UFQFPN20 3x3<br>UFQFPN32<br>LQFP32 |

# 3 Product overview

**Figure 1. STM8L101xx device block diagram**




Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog

## 3.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It features 21 internal registers, 20 addressing modes including indexed, indirect and relative addressing, and 80 instructions.

## 3.2 Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

## 3.3 Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

## 3.4 Interrupt controller

The STM8L101xx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 26 interrupt vectors with hardware priority
- Up to 29 external interrupt sources on 10 vectors
- Trap and reset interrupts.

## 3.5 Memory

The STM8L101xx devices have the following main features:

- 1.5 Kbytes of RAM
- The EEPROM is divided into two memory arrays (see the STM8L reference manual for details on the memory mapping):
  - Up to 8 Kbytes of low-density embedded Flash program including up to 2 Kbytes of data EEPROM. Data EEPROM and Flash program areas can be write protected independently by using the memory access security mechanism (MASS).
  - 64 option bytes (one block) of which 5 bytes are already used for the device.

Error correction code is implemented on the EEPROM.

## 3.6 Low power modes

To minimize power consumption, the product features three low power modes:

- Wait mode: CPU clock stopped, selected peripherals at full clock speed.
- Active-halt mode: CPU and peripheral clocks are stopped. The programmable wakeup time is controlled by the AWU unit.
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. Wakeup is triggered by an external interrupt.

## 3.7 Voltage regulators

The STM8L101xx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes: main voltage regulator mode (MVR) and low power voltage regulator mode (LPVR). When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

## 3.8 Clock control

The STM8L101xx embeds a robust clock controller. It is used to distribute the system clock to the core and the peripherals and to manage clock gating for low power modes. This system clock is a 16-MHz High Speed Internal RC oscillator (HSI RC), followed by a programmable prescaler.

In addition, a 38 kHz low speed internal RC oscillator is used by the independent watchdog (IWDG) and Auto-wakeup unit (AWU).

## 3.9 Independent watchdog

The independent watchdog (IWDG) peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 38 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

## 3.10 Auto-wakeup counter

The auto-wakeup (AWU) counter is used to wakeup the device from Active-halt mode.

## 3.11 General purpose and basic timers

STM8L101xx devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

### 16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Time base generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

### 8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

## 3.12 Beeper

The STM8L101xx devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

## 3.13 Infrared (IR) interface

The STM8L101xx devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

## 3.14 Comparators

The STM8L101xx features two zero-crossing comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal (comparison with ground) or external (comparison to a reference pin voltage).

Each comparator is connected to 4 channels, which can be used to generate interrupt, timer input capture or timer break. Their polarity can be inverted.

## 3.15 USART

The USART interface (USART) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

## 3.16 SPI

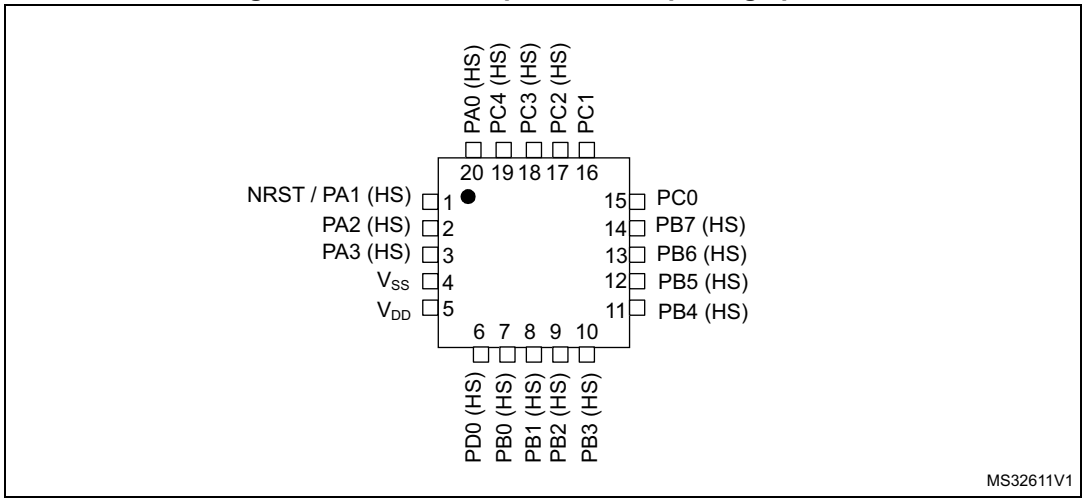
The serial peripheral interface (SPI) provides half/ full duplex synchronous serial communication with external devices. It can be configured as the master and in this case it provides the communication clock (SCK) to the external slave device. The interface can also operate in multi-master configuration.

## 3.17 I²C

The inter-integrated circuit (I2C) bus interface is designed to serve as an interface between the microcontroller and the serial $I^2C$ bus. It provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing. It manages standard and fast speed modes.

# 4 Pin description

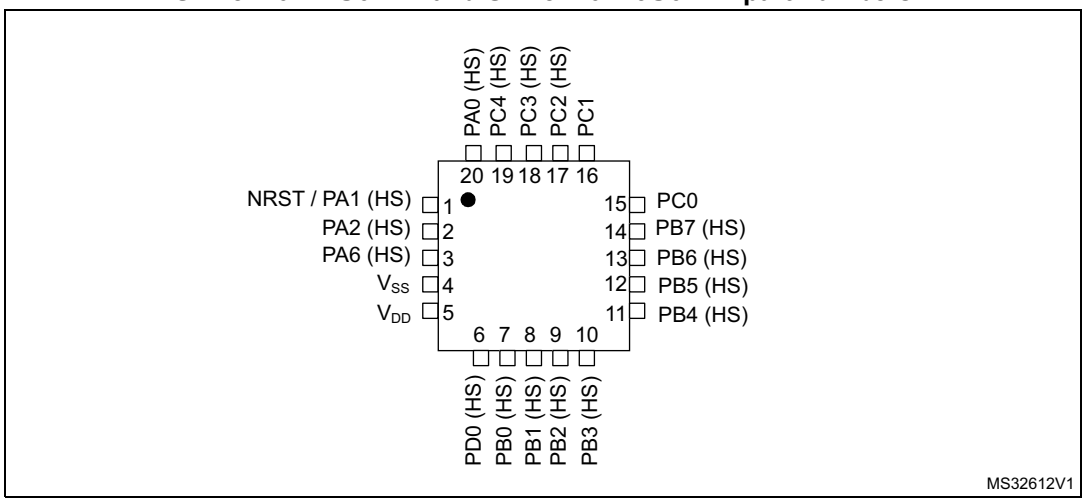
**Figure 2. Standard 20-pin UFQFPN package pinout**




1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

*Note: The COMP_REF pin is not available in this standard 20-pin UFQFPN package. It is available on Port A6 in the Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers.*

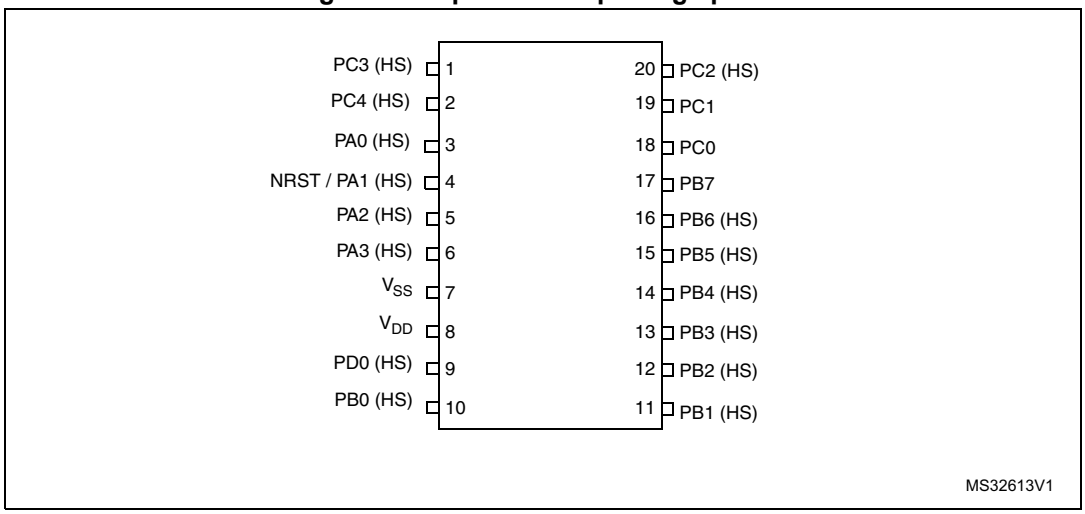
**Figure 3. 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers**




1. Please refer to the warning below.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

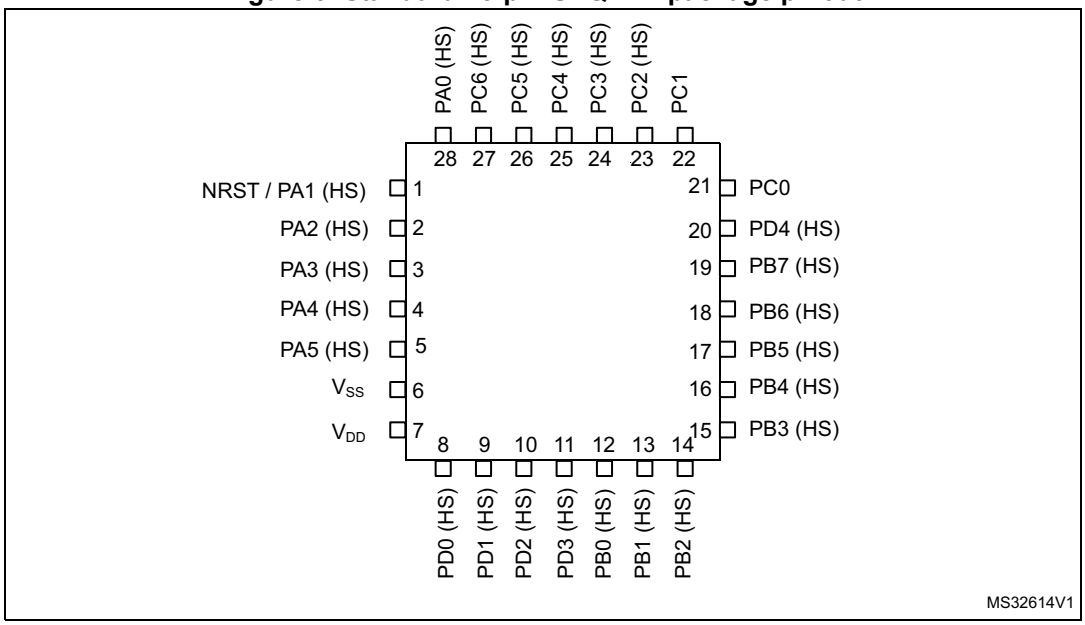
**Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.**

**Figure 4. 20-pin TSSOP package pinout**




1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

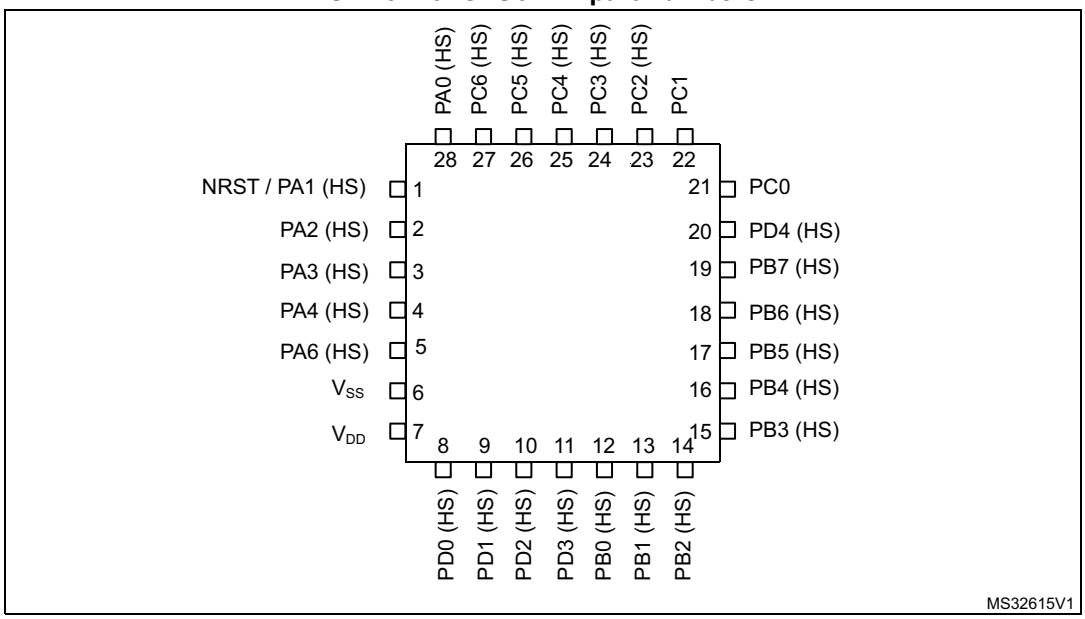
**Figure 5. Standard 28-pin UFQFPN package pinout**




1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

*Note: The COMP_REF pin is not available in this standard 28-pin UFQFPN package. It is available on Port A6 in the Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers.*

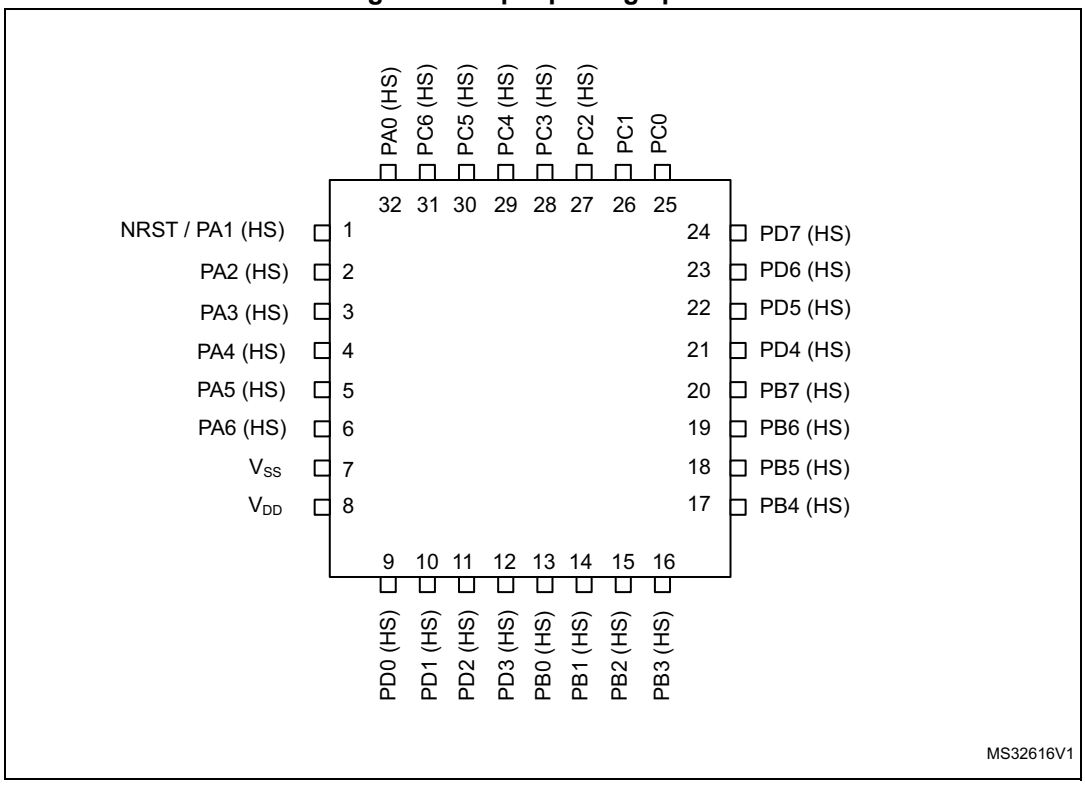
**Figure 6. 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers**




1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

**Warning: For the STM8L101G3U6ATR and STM8L101G2U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.**

**Figure 7. 32-pin package pinout**




1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

**Table 3. Legend/abbreviation for table 4**

| | | |
|---|---|---|
| **Type** | I= input, O = output, S = power supply | |
| **Level** | Input | CM = CMOS |
| | Output | HS = high sink/source (20 mA) |
| **Port and control configuration** | Input | float = floating, wpu = weak pull-up |
| | Output | T = true open drain, OD = open drain, PP = push pull |
| **Reset state** | Bold X (pin state after reset release).<br>Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state). | |

**Table 4. STM8L101xx pin description**

| Pin number | | | | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| standard UFQFPN20 | UFQFPN20 with COMP_REF(1) | TSSOP20 | standard UFQFPN28 | UFQFPN28 with COMP_REF(1) | UFQFPN32 or LQFP32 | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 1 | 1 | 4 | 1 | 1 | 1 | NRST/PA1(2) | I/O | - | **X** | - | HS | - | X | **Reset** | PA1 |
| 2 | 2 | 5 | 2 | 2 | 2 | PA2 | I/O | **X** | X | X | HS | X | X | **Port A2** | - |
| 3 | - | 6 | 3 | 3 | 3 | PA3 | I/O | **X** | X | X | HS | X | X | **Port A3** | - |
| - | - | - | 4 | 4 | 4 | PA4/TIM2_BKIN | I/O | **X** | X | X | HS | X | X | **Port A4** | Timer 2 - break input |
| - | - | - | 5 | - | 5 | PA5/TIM3_BKIN | I/O | **X** | X | X | HS | X | X | **Port A5** | Timer 3 - break input |
| - | 3 | - | - | 5 | 6 | PA6/COMP_REF | I/O | **X** | X | X | HS | X | X | **Port A6** | Comparator external reference |
| 4 | 4 | 7 | 6 | 6 | 7 | $V_{SS}$ | S | - | - | - | - | - | - | Ground | |
| 5 | 5 | 8 | 7 | 7 | 8 | $V_{DD}$ | S | - | - | - | - | - | - | Power supply | |
| 6 | 6 | 9 | 8 | 8 | 9 | PD0/TIM3_CH2/ COMP1_CH3 | I/O | **X** | X | X | HS | X | X | **Port D0** | Timer 3 - channel 2 / Comparator 1 - channel 3 |
| - | - | - | 9 | 9 | 10 | PD1/TIM3_ETR/ COMP1_CH4 | I/O | **X** | X | X | HS | X | X | **Port D1** | Timer 3 - trigger / Comparator 1 - channel 4 |
| - | - | - | 10 | 10 | 11 | PD2/ COMP2_CH3 | I/O | **X** | X | X | HS | X | X | **Port D2** | Comparator 2 - channel 3 |
| - | - | - | 11 | 11 | 12 | PD3/ COMP2_CH4 | I/O | **X** | X | X | HS | X | X | **Port D3** | Comparator 2 - channel 4 |

**Table 4. STM8L101xx pin description (continued)**

| Pin number | | | | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| standard UFQFPN20 | UFQFPN20 with COMP_REF(1) | TSSOP20 | standard UFQFPN28 | UFQFPN28 with COMP_REF(1) | UFQFPN32 or LQFP32 | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 7 | 7 | 10 | 12 | 12 | 13 | PB0/TIM2_CH1/ COMP1_CH1 (3) | I/O | **X**(3) | X(3) | X | HS | X | X | **Port B0** | Timer 2 - channel 1 / Comparator 1 - channel 1 |
| 8 | 8 | 11 | 13 | 13 | 14 | PB1/TIM3_CH1/ COMP1_CH2 | I/O | **X** | X | X | HS | X | X | **Port B1** | Timer 3 - channel 1 / Comparator 1 - channel 2 |
| 9 | 9 | 12 | 14 | 14 | 15 | PB2/ TIM2_CH2/ COMP2_CH1/ | I/O | **X** | X | X | HS | X | X | **Port B2** | Timer 2 - channel 2 / Comparator 2 - channel 1 |
| 10 | 10 | 13 | 15 | 15 | 16 | PB3/TIM2_ETR/ COMP2_CH2 | I/O | **X** | X | X | HS | X | X | **Port B3** | Timer 2 - trigger / Comparator 2 - channel 2 |
| 11 | 11 | 14 | 16 | 16 | 17 | PB4/SPI_NSS(3) | I/O | **X**(3) | X(3) | X | HS | X | X | **Port B4** | SPI master/slave select |
| 12 | 12 | 15 | 17 | 17 | 18 | PB5/SPI_SCK | I/O | **X** | X | X | HS | X | X | **Port B5** | SPI clock |
| 13 | 13 | 16 | 18 | 18 | 19 | PB6/SPI_MOSI | I/O | **X** | X | X | HS | X | X | **Port B6** | SPI master out/ slave in |
| 14 | 14 | 17 | 19 | 19 | 20 | PB7/SPI_MISO | I/O | **X** | X | X | HS | X | X | **Port B7** | SPI master in/ slave out |
| - | - | - | 20 | 20 | 21 | PD4 | I/O | **X** | X | X | HS | X | X | **Port D4** | - |
| - | - | - | - | - | 22 | PD5 | I/O | **X** | X | X | HS | X | X | **Port D5** | - |
| - | - | - | - | - | 23 | PD6 | I/O | **X** | X | X | HS | X | X | **Port D6** | - |
| - | - | - | - | - | 24 | PD7 | I/O | **X** | X | X | HS | X | X | **Port D7** | - |
| 15 | 15 | 18 | 21 | 21 | 25 | PC0/I2C_SDA | I/O | **X** | - | X | - | T(4) | | **Port C0** | I2C data |
| 16 | 16 | 19 | 22 | 22 | 26 | PC1/I2C_SCL | I/O | **X** | - | X | - | T(4) | | **Port C1** | I2C clock |
| 17 | 17 | 20 | 23 | 23 | 27 | PC2/USART_RX | I/O | **X** | X | X | HS | X | X | **Port C2** | USART receive |
| 18 | 18 | 1 | 24 | 24 | 28 | PC3/USART_TX | I/O | **X** | X | X | HS | X | X | **Port C3** | USART transmit |
| 19 | 19 | 2 | 25 | 25 | 29 | PC4/USART_CK/ CCO | I/O | **X** | X | X | HS | X | X | **Port C4** | USART synchronous clock / Configurable clock output |

**Table 4. STM8L101xx pin description (continued)**

| Pin number | | | | | | Pin name | Type | Input | | | Output | | | Main function (after reset) | Alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| standard UFQFPN20 | UFQFPN20 with COMP_REF(1) | TSSOP20 | standard UFQFPN28 | UFQFPN28 with COMP_REF(1) | UFQFPN32 or LQFP32 | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | - | - | 26 | 26 | 30 | PC5 | I/O | **X** | X | X | HS | X | X | **Port C5** | - |
| - | - | - | 27 | 27 | 31 | PC6 | I/O | **X** | X | X | HS | X | X | **Port C6** | - |
| 20 | 20 | 3 | 28 | 28 | 32 | PA0(5)/SWIM/ BEEP/IR_TIM (6) | I/O | X | **X**(5) | X | HS(6) | X | X | **Port A0** | SWIM input and output /Beep output/Timer Infrared output |

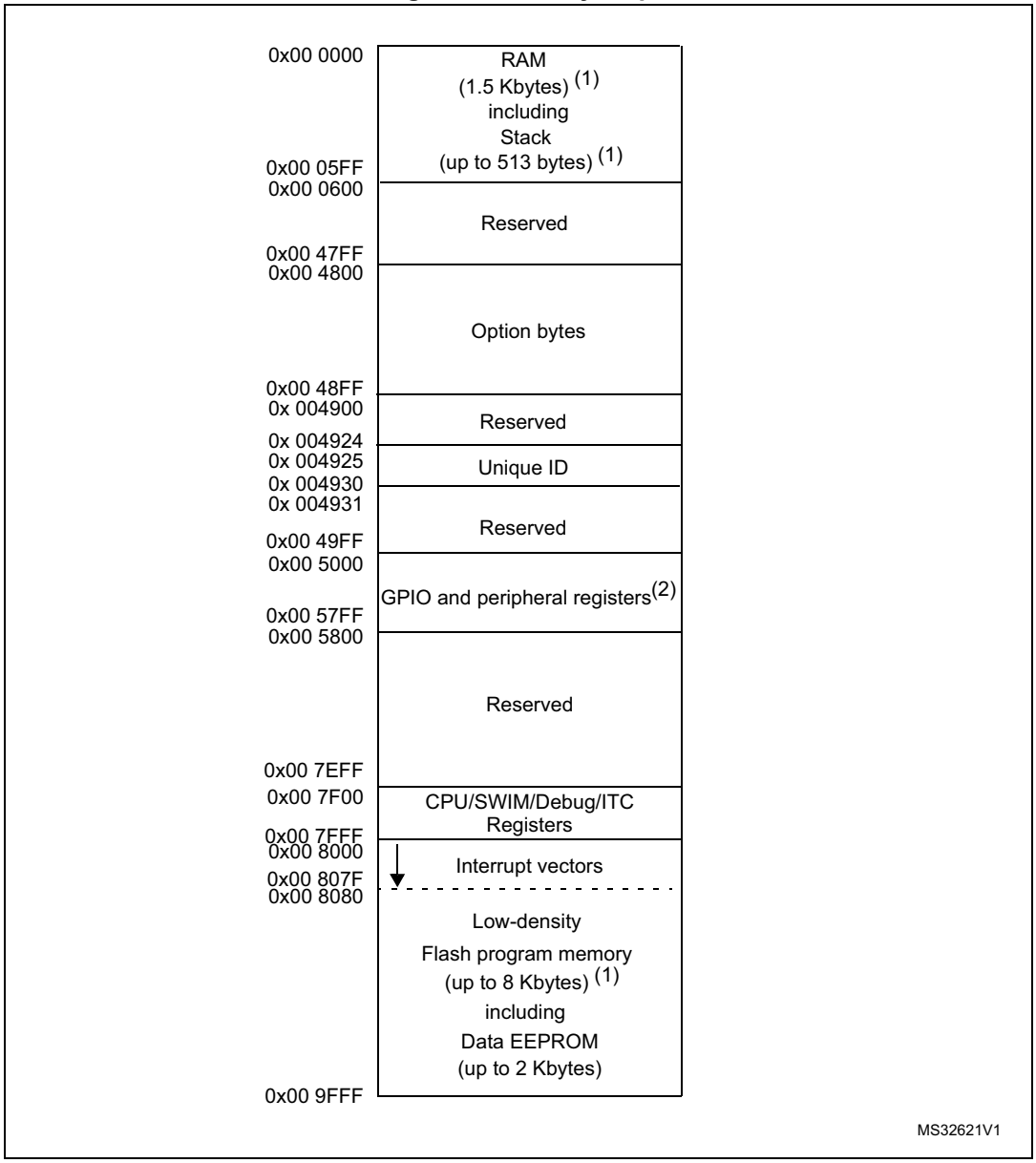
1. Please refer to the warning below.
2. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as a general purpose pin (PA1), it can be configured only as output push-pull, not neither as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L reference manual (RM0013).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to $V_{DD}$ are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High sink LED driver capability available on PA0.

*Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.*

**Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR, STM8L101F3U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.**

# 5 Memory and register map

**Figure 8. Memory map**




1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

**Table 5. Flash and RAM boundary addresses**

| Memory area | Size | Start address | End address |
|---|---|---|---|
| RAM | 1.5 Kbytes | 0x00 0000 | 0x00 05FF |
| Flash program memory | 2 Kbytes | 0x00 8000 | 0x00 87FF |
| | 4 Kbytes | 0x00 8000 | 0x00 8FFF |
| | 8 Kbytes | 0x00 8000 | 0x00 9FFF |

Note: 2 Kbytes of Data EEPROM is only available on devices with 8 Kbytes flash program memory.

**Table 6. I/O Port hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xxx |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x00 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xxx |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A | Port C | PC_ODR | Port C data output latch register | 0x00 |
| 0x00 500B | | PC_IDR | Port C input pin value register | 0xxx |
| 0x00 500C | | PC_DDR | Port C data direction register | 0x00 |
| 0x00 500D | | PC_CR1 | Port C control register 1 | 0x00 |
| 0x00 500E | | PC_CR2 | Port C control register 2 | 0x00 |
| 0x00 500F | Port D | PD_ODR | Port D data output latch register | 0x00 |
| 0x00 5010 | | PD_IDR | Port D input pin value register | 0xxx |
| 0x00 5011 | | PD_DDR | Port D data direction register | 0x00 |
| 0x00 5012 | | PD_CR1 | Port D control register 1 | 0x00 |
| 0x00 5013 | | PD_CR2 | Port D control register 2 | 0x00 |

**Table 7. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5050 | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 5051 | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 5052 | | FLASH _PUKR | Flash Program memory unprotection register | 0x00 |
| 0x00 5053 | | FLASH _DUKR | Data EEPROM unprotection register | 0x00 |
| 0x00 5054 | | FLASH _IAPSR | Flash in-application programming status register | 0xX0 |
| 0x00 5055 to 0x00 509F | Reserved area (75 bytes) | | | |
| 0x00 50A0 | ITC-EXTI | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 | | EXTI_CR3 | External interrupt control register 3 | 0x00 |
| 0x00 50A3 | | EXTI_SR1 | External interrupt status register 1 | 0x00 |
| 0x00 50A4 | | EXTI_SR2 | External interrupt status register 2 | 0x00 |
| 0x00 50A5 | | EXTI_CONF | External interrupt port select register | 0x00 |
| 0x00 50A6 | WFE | WFE_CR1 | WFE control register 1 | 0x00 |
| 0x00 50A7 | | WFE_CR2 | WFE control register 2 | 0x00 |
| 0x00 50A8 to 0x00 50AF | Reserved area (8 bytes) | | | |
| 0x00 50B0 | RST | RST_CR | Reset control register | 0x00 |
| 0x00 50B1 | | RST_SR | Reset status register | 0x01 |
| 0x00 50B2 to 0x00 50BF | Reserved area (14 bytes) | | | |
| 0x00 50C0 | CLK | CLK_CKDIVR | Clock divider register | 0x03 |
| 0x00 50C1 to 0x00 50C2 | | Reserved area (2 bytes) | | |
| 0x00 50C3 | | CLK_PCKENR | Peripheral clock gating register | 0x00 |
| 0x00 50C4 | | Reserved (1 byte) | | |
| 0x00 50C5 | | CLK_CCOR | Configurable clock control register | 0x00 |
| 0x00 50C6 to 0x00 50DF | Reserved area (25 bytes) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 bytes) | | | |
| 0x00 50F0 | AWU | AWU_CSR | AWU control/status register | 0x00 |
| 0x00 50F1 | | AWU_APR | AWU asynchronous prescaler buffer register | 0x3F |
| 0x00 50F2 | | AWU_TBR | AWU timebase selection register | 0x00 |
| 0x00 50F3 | BEEP | BEEP_CSR | BEEP control/status register | 0x1F |
| 0x00 50F4 to 0x00 51FF | Reserved area (268 bytes) | | | |
| 0x00 5200 | SPI | SPI_CR1 | SPI control register 1 | 0x00 |
| 0x00 5201 | | SPI_CR2 | SPI control register 2 | 0x00 |
| 0x00 5202 | | SPI_ICR | SPI interrupt control register | 0x00 |
| 0x00 5203 | | SPI_SR | SPI status register | 0x02 |
| 0x00 5204 | | SPI_DR | SPI data register | 0x00 |
| 0x00 5205 to 0x00 520F | Reserved area (11 bytes) | | | |
| 0x00 5210 | I2C | I2C_CR1 | I2C control register 1 | 0x00 |
| 0x00 5211 | | I2C_CR2 | I2C control register 2 | 0x00 |
| 0x00 5212 | | I2C_FREQR | I2C frequency register | 0x00 |
| 0x00 5213 | | I2C_OARL | I2C own address register low | 0x00 |
| 0x00 5214 | | I2C_OARH | I2C own address register high | 0x00 |
| 0x00 5215 | | Reserved area (1 byte) | | |
| 0x00 5216 | | I2C_DR | I2C data register | 0x00 |
| 0x00 5217 | | I2C_SR1 | I2C status register 1 | 0x00 |
| 0x00 5218 | | I2C_SR2 | I2C status register 2 | 0x00 |
| 0x00 5219 | | I2C_SR3 | I2C status register 3 | 0x00 |
| 0x00 521A | | I2C_ITR | I2C interrupt control register | 0x00 |
| 0x00 521B | | I2C_CCRL | I2C Clock control register low | 0x00 |
| 0x00 521C | | I2C_CCRH | I2C Clock control register high | 0x00 |
| 0x00 521D | | I2C_TRISER | I2C TRISE register | 0x02 |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 521E to 0x00 522F | Reserved area (18 bytes) | | | |
| 0x00 5230 | USART | USART_SR | USART status register | 0xC0 |
| 0x00 5231 | | USART_DR | USART data register | 0xXX |
| 0x00 5232 | | USART_BRR1 | USART baud rate register 1 | 0x00 |
| 0x00 5233 | | USART_BRR2 | USART baud rate register 2 | 0x00 |
| 0x00 5234 | | USART_CR1 | USART control register 1 | 0x00 |
| 0x00 5235 | | USART_CR2 | USART control register 2 | 0x00 |
| 0x00 5236 | | USART_CR3 | USART control register 3 | 0x00 |
| 0x00 5237 | | USART_CR4 | USART control register 4 | 0x00 |
| 0x00 5238 to 0x00 524F | Reserved area (18 bytes) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5250 | TIM2 | TIM2_CR1 | TIM2 control register 1 | 0x00 |
| 0x00 5251 | | TIM2_CR2 | TIM2 control register 2 | 0x00 |
| 0x00 5252 | | TIM2_SMCR | TIM2 slave mode control register | 0x00 |
| 0x00 5253 | | TIM2_ETR | TIM2 external trigger register | 0x00 |
| 0x00 5254 | | TIM2_IER | TIM2 interrupt enable register | 0x00 |
| 0x00 5255 | | TIM2_SR1 | TIM2 status register 1 | 0x00 |
| 0x00 5256 | | TIM2_SR2 | TIM2 status register 2 | 0x00 |
| 0x00 5257 | | TIM2_EGR | TIM2 event generation register | 0x00 |
| 0x00 5258 | | TIM2_CCMR1 | TIM2 capture/compare mode register 1 | 0x00 |
| 0x00 5259 | | TIM2_CCMR2 | TIM2 capture/compare mode register 2 | 0x00 |
| 0x00 525A | | TIM2_CCER1 | TIM2 capture/compare enable register 1 | 0x00 |
| 0x00 525B | | TIM2_CNTRH | TIM2 counter high | 0x00 |
| 0x00 525C | | TIM2_CNTRL | TIM2 counter low | 0x00 |
| 0x00 525D | | TIM2_PSCR | TIM2 prescaler register | 0x00 |
| 0x00 525E | | TIM2_ARRH | TIM2 auto-reload register high | 0xFF |
| 0x00 525F | | TIM2_ARRL | TIM2 auto-reload register low | 0xFF |
| 0x00 5260 | | TIM2_CCR1H | TIM2 capture/compare register 1 high | 0x00 |
| 0x00 5261 | | TIM2_CCR1L | TIM2 capture/compare register 1 low | 0x00 |
| 0x00 5262 | | TIM2_CCR2H | TIM2 capture/compare register 2 high | 0x00 |
| 0x00 5263 | | TIM2_CCR2L | TIM2 capture/compare register 2 low | 0x00 |
| 0x00 5264 | | TIM2_BKR | TIM2 break register | 0x00 |
| 0x00 5265 | | TIM2_OISR | TIM2 output idle state register | 0x00 |
| 0x00 5266 to 0x00 527F | Reserved area (26 bytes) | | | |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5280 | TIM3 | TIM3_CR1 | TIM3 control register 1 | 0x00 |
| 0x00 5281 | | TIM3_CR2 | TIM3 control register 2 | 0x00 |
| 0x00 5282 | | TIM3_SMCR | TIM3 slave mode control register | 0x00 |
| 0x00 5283 | | TIM3_ETR | TIM3 external trigger register | 0x00 |
| 0x00 5284 | | TIM3_IER | TIM3 interrupt enable register | 0x00 |
| 0x00 5285 | | TIM3_SR1 | TIM3 status register 1 | 0x00 |
| 0x00 5286 | | TIM3_SR2 | TIM3 status register 2 | 0x00 |
| 0x00 5287 | | TIM3_EGR | TIM3 event generation register | 0x00 |
| 0x00 5288 | | TIM3_CCMR1 | TIM3 capture/compare mode register 1 | 0x00 |
| 0x00 5289 | | TIM3_CCMR2 | TIM3 capture/compare mode register 2 | 0x00 |
| 0x00 528A | | TIM3_CCER1 | TIM3 capture/compare enable register 1 | 0x00 |
| 0x00 528B | | TIM3_CNTRH | TIM3 counter high | 0x00 |
| 0x00 528C | | TIM3_CNTRL | TIM3 counter low | 0x00 |
| 0x00 528D | | TIM3_PSCR | TIM3 prescaler register | 0x00 |
| 0x00 528E | | TIM3_ARRH | TIM3 auto-reload register high | 0xFF |
| 0x00 528F | | TIM3_ARRL | TIM3 auto-reload register low | 0xFF |
| 0x00 5290 | | TIM3_CCR1H | TIM3 capture/compare register 1 high | 0x00 |
| 0x00 5291 | | TIM3_CCR1L | TIM3 capture/compare register 1 low | 0x00 |
| 0x00 5292 | | TIM3_CCR2H | TIM3 capture/compare register 2 high | 0x00 |
| 0x00 5293 | | TIM3_CCR2L | TIM3 capture/compare register 2 low | 0x00 |
| 0x00 5294 | | TIM3_BKR | TIM3 break register | 0x00 |
| 0x00 5295 | | TIM3_OISR | TIM3 output idle state register | 0x00 |
| 0x00 5296 to 0x00 52DF | Reserved area (74 bytes) | | | |
| 0x00 52E0 | TIM4 | TIM4_CR1 | TIM4 control register 1 | 0x00 |
| 0x00 52E1 | | TIM4_CR2 | TIM4 control register 2 | 0x00 |
| 0x00 52E2 | | TIM4_SMCR | TIM4 Slave mode control register | 0x00 |
| 0x00 52E3 | | TIM4_IER | TIM4 interrupt enable register | 0x00 |
| 0x00 52E4 | | TIM4_SR1 | TIM4 Status register 1 | 0x00 |
| 0x00 52E5 | | TIM4_EGR | TIM4 event generation register | 0x00 |
| 0x00 52E6 | | TIM4_CNTR | TIM4 counter | 0x00 |
| 0x00 52E7 | | TIM4_PSCR | TIM4 prescaler register | 0x00 |
| 0x00 52E8 | | TIM4_ARR | TIM4 auto-reload register low | 0xFF |

**Table 7. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 52E9 to 0x00 52FE | Reserved area (23 bytes) | | | |
| 0x00 52FF | IRTIM | IR_CR | Infra-red control register | 0x00 |
| 0x00 5300 | COMP | COMP_CR | Comparator control register | 0x00 |
| 0x00 5301 | | COMP_CSR | Comparator status register | 0x00 |
| 0x00 5302 | | COMP_CCS | Comparator channel selection register | 0x00 |

**Table 8. CPU/SWIM/debug module/interrupt controller registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F00 | CPU | A | Accumulator | 0x00 |
| 0x00 7F01 | | PCE | Program counter extended | 0x00 |
| 0x00 7F02 | | PCH | Program counter high | 0x80 |
| 0x00 7F03 | | PCL | Program counter low | 0x00 |
| 0x00 7F04 | | XH | X index register high | 0x00 |
| 0x00 7F05 | | XL | X index register low | 0x00 |
| 0x00 7F06 | | YH | Y index register high | 0x00 |
| 0x00 7F07 | | YL | Y index register low | 0x00 |
| 0x00 7F08 | | SPH | Stack pointer high | 0x05 |
| 0x00 7F09 | | SPL | Stack pointer low | 0xFF |
| 0x00 7F0A | | CC | Condition code register | 0x28 |
| 0x00 7F0B to 0x00 7F5F | Reserved area (85 bytes) | | | |
| 0x00 7F60 | CFG | CFG_GCR | Global configuration register | 0x00 |
| 0x00 7F61 0x00 7F6F | Reserved area (15 bytes) | | | |
| 0x00 7F70 | ITC-SPR (1) | ITC_SPR1 | Interrupt Software priority register 1 | 0xFF |
| 0x00 7F71 | | ITC_SPR2 | Interrupt Software priority register 2 | 0xFF |
| 0x00 7F72 | | ITC_SPR3 | Interrupt Software priority register 3 | 0xFF |
| 0x00 7F73 | | ITC_SPR4 | Interrupt Software priority register 4 | 0xFF |
| 0x00 7F74 | | ITC_SPR5 | Interrupt Software priority register 5 | 0xFF |
| 0x00 7F75 | | ITC_SPR6 | Interrupt Software priority register 6 | 0xFF |
| 0x00 7F76 | | ITC_SPR7 | Interrupt Software priority register 7 | 0xFF |
| 0x00 7F77 | | ITC_SPR8 | Interrupt Software priority register 8 | 0xFF |

**Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F78 to 0x00 7F79 | Reserved area (2 bytes) | | | |
| 0x00 7F80 | SWIM | SWIM_CSR | SWIM control status register | 0x00 |
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 bytes) | | | |
| 0x00 7F90 | DM | DM_BK1RE | Breakpoint 1 register extended byte | 0xFF |
| 0x00 7F91 | | DM_BK1RH | Breakpoint 1 register high byte | 0xFF |
| 0x00 7F92 | | DM_BK1RL | Breakpoint 1 register low byte | 0xFF |
| 0x00 7F93 | | DM_BK2RE | Breakpoint 2 register extended byte | 0xFF |
| 0x00 7F94 | | DM_BK2RH | Breakpoint 2 register high byte | 0xFF |
| 0x00 7F95 | | DM_BK2RL | Breakpoint 2 register low byte | 0xFF |
| 0x00 7F96 | | DM_CR1 | Debug module control register 1 | 0x00 |
| 0x00 7F97 | | DM_CR2 | Debug module control register 2 | 0x00 |
| 0x00 7F98 | | DM_CSR1 | Debug module control/status register 1 | 0x10 |
| 0x00 7F99 | | DM_CSR2 | Debug module control/status register 2 | 0x00 |
| 0x00 7F9A | | DM_ENFCTR | Enable function register | 0xFF |

1. Refer to *Table 7: General hardware register map on page 25* (addresses 0x00 50A0 to 0x00 50A5) for a list of external interrupt registers.

# 6 Interrupt vector mapping

**Table 9. Interrupt mapping**

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode) | Vector address |
|---|---|---|---|---|---|---|---|
| - | RESET | Reset | Yes | Yes | Yes | Yes | 0x00 8000 |
| - | TRAP | Software interrupt | - | - | - | - | 0x00 8004 |
| 0 | - | Reserved | - | - | - | - | 0x00 8008 |
| 1 | FLASH | EOP/WR_PG_DIS | - | - | Yes | Yes(1) | 0x00 800C |
| 2-3 | - | Reserved | - | - | - | - | 0x00 8010 -0x00 8017 |
| 4 | AWU | Auto wakeup from Halt | - | Yes | Yes | Yes(1) | 0x00 8018 |
| 5 | - | Reserved | - | - | - | - | 0x00 801C |
| 6 | EXTIB | External interrupt port B | Yes | Yes | Yes | Yes | 0x00 8020 |
| 7 | EXTID | External interrupt port D | Yes | Yes | Yes | Yes | 0x00 8024 |
| 8 | EXTI0 | External interrupt 0 | Yes | Yes | Yes | Yes | 0x00 8028 |
| 9 | EXTI1 | External interrupt 1 | Yes | Yes | Yes | Yes | 0x00 802C |
| 10 | EXTI2 | External interrupt 2 | Yes | Yes | Yes | Yes | 0x00 8030 |
| 11 | EXTI3 | External interrupt 3 | Yes | Yes | Yes | Yes | 0x00 8034 |
| 12 | EXTI4 | External interrupt 4 | Yes | Yes | Yes | Yes | 0x00 8038 |
| 13 | EXTI5 | External interrupt 5 | Yes | Yes | Yes | Yes | 0x00 803C |
| 14 | EXTI6 | External interrupt 6 | Yes | Yes | Yes | Yes | 0x00 8040 |
| 15 | EXTI7 | External interrupt 7 | Yes | Yes | Yes | Yes | 0x00 8044 |
| 16 | - | Reserved | - | - | - | - | 0x00 8048 |
| 17 | - | Reserved | - | - | - | - | 0x00 804C -0x00 804F |
| 18 | COMP | Comparators | - | - | Yes | Yes(1) | 0x00 8050 |
| 19 | TIM2 | Update /Overflow/Trigger/Break | - | - | Yes | Yes | 0x00 8054 |
| 20 | TIM2 | Capture/Compare | - | - | Yes | Yes | 0x00 8058 |
| 21 | TIM3 | Update /Overflow/Break | - | - | Yes | Yes(1) | 0x00 805C |
| 22 | TIM3 | Capture/Compare | - | - | Yes | Yes(1) | 0x00 8060 |
| 23-24 | - | Reserved | - | - | - | - | 0x00 8064-0x00 806B |
| 25 | TIM4 | Update /Trigger | - | - | Yes | Yes(1) | 0x00 806C |
| 26 | SPI | End of Transfer | Yes | Yes | Yes | Yes(1) | 0x00 8070 |

**Table 9. Interrupt mapping (continued)**

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode) | Vector address |
|---|---|---|---|---|---|---|---|
| 27 | USART | Transmission complete/transmit data register empty | - | - | Yes | Yes(1) | 0x00 8074 |
| 28 | USART | Receive Register DATA FULL/overrun/idle line detected/parity error | - | - | Yes | Yes(1) | 0x00 8078 |
| 29 | I2C | I2C interrupt(2) | Yes | Yes | Yes | Yes(1) | 0x00 807C |

1. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. Refer to Section *Wait for event (WFE) mode* in the RM0013 reference manual.
2. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

# 7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated row of the memory.

All option bytes can be modified only in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

Refer to the STM8L Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

**Table 10. Option bytes**

| Addr. | Option name | Option byte No. | Option bits | | | | | | | | Factory default setting |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x4800 | Read-out protection (ROP) | OPT1 | ROP[7:0] | | | | | | | | 0x00 |
| 0x4807 | - | - | Must be programmed to 0x00 | | | | | | | | 0x00 |
| 0x4802 | UBC (User Boot code size) | OPT2 | UBC[7:0] | | | | | | | | 0x00 |
| 0x4803 | DATASIZE | OPT3 | DATASIZE[7:0] | | | | | | | | 0x00 |
| 0x4808 | Independent watchdog option | OPT4 [1:0] | Reserved | | | | | | IWDG _HALT | IWDG _HW | 0x00 |

**Table 11. Option byte description**

| | |
|---|---|
| OPT1 | **ROP[7:0]** *Memory readout protection (ROP)*<br>0xAA: Enable readout protection (write access via SWIM protocol)<br>Refer to *Read-out protection* section in the STM8L reference manual (RM0013) for details. |
| OPT2 | **UBC[7:0]** *Size of the user boot code area*<br>0x00: no UBC<br>0x01-0x02: UBC contains only the interrupt vectors.<br>0x03: Page 0 and 1 reserved for the interrupt vectors. Page 2 is available to store user boot code. Memory is write protected<br>...<br>0x7F - Page 0 to 126 reserved for UBC, memory is write protected<br>Refer to *User boot area (UBC)* section in the STM8L reference manual (RM0013) for more details.<br>UBC[7] is forced to 0 internally by HW. |

**Table 11. Option byte description (continued)**

| | |
|---|---|
| OPT3 | **DATASIZE[7:0]** Size of the data EEPROM area<br>0x00: no data EEPROM area (1)<br>0x01: 1 page reserved for data storage from 0x9FC0 to 0x9FFF(1)<br>0x02: 2 pages reserved for data storage from 0x9F80 to 0x9FFF(1)<br>... (1)<br>0x20: 32 pages reserved for data storage from 0x9800 to 0x9FFF(1)<br>Refer to *Data EEPROM (DATA)* section in the STM8L reference manual (RM0013) for more details.<br>DATASIZE[7:6] are forced to 0 internal by HW. |
| OPT4 | **IWDG_HW:** *Independent watchdog*<br>0: Independent watchdog activated by software<br>1: Independent watchdog activated by hardware |
| | **IWDG_HALT:** *Independent window watchdog reset on Halt/Active-halt*<br>0: Independent watchdog continues running in Halt/Active-halt mode<br>1: Independent watchdog stopped in Halt/Active-halt mode |

1. 0x00 is the only allowed value for 4 Kbyte STM8L101xx devices.

**Caution:** After a device reset, read access to the program memory is not guaranteed if address 0x4807 is not programmed to 0x00.

# 8 Unique ID

STM8L101xx devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory
- To activate secure boot processes.

**Table 12. Unique ID registers (96 bits)**

| Address | Content description | Unique ID bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x4925 | X co-ordinate on the wafer | U_ID[7:0] | | | | | | | |
| 0x4926 | | U_ID[15:8] | | | | | | | |
| 0x4927 | Y co-ordinate on the wafer | U_ID[23:16] | | | | | | | |
| 0x4928 | | U_ID[31:24] | | | | | | | |
| 0x4929 | Wafer number | U_ID[39:32] | | | | | | | |
| 0x492A | Lot number | U_ID[47:40] | | | | | | | |
| 0x492B | | U_ID[55:48] | | | | | | | |
| 0x492C | | U_ID[63:56] | | | | | | | |
| 0x492D | | U_ID[71:64] | | | | | | | |
| 0x492E | | U_ID[79:72] | | | | | | | |
| 0x492F | | U_ID[87:80] | | | | | | | |
| 0x4930 | | U_ID[95:88] | | | | | | | |

# 9 Electrical parameters

## 9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to $V_{SS}$.

### 9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$= 25 °C and $T_A$ = $T_A$ max (given by the selected temperature range).

*Note: The values given at 85 °C <$T_A$ ≤ 125 °C are only valid for suffix 3 versions.*

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

### 9.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3 V. They are given only as design guidelines and are not tested.

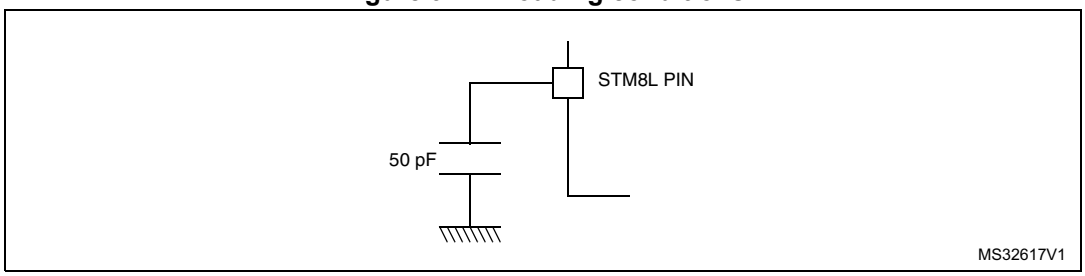
### 9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

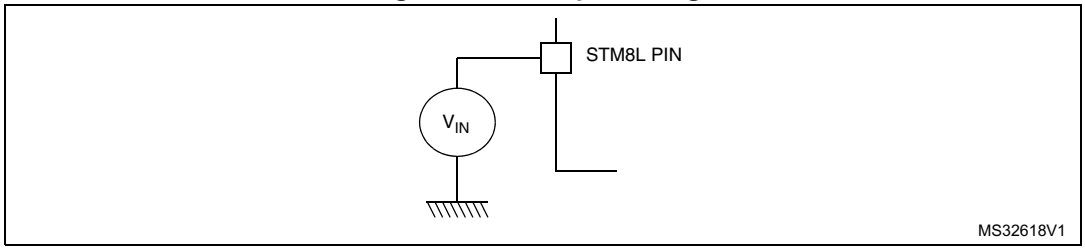
**Figure 9. Pin loading conditions**



### 9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

**Figure 10. Pin input voltage**




## 9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics* and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile is compliant with the JEDEC JESD47 qualification standard; extended mission profiles are available on demand.

**Table 13. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$- $V_{SS}$ | External supply voltage | -0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on true open drain pins (PC0 and PC1)(1) | $V_{SS}$-0.3 | $V_{DD}$ + 4.0 | |
| | Input voltage on any other pin (2) | $V_{SS}$-0.3 | 4.0 | |
| $V_{ESD}$ | Electrostatic discharge voltage | see *Absolute maximum ratings (electrical sensitivity) on page 61* | | - |

1. Positive injection is not possible on these I/Os. $V_{IN}$ maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

**Table 14. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power line (source) | 80 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground line (sink) | 80 | |
| $I_{IO}$ | Output current sunk by IR_TIM pin (with high sink LED driver capability) | 80 | |
| | Output current sunk by any other I/O and control pin | 25 | |
| | Output current sourced by any I/Os and control pin | -25 | |
| $I_{INJ(PIN)}$ | Injected current on true open-drain pins (PC0 and PC1)(1) | -5 | |
| | Injected current on any other pin (2) | ±5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) (3) | ±25 | |

1. Positive injection is not possible on these I/Os. $V_{IN}$ maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

**Table 15. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to +150 | ° C |
| $T_J$ | Maximum junction temperature | 150 | |

## 9.3 Operating conditions

Subject to general operating conditions for $V_{DD}$ and $T_A$.

### 9.3.1 General operating conditions

**Table 16. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MASTER}$ (1) | Master clock frequency | 1.65 V ≤$V_{DD}$ < 3.6 V | 2 | 16 | MHz |
| $V_{DD}$ | Standard operating voltage | - | 1.65 | 3.6 | V |
| $P_D$ (2) | Power dissipation at $T_A$= 85 °C for suffix 6 devices | LQFP32 | - | 288 | mW |
| | | UFQFPN32 | - | 288 | |
| | | UFQFPN28 | - | 250 | |
| | | TSSOP20 | - | 181 | |
| | | UFQFPN20 | - | 196 | |
| | Power dissipation at $T_A$= 125 °C for suffix 3 devices | LQFP32 | - | 83 | |
| | | UFQFPN32 | - | 185 | |
| | | UFQFPN28 | - | 62 | |
| | | TSSOP20 | - | 45 | |
| | | UFQFPN20 | - | 49 | |
| $T_A$ | Temperature range | 1.65 V ≤$V_{DD}$ < 3.6 V (6 suffix version) | –40 | 85 | °C |
| | | 1.65 V ≤$V_{DD}$ < 3.6 V (3 suffix version) | –40 | 125 | |
| $T_J$ | Junction temperature range | -40 °C ≤$T_A$ ≤85 °C (6 suffix version) | - 40 | 105 | °C |
| | | -40 °C ≤$T_A$ ≤125 °C (3 suffix version) | –40 | 130 | °C |

1. $f_{MASTER}$ = $f_{CPU}$
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with $T_{Jmax}$ in this table and $\Theta_{JA}$ in table “Thermal characteristics”

### 9.3.2 Power-up / power-down operating conditions

**Table 17. Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | - | 20 | - | 1300 | µs/V |
| $t_{TEMP}$ | Reset release delay | $V_{DD}$ rising | - | 1 | - | ms |
| $V_{POR}$(1)(2) | Power on reset threshold | - | 1.35 | - | 1.65(3) | V |
| $V_{PDR}$(1)(2) | Power down reset threshold | - | 1.40 | - | 1.60 | V |

1. Guaranteed by characterization results.
2. Correct device reset during power on sequence is guaranteed when $t_{VDD[max]}$ is respected. External reset circuit is recommended to ensure correct device reset during power down, when $V_{PDR} < V_{DD} < V_{DD[min]}$.
3. Tested in production.

### 9.3.3 Supply current characteristics

#### Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 18. Total current consumption in Run mode (1)**

| Symbol | Parameter | Conditions(2) | | Typ | Max(3) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\ (Run)}$ | Supply current in Run mode(4) (5) | Code executed from RAM | $f_{MASTER}$ = 2 MHz | 0.39 | 0.60 | mA |
| | | | $f_{MASTER}$ = 4 MHz | 0.55 | 0.70 | |
| | | | $f_{MASTER}$ = 8 MHz | 0.90 | 1.20 | |
| | | | $f_{MASTER}$ = 16 MHz | 1.60 | 2.10(6) | |
| | | Code executed from Flash | $f_{MASTER}$ = 2 MHz | 0.55 | 0.70 | |
| | | | $f_{MASTER}$ = 4 MHz | 0.88 | 1.80 | |
| | | | $f_{MASTER}$ = 8 MHz | 1.50 | 2.50 | |
| | | | $f_{MASTER}$ = 16 MHz | 2.70 | 3.50 | |

1. Based on characterization results, unless otherwise specified.
2. All peripherals off, $V_{DD}$ from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{MASTER}$
3. Maximum values are given for $T_A$ = –40 to 125 °C.
4. CPU executing typical data processing.
5. An approximate value of $I_{DD(Run)}$ can be given by the following formula: $I_{DD(Run)} = f_{MASTER}$ x 150 µA/MHz +215 µA.
6. Tested in production.

**Figure 11. $I_{DD(RUN)}$ vs. $V_{DD}$, $f_{CPU}$ = 2 MHz**

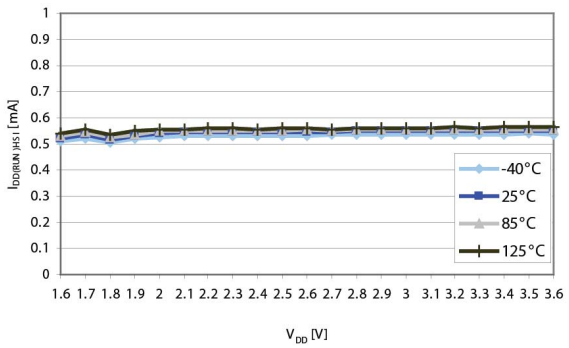
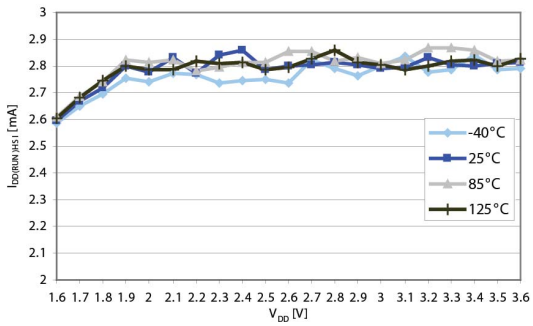



**Figure 12. $I_{DD(RUN)}$ vs. $V_{DD}$, $f_{CPU}$ = 16 MHz**




1. Typical current consumption measured with code executed from Flash.

**Table 19. Total current consumption in Wait mode(1)**

| Symbol | Parameter | Conditions | | Typ | Max(2) | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\ (Wait)}$ | Supply current in Wait mode | CPU not clocked, all peripherals off, HSI internal RC osc. | $f_{MASTER}$ = 2 MHz | 245 | 400 | µA |
| | | | $f_{MASTER}$ = 4 MHz | 300 | 450 | |
| | | | $f_{MASTER}$ = 8 MHz | 380 | 600 | |
| | | | $f_{MASTER}$ = 16 MHz | 510 | 800 | |

1. Based on characterization results, unless otherwise specified.
2. Maximum values are given for $T_A$ = -40 to 125 °C.

**Figure 13. $I_{DD(WAIT)}$ vs. $V_{DD}$, $f_{CPU}$ = 2 MHz**

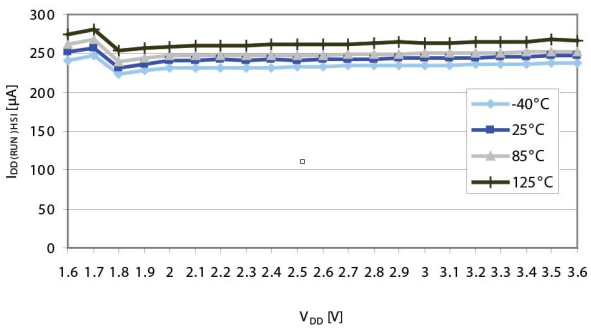
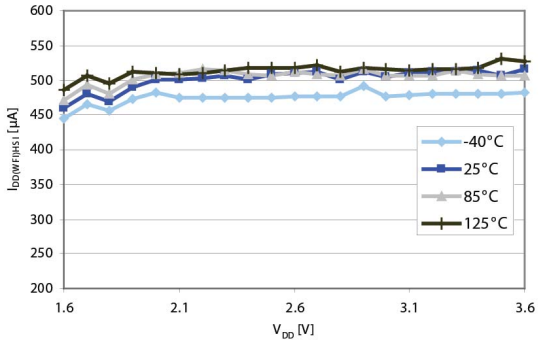



**Figure 14. $I_{DD(WAIT)}$ vs. $V_{DD}$, $f_{CPU}$ = 16 MHz**



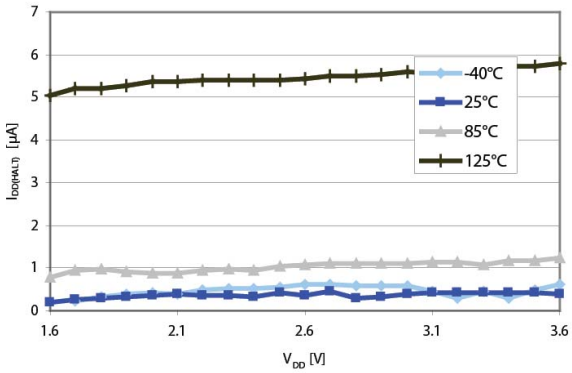

1. Typical current consumption measured with code executed from Flash.

**Table 20. Total current consumption and timing in Halt and Active-halt mode at $V_{DD}$ = 1.65 V to 3.6 V (1)(2)**

| Symbol | Parameter | Conditions | | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(AH)}$ | Supply current in Active-halt mode | LSI RC osc. (at 37 kHz) | $T_A$ = -40 °C to 25 °C | 0.8 | 2 | µA |
| | | | $T_A$ = 55 °C | 1 | 2.5 | µA |
| | | | $T_A$ = 85 °C | 1.4 | 3.2 | µA |
| | | | $T_A$ = 105 °C | 2.9 | 7.5 | µA |
| | | | $T_A$ = 125 °C | 5.8 | 13 | µA |
| $I_{DD(WUFAH)}$ | Supply current during wakeup time from Active-halt mode | - | - | 2 | - | mA |
| $t_{WU(AH)}$(3) | Wakeup time from Active-halt mode to Run mode | $f_{CPU}$= 16 MHz | | 4 | 6.5 | µs |
| $I_{DD(Halt)}$ | Supply current in Halt mode | $T_A$ = -40 °C to 25 °C | | 0.35 | 1.2(4) | µA |
| | | $T_A$ = 55 °C | | 0.6 | 1.8 | µA |
| | | $T_A$ = 85 °C | | 1 | 2.5(4) | µA |
| | | $T_A$ = 105 °C | | 2.5 | 6.5 | µA |
| | | $T_A$ = 125 °C | | 5.4 | 12(4) | µA |
| $I_{DD(WUFH)}$ | Supply current during wakeup time from Halt mode | | | 2 | - | mA |
| $t_{WU(Halt)}$(3) | Wakeup time from Halt mode to Run mode | $f_{CPU}$ = 16 MHz | | 4 | 6.5 | µs |

1. $T_A$ = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Guaranteed by characterization results.
3. Measured from interrupt event to interrupt vector fetch.
   To get $t_{WU}$ for another CPU frequency use $t_{WU}$(FREQ) = $t_{WU}$(16 MHz) + 1.5 ($T_{FREQ}$-$T_{16\ MHz}$).
   The first word of interrupt routine is fetched 5 CPU cycles after $t_{WU}$.
4. Tested in production.

**Figure 15. Typ. $I_{DD(Halt)}$ vs. $V_{DD}$, $f_{CPU}$ = 2 MHz and 16 MHz**




1. Typical current consumption measured with code executed from Flash.

### Current consumption of on-chip peripherals

Measurement made for $f_{MASTER}$ = from 2 MHz to 16 MHz

**Table 21. Peripheral current consumption**

| Symbol | Parameter | Typ. $V_{DD}$ = 3.0 V | Unit |
|---|---|---|---|
| $I_{DD(TIM2)}$ | TIM2 supply current (1) | 9 | µA/MHz |
| $I_{DD(TIM3)}$ | TIM3 supply current (1) | 9 | |
| $I_{DD(TIM4)}$ | TIM4 timer supply current (1) | 4 | |
| $I_{DD(USART)}$ | USART supply current (2) | 7 | |
| $I_{DD(SPI)}$ | SPI supply current (2) | 4 | |
| $I_{DD(I^2C1)}$ | I2C supply current (2) | 4 | |
| $I_{DD(COMP)}$ | Comparator supply current (2) | 20 | µA |

1. Data based on a differential $I_{DD}$ measurement between all peripherals off and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pin toggling. Not tested in production.
2. Data based on a differential $I_{DD}$ measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pin toggling. Not tested in production.

## 9.3.4 Clock and timing characteristics

### Internal clock sources

Subject to general operating conditions for $V_{DD}$ and $T_A$.

### High speed internal RC oscillator (HSI)

**Table 22. HSI oscillator characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | $V_{DD}$ = 3.0 V | - | 16 | - | MHz |
| $ACC_{HSI}$ | Accuracy of HSI oscillator (factory calibrated) | $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | -1 | - | 1 | % |
| | | $V_{DD}$ = 3.0 V, -10 °C ≤$T_A$ ≤ 85 °C | -2.5(2) | - | 2(2) | % |
| | | $V_{DD}$ = 3.0 V, -10 °C ≤$T_A$ ≤ 125 °C | -4.5(2) | - | 2(2) | % |
| | | $V_{DD}$ = 3.0 V, 0 °C ≤$T_A$ ≤ 55 °C | -1.5(2) | - | 1.5(2) | % |
| | | $V_{DD}$ = 3.0 V, -10 °C ≤$T_A$ ≤ 70 °C | -2(2) | - | 2(2) | % |
| | | 1.65 V ≤ $V_{DD}$ ≤ 3.6 V, -40 °C ≤ $T_A$ ≤125 °C | -4.5(2) | - | 3(2) | % |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | - | - | 70 | 100(2) | µA |

1. $V_{DD}$ = 3.0 V, $T_A$ = -40 to 125 °C unless otherwise specified.
2. Guaranteed by characterization results.

**Figure 16. Typical HSI frequency vs. $V_{DD}$**

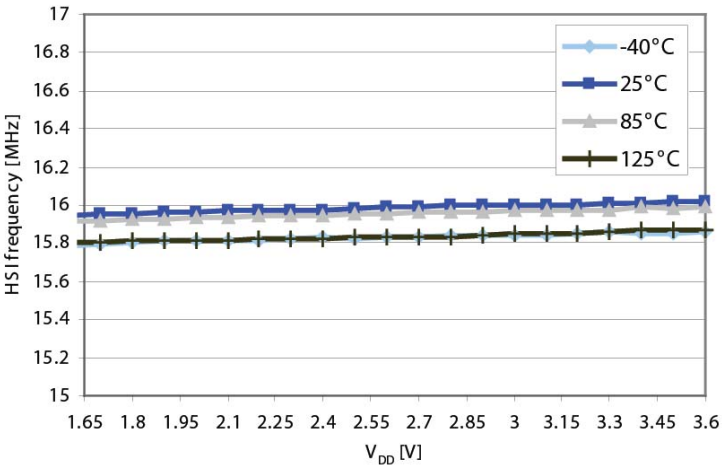



**Figure 17. Typical HSI accuracy vs. temperature, $V_{DD}$ = 3 V**

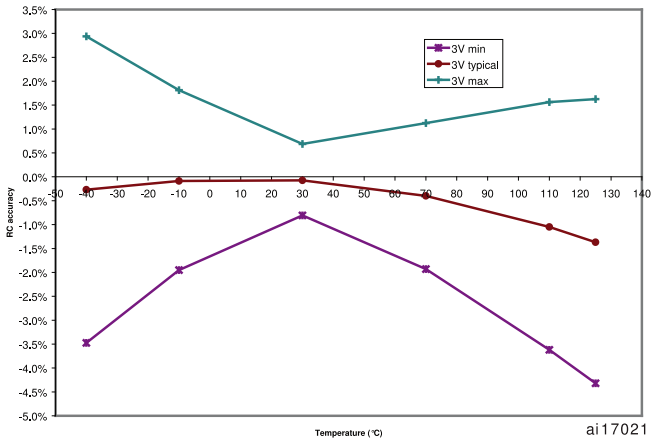
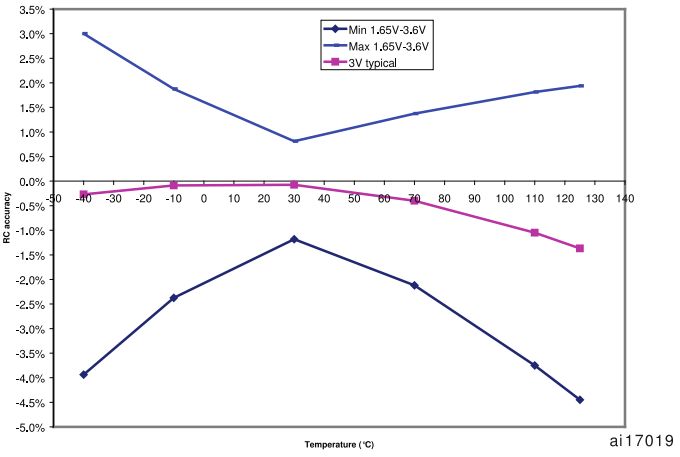



**Figure 18. Typical HSI accuracy vs. temperature, $V_{DD}$ = 1.65 V to 3.6 V**



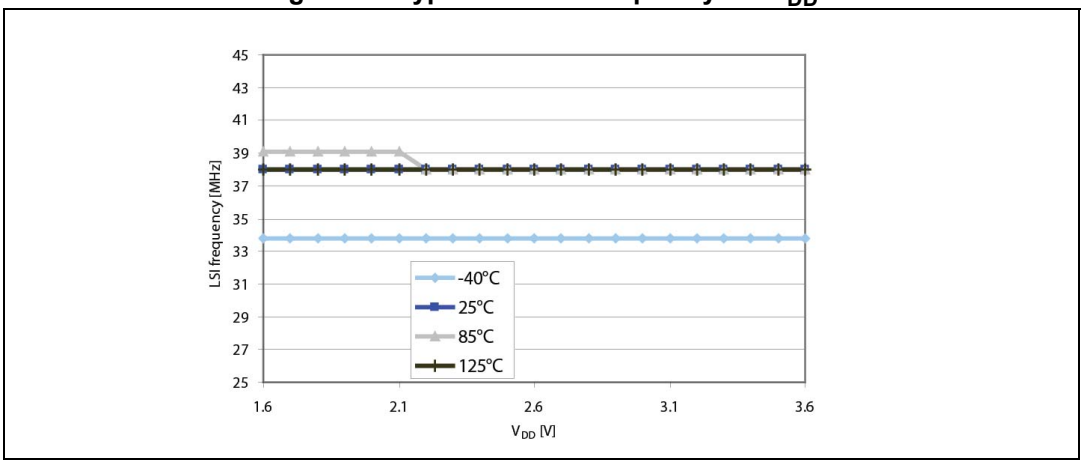
### Low speed internal RC oscillator (LSI)

**Table 23. LSI oscillator characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | - | 26 | 38 | 56 | kHz |
| $f_{drift(LSI)}$ | LSI oscillator frequency drift(2) | 0 °C ≤$T_A$ ≤85 °C | -12 | - | 11 | % |

1. $V_{DD}$ = 1.65 V to 3.6 V, $T_A$ = -40 to 125 °C unless otherwise specified.
2. For each individual part, this value is the frequency drift from the initial measured frequency.

**Figure 19. Typical LSI RC frequency vs. $V_{DD}$**




## 9.3.5 Memory characteristics

$T_A$ = -40 to 125 °C unless otherwise specified.

**Table 24. RAM and hardware registers**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{RM}$ | Data retention mode (1) | Halt mode (or Reset) | 1.4 | - | - | V |

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization results.

### Flash memory

**Table 25. Flash program memory**

| Symbol | Parameter | Conditions | Min | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage (all modes, read/write/erase) | $f_{MASTER}$ = 16 MHz | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming time for 1- or 64-byte (block) erase/write cycles (on programmed byte) | - | - | 6 | - | ms |
| | Programming time for 1- to 64-byte (block) write cycles (on erased byte) | - | - | 3 | - | ms |

**Table 25. Flash program memory (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|
| $I_{prog}$ | Programming/ erasing consumption | $T_A$=+25 °C, $V_{DD}$ = 3.0 V | - | 0.7 | - | mA |
| | | $T_A$=+25 °C, $V_{DD}$ = 1.8 V | - | | - | |
| $t_{RET}$ | Data retention (program memory) after 10k erase/write cycles at $T_A$ = +85 °C | $T_{RET}$ = 55 °C | 20(1) | - | - | years |
| | Data retention (data memory) after 10k erase/write cycles at $T_A$ = +85 °C | $T_{RET}$ = 55 °C | 20(1) | - | - | |
| | Data retention (data memory) after 300k erase/write cycles at $T_A$ = +125 °C | $T_{RET}$ = 85 °C | 1(1) | - | - | |
| $N_{RW}$ | Erase/write cycles (program memory) | See notes (1)(2) | 10(1) | - | - | kcycles |
| | Erase/write cycles (data memory) | See notes (1)(3) | 300(1)(4) | - | - | |

1. Guaranteed by characterization results.
2. Retention guaranteed after cycling is 10 years at 55 °C.
3. Retention guaranteed after cycling is 1 year at 55 °C.
4. Data based on characterization performed on the whole data memory (2 Kbytes).

## 9.3.6 I/O port pin characteristics

### General characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 26. I/O static characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage(2) | Standard I/Os | $V_{SS}$-0.3 | - | 0.3 x $V_{DD}$ | V |
| | | True open drain I/Os | $V_{SS}$-0.3 | - | 0.3 x $V_{DD}$ | |
| $V_{IH}$ | Input high level voltage (2) | Standard I/Os | 0.70 x $V_{DD}$ | - | $V_{DD}$+0.3 | V |
| | | True open drain I/Os $V_{DD}$ < 2 V | 0.70 x $V_{DD}$ | - | 5.2 | |
| | | True open drain I/Os $V_{DD}$ ≥ 2 V | | | 5.5 | |
| $V_{hys}$ | Schmitt trigger voltage hysteresis (3) | Standard I/Os | - | 200 | - | mV |
| | | True open drain I/Os | - | 250 | - | |

**Table 26. I/O static characteristics (1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{lkg}$ | Input leakage current (4) | $V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os | - | - | 50 (5) | nA |
| | | $V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os | - | - | 200(5) | |
| | | $V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability | - | - | 200(5) | |
| $R_{PU}$ | Weak pull-up equivalent resistor(6) | $V_{IN} = V_{SS}$ | 30 | 45 | 60 | kΩ |
| $C_{IO}$(7) | I/O pin capacitance | - | - | 5 | - | pF |

1. $V_{DD}$ = 3.0 V, $T_A$ = -40 to 85 °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. $R_{PU}$ pull-up equivalent resistor based on a resistive transistor (corresponding $I_{PU}$ current characteristics described in *Figure 22*).
7. Guaranteed by design.

**Figure 20. Typical $V_{IL}$ and $V_{IH}$ vs. $V_{DD}$ (High sink I/Os)**

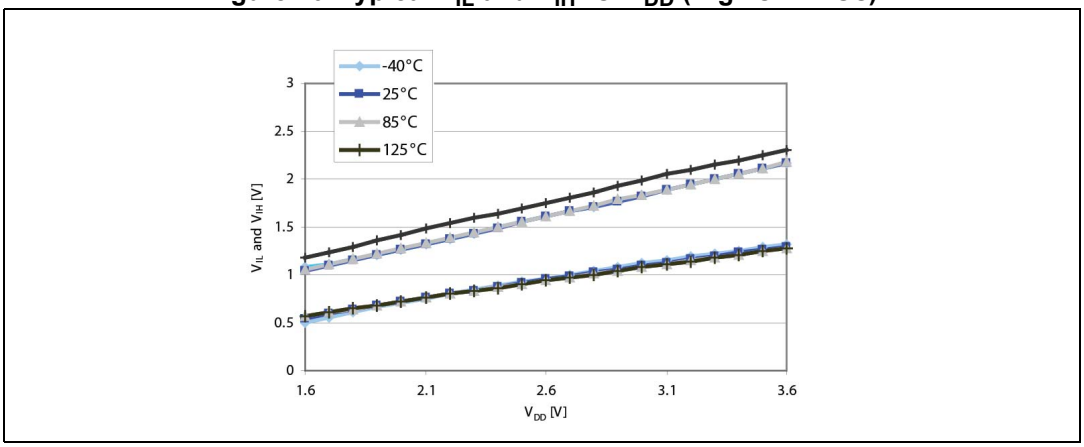


Figure 21. Typical $V_{IL}$ and $V_{IH}$ vs. $V_{DD}$ (true open drain I/Os)

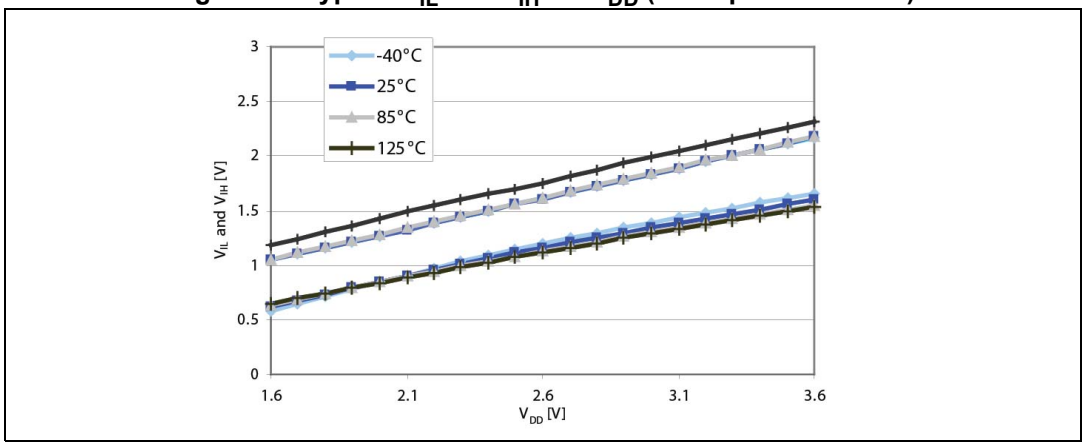



Figure 22. Typical pull-up resistance $R_{PU}$ vs. $V_{DD}$ with $V_{IN}=V_{SS}$

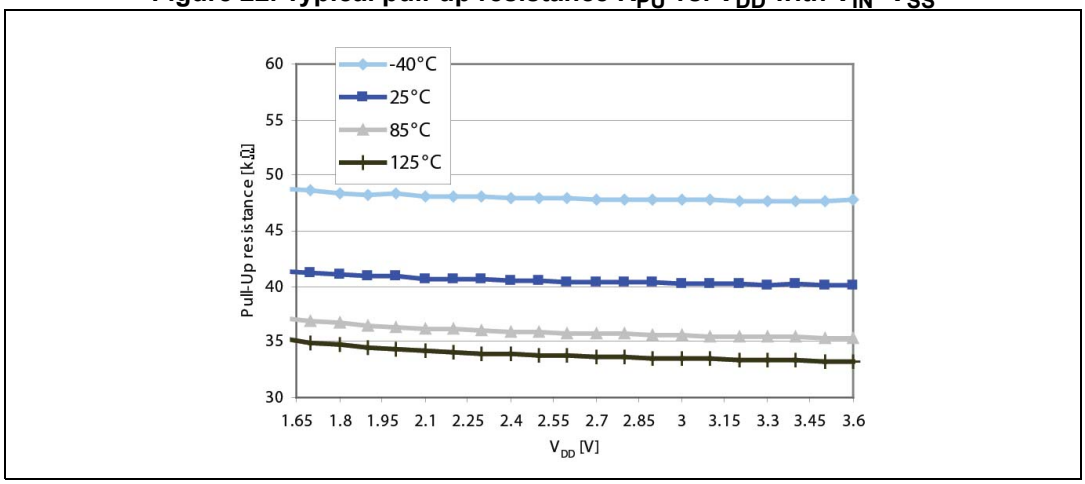
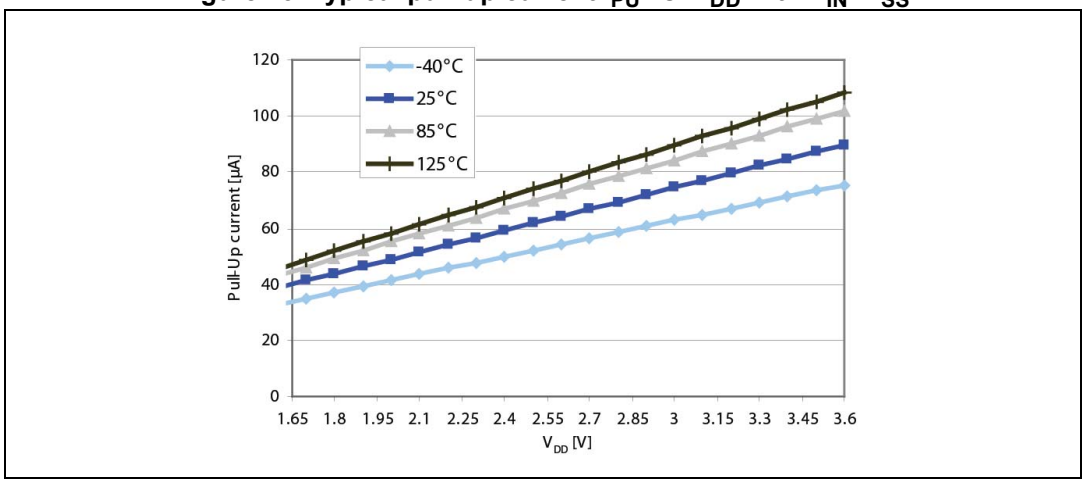



Figure 23. Typical pull-up current $I_{PU}$ vs. $V_{DD}$ with $V_{IN}=V_{SS}$



### Output driving current

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 27. Output driving current (High sink ports)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Standard | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +2 mA, $V_{DD}$ = 3.0 V | - | 0.45 | V |
| | | | $I_{IO}$ = +2 mA, $V_{DD}$ = 1.8 V | - | 0.45 | V |
| | | | $I_{IO}$ = +10 mA, $V_{DD}$ = 3.0 V | - | 1.2 | V |
| | $V_{OH}$ (2) | Output high level voltage for an I/O pin | $I_{IO}$ = -2 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.45 | - | V |
| | | | $I_{IO}$ = -1 mA, $V_{DD}$ = 1.8 V | $V_{DD}$-0.45 | - | V |
| | | | $I_{IO}$ = -10 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-1.2 | - | V |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 14* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced must always respect the absolute maximum rating specified in *Table 14* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

**Table 28. Output driving current (true open drain ports)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Open drain | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +3 mA, $V_{DD}$ = 3.0 V | - | 0.45 | V |
| | | | $I_{IO}$ = +1 mA, $V_{DD}$ = 1.8 V | - | 0.45 | V |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 14* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

**Table 29. Output driving current (PA0 with high sink LED driver capability)**

| I/O Type | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| IR | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA, $V_{DD}$ = 2.0 V | - | 0.9 | V |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 14* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

**Figure 24. Typ. $V_{OL}$ at $V_{DD}$ = 3.0 V (High sink ports)**

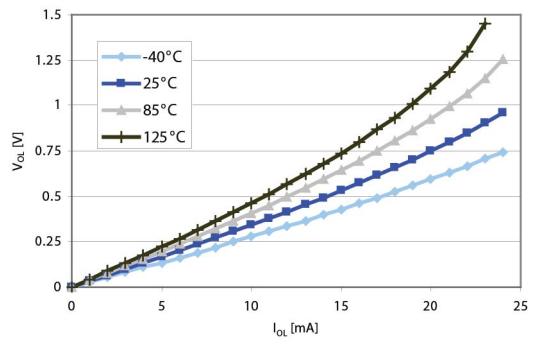



**Figure 25. Typ. $V_{OL}$ at $V_{DD}$ = 1.8 V (High sink ports)**

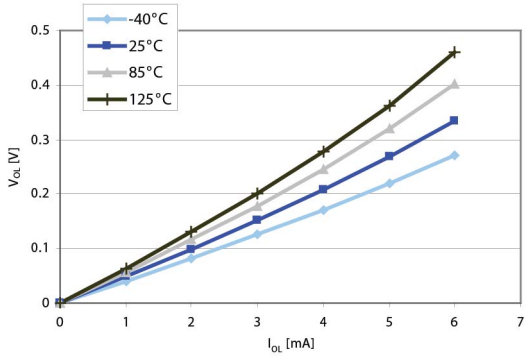



**Figure 26. Typ. $V_{OL}$ at $V_{DD}$ = 3.0 V (true open drain ports)**

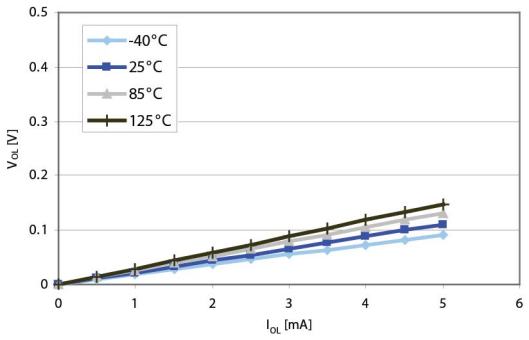



**Figure 27. Typ. $V_{OL}$ at $V_{DD}$ = 1.8 V (true open drain ports)**

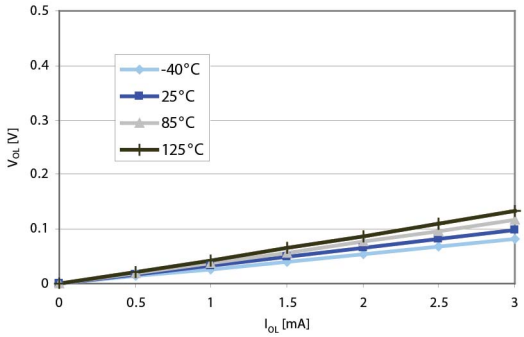



**Figure 28. Typ. $V_{DD}$ - $V_{OH}$ at $V_{DD}$ = 3.0 V (High sink ports)**

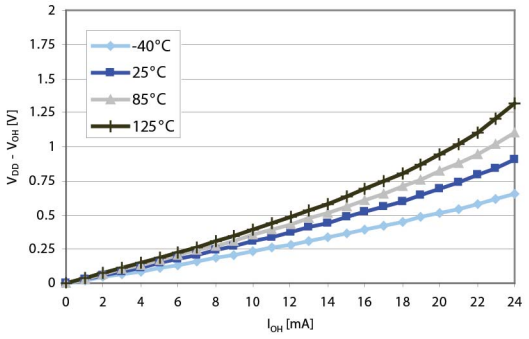
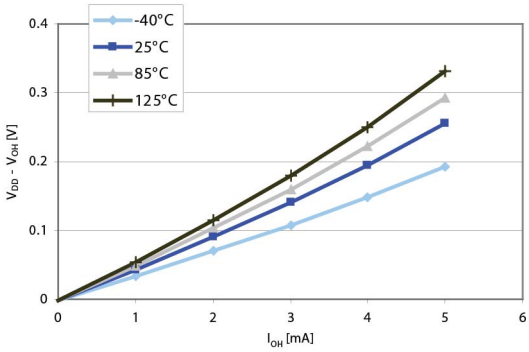



**Figure 29. Typ. $V_{DD}$ - $V_{OH}$ at $V_{DD}$ = 1.8 V (High sink ports)**



### NRST pin

The NRST pin input driver is CMOS. A permanent pull-up is present. $R_{PU(NRST)}$ has the same value as $R_{PU}$ (see *Table 26 on page 48*).

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 30. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ (1) | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low level voltage (1) | - | $V_{SS}$ | - | 0.8 | V |
| $V_{IH(NRST)}$ | NRST input high level voltage (1) | - | 1.4 | - | $V_{DD}$ | |
| $V_{OL(NRST)}$ | NRST output low level voltage | $I_{OL}$ = 2 mA | - | - | $V_{DD}$-0.8 | |
| $R_{PU(NRST)}$ | NRST pull-up equivalent resistor (2) | - | 30 | 45 | 60 | kΩ |
| $V_{F(NRST)}$ | NRST input filtered pulse (3) | - | - | - | 50 | ns |
| $t_{OP(NRST)}$ | NRST output pulse width | - | 20 | - | - | ns |
| $V_{NF(NRST)}$ | NRST input not filtered pulse (3) | - | 300 | - | - | ns |

1. Guaranteed by characterization results.
2. The $R_{PU}$ pull-up equivalent resistor is based on a resistive transistor (*Figure 30*). Corresponding $I_{PU}$ current characteristics are described in *Figure 31*.
3. Guaranteed by design.

**Figure 30. Typical NRST pull-up resistance $R_{PU}$ vs. $V_{DD}$**

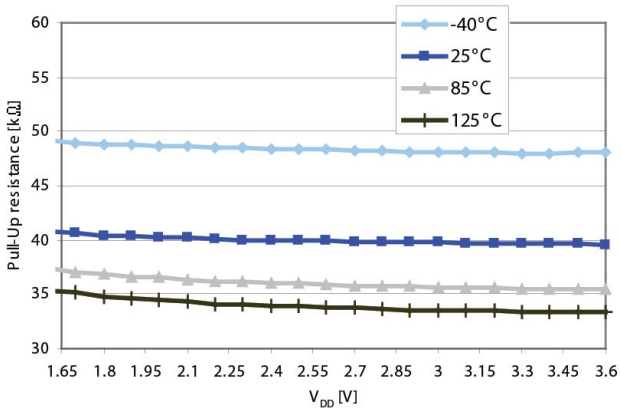
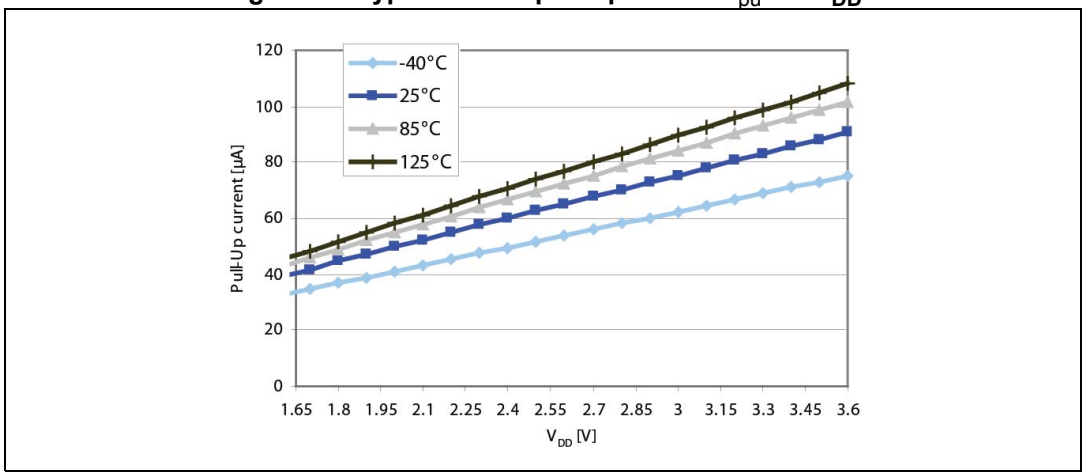
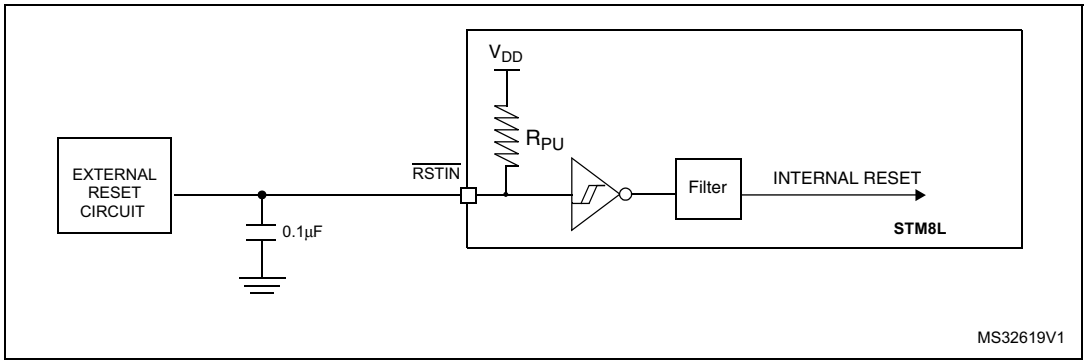


**Figure 31. Typical NRST pull-up current $I_{pu}$ vs. $V_{DD}$**




The reset network shown in *Figure 32* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the $V_{IL}$ max. level specified in *Table 30*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

**Figure 32. Recommended NRST pin configuration**




1. Correct device reset during power on sequence is guaranteed when $t_{VDD[max]}$ is respected.
2. External reset circuit is recommended to ensure correct device reset during power down, when $V_{PDR} < V_{DD} < V_{DD[min]}$.

## 9.3.7 Communication interfaces

### Serial peripheral interface (SPI)

Unless otherwise specified, the parameters given in *Table 31* are derived from tests performed under ambient temperature, $f_{MASTER}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 31. SPI characteristics**

| Symbol | Parameter | Conditions[1] | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 8 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 30 | ns |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | 4 x $T_{MASTER}$ | - | |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | 80 | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode,<br>$f_{MASTER}$ = 8 MHz, $f_{SCK}$= 4 MHz | 105 | 145 | |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup time | Master mode | 30 | - | |
| | | Slave mode | 3 | - | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold time | Master mode | 15 | - | |
| | | Slave mode | 0 | - | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode | - | 3x $T_{MASTER}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 30 | - | |
| $t_{v(SO)}$(2) | Data output valid time | Slave mode (after enable edge) | - | 60 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode<br>(after enable edge) | - | 20 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$(2) | | Master mode<br>(after enable edge) | 1 | - | |

1. Parameters are given by selecting 10-MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

**Figure 33. SPI timing diagram - slave mode and CPHA = 0**

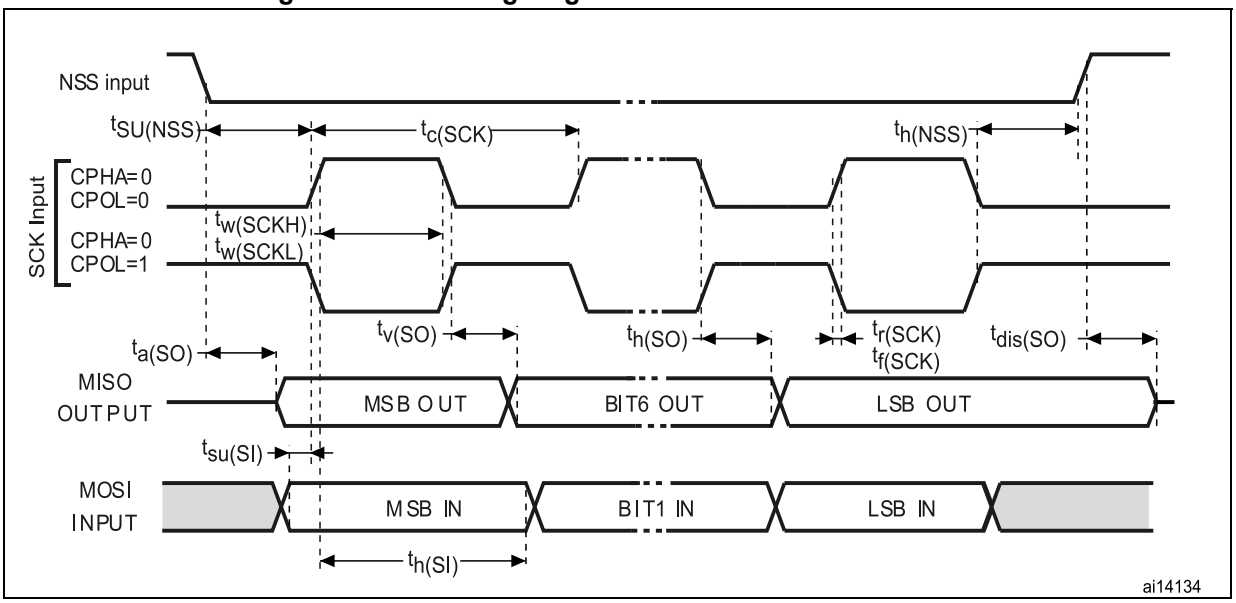
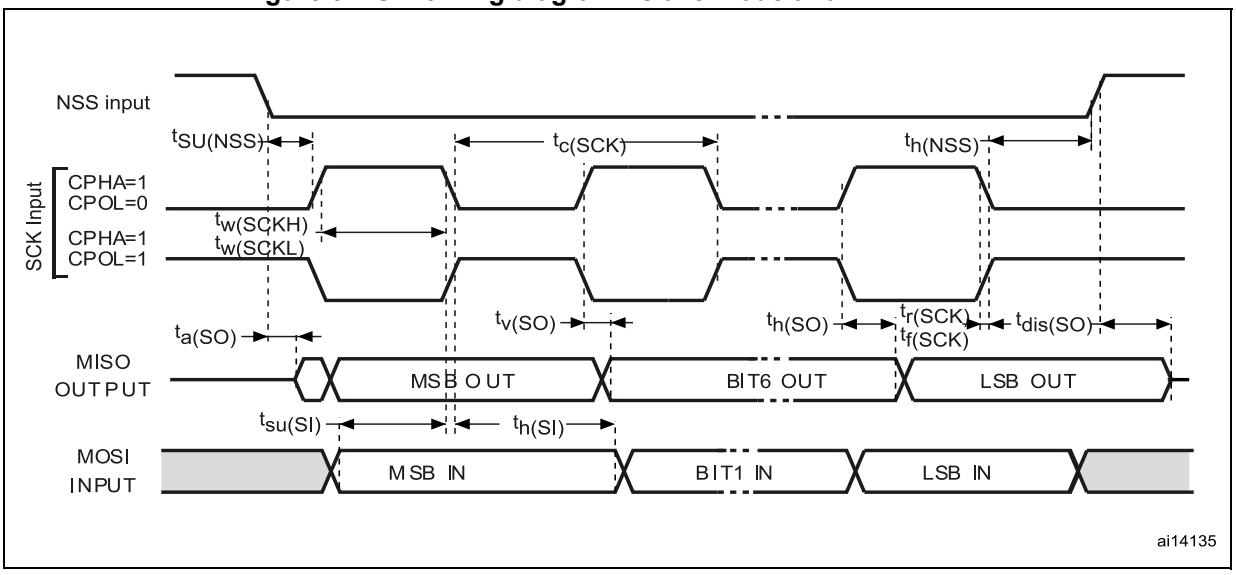
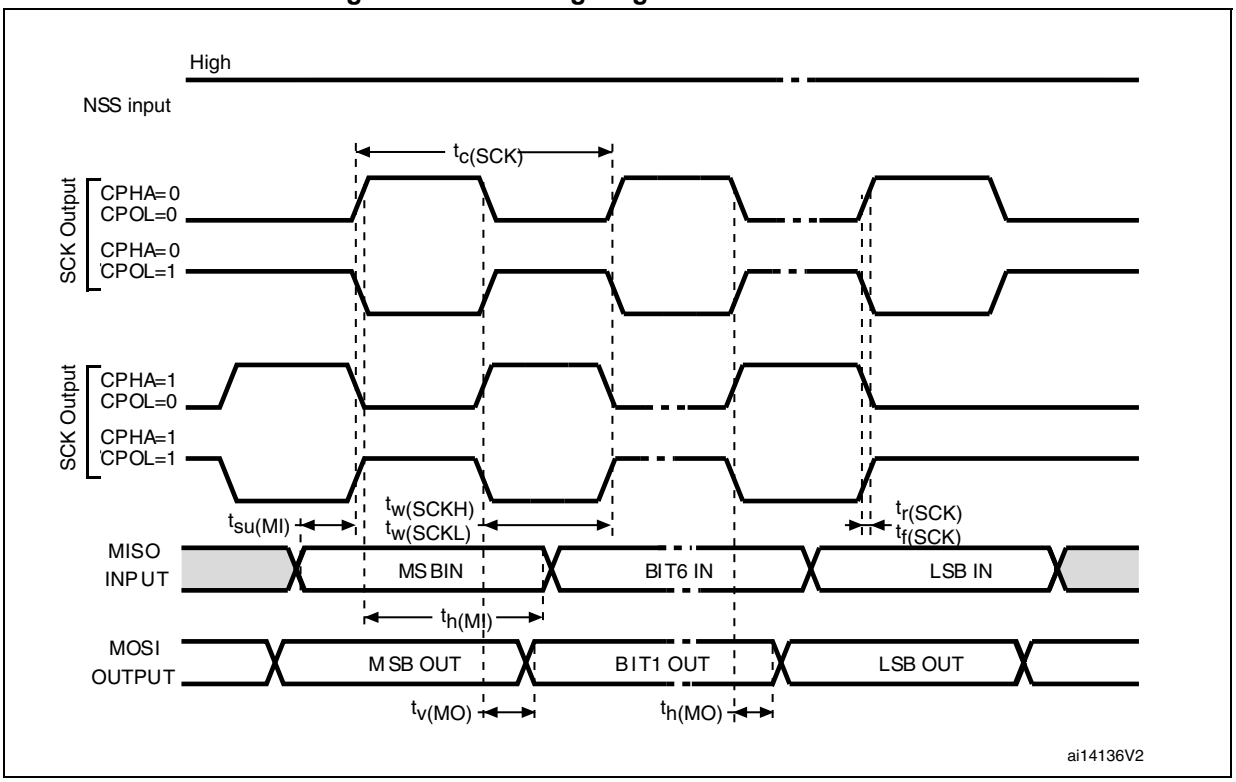



**Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 35. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

### Inter IC control interface (I2C)

Subject to general operating conditions for $V_{DD}$, $f_{MASTER}$, and $T_A$ unless otherwise specified.

The STM8L $I^2C$ interface meets the requirements of the Standard $I^2C$ communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

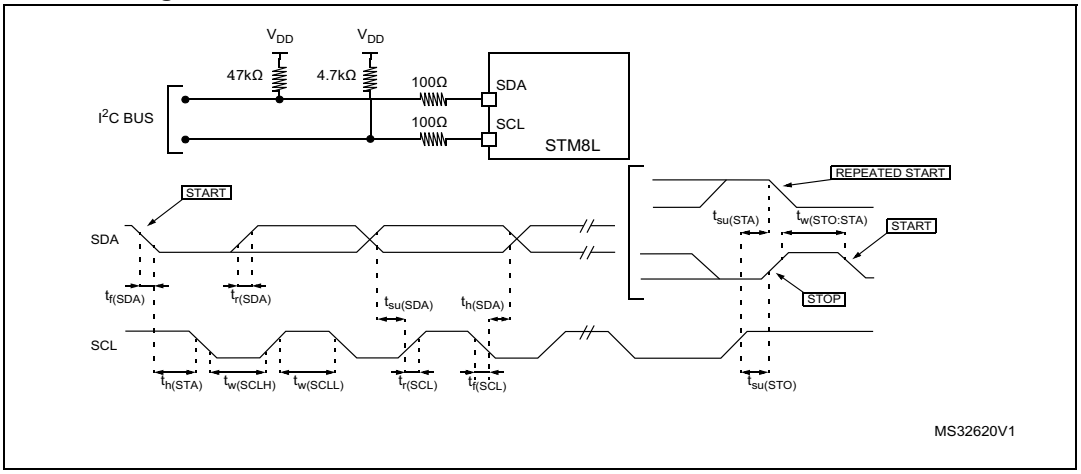
**Table 32. I2C characteristics**

| Symbol | Parameter | Standard mode I2C | | Fast mode I2C(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min(2) | Max (2) | Min (2) | Max (2) | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 (3) | - | 0 (4) | 900 (3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | START condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | STOP to START condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. $f_{SCK}$ must be at least 8 MHz to achieve max fast $I^2C$ speed (400 kHz).
2. Data based on standard $I^2C$ protocol requirement, not tested in production.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL).

*Note: For speeds around 200 kHz, achieved speed can have ±5% tolerance*
*For other speed ranges, achieved speed can have ±2% tolerance*
*The above variations depend on the accuracy of the external components used.*

**Figure 36. Typical application with I2C bus and timing diagram 1)**




1. Measurement points are done at CMOS levels: 0.3 x $V_{DD}$ and 0.7 x $V_{DD}$.

## 9.3.8 Comparator characteristics

**Table 33. Comparator characteristics**

| Symbol | Parameter | Conditions | Min (1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{IN(COMP_REF)}$ | Comparator external reference | - | -0.1 | - | $V_{DD}$-1.25 | V |
| $V_{IN}$ | Comparator input voltage range | - | -0.25 | - | $V_{DD}$+0.25 | V |
| $V_{offset}$(2) | Comparator offset error | - | - | - | ±20 | mV |
| $t_{START}$ | Startup time (after BIAS_EN) | - | - | - | 3(1) | µs |
| $I_{DD(COMP)}$ | Analog comparator consumption | - | - | - | 25(1) | µA |
| | Analog comparator consumption during power-down | - | - | - | 60(1) | nA |
| $t_{propag}$(2) | Comparator propagation delay | 100-mV input step with 5-mV overdrive, input rise time = 1 ns | - | - | 2(1) | µs |

1. Guaranteed by design.
2. The comparator accuracy depends on the environment. In particular, the following cases may reduce the accuracy of the comparator and must be avoided:
   - Negative injection current on the I/Os close to the comparator inputs
   - Switching on I/Os close to the comparator inputs
   - Negative injection current on not used comparator input.
   - Switching with a high dV/dt on not used comparator input.

   These phenomena are even more critical when a big external serial resistor is added on the inputs.

## 9.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. Refer to application note *Software techniques for improving microcontrollers EMC performance* (AN1015).

**Table 34. EMS data**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | LQFP32, $V_{DD}$ = 3.3 V | 3B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | LQFP32, $V_{DD}$ = 3.3 V, $f_{HSI}$ | 3B |
| | | LQFP32, $V_{DD}$ = 3.3 V, $f_{HSI}/2$ | 4A |

### Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

**Table 35. EMI data (1)**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. | Unit |
|---|---|---|---|---|---|
| | | | | 16 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = +25 °C, LQFP32 conforming to IEC61967-2 | 0.1 MHz to 30 MHz | -3 | dBµV |
| | | | 30 MHz to 130 MHz | -6 | |
| | | | 130 MHz to 1 GHz | -5 | |
| | | | SAE EMI Level | 1 | - |

1. Not tested in production.

### Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin).

This test conforms to the JESD22-A114A/A115A standard.

**Table 36. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Maximum value (1) | Unit |
|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | | 500 | |

1. Guaranteed by characterization results.

### Static latch-up

- **LU**: 2 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

**Table 37. Electrical sensitivities**

| Symbol | Parameter | Class |
|---|---|---|
| LU | Static latch-up class | II |

## 9.4 Thermal characteristics

The maximum chip junction temperature ($T_{Jmax}$) must never exceed the values given in *Table 16: General operating conditions on page 40*.

The maximum chip-junction temperature, $T_{Jmax}$, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- $T_{Amax}$ is the maximum ambient temperature in °C
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance in °C/W
- $P_{Dmax}$ is the sum of $P_{INTmax}$ and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- $P_{INTmax}$ is the product of $I_{DD}$ and $V_{DD}$, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual $V_{OL}/I_{OL}$ and $V_{OH}/I_{OH}$ of the I/Os at low and high level in the application.

**Table 38. Thermal characteristics(1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm | 60 | °C/W |
| | Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm | 25 | °C/W |
| | Thermal resistance junction-ambient UFQFPN 28 - 4 x 4 mm | 80 | °C/W |
| | Thermal resistance junction-ambient UFQFPN 20 - 3 x 3 mm - 0.6 mm | 102 | °C/W |
| | Thermal resistance junction-ambient TSSOP 20 | 110 | °C/W |

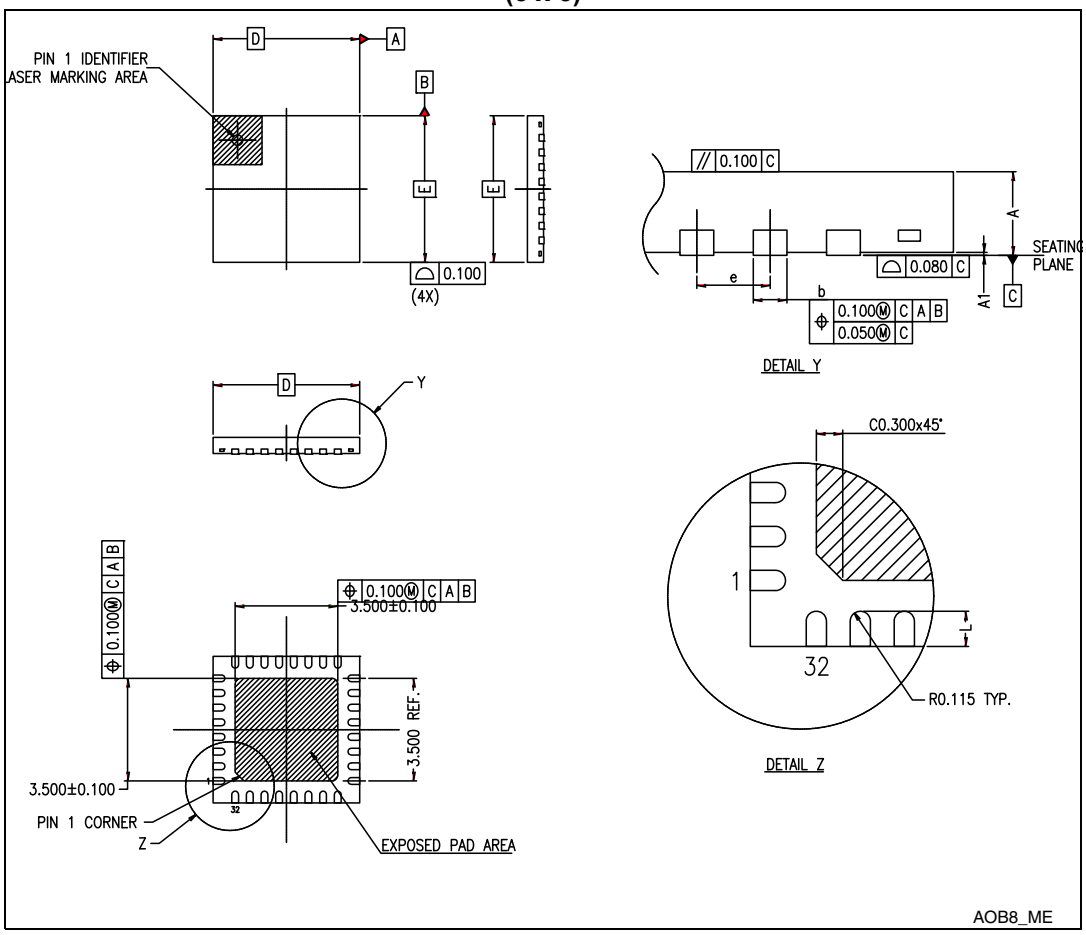
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

# 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 10.1 UFQFPN32 package information

**Figure 37. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5)**



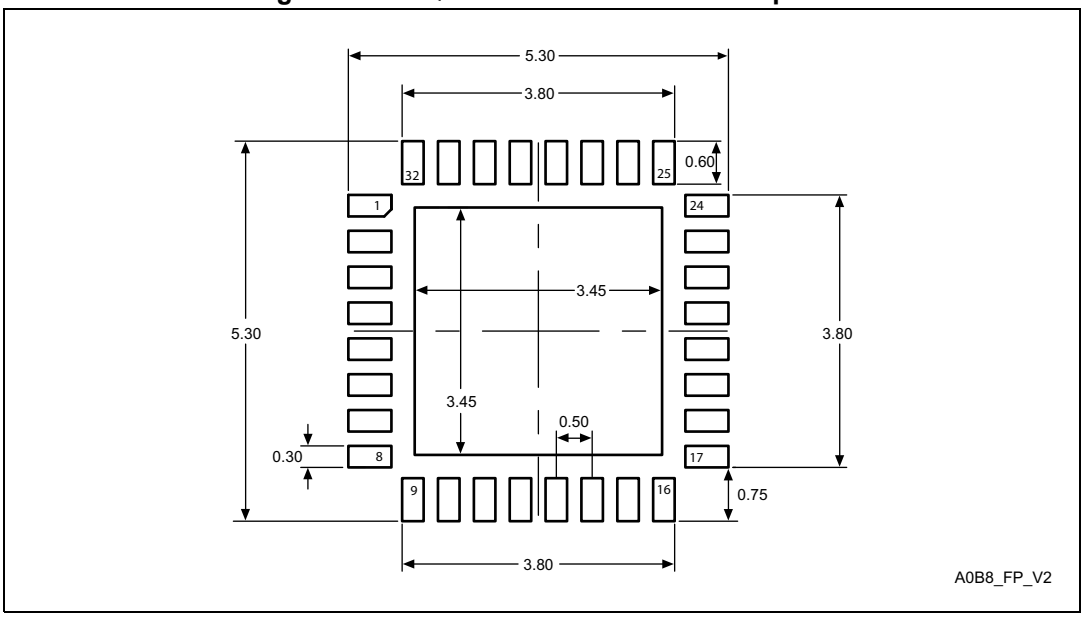

1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

**Table 39. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data**

| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.0500 | 0 | 0.0008 | 0.0020 |
| A3 | - | 0.152 | - | - | 0.0060 | - |
| b | 0.180 | 0.230 | 0.280 | 0.0071 | 0.0091 | 0.0110 |
| D | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| D2 | - | 3.500 | - | - | 0.1378 | - |
| E | 4.900 | 5.000 | 5.100 | 0.1929 | 0.1969 | 0.2008 |
| E2 | 3.400 | 3.500 | 3.600 | 0.1339 | 0.1378 | 0.1417 |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | 0.080 | | | 0.0031 | | |
| - | Number of pins | | | | | |
| N | 32 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 38. UFQFPN32 recommended footprint**



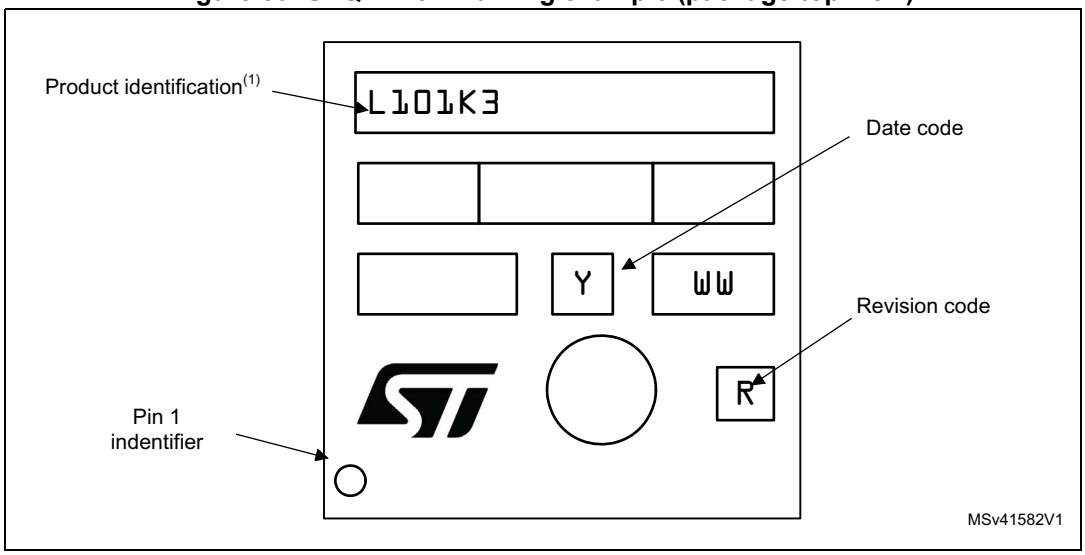

1. Dimensions are in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

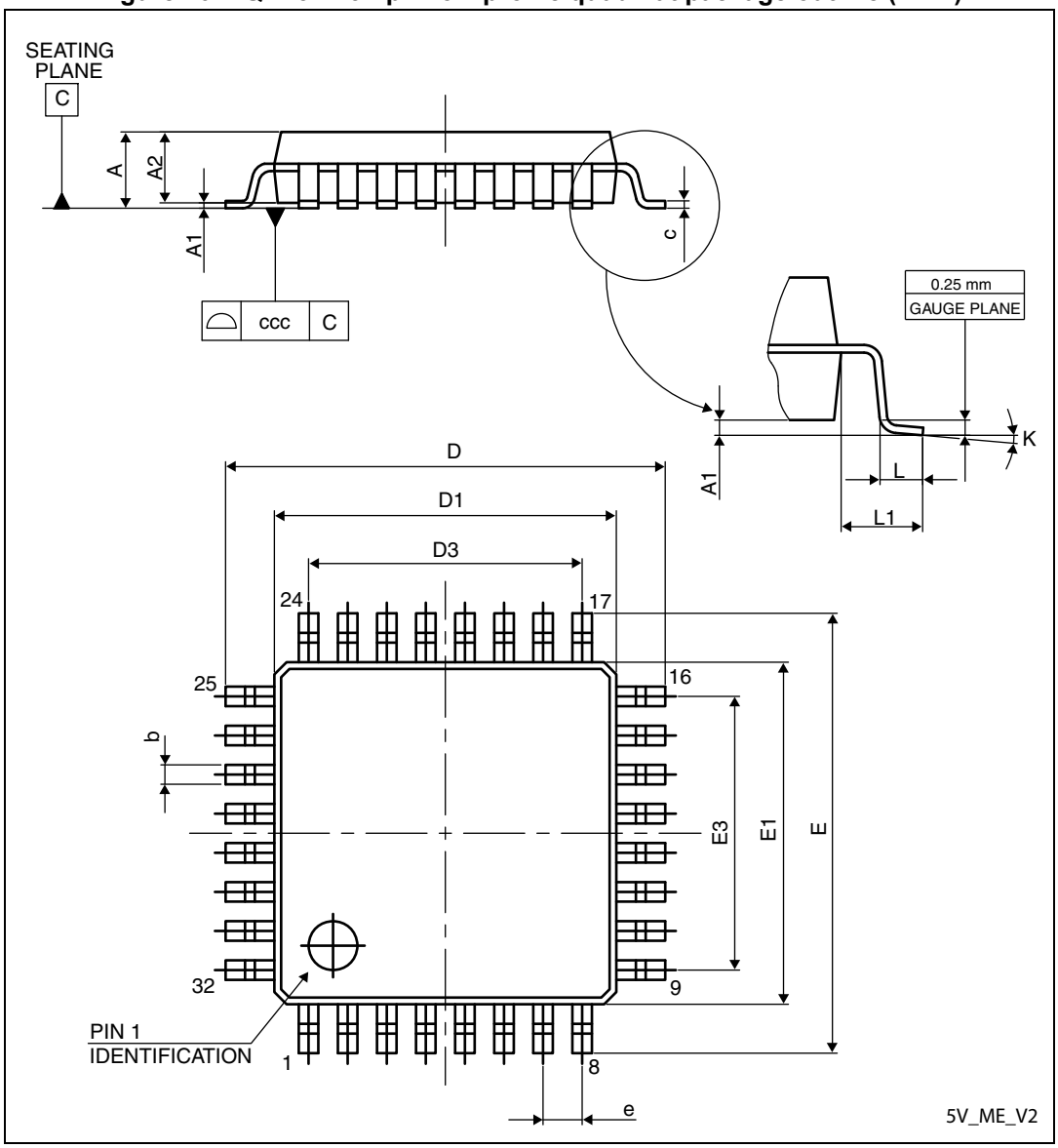
**Figure 39. UFQFPN32 marking example (package top view)**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 10.2 LQFP32 package information

**Figure 40. LQFP32 - 32-pin low profile quad flat package outline (7 x 7)**



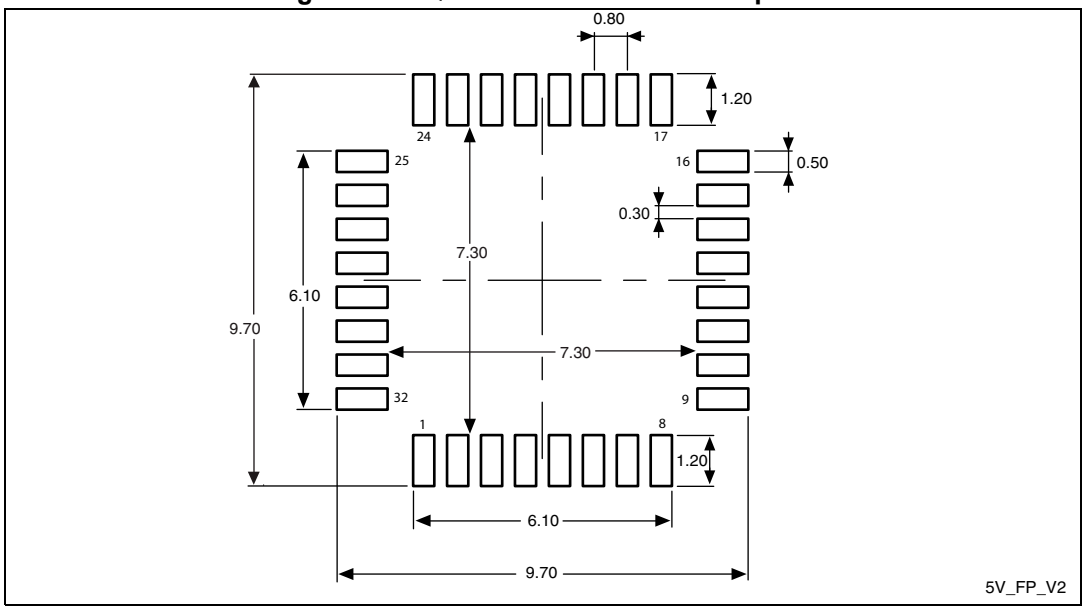

1. Drawing is not to scale.

**Table 40. LQFP32- 32-pin low profile quad flat package (7x7), package mechanical data**

| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.300 | 0.370 | 0.450 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.600 | - | - | 0.2205 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.600 | - | - | 0.2205 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| K | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | 0.100 | - | - | 0.0039 | - |
| - | Number of pins | | | | | |
| N | 32 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 41. LQFP32 recommended footprint**



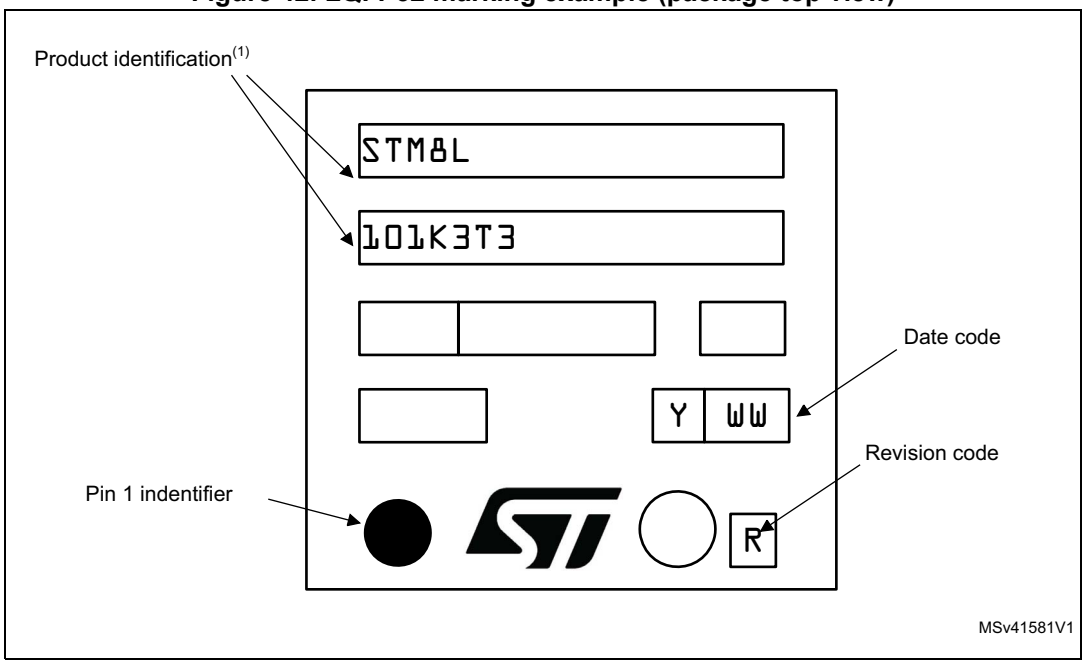

1. Dimensions are expressed in millimeters.

## Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

**Figure 42. LQFP32 marking example (package top view)**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering

samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 10.3 UFQFPN28 package information

**Figure 43. UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package outline (4 x 4 mm)**

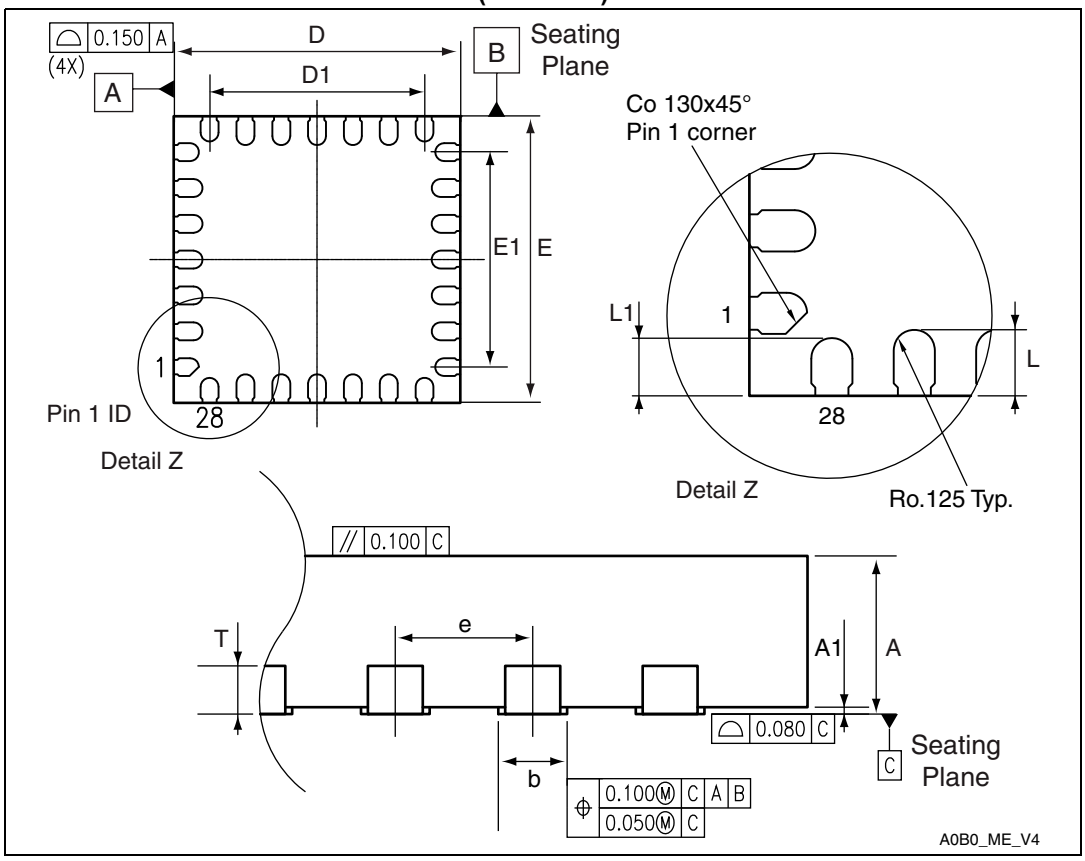
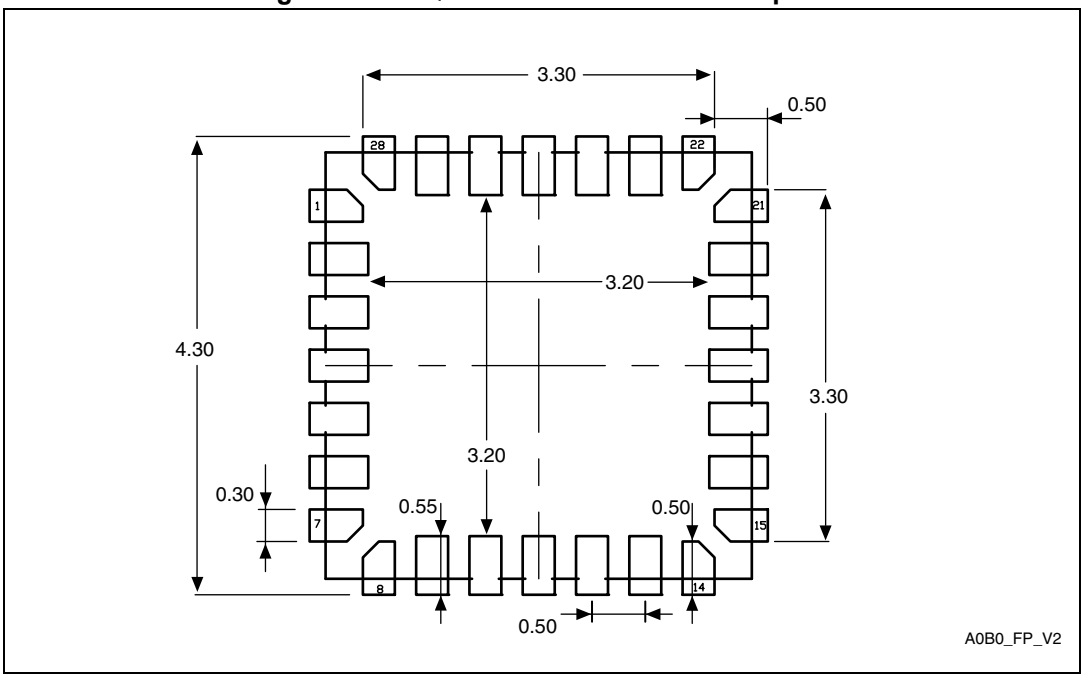


**Table 41. UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package (4 x 4), package mechanical data**

| Dim. | mm | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0 | 0.020 | 0.050 | 0 | 0.0008 | 0.002 |
| A3 | - | 0.152 | - | - | 0.0060 | - |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| D | - | 4.000 | - | - | 0.1575 | - |
| E | - | 4.000 | - | - | 0.1575 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L1 | 0.250 | 0.350 | 0.450 | 0.0098 | 0.0138 | 0.0177 |
| L2 | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| ddd | - | 0.080 | - | - | 0.0031 | - |
| - | Number of pins | | | | | |
| N | 28 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 44. UFQFPN28 recommended footprint**



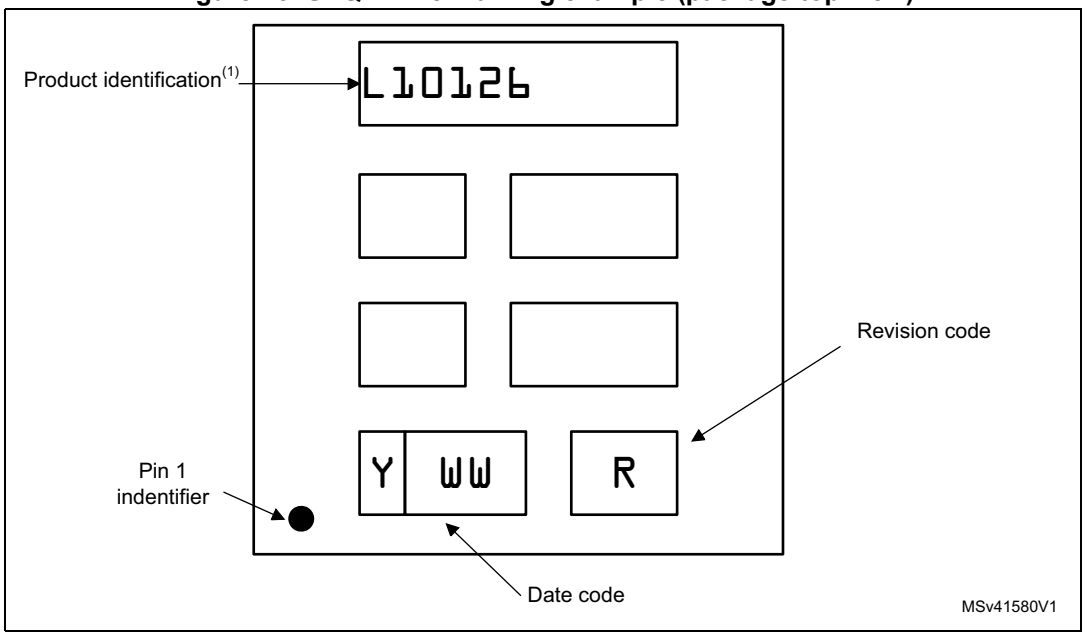

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

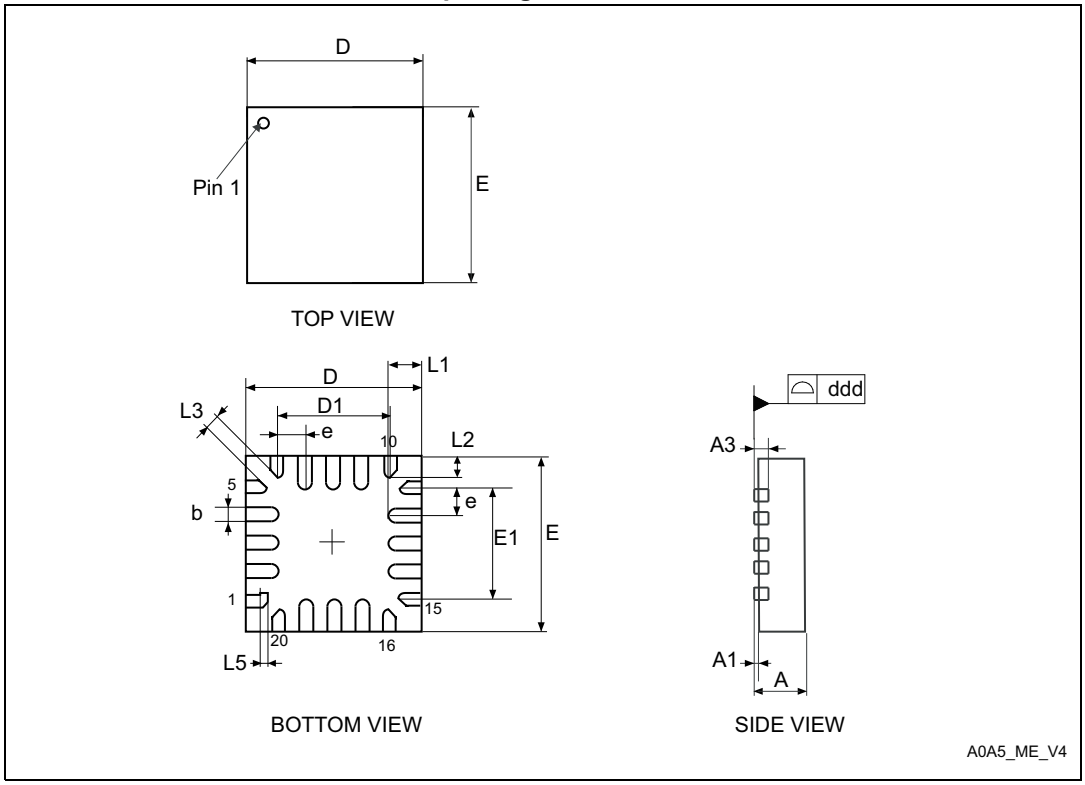
**Figure 45. UFQFPN28 marking example (package top view)**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 10.4 UFQFPN20 package information

**Figure 46. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline**



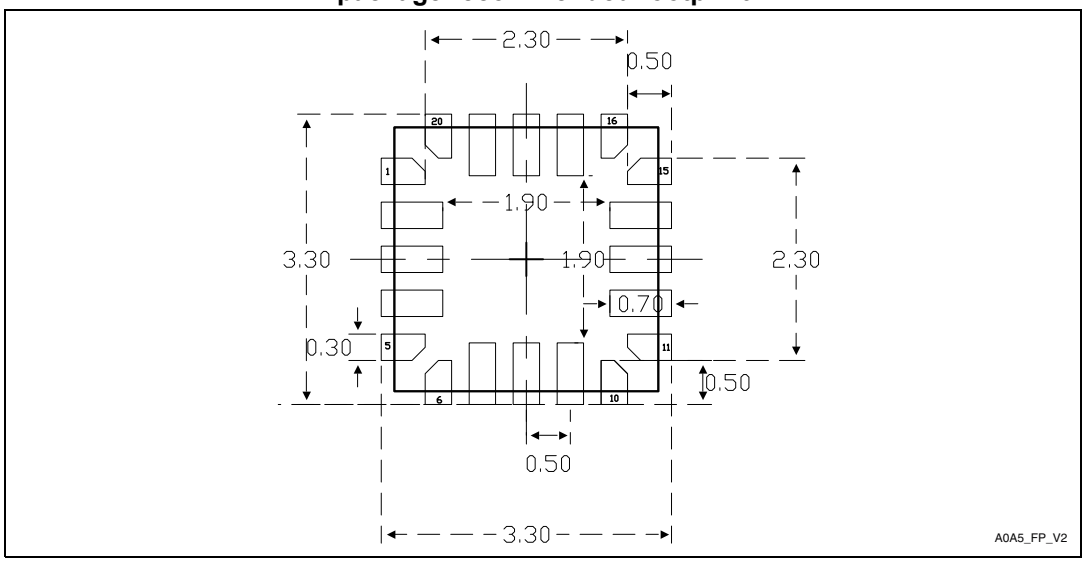

1. Drawing is not to scale.

**Table 42. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.152 | - | - | 0.060 | - |
| D | 2.900 | 3.000 | 3.100 | 0.1142 | 0.1181 | 0.1220 |
| D1 | - | 2.000 | - | - | 0.0790 | - |
| E | 2.900 | 3.000 | 3.100 | 0.1142 | 0.1181 | 0.1220 |
| E1 | - | 2.000 | - | - | 0.0790 | - |
| L1 | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| L2 | 0.300 | 0.350 | 0.400 | 0.0118 | 0.0138 | 0.0157 |
| L3 | - | 0.200 | - | - | 0.0079 | - |
| L5 | - | 0.150 | - | - | 0.0059 | - |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 47. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**



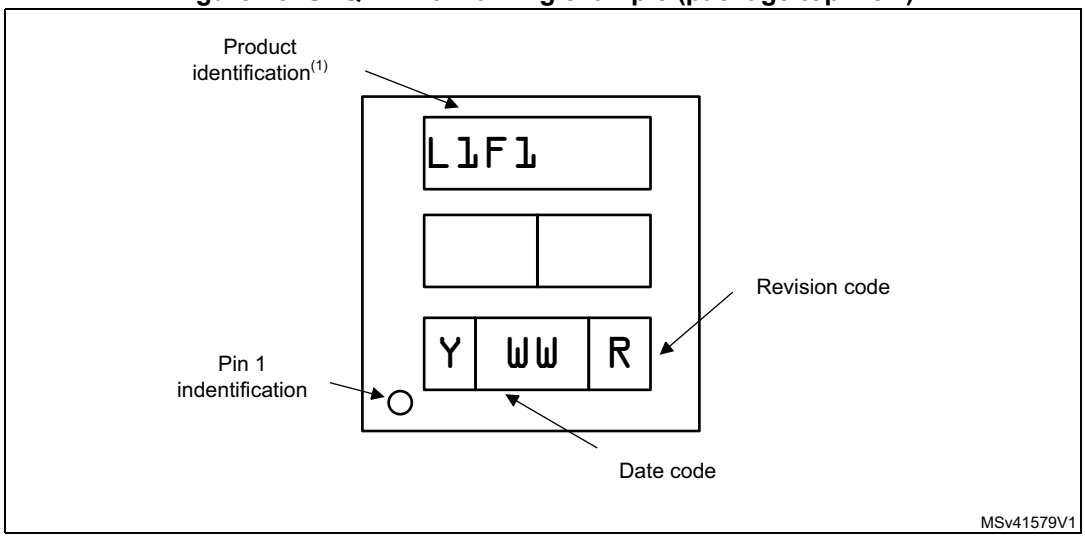

1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

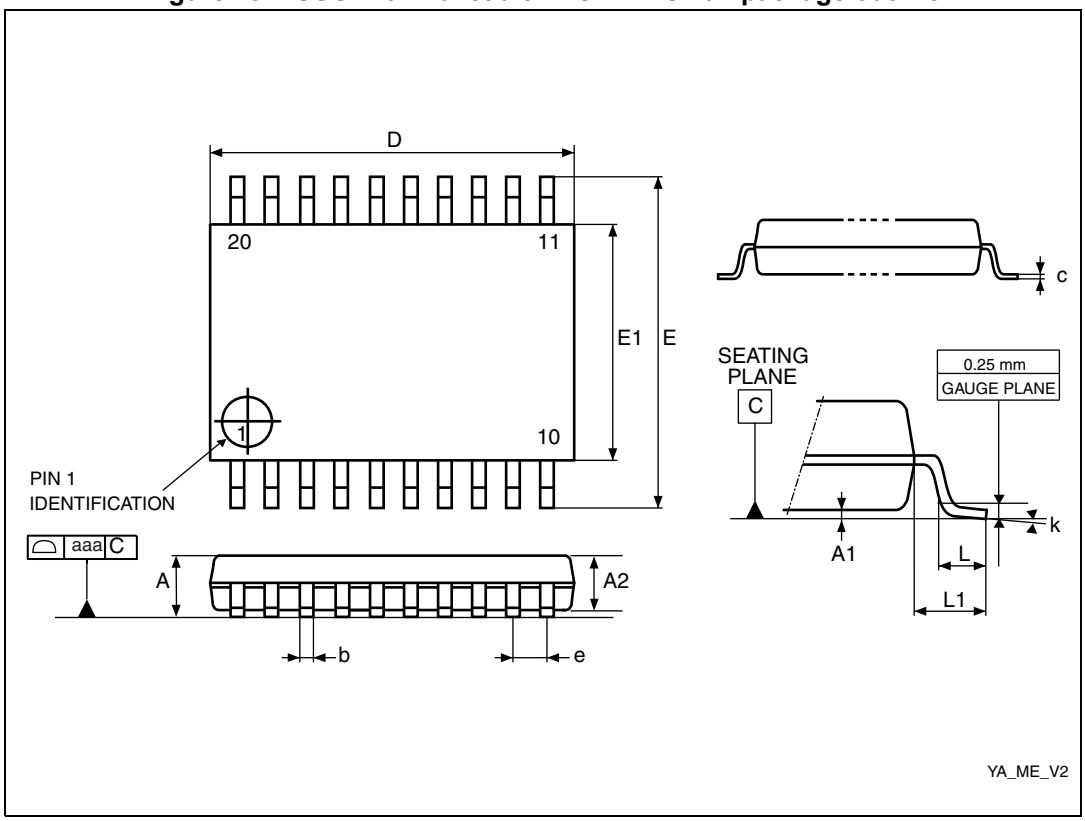
**Figure 48. UFQFPN20 marking example (package top view)**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

## 10.5 TSSOP20 package information

**Figure 49. TSSOP20 - 20-lead thin shrink small package outline**




1. Drawing is not to scale.

**Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data**

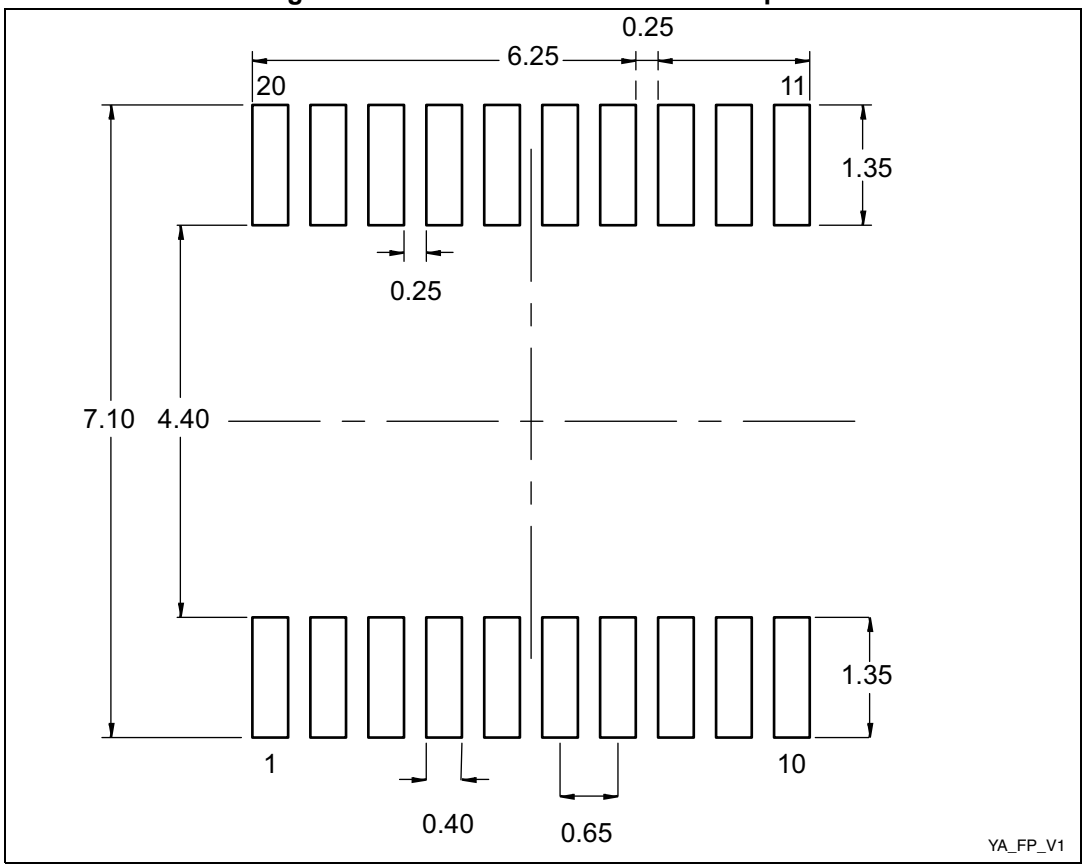
| Dim. | mm | | | | inches(1) | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 0.800 | 1.000 | 1.050 | 0.0315 | 0.0394 | 0.0413 |
| b | 0.190 | - | 0.300 | 0.0075 | - | 0.0118 |
| CP | - | - | 0.100 | - | - | 0.0039 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D(2) | 6.400 | 6.500 | 6.600 | 0.2520 | 0.2559 | 0.2598 |
| E | 6.200 | 6.400 | 6.600 | 0.2441 | 0.2520 | 0.2598 |
| E1(3) | 4.300 | 4.400 | 4.500 | 0.1693 | 0.1732 | 0.1772 |
| e | - | 0.650 | - | 0.1693 | 0.0256 | - |
| L | 0.450 | 0.600 | 0.750 | 0.1693 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |

**Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data (continued)**

| Dim. | mm | | | | inches[1] | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| k | 0° | - | 8° | 0° | - | 8° |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| Number of pins | 20 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

**Figure 50. TSSOP20 recommended footprint**



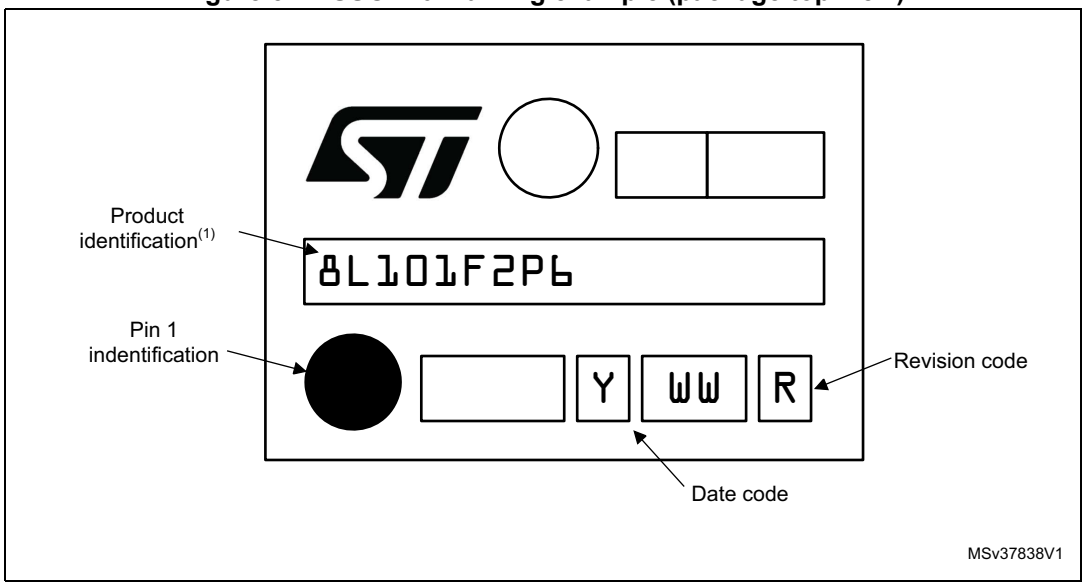

1. Dimensions are in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

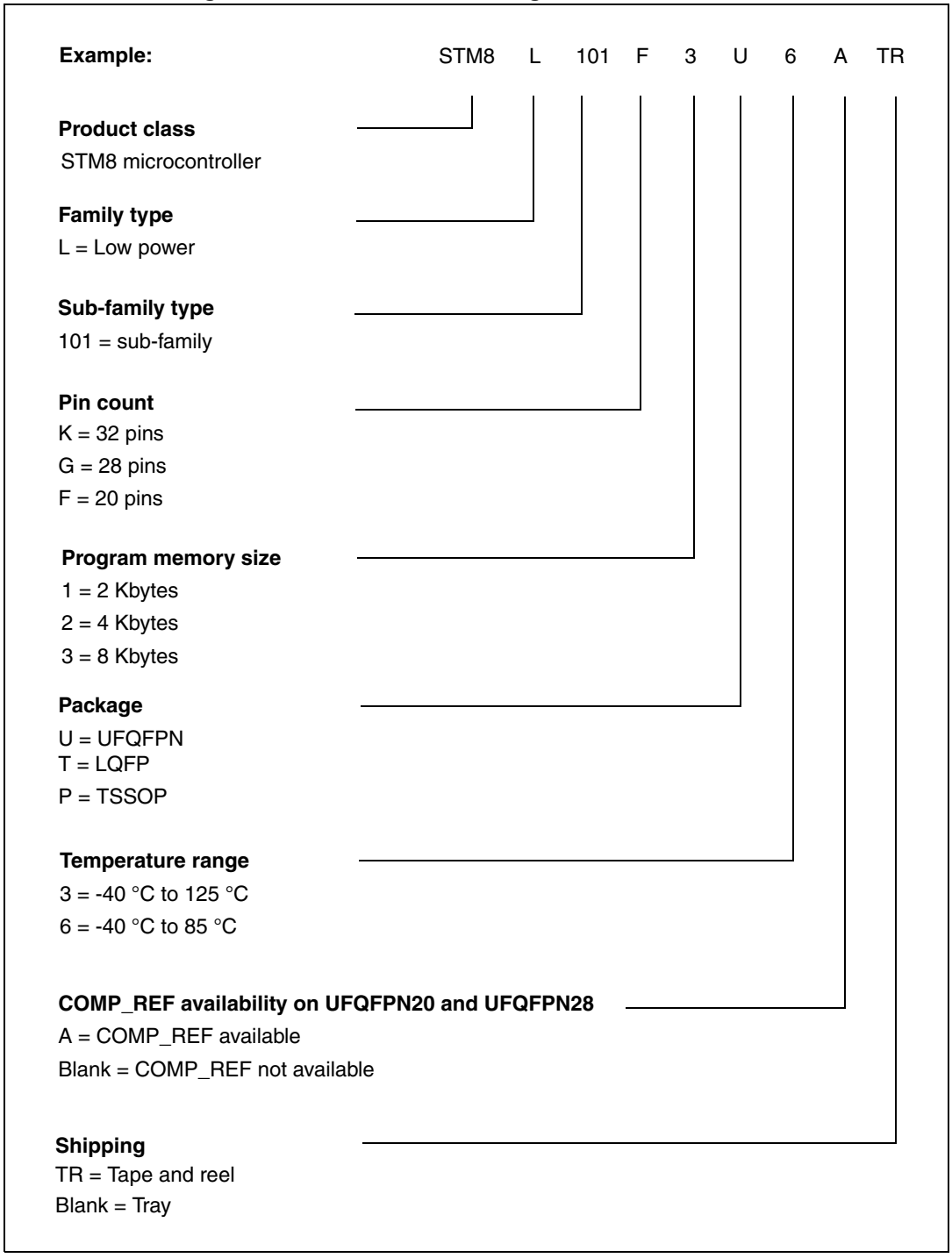
**Figure 51. TSSOP20 marking example (package top view)**




1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

# 11 Device ordering information

**Figure 52. STM8L101xx ordering information scheme**




1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

# 12 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

## 12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows the users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

### STice key features

- Occurrence and time profiling and code coverage (new features)
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows the users to specify the components that they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

## 12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

### 12.2.1 STM8 toolset

***STM8 toolset*** with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

***ST Visual Develop*** – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

***ST Visual Programmer (STVP)*** – Easy-to-use, unlimited graphical interface allowing read, write and verify of the STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

### 12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows the user to assemble and link their application source code.

## 12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user's application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

# 13 Revision history

**Table 44. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 19-Dec-2008 | 1 | Initial release. |
| 22-Apr-2009 | 2 | Added TSSOP28 package<br>Modified packages on first page<br>COMPx_OUT pins removed<br>Added *Figure 6: 28-pin TSSOP package pinout on page 17*<br>Modified *Section 9: Electrical parameters on page 38*.<br>Updated UBC[7:0] description in *Section 7: Option bytes*.<br>Updated low power current consumption on cover page.<br>Updated *Table 13: Voltage characteristics*, *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V*, *Table 26: I/O static characteristics*, *Table 30: NRST pin characteristics*, and *Section 9.3.9: EMC characteristics*.<br>Updated PA1/NRST, PC0 and PC1 in *Table 4: STM8L101xx pin description*.<br>Added ECC feature.<br>Changed internal RC frequency to 38 kHz.<br>Updated electrical characteristics in *Table 16*, *Table 18*, *Table 19*, *Table 20*, *Table 22*, *Table 23*, and *Table 26*. |
| 24-Apr-2009 | 3 | Corrected title on cover page.<br>Changed VFQFPN32 to WFQFPN32 and updated *Table 39: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data*.<br>Updated *Table 13*, *Table 26*, and *Table 33*. |
| 14-May-2009 | 4 | Replaced WFQFPN20 3 x 3 mm 0.8 mm package by UFQFPN20 3 x 3 mm 0.6 mm package (first page, *Table 16: General operating conditions on page 40*, *Table 38: Thermal characteristics on page 63*, *Section 10.2: Package mechanical data on page 67*)<br>Added one UFQFPN20 version with COMP_REF<br>Modified *Figure 40: LQFP32 recommended footprint(1) on page 69*<br>Added $I_{PROG}$ values in *Table 25: Flash program memory on page 47*<br>Updated *Table 31: SPI characteristics on page 55* |
| 15-May-2009 | 5 | Added STM8L101F3U6ATR part number in *Section 4: Pin description on page 15* and in *Figure 47: STM8L101xx ordering information scheme on page 74* |

**Table 44. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 12-Jun-2009 | 6 | Removed TSSOP28 package<br>Modified consumption value on first page<br>Added BEEP_CSR (address 00 50F3h) in *Table 7: General hardware register map on page 25*<br>TIM2_PSCRL replaced with TIM2_PSCR and CLK_PCKEN replaced with CLK_PCKENR in *Table 7: General hardware register map on page 25*<br>Added graphs in *Section 9: Electrical parameters on page 38*<br>Added $t_{WU}$(AH) and $t_{WU}$(Halt) max values in *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V on page 44*<br>Modified *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V on page 44*<br>Updated *Table 22: HSI oscillator characteristics on page 45*, *Table 23: LSI oscillator characteristics on page 47* and *Table 24: RAM and hardware registers on page 47*<br>Modified *Table 27: Output driving current (High sink ports) on page 51*<br>Removed note 1 in *Table 37: Electrical sensitivities on page 62*<br>Added note to *Table 39: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data on page 67* and<br>*Table 41: UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package (4 x 4), package mechanical data on page 70* |

**Table 44. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 07-Sep-2009 | 7 | Added STM8L101F2U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers<br>Modified *Section 2: Description on page 9*.<br>Modified *Table 2: STM8L101xx device feature summary on page 9* (Flash)<br>Modified *Figure 1: STM8L101xx device block diagram on page 10*<br>Modified *Section 3.5: Memory on page 12*<br>Added note below *Figure 2: Standard 20-pin UFQFPN package pinout on page 15* and *Figure 5: Standard 28-pin UFQFPN package pinout on page 17*<br>Added *Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers on page 18*<br>Modified reset values for Px_IDR registers in *Table 6: I/O Port hardware register map on page 24*<br>Added *Section 6: Interrupt vector mapping on page 32*<br>Modified OPT numbers in *Section 7: Option bytes*<br>Modified OPT2 in *Table 10: Option bytes*<br>Added *Section 8: Unique ID on page 36*<br>TIM_IR pin replaced with IR_TIM pin<br>Modified *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V on page 44*<br>Modified *Figure 15: Typ. IDD(Halt) vs. VDD, fCPU = 2 MHz and 16 MHz on page 44* and *Figure 19: Typical LSI RC frequency vs. VDD on page 47*<br>Modified *Table 27: Output driving current (High sink ports) on page 51*<br>Updated *Table 29: Output driving current (PA0 with high sink LED driver capability) on page 51*<br>Modified *: Functional EMS (electromagnetic susceptibility) on page 60*<br>Modified conditions in *Table 35: EMI data on page 61*<br>Added note to *Figure 37: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5) on page 67*<br>Modified *Figure 41: UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package outline (4 x 4)(1) on page 70*<br>Added *Figure 44: UFQFPN20 recommended footprint (1) on page 71*<br>Added *Figure 46: TSSOP20 recommended footprint (1) on page 72*<br>CMP replaced with COMP |

**Table 44. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 29-Nov-2009 | 8 | Modified status of the document (datasheet instead of preliminary data)<br>Replaced WFQFPN32 with UFQFPN32 and WFQFPN28 with UFQFPN28.<br>Modified title of the reference manual mentioned in *Section 2: Description on page 9*<br>Added references to “low-density” in *Section 2: Description on page 9*, *Section 3.5: Memory on page 12* and in *Figure 8: Memory map on page 23*<br>Modified *Figure 8: Memory map on page 23* (unique ID are added)<br>*Table 7: General hardware register map on page 25*: Modified reserved areas and IR block replaced with IRTIM block<br>Modified $t_{TEMP}$ in *Table 17: Operating conditions at power-up / power-down on page 41*<br>Modified *Table 23: LSI oscillator characteristics on page 47*<br>Modified *Table 25: Flash program memory on page 47* ($t_{PROG}$)<br>Modified *Table 16: General operating conditions on page 40* and *Table 38: Thermal characteristics on page 63*<br>Modified *Section 13: Revision history on page 82* |
| 18-Jun-2010 | 9 | Modified *Introduction* and *Description*<br>Modified one reserved area (0x00 5055 to 0x00 509F) in *Table 7: General hardware register map*<br>Modified*Table 4: STM8L101xx pin description*: modified note 2 and removed “wpu” for PC0 and PC1<br>Removed one note to *Table 22: HSI oscillator characteristics on page 45*<br>Modified first paragraph in *Section : NRST pin*<br>Modified OPT3 description in *Table 11: Option byte description*<br>Added note 5 to *Table 18: Total current consumption in Run mode*<br>Modified $V_{ESD(CDM)}$ in *Table 36: ESD absolute maximum ratings on page 61*<br>Modified *Figure 36: Typical application with I2C bus and timing diagram 1) on page 59*<br>Modified COMP_REF availability information in *Figure 52: STM8L101xx ordering information scheme on page 79*<br>Modified *Section 12.2: Software tools on page 78* |
| 21-Jul-2010 | 10 | Modified *Table 3: Legend/abbreviation for table 4 on page 20* and *Table 4: STM8L101xx pin description on page 20* (for PA0, PA1, PB0 and PB4)<br>Modified *Table 13: Voltage characteristics on page 38* and *Table 14: Current characteristics on page 39*<br>Modified $V_{IH}$ in *Table 26: I/O static characteristics on page 48*<br>Added notes below UFQFPN32 package |

**Table 44. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 14-Oct-2010 | 11 | Added STM8L101F1 devices:<br>Modified *Table 1: Device summary on page 1*, *Table 2: STM8L101xx device feature summary on page 9* and *Table 5: Flash and RAM boundary addresses on page 24*<br>Modified warning below *Figure 3 on page 16* and below*Table 4: STM8L101xx pin description on page 20*<br>Modified *Figure 52: STM8L101xx ordering information scheme on page 79*<br>Modified text above *Figure 32: Recommended NRST pin configuration on page 54*<br>Modified *Figure 32 on page 54* |
| 02-Aug-2013 | 12 | Added “The RAM content is preserved” in halt mode *Section 3.6: Low power modes*<br>Reformatted *Figure 2: Standard 20-pin UFQFPN package pinout*, *Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 5: Standard 28-pin UFQFPN package pinout*, *Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers* and *Figure 7: 32-pin package pinout*<br>Corrected NRST/PA1 pin OD output capability in *Table 4: STM8L101xx pin description* and corrected note *2.* and *4.*<br>Added note “Slope control of all GPIO can be programmed except...” in *Table 4: STM8L101xx pin description*<br>Added note under *Table 5: Flash and RAM boundary addresses*<br>Replaced UM0320 with UM0470 in *Section 7: Option bytes*<br>Updated OPT2 and OPT3 in *Table 10: Option bytes*<br>Added additional note *2.* references in *Table 22: HSI oscillator characteristics*<br>Added note *2.* under *Table 17: Operating conditions at power-up / power-down* and under *Figure 32: Recommended NRST pin configuration*<br>Corrected ‘SCK output’ in *Figure 35: SPI timing diagram - master mode(1)*<br>Added top view in *Figure 43: UFQFPN20 3 x 3 mm 0.6 mm package outline*<br>Repositioned the package layout and footprint for all packages.<br>Replaced “Standard ports” with “High sink ports”<br>Replaced “TIMx_TRIG” with “TIMx_ETR”<br>Replaced all ‘"Data guaranteed, each individual device tested in production” notes with “Tested in production” |
| 31-Mar-2014 | 13 | Updated L3 value on *Table 42*, added note 2) and 3) on *Table 43* |
| 18-Dec-2014 | 14 | Updated:<br>– *Figure 46: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline*,<br>– *Table 42: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3 x 3 mm) mechanical data*. |

**Table 44. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 02-Aug-2016 | 15 | Added:<br>– *Figure 39: UFQFPN32 marking example (package top view)*<br>– *Figure 42: LQFP32 marking example (package top view)*<br>– *Figure 45: UFQFPN28 marking example (package top view)*<br>– *Figure 48: UFQFPN20 marking example (package top view)*<br>– *Figure 51: TSSOP20 marking example (package top view)*<br>Updated:<br>– *Section 9.2: Absolute maximum ratings*. |
| 12-May-2017 | 16 | Updated:<br>– All table footnotes from “Data guaranteed by design, not tested in production” to “Guaranteed by design” and “Data based on characterization results, not tested in production” to “Guaranteed by characterization results”<br>– *Section : Device marking on page 66*<br>– *Section : Device marking on page 69*<br>– *Section : Device marking on page 72*<br>– *Section : Device marking on page 75*<br>– *Section : Device marking on page 78*<br>– *Figure 46: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline*<br>– *Table 42: UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data* |

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