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FAIRCHILD
SEMICONDUCTOR TM

July 1999

# FDG6301N
# Dual N-Channel, Digital FET

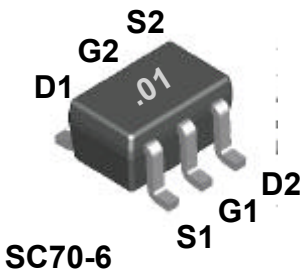
## General Description

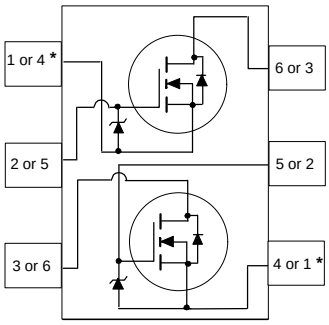
These dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs.

## Features

- 25 V, 0.22 A continuous, 0.65 A peak.
  $R_{DS(ON)}$ = 4 Ω @ $V_{GS}$= 4.5 V,
  $R_{DS(ON)}$ = 5 Ω @ $V_{GS}$= 2.7 V.
- Very low level gate drive requirements allowing direct operation in 3 V circuits ($V_{GS(th)}$ < 1.5 V).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).
- Compact industry standard SC70-6 surface mount package.

| SC70-6 | SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 |
|---|---|---|---|---|---|




*The pinouts are symmetrical; pin 1 and 4 are interchangeable.
Units inside the carrier can be of either orientation and will not affect the functionality of the device.

## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | FDG6301N | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 25 | V |
| $V_{GSS}$ | Gate-Source Voltage | 8 | V |
| $I_D$ | Drain/Output Current - Continuous | 0.22 | A |
| | - Pulsed | 0.65 | |
| $P_D$ | Maximum Power Dissipation (Note 1) | 0.3 | W |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | -55 to 150 | °C |
| ESD | Electrostatic Discharge Rating MIL-STD-883D Human Body Model(100 pF / 1500 Ω) | 6.0 | kV |
| **THERMAL CHARACTERISTICS** | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 415 | °C/W |

## Electrical Characteristics ($T_A$ = 25 °C unless otherwise noted )

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 25 | | | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | 25 | | mV /°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $T_J$ = 55°C | | | 10 | µA |
| $I_{GSS}$ | Gate - Body Leakage Current | $V_{GS}$ = 8 V, $V_{DS}$ = 0 V | | | 100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 0.65 | 0.85 | 1.5 | V |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Temp.Coefficient | $I_D$ = 250 µA, Referenced to 25 °C | | -2.1 | | mV /°C |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 0.22 A | | 2.6 | 4 | Ω |
| | | $T_J$ =125°C | | 5.3 | 7 | |
| | | $V_{GS}$ = 2.7 V, $I_D$ = 0.19 A | | 3.7 | 5 | |
| $I_{D(ON)}$ | On-State Drain Current | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | 0.22 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$= 0.22 A | | 0.2 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 9.5 | | pF |
| $C_{oss}$ | Output Capacitance | | | 6 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 1.3 | | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{D(on)}$ | Turn - On Delay Time | $V_{DD}$ = 5 V, $I_D$ = 0.5 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 50 Ω | | 5 | 10 | ns |
| $t_r$ | Turn - On Rise Time | | | 4.5 | 10 | ns |
| $t_{D(off)}$ | Turn - Off Delay Time | | | 4 | 8 | ns |
| $t_f$ | Turn - Off Fall Time | | | 3.2 | 7 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 5 V, $I_D$ = 0.22 A, $V_{GS}$ = 4.5 V | | 0.29 | 0.4 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 0.12 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 0.03 | | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Source Current | | | | 0.25 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 0.25 A (Note 2) | | 0.8 | 1.2 | V |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ = 415°C/W on minimum pad mounting on FR-4 board in still air.
2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

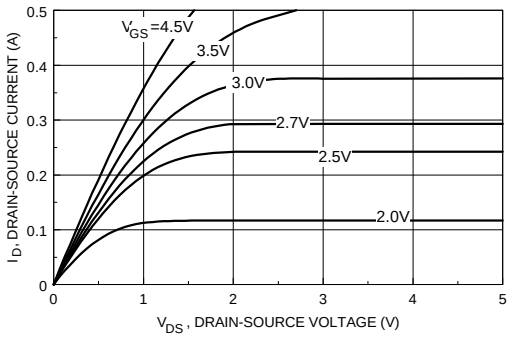



**Figure 1. On-Region Characteristics.**

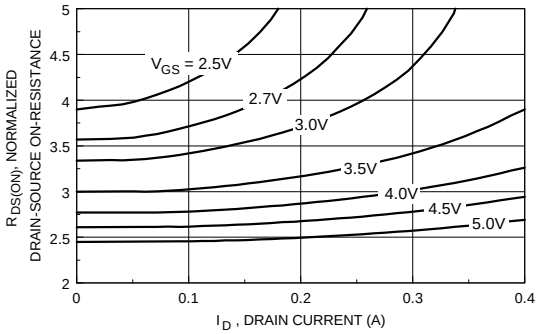



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

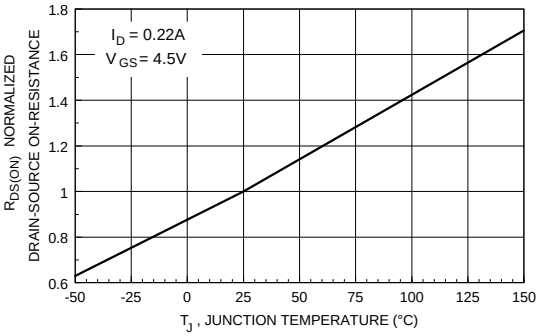



**Figure 3. On-Resistance Variation with Temperature.**

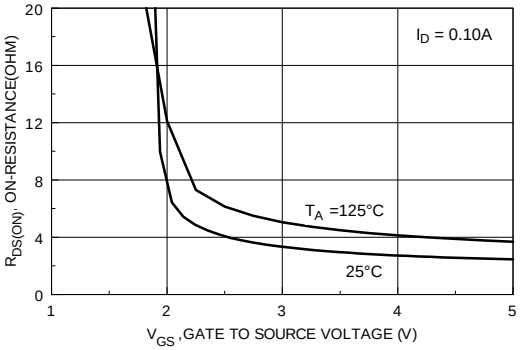



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

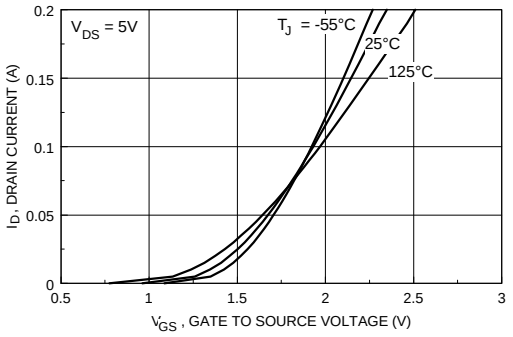



**Figure 5. Transfer Characteristics.**

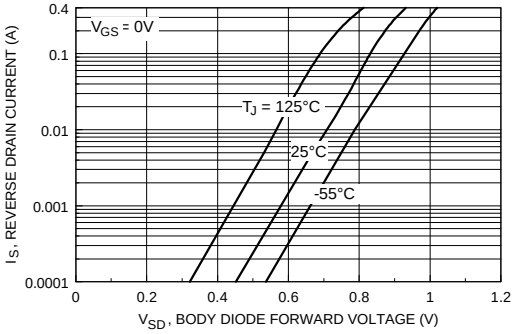



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Electrical Characteristics ( continued)

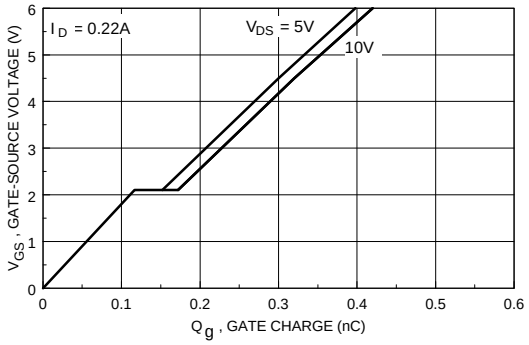



**Figure 7. Gate Charge Characteristics.**

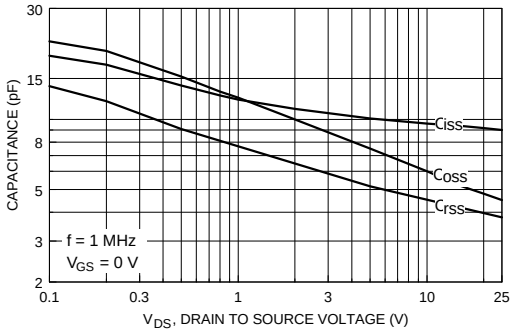



**Figure 8. Capacitance Characteristics.**

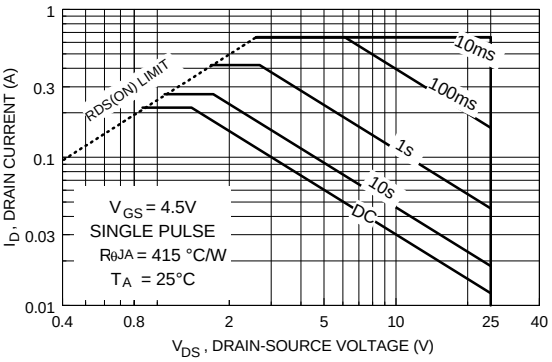



**Figure 9. Maximum Safe Operating Area.**

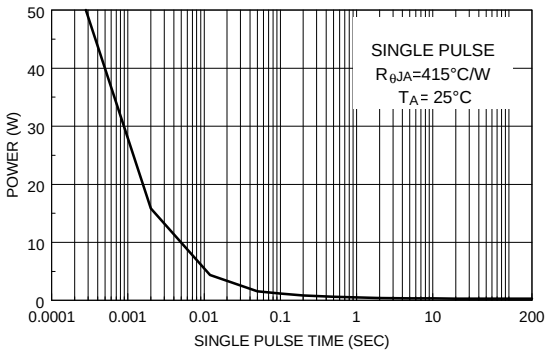



**Figure 10. Single Pulse Maximum Power Dissipation.**

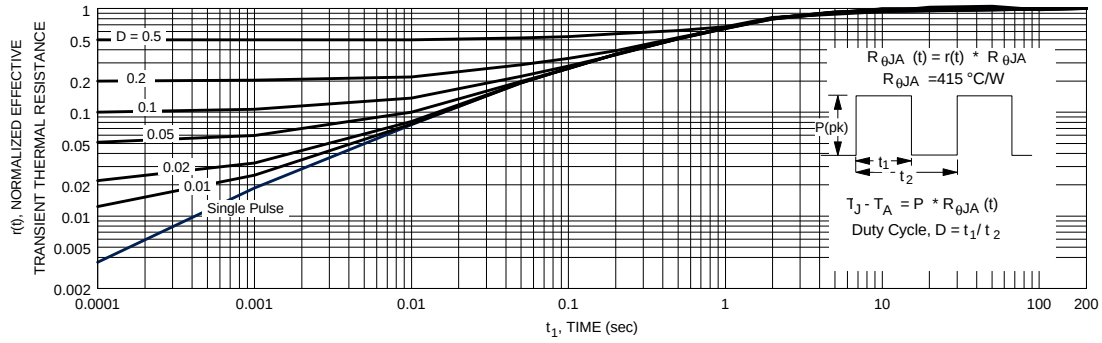



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in note 1.
Transient thermal response will change depending on the circuit board design.

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