Features



### Low-Power, Serial, 12-Bit DACs with Voltage Output

### General Description

The MAX5174/MAX5176 low-power, serial, voltage-output, 12-bit digital-to-analog converters (DACs) feature a precision output amplifier in a space-saving 16-pin QSOP package. The MAX5174 operates from a single +5V supply, and the MAX5176 operates from a single +3V supply. Both devices draw only 280µA of supply current, which reduces to 1µA in shutdown. In addition, the programmable power-up reset feature allows for a user-selectable output voltage state of either 0 or midscale.

The 3-wire, digital, serial interface is compatible with SPI™/QSPI™, and MICROWIRE™ standards. An input register followed by a DAC register provides a doublebuffered input, allowing the input and DAC registers to be updated independently or simultaneously with a 16bit serial word. Additional features include software and hardware shutdown, shutdown lockout, a hardware clear pin, and a reference input capable of accepting DC and offset AC signals. These devices provide a programmable digital output pin for added functionality and a serial-data output pin for daisy-chaining. All logic inputs are TTL/CMOS compatible and are internally buffered with Schmitt triggers to allow direct interfacing to optocouplers.

The MAX5174/MAX5176 incorporate a proprietary onchip circuit that keeps the output voltage virtually "glitch free," limiting the glitches to a few millivolts during power-up.

Both devices are available in 16-pin QSOP packages and are specified for the extended (-40°C to +85°C) temperature range. The MAX5170/MAX5172 are pincompatible 14-bit upgrades to the MAX5174/MAX5176. For 100% pin-compatible DACs with internal reference, see the 13-bit MAX5130/MAX5131 and the 12-bit MAX5120/MAX5121 data sheets.

#### **Applications**

**Industrial Process Controls** Digital Offset and Gain Adjustment Motion Control Automatic Test Equipment (ATE) Remote Industrial Controls μP-Controlled Systems

#### Functional Diagram appears at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp. Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

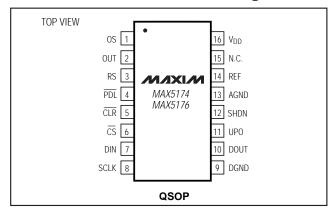
#### ♦ ±1 LSB INL

- ↑ 1µA Shutdown Current
- ◆ "Glitch Free" Output Voltage at Power-Up
- **♦** Single-Supply Operation
  - +5V (MAX5174)
  - +3V (MAX5176)
- **♦ Full-Scale Output Range** 
  - +2.048V (MAX5176,  $V_{REF} = +1.25V$ )
  - +4.096V (MAX5174,  $V_{REF} = +2.5V$ )
- ♦ Rail-to-Rail® Output Amplifier
- **♦** Adjustable Output Offset
- Low THD (-80dB) in Multiplying Operation
- **♦** SPI/QSPI/MICROWIRE-Compatible 3-Wire Serial Interface
- ♦ Programmable Shutdown Mode and Power-Up Reset
- ♦ Buffered Output Capable of Driving 5kΩ || 100pF Loads
- ♦ User-Programmable Digital Output Pin Allows **Serial Control of External Components**
- ↑ 14-Bit Upgrades Available (MAX5170/MAX5172)

### Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5174AEEE	-40°C to +85°C	16 QSOP	±1
MAX5174BEEE	-40°C to +85°C	16 QSOP	±2
MAX5176AEEE	-40°C to +85°C	16 QSOP	±2
MAX5176BEEE	-40°C to +85°C	16 QSOP	±4

### Pin Configuration



NIXIN

Maxim Integrated Products 1

### **ABSOLUTE MAXIMUM RATINGS**

V <sub>DD</sub> to AGND, DGND	0.3V to +6.0V
AGND to DGND	0.3V to +0.3V
Digital Inputs to DGND	0.3V to +6.0V
DOUT, UPO to DGND	0.3V to (V <sub>DD</sub> + 0.3V)
OUT, REF to AGND	0.3V to (V <sub>DD</sub> + 0.3V)
OS to AGND	(AGND - $4.0V$ ) to ( $V_{DD} + 0.3V$ )
Maximum Current into Any Pin.	50mA

Continuous Power Dissipation (T <sub>A</sub> = +	70°C)
16-Pin QSOP (derate 8mW/°C abov	e +70°C)667mW
Operating Temperature Range	40°C to +85°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10sec).	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS—MAX5174**

 $(V_{DD} = +5V \pm 10\%, V_{REF} = 2.5V, OS = AGND = DGND, R_L = 5k\Omega, C_L = 100pF$  referenced to ground,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25$ °C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			12			Bits
	INII	MAX5174A			±1	LCD
Integral Nonlinearity (Note 1)	INL	MAX5174B			±2	LSB
Differential Nonlinearity	DNL				±1	LSB
Offset Error (Note 2)	Vos				±10	mV
Gain Error	GE	R <sub>L</sub> = ∞		-0.6	±4	LSB
Gaill Elloi	GE	$R_L = 5k\Omega$		-1.6	±8	LSD
Power-Supply Rejection Ratio	PSRR			10	120	μV/V
Output Noise Voltage		f = 100kHz		1		LSBp-p
Output Thermal Noise Density				80		nV/√Hz
REFERENCE	•		'			
Reference Input Range	V <sub>REF</sub>		0		V <sub>DD</sub> - 1.4	V
Reference Input Resistance	RREF		18			kΩ
MULTIPLYING-MODE PERFOR	MANCE		<u>'</u>			
Reference -3dB Bandwidth		V <sub>REF</sub> = 0.5Vp-p + 1.5V <sub>DC</sub> , slew-rate limited		350		kHz
Reference Feedthrough		V <sub>REF</sub> = 3.6Vp-p + 1.8V <sub>DC</sub> , f = 1kHz, code = all 0s		-80		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	VREF = 2Vp-p + 1.5V <sub>DC</sub> , f = 10kHz, code = FFF hex		82		dB
DIGITAL INPUTS	-		'			
Input High Voltage	VIH		3			V
Input Low Voltage	VIL				0.8	V
Input Hysteresis	VHYS	200			mV	
Input Leakage Current	liN	VIN = 0 or VDD		0.001	±1	μΑ
Input Capacitance	CIN			8		pF
DIGITAL OUTPUTS						
Output High Voltage	Voh	ISOURCE = 2mA	V <sub>DD</sub> - 0.5	5		V
Output Low Voltage	VoL	I <sub>SINK</sub> = 2mA		0.13	0.4	V

### **ELECTRICAL CHARACTERISTICS—MAX5174 (continued)**

 $(V_{DD} = +5V \pm 10\%, V_{REF} = 2.5V, OS = AGND = DGND, R_L = 5k\Omega, C_L = 100pF$  referenced to ground,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25$ °C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±0.5LSB, from 10mV to full-scale		18		μs
Output Voltage Swing (Note 3)			0		$V_{DD}$	V
OS Pin Input Resistance			80	120		kΩ
Time Required to Exit Shutdown				40		μs
Digital Feedthrough		$\overline{\text{CS}}$ = V <sub>DD</sub> , f <sub>SCLK</sub> = 100kHz, V <sub>SCLK</sub> = 5Vp-p		1		nV-s
POWER SUPPLIES	•					
Positive Supply Voltage	V <sub>DD</sub>		4.5		5.5	V
Power-Supply Current (Note 4)	I <sub>DD</sub>			0.35	0.4	mA
Shutdown Current (Note 4)				1	10	μΑ
TIMING CHARACTERISTICS	•					•
SCLK Clock Period	tcp		100			ns
SCLK Pulse Width High	tсн		40			ns
SCLK Pulse Width Low	tcL		40			ns
CS Fall to SCLK Rise Setup Time	tcss		40			ns
SCLK Rise to $\overline{\text{CS}}$ Rise Hold Time	tcsh		0			ns
SDI Setup Time	tDS		40			ns
SDI Hold Time	t <sub>DH</sub>		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t <sub>DO1</sub>	C <sub>LOAD</sub> = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t <sub>DO2</sub>	C <sub>LOAD</sub> = 200pF			80	ns
SCLK Rise to CS Fall Delay	t <sub>CS0</sub>		10			ns
$\overline{\text{CS}}$ Rise to SCLK Rise Hold Time	tcs1		40			ns
CS Pulse Width High	tcsw		100			ns

### **ELECTRICAL CHARACTERISTICS—MAX5176**

 $(V_{DD}=+2.7V\ to\ +3.6V,\ V_{REF}=1.25V,\ OS=AGND=DGND,\ R_{L}=5k\Omega,\ C_{L}=100pF\ referenced\ to\ ground,\ T_{A}=T_{MIN}\ to\ T_{MAX},\ unless\ otherwise\ noted.$  Typical values are at  $T_{A}=+25^{\circ}C$ ).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE	1		1			
Resolution			12			Bits
Integral Manlinearity (Note E)	INI	MAX5176A			±2	LSB
Integral Nonlinearity (Note 5)	IINL	MAX5176B			±4	LSD
Differential Nonlinearity	DNL				±1	LSB
Offset Error (Note 2)	Vos				±10	mV
Gain Error	GE	R <sub>L</sub> = ∞		-0.6	±4	LSB
Galii Eiioi	GE	$R_L = 5k\Omega$		-1.6	±8	LSD
Power-Supply Rejection Ratio	PSRR			10	120	μV/V
Output Noise Voltage		f = 100kHz		2		LSBp-p
Output Thermal Noise Density				80		nV/√Hz
REFERENCE	•		•			•
Reference Input Range	VREF		0		V <sub>DD</sub> - 1.4	V
Reference Input Resistance	R <sub>REF</sub>		18			kΩ
MULTIPLYING-MODE PERFOR	MANCE					
Reference -3dB Bandwidth		V <sub>REF</sub> = 0.5Vp-p + 0.75V <sub>DC</sub> , slew-rate limited		350		kHz
Reference Feedthrough		VREF = 1.6Vp-p + 0.8VDC, f = 1kHz, code = all 0s		-80		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	$V_{REF} = 0.6Vp-p + 0.9V_{DC}$ , $f = 10kHz$ , $code = FFF hex$		78		dB
DIGITAL INPUT	1		1			
Input High Voltage	VIH		2.2			V
Input Low Voltage	VIL				0.8	V
Input Hysteresis	VHYS			200		mV
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 or V <sub>DD</sub>		0.001	±1	μΑ
Input Capacitance	CIN			8		pF
DIGITAL OUTPUT						
Output High Voltage	Voн	ISOURCE = 2mA	V <sub>DD</sub> - 0.5			V
Output Low Voltage	VoL	I <sub>SINK</sub> = 2mA		0.13	0.4	V

### **ELECTRICAL CHARACTERISTICS—MAX5176 (continued)**

 $(V_{DD}=+2.7V\ to\ +3.6V,\ V_{REF}=1.25V,\ OS=AGND=DGND,\ R_L=5k\Omega,\ C_L=100pF\ referenced\ to\ ground,\ T_A=T_{MIN}\ to\ T_{MAX},\ unless\ otherwise\ noted.$  Typical values are at  $T_A=+25\,^{\circ}C$ ).

PARAMETER SYMBOL		CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE	l					
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±0.5LSB, from 10mV to full-scale		18		μs
Output Voltage Swing (Note 3)			0		$V_{DD}$	V
OS Pin Input Resistance			80	120		kΩ
Time Required to Exit Shutdown				40		μs
Digital Feedthrough		$\overline{\text{CS}} = \text{V}_{\text{DD}}$ , DIN = 50kHz; $f_{\text{SCLK}} = 100$ kHz, $f_{\text{SCLK}} = 3$ Vp-p		1		nV-s
POWER SUPPLIES						l
Positive Supply Voltage	V <sub>DD</sub>		2.7		3.6	V
Power-Supply Current (Note 4)	I <sub>DD</sub>			0.35	0.4	mA
Shutdown Current (Note 4)				1	10	μΑ
TIMING CHARACTERISTICS			•			•
SCLK Clock Period	tcp		150			ns
SCLK Pulse Width High	tсн		75			ns
SCLK Pulse Width Low	tcL		75			ns
CSB Fall to SCLK Rise Setup Time	tcss		60			ns
SCLK Rise to $\overline{\text{CS}}$ Rise Hold Time	tcsh		0			ns
SDI Setup Time	t <sub>DS</sub>		60			ns
SDI Hold Time	tDH		0			ns
SCLK Rise to DOUT Valid Propagation Delay	tDO1	CLOAD = 200pF			200	ns
SCLK Fall to DOUT Valid Propagation Delay		C <sub>LOAD</sub> = 200pF			200	ns
SCLK Rise to CS Fall Delay	t <sub>CS0</sub>		10			ns
CS Rise to SCLK Rise Hold Time	t <sub>CS1</sub>		75			ns
CS Pulse Width High	tcsw		150			ns

Note 2: Offset is measured at the code that comes closest to 10mV.

Note 3: Accuracy is better than 1 LSB for V<sub>OUT</sub> = 10mV to V<sub>DD</sub> - 180mV. Guaranteed by PSR test on end points.

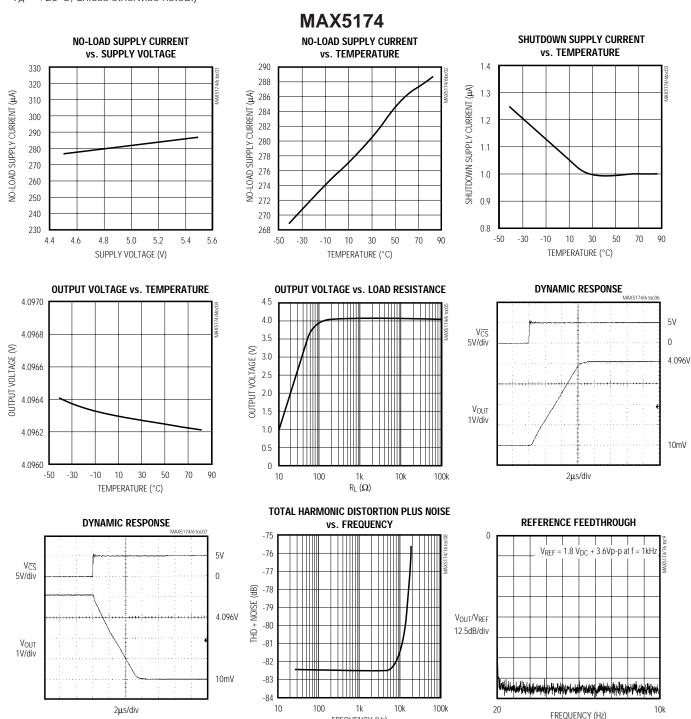
**Note 4:** R<sub>L</sub> = open and digital inputs are either V<sub>DD</sub> or DGND.

Note 5: INL guaranteed between codes 20 and 4095.

Typical Operating Characteristics

MIXIM

(MAX5174:  $V_{DD}$  = +5V,  $V_{REF}$  = 2.5V; MAX5176:  $V_{DD}$  = +3V,  $V_{REF}$  = +1.25V;  $C_L$  = 100pF, OS = AGND, code = FFF hex,  $T_A$  = +25°C, unless otherwise noted.)

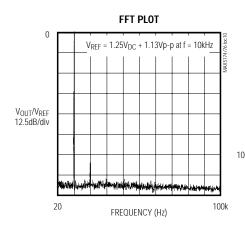


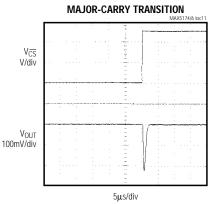
FREQUENCY (Hz)

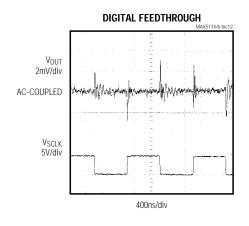
Typical Operating Characteristics (continued)

(MAX5174:  $V_{DD}$  = +5V,  $V_{REF}$  = 2.5V; MAX5176:  $V_{DD}$  = +3V,  $V_{REF}$  = +1.25V;  $C_L$  = 100pF, OS = AGND, code = FFF hex,  $T_A$  = +25°C, unless otherwise noted.)

### **MAX5174**

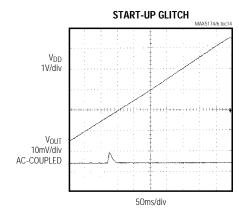




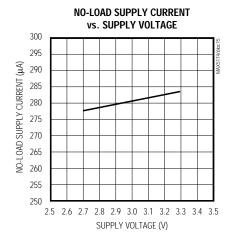


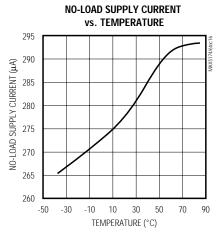
# REFERENCE INPUT FREQUENCY RESPONSE 5 0 -5 -5 -20 V<sub>REF</sub> = 0.67Vp-p + 1.5V<sub>DC</sub> -25 0 500 1000 1500 2000 2500 3000

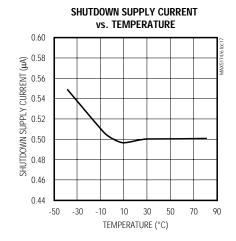
FREQUENCY (kHz)



### **MAX5176**



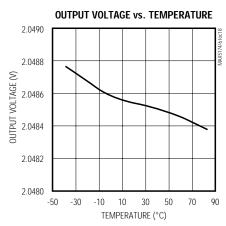


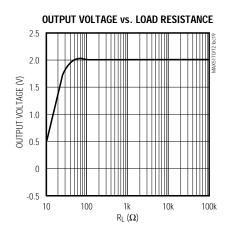


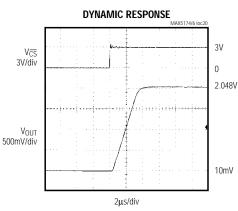
Typical Operating Characteristics (continued)

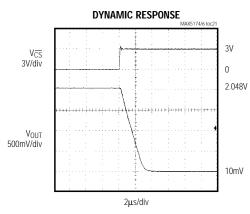
(MAX5174:  $V_{DD}$  = +5V,  $V_{REF}$  = 2.5V; MAX5176:  $V_{DD}$  = +3V,  $V_{REF}$  = +1.25V;  $C_L$  = 100pF, OS = AGND, code = FFF hex,  $T_A$  = +25°C, unless otherwise noted.)

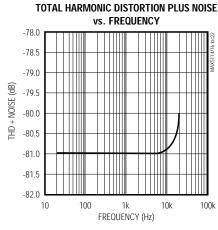
### **MAX5176**

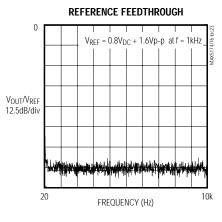


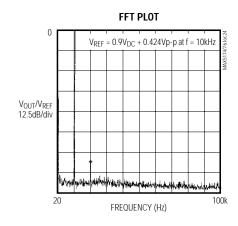


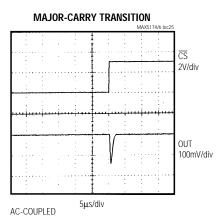








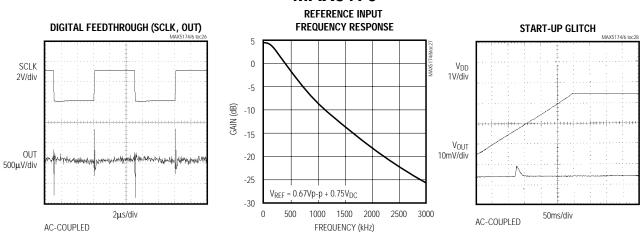




Typical Operating Characteristics (continued)

(MAX5174:  $V_{DD}$  = +5V,  $V_{REF}$  = 2.5V; MAX5176:  $V_{DD}$  = +3V,  $V_{REF}$  = +1.25V;  $C_L$  = 100pF, OS = AGND, code = FFF hex,  $T_A$  = +25°C, unless otherwise noted.)

### **MAX5176**



### Pin Description

PIN	NAME	FUNCTION
1	OS	Offset Adjustment. Connect to AGND for no offset.
2	OUT	Voltage Output. High impedance when in shutdown. The output voltage is limited to V <sub>DD</sub> .
3	RS	Reset Mode Select (digital input). Connect to $V_{DD}$ to select midscale reset output voltage. Connect to DGND to select 0 reset output voltage.
4	PDL	Power-Down Lockout. (digital input). Connect to $V_{DD}$ to allow shutdown. Connect to DGND to disable software and hardware shutdown.
5	CLR	Clear DAC. (digital input) Clears the DAC to either zero or midscale as determined by RS.
6	CS	Chip-Select Input (digital input). DIN ignored when $\overline{\text{CS}}$ is high.
7	DIN	Serial-Data Input (digital input). Data is clocked in on the rising edge of SCLK.
8	SCLK	Serial Clock Input (digital input).
9	DGND	Digital Ground
10	DOUT	Serial-Data Output
11	UPO	User-Programmable Output. State is set by the serial input.
12	SHDN	Shutdown (digital input). Pulling SHDN high when $\overline{PDL} = V_{DD}$ places the chip in shutdown with a maximum shutdown current of 10 $\mu$ A.
13	AGND	Analog Ground
14	REF	Reference Input. Maximum V <sub>REF</sub> is V <sub>DD</sub> - 1.4V.
15	N.C.	No Connection
16	V <sub>DD</sub>	Positive Supply. Bypass to AGND with a 4.7µF capacitor in parallel with a 0.1µF capacitor.

### Detailed Description

The MAX5174/MAX5176 12-bit, serial, voltage-output DACs operate with a 3-wire serial interface. These devices include a 16-bit shift register and a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition, these devices employ a rail-to-rail output amplifier and internal trimmed resistors to provide a gain of +1.638V/V, maximizing the output voltage swing. The MAX5174/MAX5176's offset adjust pin allows for a DC shift in DAC outputs. The DACs are designed with an inverted R-2R ladder network (Figure 1) that produces a weighted voltage proportional to the reference voltage.

#### Reference Inputs

The reference input accepts both AC and DC values with a voltage range extending from 0 to  $V_{DD}$  - 1.4V. The following equation represents the resulting output voltage:

$$V_{OUT} = \frac{V_{REF} \cdot N \cdot Gain}{4096}$$

where N is the numeric value of the DAC's binary input code (0 to 4095), VREF is the reference voltage, and Gain is the internally set voltage gain (1.638V/V if OS = AGND). The maximum output voltage is VDD. The reference pin has a minimum impedance of  $18k\Omega$  and is code dependent.

#### **Output Amplifier**

With OS connected to AGND, the output amplifier employs an internal trimmed resistor-divider, setting the gain to 1.638V/V and minimizing gain error. The output amplifier has a typical slew rate of 0.6V/ $\mu$ s, and settles to  $\pm 0.5$ LSB from a full-scale transition within 18 $\mu$ s when loaded with 5k $\Omega$  in parallel with 100pF. Loads less than 2k $\Omega$  degrade performance. For alternative output amplifier setups, refer to the *Applications Information* section.

#### Shutdown Mode

The MAX5174/MAX5176 feature a software- and hard-ware-programmable shutdown mode that reduces the typical supply current to 1µA. Enter shutdown by writing the appropriate input-control word as shown in Table 1 or by using the hardware shutdown. In shutdown mode, the reference input and amplifier output both become high impedance, and the serial interface remains active. Data in the input register is saved, allowing the MAX5174/MAX5176 to recall the prior output state when returning to normal operation. Exit shutdown by

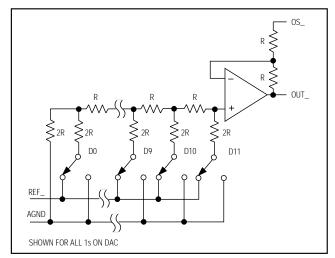


Figure 1. Simplified DAC Circuit Diagram

reloading the DAC register from the shift register, by simultaneously loading the input and DAC registers, or by toggling PDL. When returning from shutdown wait 40µs for the output to settle.

#### Power-Down Lockout

Power-down lockout disables the software/hardware shutdown mode. A high-to-low transition on PDL brings the device out of shutdown and returns the output to its previous state.

#### Shutdown

Pulling SHDN high while PDL is high places the MAX5174/MAX5176 in shutdown. Pulling SHDN low will not return the device to normal operation. A high-to-low transition on PDL or an appropriate command from the serial data line (see Table 1 for commands) is required to exit shutdown.

#### Serial-Interface

The MAX5174/MAX5176 3-wire serial interface is compatible with SPI and QSPI (Figure 2), and MICROWIRE (Figure 3) interface standards. The 16-bit serial input word consists of two control bits, 12 bits of data (MSB to LSB), and two sub-bits.

The control bits determine the MAX5174/MAX5176's response as outlined in Table 1. The MAX5174/MAX5176's digital inputs are double buffered, which allows any of the following:

- Loading the input register without updating the DAC register.
- Updating the DAC register from the input register.
- Updating the input and DAC registers simultaneously.

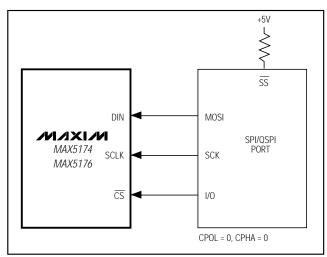


Figure 2. Connections for SPI and QSPI Standards

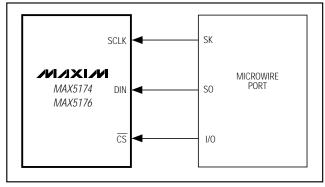


Figure 3. Connections for MICROWIRE

The MAX5174/MAX5176 accepts one 16-bit packet or two 8-bit packets sent while  $\overline{\text{CS}}$  remains low. The MAX5174/MAX5176 allow the following to be configured:

- Clock edge on which serial data output (DOUT) is clocked.
- State of the user-programmable logic output.
- · Configuration of the reset state.

Specific commands for setting these are shown in Table 1.

The general timing diagram in Figure 4 illustrates how the MAX5174/MAX5176 acquires data.  $\overline{\text{CS}}$  must go low at least t<sub>CSS</sub> before the rising edge of the serial clock (SCLK). With  $\overline{\text{CS}}$  low, data is clocked into the register on the rising edge of SCLK. The maximum serial clock frequency guaranteed for proper operation is 10MHz for the MAX5174 and 6MHz for the MAX5176. See Figure 5 for a detailed timing diagram of the serial interface.

#### Serial Data Output (DOUT)

The serial-data output (DOUT) is the internal shift register's output and allows for daisy-chaining of multiple devices as well as data readback (see *Applications Information*). By default upon start-up, data shifts out of DOUT on the serial clock's rising edge (Mode 0) and provides a lag of 16 clock cycles, thus maintaining SPI, QSPI, and MICROWIRE compatibility. However, if the device is programmed for Mode 1, then the output data lags DIN by 16.5 clock cycles and is clocked out on the serial clock's rising edge. During shutdown, DOUT retains its last digital state prior to shutdown.

**Table 1. Serial-Interface Programming Commands** 

		_	_	
	16-BIT SERIAL WORD		S1, S0	FUNCTION
C1	C0	D11D0	31, 30	FUNCTION
0	0	12-bit DAC data	0.0	Load input register; DAC registers are unchanged.
0	1	12-bit DAC data	0 0	Load input register; DAC registers are updated (start-up DAC with new data).
1	0	XXXXXXXXXXX	XX	Update DAC register from input register (start-up DAC with data previously stored in the input registers).
1	1	0 0 x x xxxx xxxx	XX	No operation (NOP).
1	1	0 1 x x xxxx xxxx	XX	Shut down DAC (provided PDL = 1).
1	1	1 0 0 x xxxx xxxx	XX	UPO goes low (default).
1	1	1 0 1 x xxxx xxxx	XX	UPO goes high.
1	1	1 1 0 x xxxx xxxx	XX	Mode 1, DOUT clocked out on SCLK's rising edge.
1	1	1 1 1 x xxxx xxxx	XX	Mode 0, DOUT clocked out on SCLK's falling edge (default).

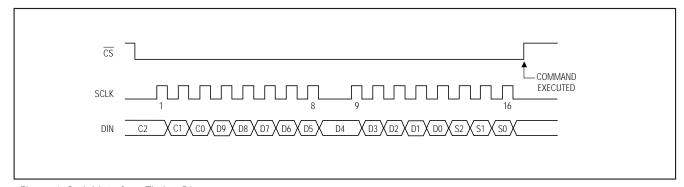


Figure 4. Serial-Interface Timing Diagram

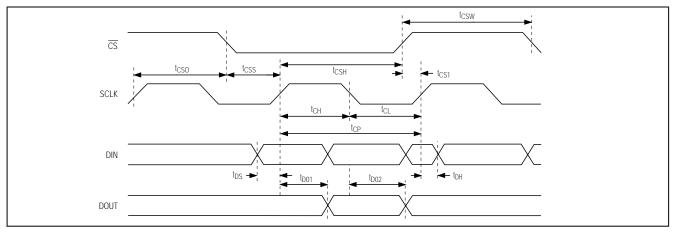


Figure 5. Detailed Serial-Interface Timing Diagram

User-Programmable Logic Output (UPO) The user-programmable logic output (UPO) allows control of an external device through the serial interface, thereby reducing the number of microcontroller I/O pins required. During power-down, this output will retain its digital state prior to shutdown. When CLR is pulled low, UPO will reset to its programmed default state. See Table 1 for specific commands to control the UPO.

Reset (RS) and Clear (CLR)

The MAX5174/MAX5176 offers a clear pin  $(\overline{CLR})$ , which resets the output voltage. If RS = DGND, then  $\overline{CLR}$  resets the output voltage to 0. If RS = V<sub>DD</sub>, then  $\overline{CLR}$  resets the output voltage to mid-scale. In either case,  $\overline{CLR}$  will reset UPO to its programmed default state.

### \_Applications Information

Unipolar Output

Figure 6 shows the MAX5174/MAX5176 configured for unipolar, rail-to-rail operation with a gain of 1.638V/V.

Table 2 lists the codes for unipolar output voltages. The output voltage is limited to V<sub>DD</sub>. Use the OS pin to introduce an offset voltage as shown in Figure 7 and described in the *Offset and Buffer Configurations* section.

Bipolar Output

Figure 8 shows the MAX5174/MAX5176 configured for bipolar output operation. The output voltage is given by the following equation (OS = AGND):

$$V_{OUT} = V_{REF} \left( \frac{2 \cdot N}{4096} - 1 \right)$$

where N represents the numeric value of the DAC's binary input code and  $V_{REF}$  is the voltage of the external reference. Table 3 shows digital codes and the corresponding output voltage for Figure 8's circuit.

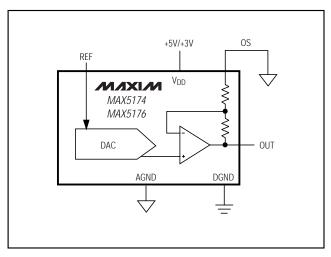


Figure 6. Unipolar Output Circuit (Rail-to-Rail)

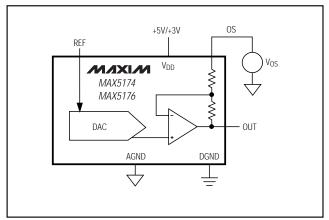


Figure 7. Setting OS for Output Offset

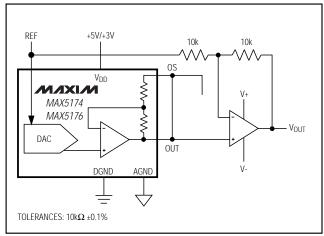


Figure 8. Bipolar Output Circuit

#### Offset and Buffer Configurations

The simple circuit of Figure 7 illustrates how to introduce an offset to the output voltage. The amount of offset introduced by a voltage at the OS pin is shown in the following equation:

Voffset = Vos • (1- Gain)

where Gain = 1.638.

However, the total output voltage of the device cannot exceed V<sub>DD</sub>, regardless of the voltage on the OS pin.

To set the gain of the output amplifier to 1, connect OS to OUT.

#### Daisy-Chaining Devices

The serial-data output pin (DOUT) allows multiple MAX5174/MAX5176s to be daisy-chained together as shown in Figure 9. The advantage of this is that only two lines are needed to control all the DACs. The disadvantage is that it takes *n* commands to program the DACs.

Figure 10 shows several MAX5174/MAX5176s sharing one common DIN signal line. In this configuration the data bus is common to all devices; however, more I/O lines are required because each device needs a dedicated  $\overline{CS}$  line. The advantage of this configuration is that only one command is needed to program any DAC.

### Table 2. Unipolar Code Table (Circuit of Figure 6)

`	•
DAC CONTENTS MSB LSB	ANALOG OUTPUT
11 1111 1111 11 (00)	+V <sub>REF</sub> (4095/4096) • 1.638
10 0000 0000 01 (00)	+V <sub>REF</sub> (2049/4096) • 1.638
10 0000 0000 00 (00)	+V <sub>REF</sub> (2048/4096) • 1.638
01 1111 1111 11 (00)	+V <sub>REF</sub> (2047/4096) • 1.638
00 0000 0000 01 (00)	+V <sub>REF</sub> (1/4096) • 1.638
00 0000 0000 00 (00)	0

### Table 3. Bipolar Code Table (Circuit of Figure 8)

`	,
DAC CONTENTS MSB LSB	ANALOG OUTPUT
11 1111 1111 11 (00)	+V <sub>REF</sub> [(2 · 4095/4096) - 1]
10 0000 0000 01 (00)	+V <sub>REF</sub> [(2 · 2049/4096) - 1]
10 0000 0000 00 (00)	+V <sub>REF</sub> [(2 · 2048/4096) - 1]
01 1111 1111 11 (00)	+V <sub>REF</sub> [(2 · 2047/4096) - 1]
00 0000 0000 01 (00)	+V <sub>REF</sub> [(2 · 1/4096) - 1]
00 0000 0000 00 00	-V <sub>REF</sub>

#### Using an AC Reference

The MAX5174/MAX5176 accept references with AC components, as long as the reference voltage remains between 0 and V<sub>DD</sub> - 1.4V. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must remain above AGND.

Power-Supply and Layout Considerations Wire-wrap boards are not recommended. For optimum system performance, use printed circuit boards with separate analog and digital ground planes. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND pins together at the IC. The best ground connection is achieved by connecting the DAC's DGND and AGND

pins together and connecting that point to the system analog ground plane. This is useful because if the DAC's DGND is connected to the system digital ground, digital noise may infiltrate the DAC's analog portion.

Bypass the power supply with a  $4.7\mu F$  capacitor in parallel with a  $0.1\mu F$  capacitor to AGND. Minimize capacitor lead lengths to reduce inductance. If noise becomes an issue, use shielding and/or ferrite beads to increase isolation.

To maintain INL and DNL performance as well as gain drift, it is extremely important to provide the lowest possible reference output impedance at the DAC reference input pin. INL degrades if the series resistance on REF pin exceeds  $0.1\Omega$ . The same consideration must be made for the AGND pin.

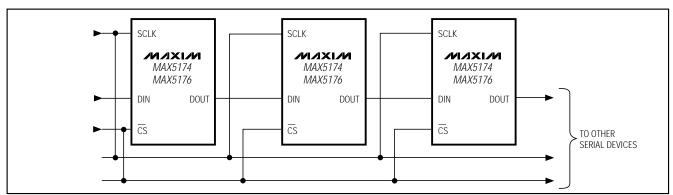


Figure 9. Daisy-Chaining MAX5174/MAX5175 Devices

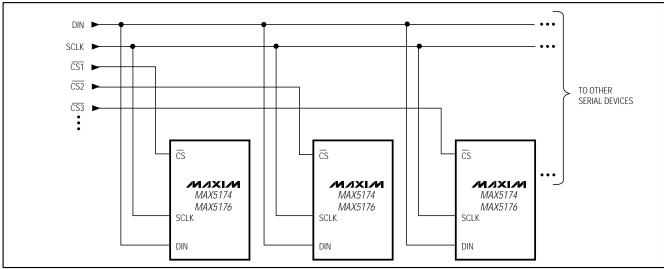


Figure 10. Multiple MAX5174/MAX5176s Sharing Common DIN and SCLK Lines

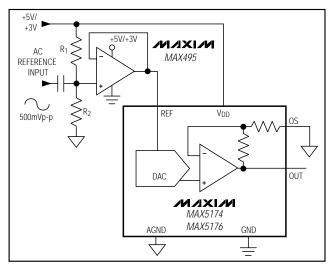
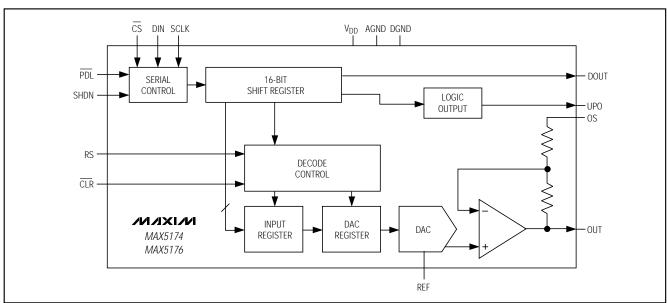


Figure 11. AC Reference Input Circuit

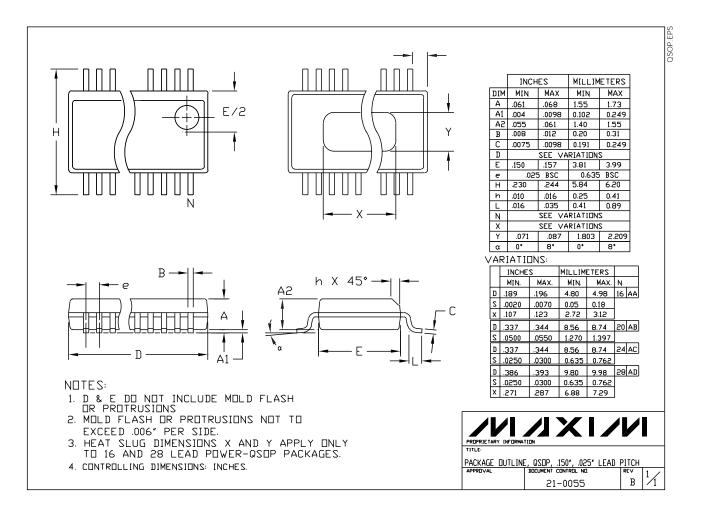
\_\_\_\_\_Chip Information

TRANSISTOR COUNT: 3457

### Functional Diagram



Package Information



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