



KSZ9021GN

Gigabit Ethernet Transceiver with GMII / MII Support

General Description

The KSZ9021GN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data on standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ9021GN provides the industry standard GMII/MII (Gigabit Media Independent Interface / Media Independent Interface) for connection to GMII/MII MACs in Gigabit Ethernet Processors and Switches for data transfer at 1000 Mbps or 10/100Mbps speed.

The KSZ9021GN reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

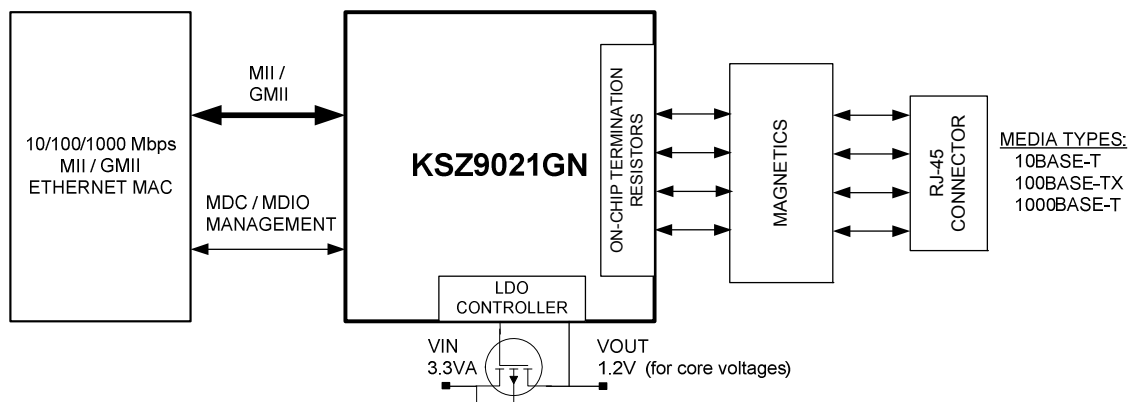
The KSZ9021GN provides diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9021 I/Os and board. Micrel LinkMD[®] TDR-based cable diagnostics permit identification of faulty copper cabling. Remote and local loopback functions provide verification of analog and digital data paths.

The KSZ9021GN is available in a 64-pin, lead-free QFN package (See Ordering Information).

Features

- Single-chip 10/100/1000Mbps IEEE 802.3 compliant Ethernet Transceiver
- GMII/MII standard compliant interface
- Auto-negotiation to automatically select the highest link up speed (10/100/100Mbps) and duplex (half/full)
- On-chip termination resistors for the differential pairs
- On-chip LDO controller to support single 3.3V supply operation – requires only external FET to generate 1.2V for the core
- Jumbo frame support up to 16KB
- 125MHz Reference Clock Output
- Programmable LED outputs for link, activity and speed
- Baseline Wander Correction
- LinkMD[®] TDR-based cable diagnostics for identification of faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and board.
- Loopback modes for diagnostics
- Automatic MDI/MDI-X crossover for detection and correction of pair swap at all speeds of operation

Functional Diagram



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More Features

- Automatic detection and correction of pair swaps, pair skew and pair polarity
- MDC/MDIO Management Interface for PHY register configuration
- Interrupt pin option
- Power down and power saving modes
- Operating Voltages
 - Core: 1.2V (external FET or regulator)
 - I/O: 3.3V or 2.5V
 - Transceiver: 3.3V
- Available in 64-pin QFN (8mm x 8mm) package

Applications

- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Gigabit LAN on Motherboard (GLOM)
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-top Box
- Game Console
- Triple-play (data, voice, video) Media Center
- Media Converter

Ordering Information

| Part Number | Temp. Range | Package | Lead Finish | Description |
|---------------------------|---------------|------------|-------------|------------------------------------|
| KSZ9021GN | 0°C to 70°C | 64-Pin QFN | Pb-Free | GMII / MII, Commercial Temperature |
| KSZ9021GNI ⁽¹⁾ | -40°C to 85°C | 64-Pin QFN | Pb-Free | GMII / MII, Industrial Temperature |

Note:

1. Contact factory for lead time.

Revision History

| Revision | Date | Summary of Changes |
|----------|----------|---|
| 1.0 | 10/13/09 | Data sheet created |
| 1.1 | 9/10/10 | Added industrial temperature part number KSZ9021GNI. Added support for 2.5V VDD I/O. Added LED drive current. Corrected GMII receive timing for t_{su} . Updated KSZ9021GN pin outs throughout data sheet to reflect pin out changes for silicon revision A3. Updated boilerplate. |

Contents

| | |
|--|-----------|
| Pin Configuration | 8 |
| Pin Description | 9 |
| Strapping Options | 14 |
| Functional Overview | 15 |
| Functional Description: 10Base-T/100Base-TX Transceiver | 16 |
| 100Base-TX Transmit | 16 |
| 100Base-TX Receive | 16 |
| Scrambler/De-scrambler (100Base-TX only) | 16 |
| 10Base-T Transmit | 16 |
| 10Base-T Receive | 16 |
| Functional Description: 1000Base-T Transceiver | 17 |
| Analog Echo Cancellation Circuit | 17 |
| Automatic Gain Control (AGC) | 17 |
| Analog-to-Digital Converter (ADC) | 17 |
| Timing Recovery Circuit | 18 |
| Adaptive Equalizer | 18 |
| Trellis Encoder and Decoder | 18 |
| Functional Description: Additional 10/100/1000 PHY Features | 18 |
| Auto MDI/MDI-X | 18 |
| Pair- Swap, Alignment, and Polarity Check | 19 |
| Wave Shaping, Slew Rate Control and Partial Response | 19 |
| PLL Clock Synthesizer | 19 |
| Auto-Negotiation | 19 |
| GMII Interface | 21 |
| GMII Signal Definition | 22 |
| GMII Signal Diagram | 22 |
| MII Interface | 23 |
| MII Signal Definition | 24 |
| MII Signal Diagram | 24 |
| MII Management (MIIM) Interface | 25 |
| Interrupt (INT_N) | 25 |
| LED Mode | 25 |
| Single LED Mode | 26 |
| Tri-color Dual LED Mode | 26 |
| NAND Tree Support | 27 |
| Power Management | 28 |
| Power Saving Mode | 28 |
| Software Power Down Mode | 28 |
| Chip Power Down Mode | 28 |
| Register Map | 29 |
| Register Description | 30 |
| IEEE Defined Registers | 30 |
| Vendor Specific Registers | 36 |
| Extended Registers | 39 |

| | |
|---|-----------|
| Absolute Maximum Ratings | 41 |
| Operating Ratings | 41 |
| Electrical Characteristics | 41 |
| Timing Diagrams | 44 |
| GMII Transmit Timing..... | 44 |
| GMII Receive Timing..... | 45 |
| MII Transmit Timing..... | 46 |
| MII Receive Timing..... | 47 |
| Auto-Negotiation Timing..... | 48 |
| MDC/MDIO Timing..... | 49 |
| Reset Timing..... | 50 |
| Reset Circuit | 50 |
| Reference Circuits – LED Strap-in Pins | 51 |
| Reference Clock – Connection and Selection | 52 |
| Magnetics Specification | 52 |
| Package Information | 53 |

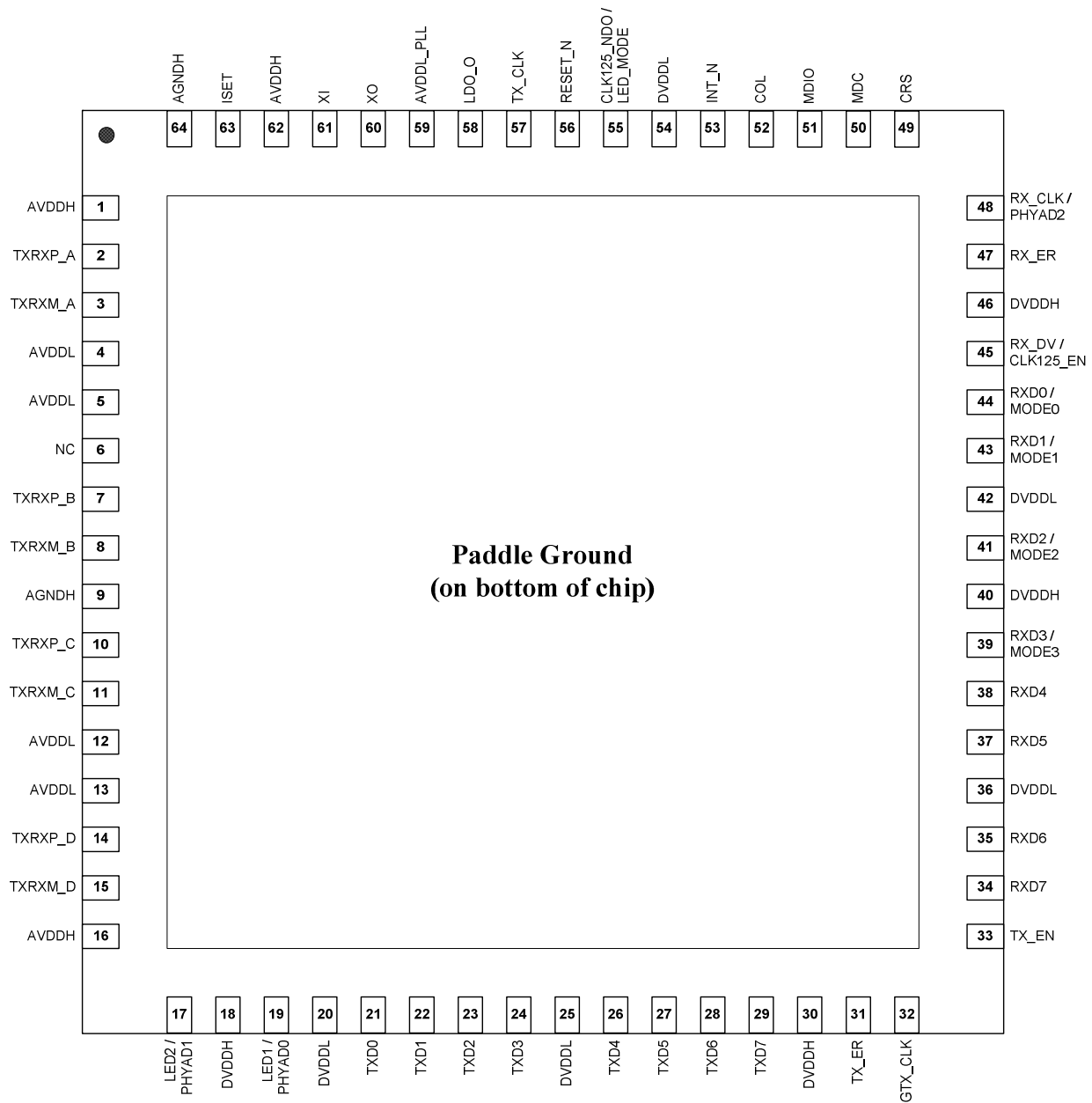
List of Figures

| | |
|---|----|
| Figure 1. KSZ9021GN Block Diagram | 15 |
| Figure 2. KSZ9021GN 1000Base-T Block Diagram – Single Channel..... | 17 |
| Figure 3. Auto-Negotiation Flow Chart..... | 20 |
| Figure 4. KSZ9021GN GMII Interface..... | 22 |
| Figure 5. KSZ9021GN MII Interface | 24 |
| Figure 6. GMII Transmit Timing – Data Input to PHY | 44 |
| Figure 7. GMII Receive Timing – Data Input to MAC | 45 |
| Figure 8. MII Transmit Timing – Data Input to PHY | 46 |
| Figure 9. MII Receive Timing – Data Input to MAC | 47 |
| Figure 10. Auto-Negotiation Fast Link Pulse (FLP) Timing | 48 |
| Figure 11. MDC/MDIO Timing..... | 49 |
| Figure 12. Reset Timing..... | 50 |
| Figure 13. Recommended Reset Circuit..... | 50 |
| Figure 14. Recommended Reset Circuit for Interfacing with CPU/FPGA Reset Output. | 51 |
| Figure 15. Reference Circuits for LED Strapping Pins..... | 51 |
| Figure 16. 25MHz Crystal / Oscillator Reference Clock Connection | 52 |

List of Tables

| | |
|--|----|
| Table 1. MDI / MDI-X Pin Mapping | 18 |
| Table 2. Auto-Negotiation Timers | 21 |
| Table 3. GMII Signal Definition | 22 |
| Table 4. MII Signal Definition | 24 |
| Table 5. MII Management Frame Format – for KSZ9021GN | 25 |
| Table 6: Single LED Mode – Pin Definition | 26 |
| Table 7: Tri-color Dual LED Mode – Pin Definition | 26 |
| Table 8. NAND Tree Test Pin Order – for KSZ9021GN | 27 |
| Table 9. GMII Transmit Timing Parameters | 44 |
| Table 10. GMII Receive Timing Parameters | 45 |
| Table 11. MII Transmit Timing Parameters | 46 |
| Table 12. MII Receive Timing Parameters | 47 |
| Table 13. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters | 48 |
| Table 14. MDC/MDIO Timing Parameters | 49 |
| Table 15. Reset Timing Parameters | 50 |
| Table 16. Reference Crystal/Clock Selection Criteria | 52 |
| Table 17. Magnetics Selection Criteria | 52 |
| Table 18. Qualified Single Port 10/100/1000 Magnetics | 52 |

Pin Configuration



**64-Pin QFN
(Top View)**

Pin Description

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|----------|---------------------|--|
| 1 | AVDDH | P | 3.3V analog V _{DD} |
| 2 | TXRXP_A | I/O | Media Dependent Interface[0], positive signal of differential pair 1000Base-T Mode: TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively. |
| 3 | TXRXM_A | I/O | Media Dependent Interface[0], negative signal of differential pair 1000Base-T Mode: TXRXM_A corresponds to BI_DA- for MDI configuration and BI_DB- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_A is the negative transmit signal (TX-) for MDI configuration and the negative receive signal (RX-) for MDI-X configuration, respectively. |
| 4 | AVDDL | P | 1.2V analog V _{DD} |
| 5 | AVDDL | P | 1.2V analog V _{DD} |
| 6 | NC | - | No connect |
| 7 | TXRXP_B | I/O | Media Dependent Interface[1], positive signal of differential pair 1000Base-T Mode: TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively. |
| 8 | TXRXM_B | I/O | Media Dependent Interface[1], negative signal of differential pair 1000Base-T Mode: TXRXM_B corresponds to BI_DB- for MDI configuration and BI_DA- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_B is the negative receive signal (RX-) for MDI configuration and the negative transmit signal (TX-) for MDI-X configuration, respectively. |
| 9 | AGNDH | Gnd | Analog ground |
| 10 | TXRXP_C | I/O | Media Dependent Interface[2], positive signal of differential pair 1000Base-T Mode: TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_C is not used. |
| 11 | TXRXM_C | I/O | Media Dependent Interface[2], negative signal of differential pair 1000Base-T Mode: TXRXM_C corresponds to BI_DC- for MDI configuration and BI_DD- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_C is not used. |

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------------|------------------|---------------------|--|----------|-----------|----------------|----------|---|-----|---------------------|---|----|-----------------|-----------|--|----------------|--|------|------|------|------|----------|---|---|-----|-----|-------------------------|---|---|----|-----|-------------------------------|--------|---|----------|-----|------------------------|---|---|-----|----|------------------------------|---|--------|-----|----------|-----------------------|---|---|----|----|-----------------------------|--------|--------|----------|----------|
| 12 | AVDDL | P | 1.2V analog V _{DD} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13 | AVDDL | P | 1.2V analog V _{DD} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | TXRXP_D | I/O | Media Dependent Interface[3], positive signal of differential pair 1000Base-T Mode: TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXP_D is not used. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 15 | TXRXM_D | I/O | Media Dependent Interface[3], negative signal of differential pair 1000Base-T Mode: TXRXM_D corresponds to BI_DD- for MDI configuration and BI_DC- for MDI-X configuration, respectively. 10Base-T / 100Base-TX Mode: TXRXM_D is not used. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | AVDDH | P | 3.3V analog V _{DD} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 17 | LED2 / PHYAD1 | I/O | LED Output: Programmable LED2 Output / Config Mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up / reset. See "Strapping Options" section for details. The LED2 pin is programmed by the LED_MODE strapping option (pin 55, and is defined as follows. Single LED Mode <table border="1"> <thead> <tr> <th>Link</th> <th>Pin State</th> <th>LED Definition</th> </tr> </thead> <tbody> <tr> <td>Link off</td> <td>H</td> <td>OFF</td> </tr> <tr> <td>Link on (any speed)</td> <td>L</td> <td>ON</td> </tr> </tbody> </table> Tri-color Dual LED Mode <table border="1"> <thead> <tr> <th rowspan="2">Link / Activity</th> <th colspan="2">Pin State</th> <th colspan="2">LED Definition</th> </tr> <tr> <th>LED2</th> <th>LED1</th> <th>LED2</th> <th>LED1</th> </tr> </thead> <tbody> <tr> <td>Link off</td> <td>H</td> <td>H</td> <td>OFF</td> <td>OFF</td> </tr> <tr> <td>1000 Link / No Activity</td> <td>L</td> <td>H</td> <td>ON</td> <td>OFF</td> </tr> <tr> <td>1000 Link / Activity (RX, TX)</td> <td>Toggle</td> <td>H</td> <td>Blinking</td> <td>OFF</td> </tr> <tr> <td>100 Link / No Activity</td> <td>H</td> <td>L</td> <td>OFF</td> <td>ON</td> </tr> <tr> <td>100 Link / Activity (RX, TX)</td> <td>H</td> <td>Toggle</td> <td>OFF</td> <td>Blinking</td> </tr> <tr> <td>10 Link / No Activity</td> <td>L</td> <td>L</td> <td>ON</td> <td>ON</td> </tr> <tr> <td>10 Link / Activity (RX, TX)</td> <td>Toggle</td> <td>Toggle</td> <td>Blinking</td> <td>Blinking</td> </tr> </tbody> </table> For Tri-color Dual LED Mode, LED2 works in conjunction with LED1 (pin 19 to indicate 10 Mbps Link and Activity. | Link | Pin State | LED Definition | Link off | H | OFF | Link on (any speed) | L | ON | Link / Activity | Pin State | | LED Definition | | LED2 | LED1 | LED2 | LED1 | Link off | H | H | OFF | OFF | 1000 Link / No Activity | L | H | ON | OFF | 1000 Link / Activity (RX, TX) | Toggle | H | Blinking | OFF | 100 Link / No Activity | H | L | OFF | ON | 100 Link / Activity (RX, TX) | H | Toggle | OFF | Blinking | 10 Link / No Activity | L | L | ON | ON | 10 Link / Activity (RX, TX) | Toggle | Toggle | Blinking | Blinking |
| Link | Pin State | LED Definition | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Link off | H | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Link on (any speed) | L | ON | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Link / Activity | Pin State | | LED Definition | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | LED2 | LED1 | LED2 | LED1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Link off | H | H | OFF | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 Link / No Activity | L | H | ON | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 Link / Activity (RX, TX) | Toggle | H | Blinking | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 Link / No Activity | H | L | OFF | ON | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 Link / Activity (RX, TX) | H | Toggle | OFF | Blinking | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 Link / No Activity | L | L | ON | ON | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 Link / Activity (RX, TX) | Toggle | Toggle | Blinking | Blinking | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 18 | DVDDH | P | 3.3V or 2.5V digital V _{DD} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 19 | LED1 / PHYAD0 | I/O | LED Output: Programmable LED1 Output / Config Mode: The pull-up/pull-down value is latched as PHYAD[0] during power-up / reset. See "Strapping Options" section for details. The LED1 pin is programmed by the LED_MODE strapping option (pin 55, and is defined as follows. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------------|-----------|---------------------|---|----------|-----------|----------------|-------------|---|-----|-------------------|--------|----------|-----------------|-----------|--|----------------|--|------|------|------|------|----------|---|---|-----|-----|-------------------------|---|---|----|-----|-------------------------------|--------|---|----------|-----|------------------------|---|---|-----|----|------------------------------|---|--------|-----|----------|-----------------------|---|---|----|----|-----------------------------|--------|--------|----------|----------|
| | | | <p>Single LED Mode</p> <table border="1"> <thead> <tr> <th>Activity</th> <th>Pin State</th> <th>LED Definition</th> </tr> </thead> <tbody> <tr> <td>No Activity</td> <td>H</td> <td>OFF</td> </tr> <tr> <td>Activity (RX, TX)</td> <td>Toggle</td> <td>Blinking</td> </tr> </tbody> </table> <p>Tri-color Dual LED Mode</p> <table border="1"> <thead> <tr> <th rowspan="2">Link / Activity</th> <th colspan="2">Pin State</th> <th colspan="2">LED Definition</th> </tr> <tr> <th>LED2</th> <th>LED1</th> <th>LED2</th> <th>LED1</th> </tr> </thead> <tbody> <tr> <td>Link off</td> <td>H</td> <td>H</td> <td>OFF</td> <td>OFF</td> </tr> <tr> <td>1000 Link / No Activity</td> <td>L</td> <td>H</td> <td>ON</td> <td>OFF</td> </tr> <tr> <td>1000 Link / Activity (RX, TX)</td> <td>Toggle</td> <td>H</td> <td>Blinking</td> <td>OFF</td> </tr> <tr> <td>100 Link / No Activity</td> <td>H</td> <td>L</td> <td>OFF</td> <td>ON</td> </tr> <tr> <td>100 Link / Activity (RX, TX)</td> <td>H</td> <td>Toggle</td> <td>OFF</td> <td>Blinking</td> </tr> <tr> <td>10 Link / No Activity</td> <td>L</td> <td>L</td> <td>ON</td> <td>ON</td> </tr> <tr> <td>10 Link / Activity (RX, TX)</td> <td>Toggle</td> <td>Toggle</td> <td>Blinking</td> <td>Blinking</td> </tr> </tbody> </table> <p>For Tri-color Dual LED Mode, LED1 works in conjunction with LED2 (pin 17 to indicate 10 Mbps Link and Activity.</p> | Activity | Pin State | LED Definition | No Activity | H | OFF | Activity (RX, TX) | Toggle | Blinking | Link / Activity | Pin State | | LED Definition | | LED2 | LED1 | LED2 | LED1 | Link off | H | H | OFF | OFF | 1000 Link / No Activity | L | H | ON | OFF | 1000 Link / Activity (RX, TX) | Toggle | H | Blinking | OFF | 100 Link / No Activity | H | L | OFF | ON | 100 Link / Activity (RX, TX) | H | Toggle | OFF | Blinking | 10 Link / No Activity | L | L | ON | ON | 10 Link / Activity (RX, TX) | Toggle | Toggle | Blinking | Blinking |
| Activity | Pin State | LED Definition | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| No Activity | H | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Activity (RX, TX) | Toggle | Blinking | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Link / Activity | Pin State | | LED Definition | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | LED2 | LED1 | LED2 | LED1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Link off | H | H | OFF | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 Link / No Activity | L | H | ON | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 Link / Activity (RX, TX) | Toggle | H | Blinking | OFF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 Link / No Activity | H | L | OFF | ON | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 Link / Activity (RX, TX) | H | Toggle | OFF | Blinking | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 Link / No Activity | L | L | ON | ON | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 Link / Activity (RX, TX) | Toggle | Toggle | Blinking | Blinking | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 20 | DVDDL | P | 1.2V digital V _{DD} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 21 | TXD0 | I | GMII Mode: GMII TXD0 (Transmit Data 0) Input MII Mode: MII TXD0 (Transmit Data 0) Input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 22 | TXD1 | I | GMII Mode: GMII TXD1 (Transmit Data 1) Input MII Mode: MII TXD1 (Transmit Data 1) Input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 23 | TXD2 | I | GMII Mode: GMII TXD2 (Transmit Data 2) Input MII Mode: MII TXD2 (Transmit Data 2) Input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 24 | TXD3 | I | GMII Mode: GMII TXD3 (Transmit Data 3) Input MII Mode: MII TXD3 (Transmit Data 3) Input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 25 | DVDDL | P | 1.2V digital V _{DD} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 26 | TXD4 | I | GMII Mode: GMII TXD4 (Transmit Data 4) Input MII Mode: This pin is not used and can be driven high or low. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 27 | TXD5 | I | GMII Mode: GMII TXD5 (Transmit Data 5) Input MII Mode: This pin is not used and can be driven high or low. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 28 | TXD6 | I | GMII Mode: GMII TXD6 (Transmit Data 6) Input MII Mode: This pin is not used and can be driven high or low. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 29 | TXD7 | I | GMII Mode: GMII TXD7 (Transmit Data 7) Input MII Mode: This pin is not used and can be driven high or low. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 30 | DVDDH | P | 3.3V or 2.5V digital V _{DD} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | TX_ER | I | GMII Mode: GMII TX_ER (Transmit Error) Input MII Mode: MII TX_ER (Transmit Error) Input If GMII / MII MAC does not provide the TX_ER output signal, this pin should be tied low. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 32 | GTX_CLK | I | GMII Mode: GMII GTX_CLK (Transmit Reference Clock) Input | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|----------------------|---------------------|---|
| 33 | TX_EN | I | GMII Mode: GMII TX_EN (Transmit Enable) Input MII Mode: MII TX_EN (Transmit Enable) Input |
| 34 | RXD7 | O | GMII Mode: GMII RXD7 (Receive Data 7) Output MII Mode: This pin is not used and is driven low. |
| 35 | RXD6 | O | GMII Mode: GMII RXD6 (Receive Data 6) Output MII Mode: This pin is not used and is driven low. |
| 36 | DVDDL | P | 1.2V digital V _{DD} |
| 37 | RXD5 | O | GMII Mode: GMII RXD5 (Receive Data 5) Output MII Mode: This pin is not used and is driven low. |
| 38 | RXD4 | O | GMII Mode: GMII RXD4 (Receive Data 4) Output MII Mode: This pin is not used and is driven low. |
| 39 | RXD3 / MODE3 | I/O | GMII Mode: GMII RXD3 (Receive Data 3) Output MII Mode: MII RXD3 (Receive Data 3) Output / Config Mode: The pull-up/pull-down value is latched as MODE3 during power-up / reset. See "Strapping Options" section for details. |
| 40 | DVDDH | P | 3.3V or 2.5V digital V _{DD} |
| 41 | RXD2 / MODE2 | I/O | GMII Mode: GMII RXD2 (Receive Data 2) Output MII Mode: MII RXD2 (Receive Data 2) Output / Config Mode: The pull-up/pull-down value is latched as MODE2 during power-up / reset. See "Strapping Options" section for details. |
| 42 | DVDDL | P | 1.2V digital V _{DD} |
| 43 | RXD1 / MODE1 | I/O | GMII Mode: GMII RXD1 (Receive Data 1) Output MII Mode: MII RXD1 (Receive Data 1) Output / Config Mode: The pull-up/pull-down value is latched as MODE1 during power-up / reset. See "Strapping Options" section for details. |
| 44 | RXD0 / MODE0 | I/O | GMII Mode: GMII RXD0 (Receive Data 0) Output MII Mode: MII RXD0 (Receive Data 0) Output / Config Mode: The pull-up/pull-down value is latched as MODE0 during power-up / reset. See "Strapping Options" section for details. |
| 45 | RX_DV / CLK125_EN | I/O | GMII Mode: GMII RX_DV (Receive Data Valid) Output MII Mode: MII RX_DV (Receive Data Valid) Output / Config Mode: Latched as CLK125_NDO Output Enable during power-up / reset. See "Strapping Options" section for details. |
| 46 | DVDDH | P | 3.3V or 2.5V digital V _{DD} |
| 47 | RX_ER | O | GMII Mode: GMII RX_ER (Receive Error) Output MII Mode: MII RX_ER (Receive Error) Output |
| 48 | RX_CLK / PHYAD2 | I/O | GMII Mode: GMII RX_CLK (Receive Reference Clock) Output MII Mode: MII RX_CLK (Receive Reference Clock) Output / Config Mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up / reset. See "Strapping Options" section for details. |
| 49 | CRS | O | GMII Mode: GMII CRS (Carrier Sense) Output MII Mode: MII CRS (Carrier Sense) Output |
| 50 | MDC | Ipu | Management Data Clock Input This pin is the input reference clock for MDIO (pin 51) |

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function |
|------------|--------------------------|---------------------|---|
| 51 | MDIO | Ipu/O | Management Data Input / Output This pin is synchronous to MDC (pin 50) and requires an external pull-up resistor to DVDDH (digital V _{DD}) in a range from 1.0KΩ to 4.7KΩ. |
| 52 | COL | O | GMII Mode: GMII COL (Collision Detected) Output MII Mode: MII COL (Collision Detected) Output |
| 53 | INT_N | O | Interrupt Output This pin provides a programmable interrupt output and requires an external pull-up resistor to DVDDH (digital V _{DD}) in a range from 1.0KΩ to 4.7KΩ when active low. Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 14 sets the interrupt output to active low (default) or active high. |
| 54 | DVDDL | P | 1.2V digital V _{DD} |
| 55 | CLK125_NDO / LED_MODE | I/O | 125MHz Clock Output This pin provides a 125MHz reference clock output option for use by the MAC. / Config Mode: The pull-up/pull-down value is latched as LED_MODE during power-up / reset. See "Strapping Options" section for details. |
| 56 | RESET_N | Ipu | Chip Reset (active low) Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See "Strapping Options" section for more details. |
| 57 | TX_CLK | O | MII Mode: MII TX_CLK (Transmit Reference Clock) Output |
| 58 | LDO_O | O | On-chip 1.2V LDO Controller Output This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip's core voltages. If 1.2V is provided by the system and this pin is not used, it can be left floating. |
| 59 | AVDDL_PLL | P | 1.2V analog V _{DD} for PLL |
| 60 | XO | O | 25MHz Crystal feedback This pin is a no connect if oscillator or external clock source is used. |
| 61 | XI | I | Crystal / Oscillator / External Clock Input 25MHz +/-50ppm tolerance |
| 62 | AVDDH | P | 3.3V analog V _{DD} |
| 63 | ISET | I/O | Set transmit output level Connect a 4.99KΩ 1% resistor to ground on this pin. |
| 64 | AGNDH | Gnd | Analog ground |
| PADDLE | P_GND | Gnd | Exposed Paddle on bottom of chip Connect P_GND to ground. |

Note:

1. P = Power supply.
Gnd = Ground.
I = Input.
O = Output.
I/O = Bi-directional.
Ipu = Input with internal pull-up.
Ipu/O = Input with internal pull-up / Output.

Strapping Options

| Pin Number | Pin Name | Type ⁽¹⁾ | Pin Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----------------------------------|--------------------------|--|-----------|------|------|---------------------|------|-----------------|------|---------------------|------|---------------------|------|----------------|------|---------------------|------|---------------------|------|----------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|
| 48 17 19 | PHYAD2 PHYAD1 PHYAD0 | I/O I/O I/O | <p>The PHY Address, PHYAD[2:0], is latched at power-up / reset and is configurable to any value from 1 to 7. Each PHY address bit is configured as follows:</p> <p style="padding-left: 40px;">Pull-up = 1 Pull-down = 0</p> <p>PHY Address bits [4:3] are always set to '00'.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 39 41 43 44 | MODE3 MODE2 MODE1 MODE0 | I/O I/O I/O I/O | <p>The MODE[3:0] strap-in pins are latched at power-up / reset and are defined as follows:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>MODE[3:0]</th> <th>Mode</th> </tr> </thead> <tbody> <tr><td>0000</td><td>Reserved – not used</td></tr> <tr><td>0001</td><td>GMII / MII Mode</td></tr> <tr><td>0010</td><td>Reserved – not used</td></tr> <tr><td>0011</td><td>Reserved – not used</td></tr> <tr><td>0100</td><td>NAND Tree Mode</td></tr> <tr><td>0101</td><td>Reserved – not used</td></tr> <tr><td>0110</td><td>Reserved – not used</td></tr> <tr><td>0111</td><td>Chip Power Down Mode</td></tr> <tr><td>1000</td><td>Reserved – not used</td></tr> <tr><td>1001</td><td>Reserved – not used</td></tr> <tr><td>1010</td><td>Reserved – not used</td></tr> <tr><td>1011</td><td>Reserved – not used</td></tr> <tr><td>1100</td><td>Reserved – not used</td></tr> <tr><td>1101</td><td>Reserved – not used</td></tr> <tr><td>1110</td><td>Reserved – not used</td></tr> <tr><td>1111</td><td>Reserved – not used</td></tr> </tbody> </table> | MODE[3:0] | Mode | 0000 | Reserved – not used | 0001 | GMII / MII Mode | 0010 | Reserved – not used | 0011 | Reserved – not used | 0100 | NAND Tree Mode | 0101 | Reserved – not used | 0110 | Reserved – not used | 0111 | Chip Power Down Mode | 1000 | Reserved – not used | 1001 | Reserved – not used | 1010 | Reserved – not used | 1011 | Reserved – not used | 1100 | Reserved – not used | 1101 | Reserved – not used | 1110 | Reserved – not used | 1111 | Reserved – not used |
| MODE[3:0] | Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001 | GMII / MII Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0010 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0011 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0100 | NAND Tree Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0110 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 | Chip Power Down Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1001 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1010 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1011 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1100 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1101 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1110 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1111 | Reserved – not used | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 45 | CLK125_EN | I/O | <p>CLK125_EN is latched at power-up / reset and is defined as follows:</p> <p style="padding-left: 40px;">Pull-up = Enable 125MHz Clock Output Pull-down = Disable 125MHz Clock Output</p> <p>Pin 55 (CLK125_NDO) provides the 125MHz reference clock output option for use by the MAC.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 55 | LED_MODE | I/O | <p>LED_MODE is latched at power-up / reset and is defined as follows:</p> <p style="padding-left: 40px;">Pull-up = Single LED Mode Pull-down = Tri-color Dual LED Mode</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note:

1. I/O = Bi-directional.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the GMII/MII signals to be latched to the incorrect configuration. In this case, it is recommended to add external pull-ups/pull-downs on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

Functional Overview

The KSZ9021GN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable. Its on-chip proprietary 1000Base-T transceiver and Manchester/MLT-3 signaling-based 10Base-T/100Base-TX transceivers are all IEEE 802.3 compliant.

The KSZ9021GN reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9021GN can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

The KSZ9021GN provides the GMII/MII interface for connection to GMACs in Gigabit Ethernet Processors and Switches for data transfer at 10/100/1000 Mbps speed.

The following figure shows a high-level block diagram of the KSZ9021GN.

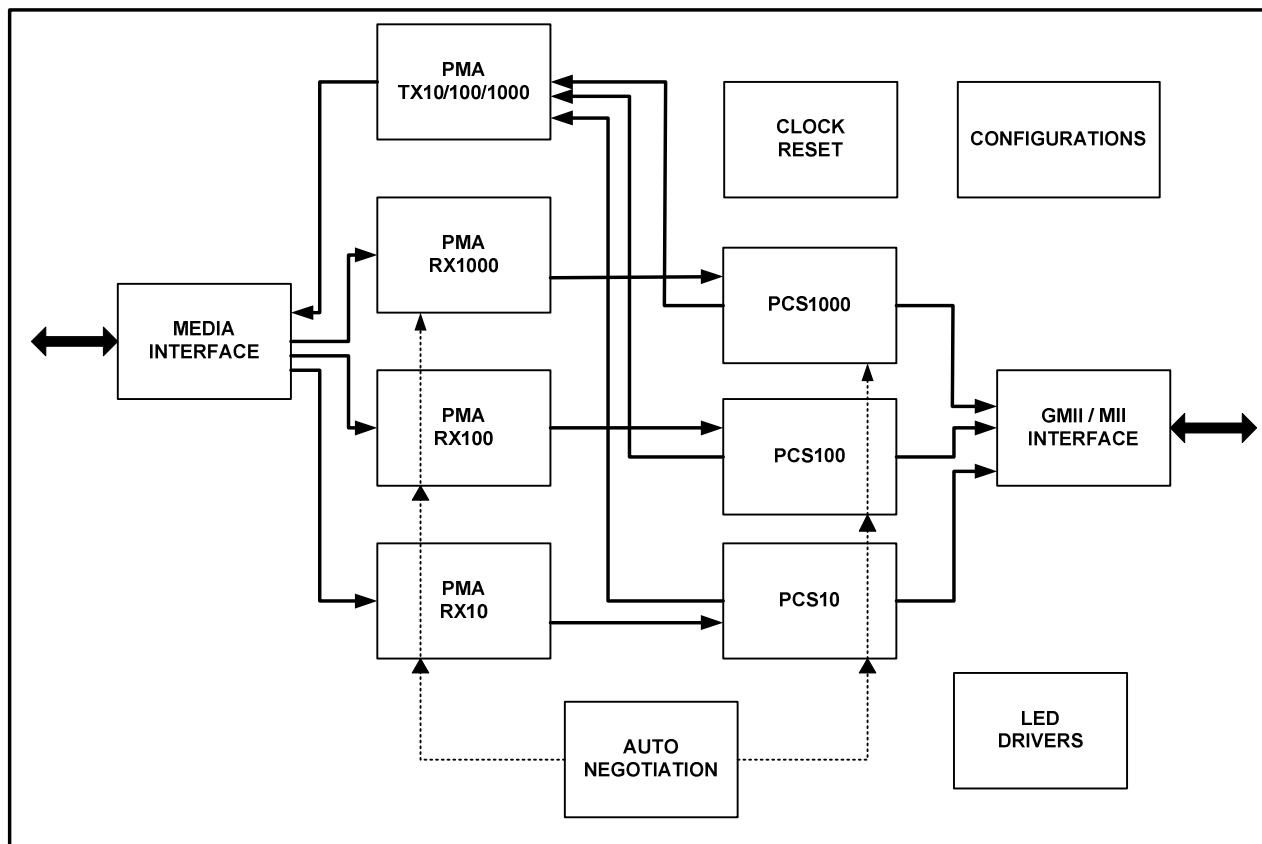


Figure 1. KSZ9021GN Block Diagram

Functional Description: 10Base-T/100Base-TX Transceiver

100Base-TX Transmit

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 4.99K Ω 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the GMII/MII format and provided as the input data to the MAC.

Scrambler/De-scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, and the receiver then de-scrambles the incoming data stream using the same sequence as at the transmitter.

10Base-T Transmit

The output 10Base-T driver is incorporated into the 100Base-TX driver to allow transmission with the same magnetic. They are internally wave-shaped and pre-emphasized into typical outputs of 2.5V amplitude. The harmonic contents are at least 31 dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths in order to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9021GN decodes a data frame. The receiver clock is maintained active during idle periods in between receiving data frames.

Timing Recovery Circuit

In 1000Base-T mode, the mixed-signal clock recovery circuit together with the digital phase locked loop is used to recover and track the incoming timing information from the received data. The digital phase locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000Base-T slave PHY is required to transmit the exact receive clock frequency recovered from the received data back to the 1000Base-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. Additionally, this helps to facilitate echo cancellation and NEXT removal.

Adaptive Equalizer

In 1000Base-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid and echo due to impedance mismatch. The KSZ9021GN employs a digital echo canceller to further reduce echo components on the receive signal.

In 1000Base-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high frequency cross-talk coming from adjacent wires. The KSZ9021GN employs three NEXT cancellers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10Base-T/100Base-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

Trellis Encoder and Decoder

In 1000Base-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9021GN are used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order and polarity have to be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and then de-scrambled into 8-bit data.

Functional Description: Additional 10/100/1000 PHY Features

Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9021GN and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and then assigns the MDI/MDI-X pair mapping of the KSZ9021GN accordingly.

The following table shows the KSZ9021GN 10/100/1000 pin-out assignments for MDI/MDI-X pin mapping.

| Pin (RJ-45 pair) | MDI | | | MDI-X | | |
|------------------|------------|------------|----------|------------|------------|----------|
| | 1000Base-T | 100Base-TX | 10Base-T | 1000Base-T | 100Base-TX | 10Base-T |
| TXRXP/M_A (1,2) | A+/- | TX+/- | TX+/- | B+/- | RX+/- | RX+/- |
| TXRXP/M_B (3,6) | B+/- | RX+/- | RX+/- | A+/- | TX+/- | TX+/- |
| TXRXP/M_C (4,5) | C+/- | Not used | Not used | D+/- | Not used | Not used |
| TXRXP/M_D (7,8) | D+/- | Not used | Not used | C+/- | Not used | Not used |

Table 1. MDI / MDI-X Pin Mapping

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to register 28 (1Ch) bit 6. MDI and MDI-X mode is set by register 28 (1Ch) bit 7 if auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X.

Pair- Swap, Alignment, and Polarity Check

In 1000Base-T mode, the KSZ9021GN

- Detects incorrect channel order and automatically restore the pair order for the A, B, C, D pairs (four channels)
- Supports 50 ± 10 ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

Wave Shaping, Slew Rate Control and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000Base-T, a special partial response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100Base-TX, a simple slew rate control method is used to minimize EMI.
- For 10Base-T, pre-emphasis is used to extend the signal quality through the cable.

PLL Clock Synthesizer

The KSZ9021GN generates 125MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from the external 25 MHz crystal or reference clock.

Auto-Negotiation

The KSZ9021GN conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (Unshielded Twisted Pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 1000Base-T, full-duplex
- Priority 2: 1000Base-T, half-duplex
- Priority 3: 100Base-TX, full-duplex
- Priority 4: 100Base-TX, half-duplex
- Priority 5: 10Base-T, full-duplex
- Priority 6: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ9021GN link partner is forced to bypass auto-negotiation for 10Base-T and 100Base-TX modes, then the KSZ9021GN sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9021GN to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link up process is shown in the following flow chart.

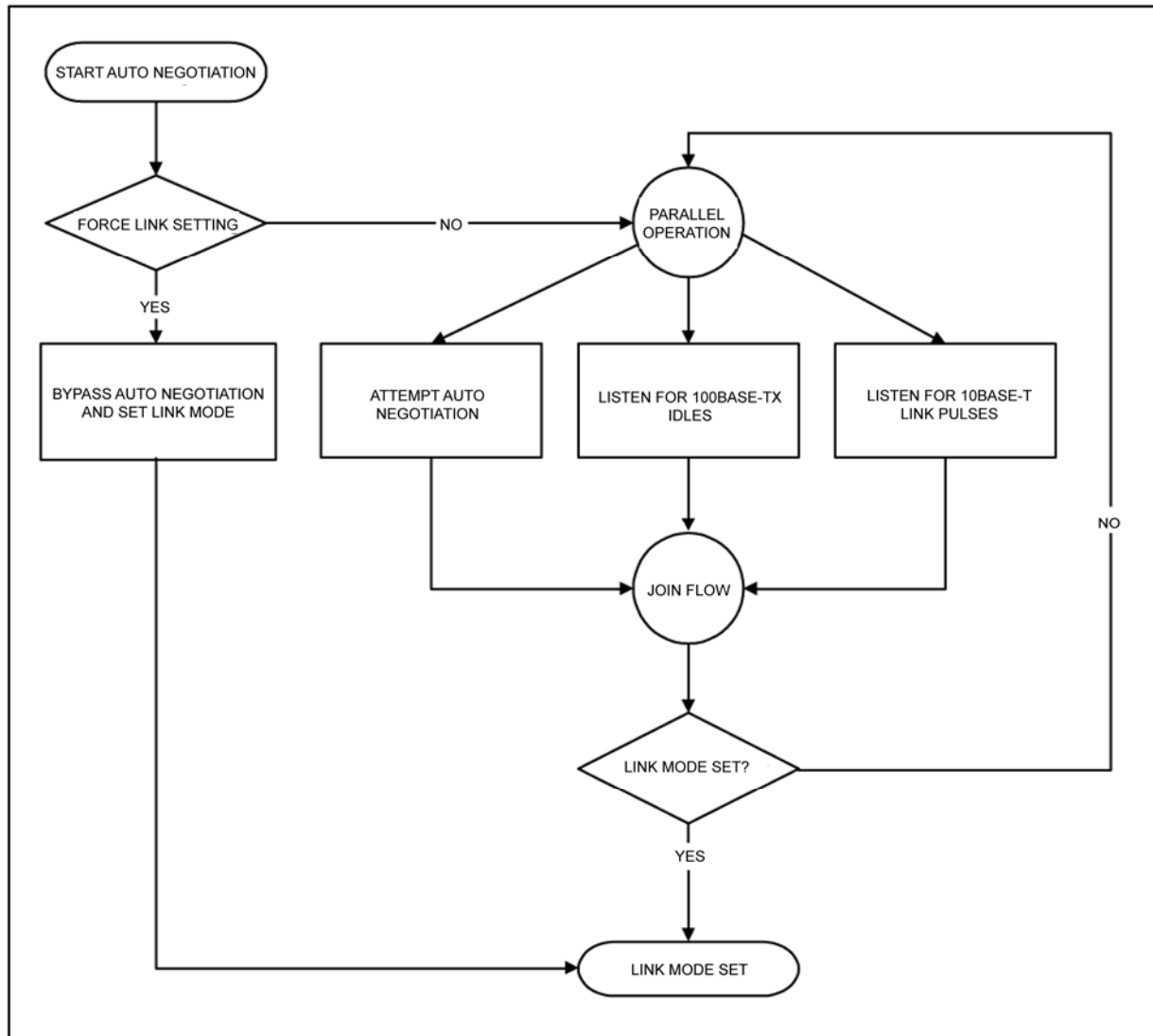


Figure 3. Auto-Negotiation Flow Chart

For 1000Base-T mode, auto-negotiation is required and always used to establish a link. During 1000Base-T auto-negotiation, the Master and Slave configuration is first resolved between link partners, and then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default at power-up or after hardware reset. Afterwards, auto-negotiation can be enabled or disabled through register 0 bit 12. If auto-negotiation is disabled, the speed is set by register 0 bits 6 and 13, and the duplex is set by register 0 bit 8.

If the speed is changed on the fly, the link goes down and either auto-negotiation or parallel detection will initiate until a common speed between KSZ9021GN and its link partner is re-established for a link.

If link is already established and there is no change of speed on the fly, then the changes will not take effect unless either auto-negotiation is restarted through register 0 bit 9, or a link down to link up transition occurs (i.e., disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in register 1 and the link partner capabilities are updated in registers 5, 6, and 10.

The auto-negotiation finite state machines employ interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions are summarized in the following table.

| Auto-Negotiation Interval Timers | Time Duration |
|----------------------------------|---------------|
| Transmit Burst interval | 16 ms |
| Transmit Pulse interval | 68 us |
| FLP detect minimum time | 17.2 us |
| FLP detect maximum time | 185 us |
| Receive minimum Burst interval | 6.8 ms |
| Receive maximum Burst interval | 112 ms |
| Data detect minimum interval | 35.4 us |
| Data detect maximum interval | 95 us |
| NLP test minimum interval | 4.5 ms |
| NLP test maximum interval | 30 ms |
| Link Loss time | 52 ms |
| Break Link time | 1480 ms |
| Parallel Detection wait time | 830 ms |
| Link Enable wait time | 1000 ms |

Table 2. Auto-Negotiation Timers

GMII Interface

The Gigabit Media Independent Interface (GMII) is compliant to the IEEE 802.3 Specification. It provides a common interface between GMII PHYs and MACs, and has the following key characteristics:

- Pin count is 24 pins (11 pins for data transmission, 11 pins for data reception, and 2 pins for carrier and collision indication).
- 1000Mbps is supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 8-bit wide, a byte.

In GMII operation, the GMII pins function as follow:

- The MAC sources the transmit reference clock, GTX_CLK, at 125MHz for 1000Mbps.
- The PHY recovers and sources the receive reference clock, RX_CLK, at 125MHz for 1000Mbps.
- TX_EN, TXD[7:0] and TX_ER are sampled by the KSZ9021GN on the rising edge of GTX_CLK.
- RX_DV, RXD[7:0], and RX_ER are sampled by the MAC on the rising edge of RX_CLK.
- CRS and COL are driven by the KSZ9021GN and are not required to transition synchronously with respect to either GTX_CLK or RX_CLK.

The KSZ9021GN combines GMII mode with MII mode to form GMII/MII mode to support data transfer at 10/100/1000 Mbps speed. After power-up or reset, the KSZ9021GN is configured to GMII/MII mode if the MODE[3:0] strap-in pins are set to 0001. See Strapping Options section.

The KSZ9021GN has the option to output a low jitter 125MHz reference clock on CLK125_NDO (pin 55). This clock provides a lower cost reference clock alternative for GMII/MII MACs that require a 125MHz crystal or oscillator. The 125MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

The KSZ9021GN provides a dedicated transmit clock input pin for GMII mode, defined as follow:

- GTX_CLK (input, pin 32): Sourced by MAC in GMII mode for 1000Mbps speed

GMII Signal Definition

The following table describes the GMII signals. Refer to Clause 35 of the IEEE 802.3 Specification for more detailed information.

| GMII Signal Name (per spec) | GMII Signal Name (per KSZ9021GN) | Pin Type (with respect to PHY) | Pin Type (with respect to MAC) | Description |
|-----------------------------|----------------------------------|--------------------------------|--------------------------------|--|
| GTX_CLK | GTX_CLK | Input | Output | Transmit Reference Clock (125MHz for 1000Mbps) |
| TX_EN | TX_EN | Input | Output | Transmit Enable |
| TXD[7:0] | TXD[7:0] | Input | Output | Transmit Data [7:0] |
| TX_ER | TX_ER | Input | Output | Transmit Error |
| RX_CLK | RX_CLK | Output | Input | Receive Reference Clock (125MHz for 1000Mbps) |
| RX_DV | RX_DV | Output | Input | Receive Data Valid |
| RXD[7:0] | RXD[7:0] | Output | Input | Receive Data [7:0] |
| RX_ER | RX_ER | Output | Input | Receive Error |
| CRS | CRS | Output | Input | Carrier Sense |
| COL | COL | Output | Input | Collision Detected |

Table 3. GMII Signal Definition

GMII Signal Diagram

The KSZ9021GN GMII pin connections to the MAC are shown in the following figure.

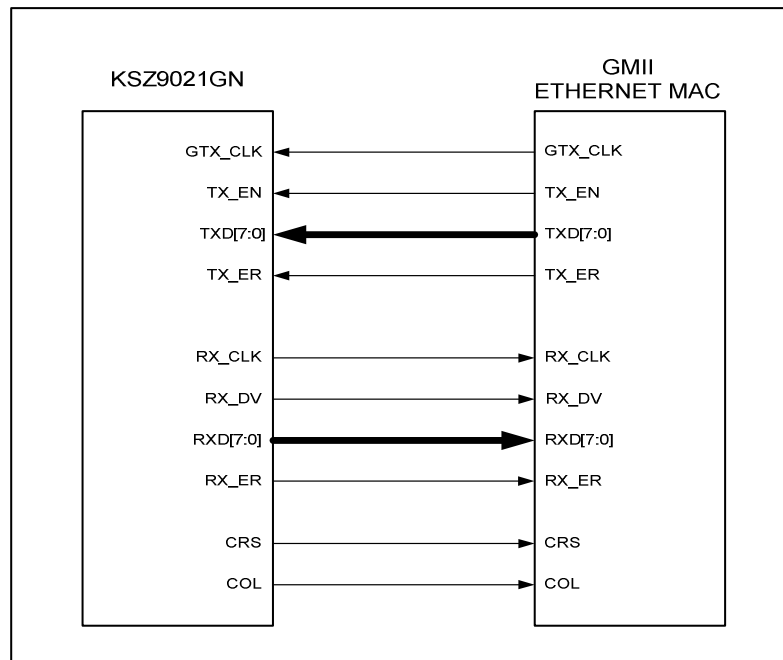


Figure 4. KSZ9021GN GMII Interface

MII Interface

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 16 pins (7 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10Mbps and 100Mbps are supported at both half and full duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4-bit wide, a nibble.

In MII operation, the MII pins function as follow:

- The PHY sources the transmit reference clock, TX_CLK, at 25MHz for 100Mbps and 2.5MHz for 10Mbps.
- The PHY recovers and sources the receive reference clock, RX_CLK, at 25MHz for 100Mbps and 2.5MHz for 10Mbps.
- TX_EN, TXD[3:0] and TX_ER are driven by the MAC and shall transition synchronously with respect to TX_CLK.
- RX_DV, RXD[3:0], and RX_ER are driven by the KSZ9021GN and shall transition synchronously with respect to RX_CLK.
- CRS and COL are driven by the KSZ9021GN and are not required to transition synchronously with respect to either TX_CLK or RX_CLK.

The KSZ9021GN combines GMII mode with MII mode to form GMII/MII mode to support data transfer at 10/100/1000 Mbps speeds. After the power-up or reset, the KSZ9021GN is then configured to GMII/MII mode if the MODE[3:0] strap-in pins are set to 0001. See Strapping Options section.

The KSZ9021GN has the option to output a low jitter 125MHz reference clock on CLK125_NDO (pin 55). This clock provides a lower cost reference clock alternative for GMII/MII MACs that require a 125MHz crystal or oscillator. The 125MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

The KSZ9021GN provides a dedicated transmit clock output pin for MII mode, defined as follow:

- TX_CLK (output, pin 57): Sourced by KSZ9021GN in MII mode for 10/100Mbps speed

MII Signal Definition

The following table describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

| MII Signal Name (per spec) | MII Signal Name (per KSZ9021GN) | Pin Type (with respect to PHY) | Pin Type (with respect to MAC) | Description |
|----------------------------|---------------------------------|--------------------------------|--------------------------------|---|
| TX_CLK | TX_CLK | Output | Input | Transmit Reference Clock (25MHz for 100Mbps, 2.5MHz for 10Mbps) |
| TX_EN | TX_EN | Input | Output | Transmit Enable |
| TXD[3:0] | TXD[3:0] | Input | Output | Transmit Data [3:0] |
| TX_ER | TX_ER | Input | Output | Transmit Error |
| RX_CLK | RX_CLK | Output | Input | Receive Reference Clock (25MHz for 100Mbps, 2.5MHz for 10Mbps) |
| RX_DV | RX_DV | Output | Input | Receive Data Valid |
| RXD[3:0] | RXD[3:0] | Output | Input | Receive Data [3:0] |
| RX_ER | RX_ER | Output | Input | Receive Error |
| CRS | CRS | Output | Input | Carrier Sense |
| COL | COL | Output | Input | Collision Detected |

Table 4. MII Signal Definition

MII Signal Diagram

The KSZ9021GN MII pin connections to the MAC are shown in the following figure.

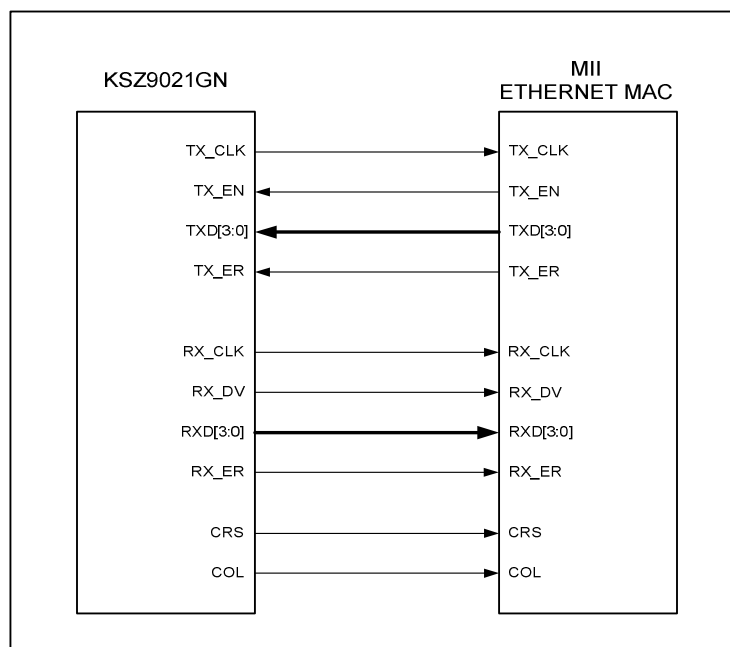


Figure 5. KSZ9021GN MII Interface

MII Management (MIIM) Interface

The KSZ9021GN supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9021GN. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. Further detail on the MIIM interface can be found in Clause 22.2.4.5 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with one or more KSZ9021GN device. Each KSZ9021GN device is assigned a PHY address between 1 and 7 by the PHYAD[2:0] strapping pins.
- A 32 register address space to access the KSZ9021GN IEEE Defined Registers, Vendor Specific Registers and Extended Registers. See Register Map section.

The following table shows the MII Management frame format for the KSZ9021GN.

| | Preamble | Start of Frame | Read/Write OP Code | PHY Address Bits [4:0] | REG Address Bits [4:0] | TA | Data Bits [15:0] | Idle |
|--------------|----------|----------------|--------------------|------------------------|------------------------|----|-------------------|------|
| Read | 32 1's | 01 | 10 | 00AAA | RRRRR | Z0 | DDDDDDDD_DDDDDDDD | Z |
| Write | 32 1's | 01 | 01 | 00AAA | RRRRR | 10 | DDDDDDDD_DDDDDDDD | Z |

Table 5. MII Management Frame Format – for KSZ9021GN

Interrupt (INT_N)

INT_N (pin 53) is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9021GN PHY register. Bits [15:8] of register 27 (1Bh) are the interrupt control bits to enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of register 27 (1Bh) are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 27 (1Bh).

Bit 14 of register 31 (1Fh) sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ9021GN control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

LED Mode

The KSZ9021GN provides two programmable LED output pins, LED2 and LED1, which are configurable to support two LED modes. The LED mode is configured by the LED_MODE strap-in (pin 55). It is latched at power-up / reset and is defined as follows:

- Pull-up: Single LED Mode
- Pull-down: Tri-color Dual LED Mode

Single LED Mode

In Single LED Mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in the following table.

| LED pin | Pin State | LED Definition | Link / Activity |
|---------|-----------|----------------|---------------------|
| LED2 | H | OFF | Link off |
| | L | ON | Link on (any speed) |
| LED1 | H | OFF | No Activity |
| | Toggle | Blinking | Activity (RX, TX) |

Table 6. Single LED Mode – Pin Definition

Tri-color Dual LED Mode

In Tri-color Dual LED Mode, the Link and Activity status are indicated by the LED2 pin for 1000Base-T, by the LED1 pin for 100Base-TX, and by both LED2 and LED1 pin, working in conjunction, for 10Base-T. This is summarized in the following table.

| LED Pin (State) | | LED Pin (Definition) | | Link / Activity |
|-----------------|--------|----------------------|----------|-------------------------------|
| LED2 | LED1 | LED2 | LED1 | |
| H | H | OFF | OFF | Link off |
| L | H | ON | OFF | 1000 Link / No Activity |
| Toggle | H | Blinking | OFF | 1000 Link / Activity (RX, TX) |
| H | L | OFF | ON | 100 Link / No Activity |
| H | Toggle | OFF | Blinking | 100 Link / Activity (RX, TX) |
| L | L | ON | ON | 10 Link / No Activity |
| Toggle | Toggle | Blinking | Blinking | 10 Link / Activity (RX, TX) |

Table 7. Tri-color Dual LED Mode – Pin Definition

Each LED output pin can directly drive a LED with a series resistor (typically 220Ω to 470Ω).

For activity indication, the LED output toggles at approximately 12.5Hz (80ms) to ensure visibility to the human eye.

NAND Tree Support

The KSZ9021GN provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree mode is enabled at power-up / reset with the MODE[3:0] strap-in pins set to 0100.

The following table lists the NAND tree pin order.

| Pin | Description |
|------------|-------------|
| LED2 | Input |
| LED1 | Input |
| TXD0 | Input |
| TXD1 | Input |
| TXD2 | Input |
| TXD3 | Input |
| TX_ER | Input |
| GTX_CLK | Input |
| TX_EN | Input |
| RX_DV | Input |
| RX_ER | Input |
| RX_CLK | Input |
| CRS | Input |
| COL | Input |
| INT_N | Input |
| MDC | Input |
| MDIO | Input |
| CLK125_NDO | Output |

Table 8. NAND Tree Test Pin Order – for KSZ9021GN

Power Management

The KSZ9021GN offers the following power management modes:

Power Saving Mode

This mode is a KSZ9021GN green feature to reduce power consumption when the cable is unplugged. It is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

Software Power-Down Mode

This mode is used to power down the KSZ9021GN device when it is not in use after power-up. Power-down mode is enabled by writing a one to register 0h bit 11. In the power-down state, the KSZ9021GN disables all internal functions, except for the MII management interface. The KSZ9021GN exits power-down mode after writing a zero to register 0h bit 11.

Chip Power-Down Mode

This mode provides the lowest power state for the KSZ9021GN when it is not in use and is mounted on the board. Chip power-down mode is enabled at power-up / reset with the MODE[3:0] strap-in pins set to 0111. The KSZ9021GN exits chip power down mode when a hardware reset is applied to RESET_N (pin 56) with the MODE[3:0] strap-in pins set to an operating mode other than chip power-down mode.

Register Map

The IEEE 802.3 Specification provides a 32 register address space for the PHY. Registers 0 thru 15 are standard PHY registers, defined per the specification. Registers 16 thru 31 are vendor specific registers.

The KSZ9021GN uses the IEEE provided register space for IEEE Defined Registers and Vendor Specific Registers, and uses the following registers to access Extended Registers:

- Register 11 (Bh) for Extended Register – Control
- Register 12 (Ch) for Extended Register – Data Write
- Register 13 (Dh) for Extended Register – Data Read

Examples:

- Extended Register Read // Read from Operation Mode Strap Status Register
 1. Write register 11 (Bh) with 0103h // Set register 259 (103h) for read
 2. Read register 13 (Dh) // Read register value
- Extended Register Write // Write to Operation Mode Strap Override Register
 1. Write register 11 (Bh) with 8102h // Set register 258 (102h) for write
 2. Write register 12 (Ch) with 0010h // Write 0010h value to register to set NAND Tree mode

| Register Number (Hex) | Description |
|----------------------------------|---|
| IEEE Defined Registers | |
| 0 (0h) | Basic Control |
| 1 (1h) | Basic Status |
| 2 (2h) | PHY Identifier 1 |
| 3 (3h) | PHY Identifier 2 |
| 4 (4h) | Auto-Negotiation Advertisement |
| 5 (5h) | Auto-Negotiation Link Partner Ability |
| 6 (6h) | Auto-Negotiation Expansion |
| 7 (7h) | Auto-Negotiation Next Page |
| 8 (8h) | Auto-Negotiation Link Partner Next Page Ability |
| 9 (9h) | 1000Base-T Control |
| 10 (Ah) | 1000Base-T Status |
| 11 (Bh) | Extended Register – Control |
| 12 (Ch) | Extended Register – Data Write |
| 13 (Dh) | Extended Register – Data Read |
| 14 (Eh) | Reserved |
| 15 (Fh) | Extended – MII Status |
| Vendor Specific Registers | |
| 16 (10h) | Reserved |
| 17 (11h) | Remote Loopback, LED Mode |
| 18 (12h) | LinkMD [®] – Cable Diagnostic |
| 19 (13h) | Digital PMA/PCS Status |
| 20 (14h) | Reserved |
| 21 (15h) | RXER Counter |
| 22 (16h) – 26 (1Ah) | Reserved |

| Register Number (Hex) | Description |
|---------------------------|-------------------------------|
| 27 (1Bh) | Interrupt Control/Status |
| 28 (1Ch) | Digital Debug Control 1 |
| 29 (1Dh) – 30 (1Eh) | Reserved |
| 31 (1Fh) | PHY Control |
| Extended Registers | |
| 257 (101h) | Strap Status |
| 258 (102h) | Operation Mode Strap Override |
| 259 (103h) | Operation Mode Strap Status |
| 263 (107h) | Analog Test Register |

Register Description

IEEE Defined Registers

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|--|--------------------------|--|---------------------|------------------|
| Register 0 (0h) – Basic Control | | | | |
| 0.15 | Reset | 1 = Software PHY reset 0 = Normal operation This bit is self-cleared after a '1' is written to it. | RW/SC | 0 |
| 0.14 | Loop-back | 1 = Loop-back mode 0 = Normal operation | RW | 0 |
| 0.13 | Speed Select (LSB) | [0.6, 0.13] [1,1] = Reserved [1,0] = 1000Mbps [0,1] = 100Mbps [0,0] = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1). | RW | Hardware Setting |
| 0.12 | Auto-Negotiation Enable | 1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, auto-negotiation result overrides settings in register 0.13, 0.8 and 0.6. | RW | 1 |
| 0.11 | Power Down | 1 = Power down mode 0 = Normal operation | RW | 0 |
| 0.10 | Isolate | 1 = Electrical isolation of PHY from GMII/MII 0 = Normal operation | RW | 0 |
| 0.9 | Restart Auto-Negotiation | 1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a '1' is written to it. | RW/SC | 0 |
| 0.8 | Duplex Mode | 1 = Full-duplex 0 = Half-duplex | RW | Hardware Setting |
| 0.7 | Collision Test | 1 = Enable COL test 0 = Disable COL test | RW | 0 |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|---|---------------------------|---|---------------------|---------|
| 0.6 | Speed Select (MSB) | [0.6, 0.13] [1,1] = Reserved [1,0] = 1000Mbps [0,1] = 100Mbps [0,0] = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1). | RW | 0 |
| 0.5:0 | Reserved | | RO | 00_0000 |
| Register 1 (1h) – Basic Status | | | | |
| 1.15 | 100Base-T4 | 1 = T4 capable 0 = Not T4 capable | RO | 0 |
| 1.14 | 100Base-TX Full Duplex | 1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full-duplex | RO | 1 |
| 1.13 | 100Base-TX Half Duplex | 1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half-duplex | RO | 1 |
| 1.12 | 10Base-T Full Duplex | 1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full-duplex | RO | 1 |
| 1.11 | 10Base-T Half Duplex | 1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half-duplex | RO | 1 |
| 1.10:9 | Reserved | | RO | 00 |
| 1.8 | Extended Status | 1 = Extended Status Information in Reg. 15. 0 = No Extended Status Information in Reg. 15. | RO | 1 |
| 1.7 | Reserved | | RO | 0 |
| 1.6 | No Preamble | 1 = Preamble suppression 0 = Normal preamble | RO | 1 |
| 1.5 | Auto-Negotiation Complete | 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed | RO | 0 |
| 1.4 | Remote Fault | 1 = Remote fault 0 = No remote fault | RO/LH | 0 |
| 1.3 | Auto-Negotiation Ability | 1 = Capable to perform auto-negotiation 0 = Not capable to perform auto-negotiation | RO | 1 |
| 1.2 | Link Status | 1 = Link is up 0 = Link is down | RO/LL | 0 |
| 1.1 | Jabber Detect | 1 = Jabber detected 0 = Jabber not detected (default is low) | RO/LH | 0 |
| 1.0 | Extended Capability | 1 = Supports extended capabilities registers | RO | 1 |
| Register 2 (2h) – PHY Identifier 1 | | | | |
| 2.15:0 | PHY ID Number | Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex) | RO | 0022h |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|--|------------------------|--|---------------------|----------------------------|
| Register 3 (3h) – PHY Identifier 2 | | | | |
| 3.15:10 | PHY ID Number | Assigned to the 19th through 24 th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex) | RO | 0001_01 |
| 3.9:4 | Model Number | Six bit manufacturer's model number | RO | 10_0001 |
| 3.3:0 | Revision Number | Four bit manufacturer's revision number | RO | Indicates silicon revision |
| Register 4 (4h) – Auto-Negotiation Advertisement | | | | |
| 4.15 | Next Page | 1 = Next page capable 0 = No next page capability. | RW | 0 |
| 4.14 | Reserved | | RO | 0 |
| 4.13 | Remote Fault | 1 = Remote fault supported 0 = No remote fault | RW | 0 |
| 4.12 | Reserved | | RO | 0 |
| 4.11:10 | Pause | [4.11, 4.10] [0,0] = No PAUSE [1,0] = Asymmetric PAUSE (link partner) [0,1] = Symmetric PAUSE [1,1] = Symmetric & Asymmetric PAUSE (local device) | RW | 00 |
| 4.9 | 100Base-T4 | 1 = T4 capable 0 = No T4 capability | RO | 0 |
| 4.8 | 100Base-TX Full-Duplex | 1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability | RW | 1 |
| 4.7 | 100Base-TX Half-Duplex | 1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability | RW | 1 |
| 4.6 | 10Base-T Full-Duplex | 1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability | RW | 1 |
| 4.5 | 10Base-T Half-Duplex | 1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability | RW | 1 |
| 4.4:0 | Selector Field | [00001] = IEEE 802.3 | RW | 0_0001 |
| Register 5 (5h) – Auto-Negotiation Link Partner Ability | | | | |
| 5.15 | Next Page | 1 = Next page capable 0 = No next page capability | RO | 0 |
| 5.14 | Acknowledge | 1 = Link code word received from partner 0 = Link code word not yet received | RO | 0 |
| 5.13 | Remote Fault | 1 = Remote fault detected 0 = No remote fault | RO | 0 |
| 5.12 | Reserved | | RO | 0 |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|---|--|--|---------------------|---------------|
| 5.11:10 | Pause | [5.11, 5.10] [0,0] = No PAUSE [1,0] = Asymmetric PAUSE (link partner) [0,1] = Symmetric PAUSE [1,1] = Symmetric & Asymmetric PAUSE (local device) | RW | 00 |
| 5.9 | 100Base-T4 | 1 = T4 capable 0 = No T4 capability | RO | 0 |
| 5.8 | 100Base-TX Full-Duplex | 1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability | RO | 0 |
| 5.7 | 100Base-TX Half-Duplex | 1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability | RO | 0 |
| 5.6 | 10Base-T Full-Duplex | 1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability | RO | 0 |
| 5.5 | 10Base-T Half-Duplex | 1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability | RO | 0 |
| 5.4:0 | Selector Field | [00001] = IEEE 802.3 | RO | 0_0000 |
| Register 6 (6h) – Auto-Negotiation Expansion | | | | |
| 6.15:5 | Reserved | | RO | 0000_0000_000 |
| 6.4 | Parallel Detection Fault | 1 = Fault detected by parallel detection 0 = No fault detected by parallel detection. | RO/LH | 0 |
| 6.3 | Link Partner Next Page Able | 1 = Link partner has next page capability 0 = Link partner does not have next page capability | RO | 0 |
| 6.2 | Next Page Able | 1 = Local device has next page capability 0 = Local device does not have next page capability | RO | 1 |
| 6.1 | Page Received | 1 = New page received 0 = New page not received yet | RO/LH | 0 |
| 6.0 | Link Partner Auto- Negotiation Able | 1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability | RO | 0 |
| Register 7 (7h) – Auto-Negotiation Next Page | | | | |
| 7.15 | Next Page | 1 = Additional next page(s) will follow 0 = Last page | RW | 0 |
| 7.14 | Reserved | | RO | 0 |
| 7.13 | Message Page | 1 = Message page 0 = Unformatted page | RW | 1 |
| 7.12 | Acknowledge2 | 1 = Will comply with message 0 = Cannot comply with message | RW | 0 |
| 7.11 | Toggle | 1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero | RO | 0 |
| 7.10:0 | Message Field | 11-bit wide field to encode 2048 messages | RW | 000_0000_0001 |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|--|-----------------------------------|---|---------------------|---------------|
| Register 8 (8h) – Auto-Negotiation Link Partner Next Page Ability | | | | |
| 8.15 | Next Page | 1 = Additional Next Page(s) will follow 0 = Last page | RO | 0 |
| 8.14 | Acknowledge | 1 = Successful receipt of link word 0 = No successful receipt of link word | RO | 0 |
| 8.13 | Message Page | 1 = Message page 0 = Unformatted page | RO | 0 |
| 8.12 | Acknowledge2 | 1 = Able to act on the information 0 = Not able to act on the information | RO | 0 |
| 8.11 | Toggle | 1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one | RO | 0 |
| 8.10:0 | Message Field | | RO | 000_0000_0000 |
| Register 9 (9h) – 1000Base-T Control | | | | |
| 9:15:13 | Test Mode Bits | Transmitter test mode operations [9.15:13] Mode [000] Normal Operation [001] Test mode 1 –Transmit waveform test [010] Test mode 2 –Transmit jitter test in Master mode [011] Test mode 3 –Transmit jitter test in Slave mode [100] Test mode 4 –Transmitter distortion test [101] Reserved, operations not identified [110] Reserved, operations not identified [111] Reserved, operations not identified | RW | 000 |
| 9.12 | MASTER-SLAVE Manual Config Enable | 1 = Enable MASTER-SLAVE Manual configuration value 0 = Disable MASTER-SLAVE Manual configuration value | RW | 0 |
| 9.11 | MASTER-SLAVE Manual Config Value | 1 = Configure PHY as MASTER during MASTER-SLAVE negotiation 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation This bit is ignored if MASTER-SLAVE Manual Config is disabled (register 9.12 = 0). | RW | 0 |
| 9.10 | Port Type | 1 = Indicate the preference to operate as multiport device (MASTER) 0 = Indicate the preference to operate as single-port device (SLAVE) This bit is valid only if the MASTER-SLAVE Manual Config Enable bit is disabled (register 9.12 = 0). | RW | 0 |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|---|---------------------------------------|---|---------------------|------------------|
| 9.9 | 1000Base-T Full-Duplex | 1 = Advertise PHY is 1000Base-T full-duplex capable 0 = Advertise PHY is not 1000Base-T full-duplex capable | RW | 1 |
| 9.8 | 1000Base-T Half-Duplex | 1 = Advertise PHY is 1000Base-T half-duplex capable 0 = Advertise PHY is not 1000Base-T half-duplex capable | RW | Hardware Setting |
| 9.7:0 | Reserved | Write as 0, ignore on read | RO | |
| Register 10 (Ah) – 1000Base-T Status | | | | |
| 10.15 | MASTER-SLAVE configuration fault | 1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected | RO/LH/SC | 0 |
| 10.14 | MASTER-SLAVE configuration resolution | 1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE | RO | 0 |
| 10.13 | Local Receiver Status | 1 = Local Receiver OK (loc_rcvr_status = 1) 0 = Local Receiver not OK (loc_rcvr_status = 0) | RO | 0 |
| 10.12 | Remote Receiver Status | 1 = Remote Receiver OK (rem_rcvr_status = 1) 0 = Remote Receiver not OK (rem_rcvr_status = 0) | RO | 0 |
| 10.11 | LP 1000T FD | 1 = Link Partner is capable of 1000Base-T full-duplex 0 = Link Partner is not capable of 1000Base-T full-duplex | RO | 0 |
| 10.10 | LP 1000T HD | 1 = Link Partner is capable of 1000Base-T half-duplex 0 = Link Partner is not capable of 1000Base-T half-duplex | RO | 0 |
| 10.9:8 | Reserved | | RO | 00 |
| 10.7:0 | Idle Error Count | Cumulative count of errors detected when receiver is receiving idles and PMA_TXMODE.indicate = SEND_N. The counter is incremented every symbol period that rxerror_status = ERROR. | RO/SC | 0000_0000 |
| Register 11 (Bh) – Extended Register – Control | | | | |
| 11.15 | Extended Register – read/write select | 1 = Write Extended Register 0 = Read Extended Register | RW | 0 |
| 11.14:9 | Reserved | | RW | 000_000 |
| 11.8 | Extended Register – page | Select page for Extended Register | RW | 0 |
| 11.7:0 | Extended Register – address | Select Extended Register Address | RW | 0000_0000 |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|--|---------------------------|---|---------------------|---------------------|
| Register 12 (Ch) – Extended Register – Data Write | | | | |
| 12.15:0 | Extended Register – write | 16-bit value to write to Extend Register Address in register 11 (Bh) bits [7:0] | RW | 0000_0000_0000_0000 |
| Register 13 (Dh) – Extended Register – Data Read | | | | |
| 13.15:0 | Extended Register – read | 16-bit value read from Extend Register Address in register 11 (Bh) bits [7:0] | RO | 0000_0000_0000_0000 |
| Register 15 (Fh) – Extended – MII Status | | | | |
| 15.15 | 1000Base-X Full-duplex | 1 = PHY able to perform 1000Base-X full-duplex 0 = PHY not able to perform 1000Base-X full-duplex | RO | 0 |
| 15.14 | 1000Base-X Half-duplex | 1 = PHY able to perform 1000Base-X half-duplex 0 = PHY not able to perform 1000Base-X half-duplex | RO | 0 |
| 15.13 | 1000Base-T Full-duplex | 1 = PHY able to perform 1000Base-T full-duplex 1000BASE-X 0 = PHY not able to perform 1000Base-T full-duplex | RO | 1 |
| 15.12 | 1000Base-T Half-duplex | 1 = PHY able to perform 1000Base-T half-duplex 0 = PHY not able to perform 1000Base-T half-duplex | RO | 1 |
| 15.11:0 | Reserved | Ignore when read | RO | - |

Note:

1. RW = Read/Write.
RO = Read only.
SC = Self-cleared.
LH = Latch high.
LL = Latch low.

Vendor Specific Registers

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|--|-----------------|---|---------------------|----------|
| Register 17 (11h) – Remote Loopback, LED Mode | | | | |
| 17.15:9 | Reserved | | RW | 0000_001 |
| 17.8 | Remote Loopback | 1 = Enable Remote Loopback 0 = Disable Remote Loopback | RW | 0 |
| 17.7:6 | Reserved | | RW | 11 |
| 17.5:4 | Reserved | | RW | 11 |
| 17.3 | LED Test Enable | 1 = Enable LED test mode 0 = Disable LED test mode | RW | 0 |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|--|---|---|---------------------|---------------------|
| 17.2:1 | Reserved | | RW | 00 |
| 17.0 | Reserved | | RO | 0 |
| Register 18 (12h) – LinkMD[®] – Cable Diagnostic | | | | |
| 18.15 | Reserved | | RW/SC | 0 |
| 18.14:8 | Reserved | | RW | 000_0000 |
| 18.7:0 | Reserved | | RO | 0000_0000 |
| Register 19 (13h) – Digital PMA/PCS Status | | | | |
| 19.15:3 | Reserved | | RO/LH | 0000_0000_0000_0 |
| 19.2 | 1000Base-T Link Status | 1000 Base-T Link Status 1 = Link status is OK 0 = Link status is not OK | RO | 0 |
| 19.1 | 100Base-TX Link Status | 100 Base-TX Link Status 1 = Link status is OK 0 = Link status is not OK | RO | 0 |
| 19.0 | Reserved | | RO | 0 |
| Register 21 (15h) – RXER Counter | | | | |
| 21.15:0 | RXER Counter | Receive error counter for Symbol Error frames | RO/RC | 0000_0000_0000_0000 |
| Register 27 (1Bh) – Interrupt Control/Status | | | | |
| 27.15 | Jabber Interrupt Enable | 1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt | RW | 0 |
| 27.14 | Receive Error Interrupt Enable | 1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt | RW | 0 |
| 27.13 | Page Received Interrupt Enable | 1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt | RW | 0 |
| 27.12 | Parallel Detect Fault Interrupt Enable | 1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt | RW | 0 |
| 27.11 | Link Partner Acknowledge Interrupt Enable | 1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt | RW | 0 |
| 27.10 | Link Down Interrupt Enable | 1 = Enable Link Down Interrupt 0 = Disable Link Down Interrupt | RW | 0 |
| 27.9 | Remote Fault Interrupt Enable | 1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt | RW | 0 |
| 27.8 | Link Up Interrupt Enable | 1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt | RW | 0 |
| 27.7 | Jabber Interrupt | 1 = Jabber occurred 0 = Jabber did not occurred | RO/RC | 0 |
| 27.6 | Receive Error Interrupt | 1 = Receive Error occurred 0 = Receive Error did not occurred | RO/RC | 0 |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|--|------------------------------------|---|---------------------|-----------|
| 27.5 | Page Receive Interrupt | 1 = Page Receive occurred 0 = Page Receive did not occurred | RO/RC | 0 |
| 27.4 | Parallel Detect Fault Interrupt | 1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occurred | RO/RC | 0 |
| 27.3 | Link Partner Acknowledge Interrupt | 1 = Link Partner Acknowledge occurred 0 = Link Partner Acknowledge did not occurred | RO/RC | 0 |
| 27.2 | Link Down Interrupt | 1 = Link Down occurred 0 = Link Down did not occurred | RO/RC | 0 |
| 27.1 | Remote Fault Interrupt | 1 = Remote Fault occurred 0 = Remote Fault did not occurred | RO/RC | 0 |
| 27.0 | Link Up Interrupt | 1 = Link Up occurred 0 = Link Up did not occurred | RO/RC | 0 |
| Register 28 (1Ch) – Digital Debug Control 1 | | | | |
| 28.15:8 | Reserved | | RW | 0000_0000 |
| 28.7 | mdi_set | mdi_set has no function when swapoff (reg28.6) is de-asserted. 1 = When swapoff is asserted, if mdi_set is asserted, chip will operate at MDI mode. 0 = When swapoff is asserted, if mdi_set is de-asserted, chip will operate at MDI-X mode. | RW | 0 |
| 28.6 | swapoff | 1 = Disable auto crossover function 0 = Enable auto crossover function | RW | 0 |
| 28.5:1 | Reserved | | RW | 00_000 |
| 28.0 | PCS Loopback | 1 = Enable 10Base-T and 100Base-TX Loopback for register 0h bit 14. 0 = normal function | RW | 0 |
| Register 31 (1Fh) – PHY Control | | | | |
| 31.15 | Reserved | | RW | 0 |
| 31.14 | Interrupt Level | 1 = Interrupt pin active high 0 = Interrupt pin active low | RW | 0 |
| 31.13:12 | Reserved | | RW | 00 |
| 31.11:10 | Reserved | | RO/LH/RC | 00 |
| 31.9 | Enable Jabber | 1 = Enable jabber counter 0 = Disable jabber counter | RW | 1 |
| 31.8:7 | Reserved | | RW | 00 |
| 31.6 | Speed status 1000Base-T | 1 = Indicate chip final speed status at 1000Base-T | RO | 0 |
| 31.5 | Speed status 100Base-TX | 1 = Indicate chip final speed status at 100Base-TX | RO | 0 |
| 31.4 | Speed status 10Base-T | 1 = Indicate chip final speed status at 10Base-T | RO | 0 |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|---------|--------------------------------|---|---------------------|---------|
| 31.3 | Duplex status | Indicate chip duplex status 1 = Full-duplex 0 = Half-duplex | RO | 0 |
| 31.2 | 1000Base-T Master/Slave status | 1 = Indicate 1000Base-T Master mode 0 = Indicate 1000Base-T Slave mode | RO | 0 |
| 31.1 | Software Reset | 1 = Reset chip, except all registers 0 = Disable reset | RW | 0 |
| 31.0 | Link Status Check Fail | 1 = Fail 0 = Not Failing | RO | 0 |

Note:

1. RW = Read/Write.
RC = Read-cleared
RO = Read only.
SC = Self-cleared.
LH = Latch high.

Extended Registers

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|--|----------------------------|--|---------------------|---------|
| Register 257 (101h) – Strap Status | | | | |
| 257.15:6 | Reserved | | RO | |
| 257.5 | CLK125_EN status | 1 = CLK125_EN strap-in is enabled 0 = CLK125_EN strap-in is disabled | RO | |
| 257.4:0 | PHYAD[4:0] status | Strapped-in value for PHY Address | RO | |
| Register 258 (102h) – Operation Mode Strap Override | | | | |
| 258.15:8 | Reserved | | RW | |
| 258.7 | Tri-state all digital I/Os | 1 = Tri-state all digital I/Os for further power saving during software power down | RW | 0 |
| 258.6:5 | Reserved | | RW | |
| 258.4 | NAND Tree override | 1 = Override strap-in for NAND Tree mode | RW | |
| 258.3:2 | Reserved | | RW | |
| 258.1 | GMII / MII override | 1 = Override strap-in for GMII / MII mode | RW | |
| 258.0 | Reserved | | RW | |
| Register 259 (103h) – Operation Mode Strap Status | | | | |
| 259.15:5 | Reserved | | RO | |
| 259.4 | NAND Tree strap-in status | 1 = Strap to NAND tree mode | RO | |
| 259.3:2 | Reserved | | RO | |
| 259.1 | GMII / MII strap-in status | 1 = Strap to GMII / MII mode | RO | |
| 259.0 | Reserved | | RO | |

| Address | Name | Description | Mode ⁽¹⁾ | Default |
|---|-------------------------------|---|---------------------|-----------|
| Register 263 (107h) – Analog Test Register | | | | |
| 263.15 | LDO disable | 1 = LDO controller disable 0 = LDO controller enable | RW | 0 |
| 263.14:9 | Reserved | | RW | 000_000 |
| 263.8 | Low frequency oscillator mode | 1 = Low frequency oscillator mode enable 0 = Low frequency oscillator mode disable Use for further power saving during software power down. | RW | 0 |
| 263.7:0 | Reserved | | RW | 0000_0000 |

Note:

1. RW = Read/Write.
RO = Read only.

Absolute Maximum Ratings⁽¹⁾

| | |
|---|--|
| Supply Voltage | (DVDDL, AVDDL, AVDDL_PLL)..... -0.5V to V _{DD} +10% |
| (AVDDH)..... | -0.5V to V _{DD} +10% |
| (DVDDH)..... | -0.5V to V _{DD} +10% |
| Input Voltage (all inputs) | -0.5V to V _{DD} +10% |
| Output Voltage (all outputs) | -0.5V to V _{DD} +10% |
| Lead Temperature (soldering, 10sec.)..... | 260°C |
| Storage Temperature (T _s) | -55°C to +150°C |

Operating Ratings⁽²⁾

| | |
|---|--|
| Supply Voltage | (DVDDL, AVDDL, AVDDL_PLL).... +1.140V to +1.260V |
| (AVDDH)..... | +3.135V to +3.465V |
| (DVDDH @ 3.3V) | +3.135V to +3.465V |
| (DVDDH @ 2.5V) | +2.375V to +2.625V |
| Ambient Temperature | (T _A Commercial: KSZ9021GN)..... 0°C to +70°C |
| (T _A Industrial: KSZ9021GNI) | -40°C to +85°C |
| Maximum Junction Temperature (T _J Max) | 125°C |
| Thermal Resistance (θ _{JA}) | 41.54°C/W |
| Thermal Resistance (θ _{JC}) | 19.78°C/W |

Electrical Characteristics⁽³⁾

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|-----|-----|-----|-------|
| Supply Current – Core / Digital I/Os | | | | | | |
| I _{CORE} | 1.2V total of: DVDDL (1.2V digital core) + AVDDL (1.2V analog core) + AVDDL_PLL (1.2V for PLL) | 1000Base-T Link-up (no traffic) | | 522 | | mA |
| | | 1000Base-T Full-duplex @ 100% utilization | | 555 | | mA |
| | | 100Base-TX Link-up (no traffic) | | 159 | | mA |
| | | 100Base-TX Full-duplex @ 100% utilization | | 160 | | mA |
| | | 10Base-T Link-up (no traffic) | | 7 | | mA |
| | | 10Base-T Full-duplex @ 100% utilization | | 7 | | mA |
| | | Power-saving Mode (cable un-plugged) | | 15 | | mA |
| | | Software Power Down Mode (register 0.11 =1) | | 1.3 | | mA |
| | Chip Power Down Mode (strap-in pins MODE[3:0] = 0111) | | 1.2 | | mA | |
| I _{DVDDH_2.5} | 2.5V for digital I/Os (GMII / MII operating @ 2.5V) | 1000Base-T Link-up (no traffic) | | 22 | | mA |
| | | 1000Base-T Full-duplex @ 100% utilization | | 39 | | mA |
| | | 100Base-TX Link-up (no traffic) | | 15 | | mA |
| | | 100Base-TX Full-duplex @ 100% utilization | | 19 | | mA |
| | | 10Base-T Link-up (no traffic) | | 10 | | mA |
| | | 10Base-T Full-duplex @ 100% utilization | | 11 | | mA |
| | | Power-saving Mode (cable un-plugged) | | 14 | | mA |
| | | Software Power Down Mode (register 0.11 =1) | | 8 | | mA |
| | Chip Power Down Mode (strap-in pins MODE[3:0] = 0111) | | 1 | | mA | |
| I _{DVDDH_3.3} | 3.3V for digital I/Os (GMII / MII operating @ 3.3V) | 1000Base-T Link-up (no traffic) | | 32 | | mA |
| | | 1000Base-T Full-duplex @ 100% utilization | | 57 | | mA |
| | | 100Base-TX Link-up (no traffic) | | 19 | | mA |
| | | 100Base-TX Full-duplex @ 100% utilization | | 25 | | mA |
| | | 10Base-T Link-up (no traffic) | | 13 | | mA |
| | | 10Base-T Full-duplex @ 100% utilization | | 17 | | mA |
| | | Power-saving Mode (cable un-plugged) | | 23 | | mA |
| | | Software Power Down Mode (register 0.11 =1) | | 16 | | mA |
| | Chip Power Down Mode (strap-in pins MODE[3:0] = 0111) | | 1 | | mA | |

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---------------------------------------|---|------|-------|--------|-------|
| Supply Current – Transceiver (equivalent to current draw through external transformer center taps for PHY transceivers with current-mode transmit drivers) | | | | | | |
| I _{AVDDH} | 3.3V for transceiver | 1000Base-T Link-up (no traffic) | | 74 | | mA |
| | | 1000Base-T Full-duplex @ 100% utilization | | 73 | | mA |
| | | 100Base-TX Link-up (no traffic) | | 28 | | mA |
| | | 100Base-TX Full-duplex @ 100% utilization | | 28 | | mA |
| | | 10Base-T Link-up (no traffic) | | 35 | | mA |
| | | 10Base-T Full-duplex @ 100% utilization | | 43 | | mA |
| | | Power-saving Mode (cable un-plugged) | | 35 | | mA |
| | | Software Power Down Mode (register 0.11 =1) | | 2 | | mA |
| | | Chip Power Down Mode (strap-in pins MODE[3:0] = 0111) | | 1 | | mA |
| CMOS Inputs | | | | | | |
| V _{IH} | Input High Voltage | DVDDH = 3.3V | 2.0 | | | V |
| | | DVDDH = 2.5V | 1.8 | | | V |
| V _{IL} | Input Low Voltage | DVDDH = 3.3V | | | 0.8 | V |
| | | DVDDH = 2.5V | | | 0.7 | V |
| I _{IN} | Input Current | V _{IN} = GND ~ V _{DDIO} | | -10 | 10 | μA |
| CMOS Outputs | | | | | | |
| V _{OH} | Output High Voltage | DVDDH = 3.3V | 2.4 | | | V |
| | | DVDDH = 2.5V | 2.0 | | | V |
| V _{OL} | Output Low Voltage | DVDDH = 3.3V | | | 0.4 | V |
| | | DVDDH = 2.5V | | | 0.4 | V |
| I _{oz} | Output Tri-State Leakage | | | | 10 | μA |
| LED Outputs | | | | | | |
| I _{LED} | Output Drive Current | Each LED pin (LED1, LED2) | | 8 | | mA |
| 100Base-TX Transmit (measured differentially after 1:1 transformer) | | | | | | |
| V _O | Peak Differential Output Voltage | 100Ω termination across differential output | 0.95 | | 1.05 | V |
| V _{IMB} | Output Voltage Imbalance | 100Ω termination across differential output | | | 2 | % |
| t _r , t _f | Rise/Fall Time | | 3 | | 5 | ns |
| | Rise/Fall Time Imbalance | | 0 | | 0.5 | ns |
| | Duty Cycle Distortion | | | | ± 0.25 | ns |
| | Overshoot | | | | 5 | % |
| V _{SET} | Reference Voltage of I _{SET} | R(I _{SET}) = 4.99K | | 0.535 | | V |
| | Output Jitter | Peak-to-peak | | 0.7 | 1.4 | ns |
| 10Base-T Transmit (measured differentially after 1:1 transformer) | | | | | | |
| V _P | Peak Differential Output Voltage | 100Ω termination across differential output | 2.2 | | 2.8 | V |
| | Jitter Added | Peak-to-peak | | | 3.5 | ns |
| | Harmonic Rejection | Transmit all-one signal sequence | | -31 | | dB |
| 10Base-T Receive | | | | | | |
| V _{SQ} | Squelch Threshold | 5MHz square wave | 300 | 400 | | mV |

Notes:

1. Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
2. The device is not guaranteed to function outside its operating rating.
3. $T_A = 25^\circ\text{C}$. Specification is for packaged product only.

Timing Diagrams

GMII Transmit Timing

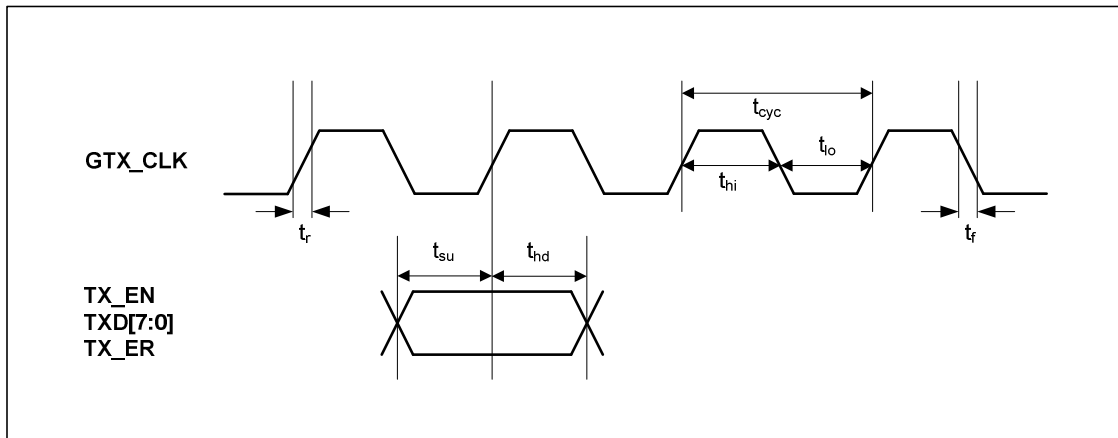


Figure 6. GMII Transmit Timing – Data Input to PHY

| Timing Parameter | Description | Min | Typ | Max | Unit |
|-------------------|--|-----|-----|-----|------|
| 1000Base-T | | | | | |
| t_{cyc} | GTX_CLK period | 7.5 | 8.0 | 8.5 | ns |
| t_{su} | TX_EN, TXD[7:0], TX_ER setup time to rising edge of GTX_CLK | 2.0 | | | ns |
| t_{hd} | TX_EN, TXD[7:0], TX_ER hold time from rising edge of GTX_CLK | 0 | | | ns |
| t_{hi} | GTX_CLK high pulse width | 2.5 | | | ns |
| t_{lo} | GTX_CLK low pulse width | 2.5 | | | ns |
| t_r | GTX_CLK rise time | | | 1.0 | ns |
| t_f | GTX_CLK fall time | | | 1.0 | ns |

Table 9. GMII Transmit Timing Parameters

GMII Receive Timing

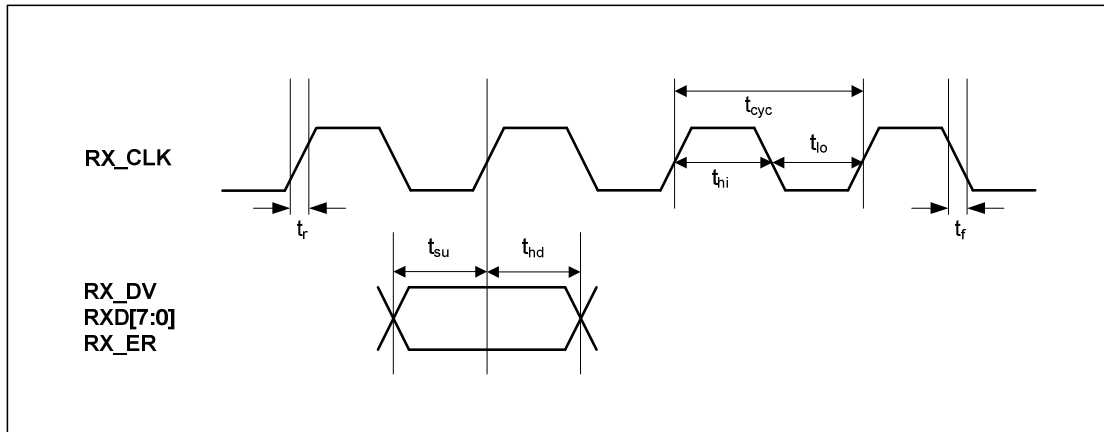


Figure 7. GMII Receive Timing – Data Input to MAC

| Timing Parameter | Description | Min | Typ | Max | Unit |
|-------------------|---|-----|-----|-----|------|
| 1000Base-T | | | | | |
| t_{cyc} | RX_CLK period | 7.5 | 8.0 | 8.5 | ns |
| t_{su} | RX_DV, RXD[7:0], RX_ER setup time to rising edge of RX_CLK | 2.5 | | | ns |
| t_{hd} | RX_DV, RXD[7:0], RX_ER hold time from rising edge of RX_CLK | 0.5 | | | ns |
| t_{hi} | RX_CLK high pulse width | 2.5 | | | ns |
| t_{lo} | RX_CLK low pulse width | 2.5 | | | ns |
| t_r | RX_CLK rise time | | | 1.0 | ns |
| t_f | RX_CLK fall time | | | 1.0 | ns |

Table 10. GMII Receive Timing Parameters

MII Transmit Timing

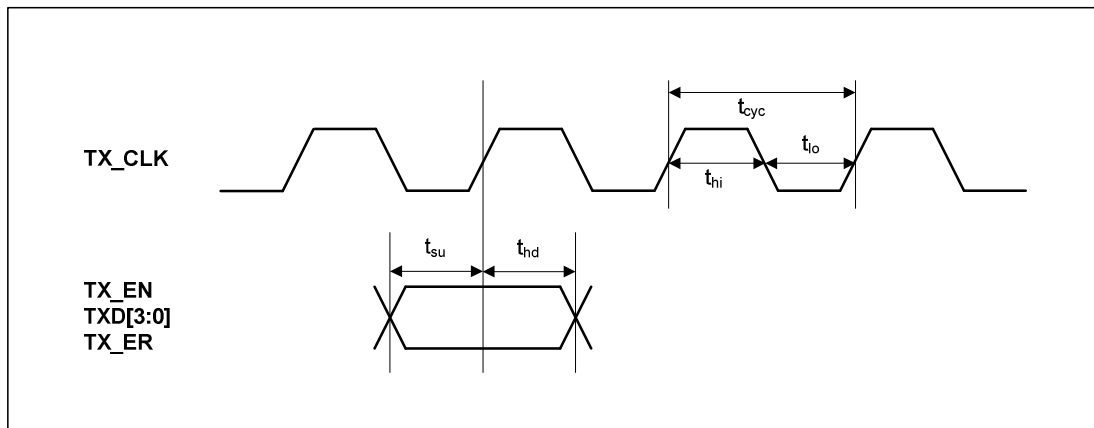


Figure 8. MII Transmit Timing – Data Input to PHY

| Timing Parameter | Description | Min | Typ | Max | Unit |
|-------------------|---|-----|-----|-----|------|
| 10Base-T | | | | | |
| t_{cyc} | TX_CLK period | | 400 | | ns |
| t_{su} | TX_EN, TXD[3:0], TX_ER setup time to rising edge of TX_CLK | 15 | | | ns |
| t_{hd} | TX_EN, TXD[3:0], TX_ER hold time from rising edge of TX_CLK | 0 | | | ns |
| t_{hi} | TX_CLK high pulse width | 140 | | 260 | ns |
| t_{lo} | TX_CLK low pulse width | 140 | | 260 | ns |
| 100Base-TX | | | | | |
| t_{cyc} | TX_CLK period | | 40 | | ns |
| t_{su} | TX_EN, TXD[3:0], TX_ER setup time to rising edge of TX_CLK | 15 | | | ns |
| t_{hd} | TX_EN, TXD[3:0], TX_ER hold time from rising edge of TX_CLK | 0 | | | ns |
| t_{hi} | TX_CLK high pulse width | 14 | | 26 | ns |
| t_{lo} | TX_CLK low pulse width | 14 | | 26 | ns |

Table 11. MII Transmit Timing Parameters

MII Receive Timing

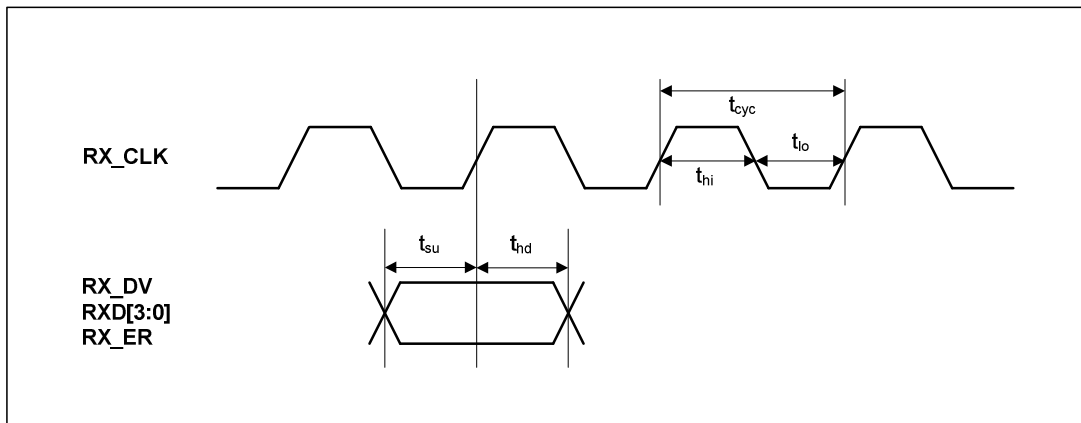


Figure 9. MII Receive Timing – Data Input to MAC

| Timing Parameter | Description | Min | Typ | Max | Unit |
|-------------------|---|-----|-----|-----|------|
| 10Base-T | | | | | |
| t_{cyc} | RX_CLK period | | 400 | | ns |
| t_{su} | RX_DV, RXD[3:0], RX_ER setup time to rising edge of RX_CLK | 10 | | | ns |
| t_{hd} | RX_DV, RXD[3:0], RX_ER hold time from rising edge of RX_CLK | 10 | | | ns |
| t_{hi} | RX_CLK high pulse width | 140 | | 260 | ns |
| t_{lo} | RX_CLK low pulse width | 140 | | 260 | ns |
| 100Base-TX | | | | | |
| t_{cyc} | RX_CLK period | | 40 | | ns |
| t_{su} | RX_DV, RXD[3:0], RX_ER setup time to rising edge of RX_CLK | 10 | | | ns |
| t_{hd} | RX_DV, RXD[3:0], RX_ER hold time from rising edge of RX_CLK | 10 | | | ns |
| t_{hi} | RX_CLK high pulse width | 14 | | 26 | ns |
| t_{lo} | RX_CLK low pulse width | 14 | | 26 | ns |

Table 12. MII Receive Timing Parameters

Auto-Negotiation Timing

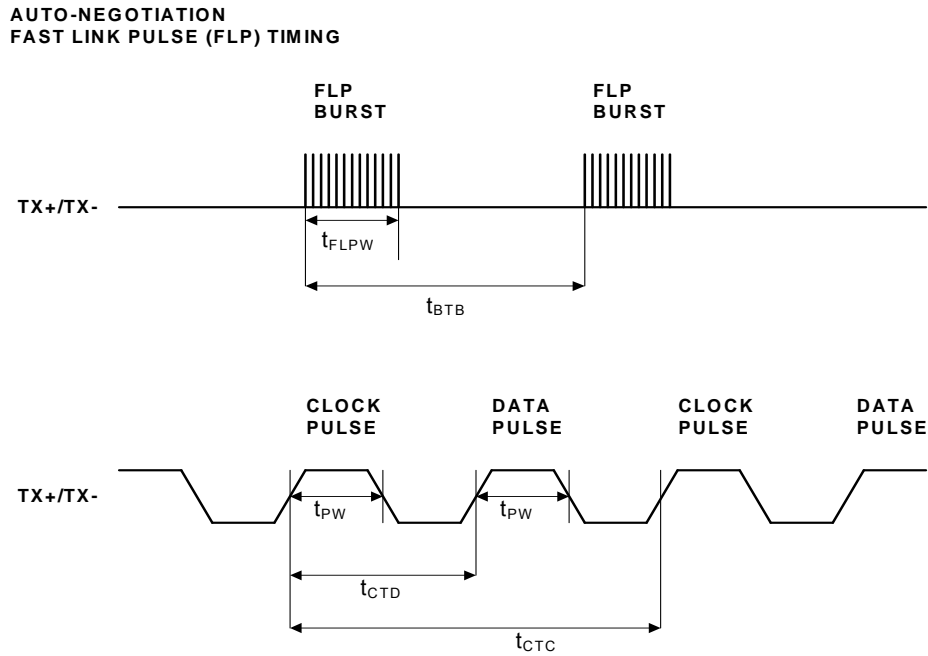


Figure 10. Auto-Negotiation Fast Link Pulse (FLP) Timing

| Timing Parameter | Description | Min | Typ | Max | Units |
|------------------|--|------|-----|------|---------|
| t_{BTB} | FLP Burst to FLP Burst | 8 | 16 | 24 | ms |
| t_{FLPW} | FLP Burst width | | 2 | | ms |
| t_{PW} | Clock/Data Pulse width | | 100 | | ns |
| t_{CTD} | Clock Pulse to Data Pulse | 55.5 | 64 | 69.5 | μ s |
| t_{CTC} | Clock Pulse to Clock Pulse | 111 | 128 | 139 | μ s |
| | Number of Clock/Data Pulse per FLP Burst | 17 | | 33 | |

Table 13. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

MDC/MDIO Timing

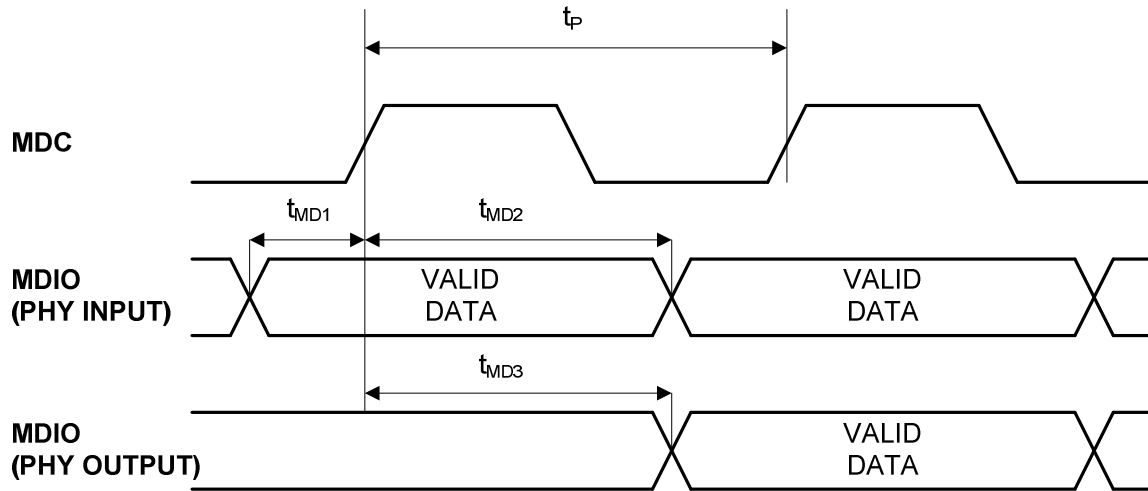


Figure 11. MDC/MDIO Timing

| Timing Parameter | Description | Min | Typ | Max | Unit |
|------------------|---|-----|-----|-----|------|
| t_P | MDC period | | 400 | | ns |
| t_{1MD1} | MDIO (PHY input) setup to rising edge of MDC | 10 | | | ns |
| t_{MD2} | MDIO (PHY input) hold from rising edge of MDC | 10 | | | ns |
| t_{MD3} | MDIO (PHY output) delay from rising edge of MDC | 0 | | | ns |

Table 14. MDC/MDIO Timing Parameters

Reset Timing

The recommended KSZ9021GN power-up reset timing is summarized in the following figure and table.

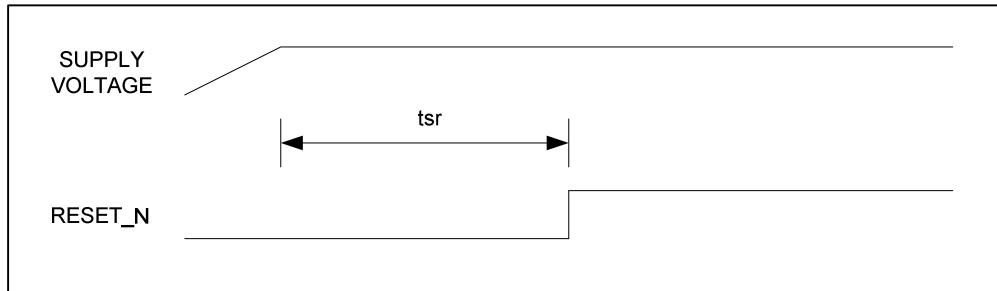


Figure 12. Reset Timing

| Parameter | Description | Min | Max | Units |
|-----------|-------------------------------------|-----|-----|-------|
| t_{sr} | Stable supply voltage to reset high | 10 | | ms |

Table 15. Reset Timing Parameters

After the de-assertion of reset, it is recommended to wait a minimum of 100 μ s before starting programming on the MIIM (MDC/MDIO) Interface.

Reset Circuit

The following reset circuit is recommended for powering up the KSZ9021GN if reset is triggered by the power supply.

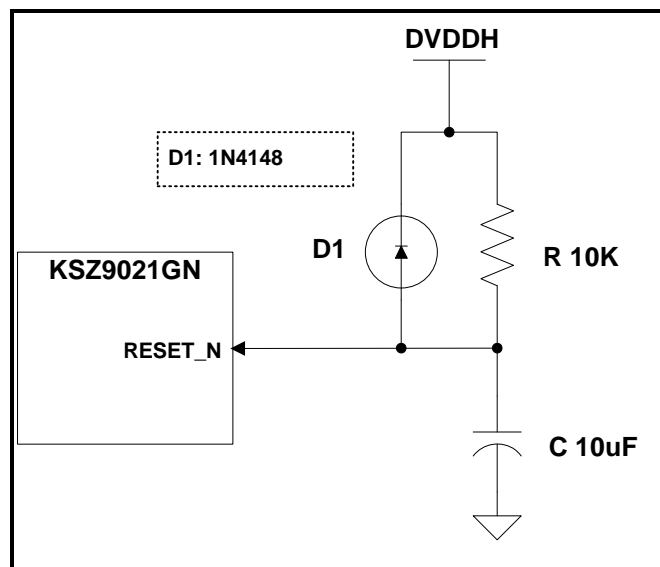


Figure 13. Recommended Reset Circuit

The following reset circuit is recommended for applications where reset is driven by another device (e.g., CPU or FPGA). At power-on-reset, R, C and D1 provide the necessary ramp rise time to reset the KSZ9021GN device. The RST_OUT_N from CPU/FPGA provides the warm reset after power up.

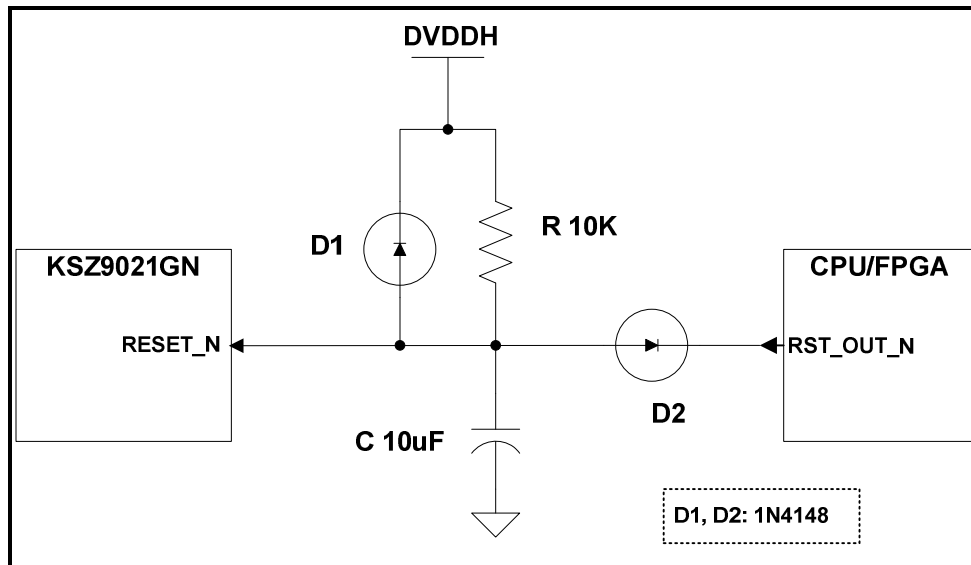


Figure 14. Recommended Reset Circuit for Interfacing with CPU/FPGA Reset Output.

Reference Circuits – LED Strap-in Pins

The pull-up and pull-down reference circuits for the LED2/PHYAD1 and LED1/PHYAD0 strapping pins are shown in the following figure.

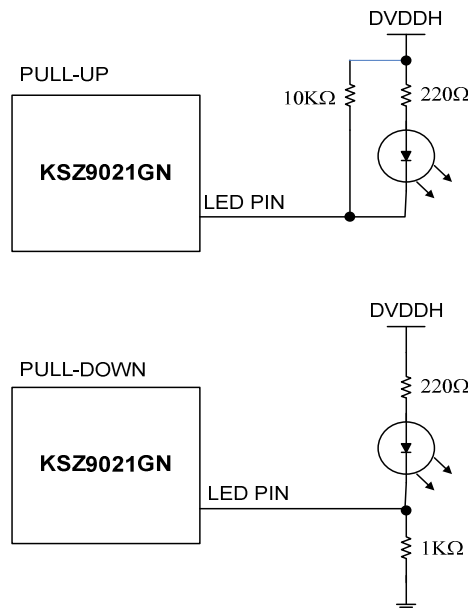


Figure 15. Reference Circuits for LED Strapping Pins

Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ9021GN. The reference clock is 25 MHz for all operating modes of the KSZ9021GN.

The following figure and table shows the reference clock connection to XI (pin 61) and XO (pin 60) of the KSZ9021GN, and the reference clock selection criteria.

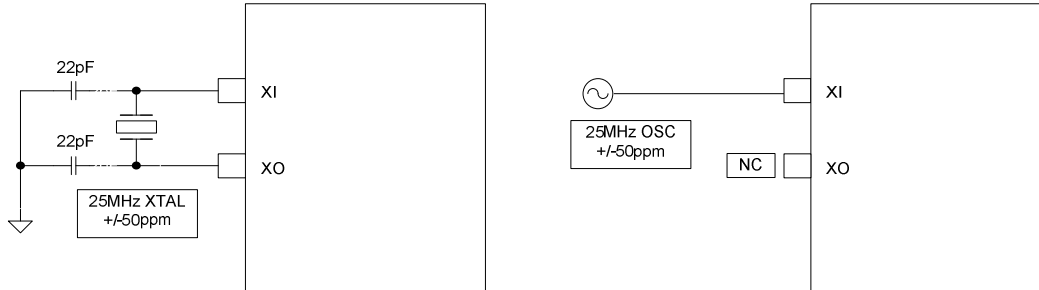


Figure 16. 25MHz Crystal / Oscillator Reference Clock Connection

| Characteristics | Value | Units |
|---------------------------|-------|-------|
| Frequency | 25 | MHz |
| Frequency tolerance (max) | ±50 | ppm |

Table 16. Reference Crystal/Clock Selection Criteria

Magnetics Specification

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode chokes is recommended for exceeding FCC requirements.

The following tables provide recommended magnetic characteristics and a list of qualified magnetics for the KSZ9021GN.

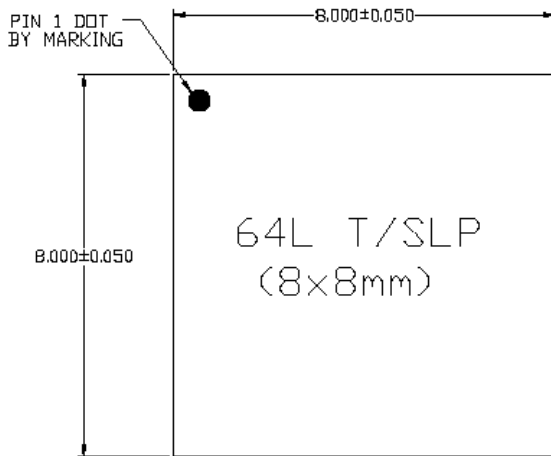
| Parameter | Value | Test Condition |
|--------------------------------|-------------|--------------------|
| Turns ratio | 1 CT : 1 CT | |
| Open-circuit inductance (min.) | 350μH | 100mV, 100kHz, 8mA |
| Insertion loss (max.) | 1.0dB | 0MHz – 100MHz |
| HIPOT (min.) | 1500Vrms | |

Table 17. Magnetics Selection Criteria

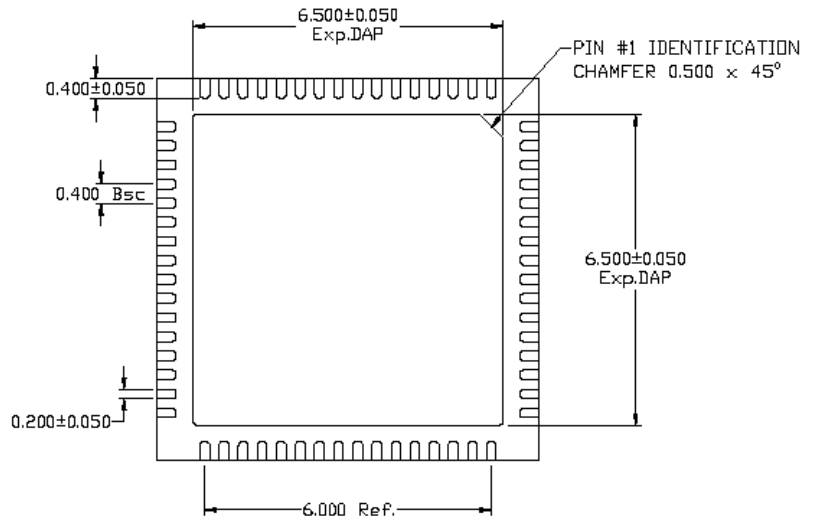
| Magnetic Manufacturer | Part Number | Auto MDI-X | Number of Port |
|-----------------------|-------------|------------|----------------|
| Pulse | H5007NL | Yes | 1 |
| TDK | TLA-7T101LF | Yes | 1 |

Table 18. Qualified Single Port 10/100/1000 Magnetics

Package Information



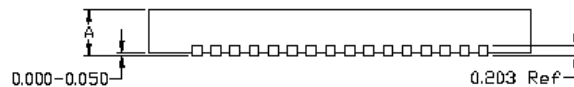
TOP VIEW



BOTTOM VIEW

NOTE:
 1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

| | | TSLP | SLP |
|---|------|-------|-------|
| A | MAX. | 0.800 | 0.900 |
| | NOM. | 0.750 | 0.850 |
| | MIN. | 0.700 | 0.800 |



SIDE VIEW

64-Pin (8mm x 8mm) QFN

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