

## High-Speed CMOS Logic Decade Counter/Divider with 10 Decoded Outputs

### Features

- Fully Static Operation
- Buffered Inputs
- Common Reset
- Positive Edge Clocking
- Typical  $f_{MAX} = 50\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$

### Description

The 'HC4017 is a high speed silicon gate CMOS 5-stage Johnson counter with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition clock period of the 10 clock period cycle. The CARRY (TC) output transitions low to high after OUTPUT 10 goes from high to low, and can be used in conjunction with the CLOCK ENABLE ( $\overline{CE}$ ) to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET (MR) input is also provided which when taken high sets all the decoded outputs, except "0", low.

The device can drive up to 10 low power Schottky equivalent loads.

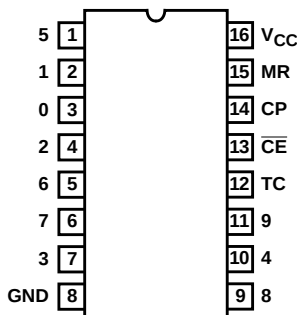
### Ordering Information

| PART NUMBER   | TEMP. RANGE<br>( $^\circ\text{C}$ ) | PACKAGE      |
|---------------|-------------------------------------|--------------|
| CD54HC4017F3A | -55 to 125                          | 16 Ld CERDIP |
| CD74HC4017E   | -55 to 125                          | 16 Ld PDIP   |
| CD74HC4017M   | -55 to 125                          | 16 Ld SOIC   |
| CD74HC4017MT  | -55 to 125                          | 16 Ld SOIC   |
| CD74HC4017M96 | -55 to 125                          | 16 Ld SOIC   |
| CD74HC4017NSR | -55 to 125                          | 16 Ld SOP    |
| CD74HC4017PW  | -55 to 125                          | 16 Ld TSSOP  |
| CD74HC4017PWR | -55 to 125                          | 16 Ld TSSOP  |

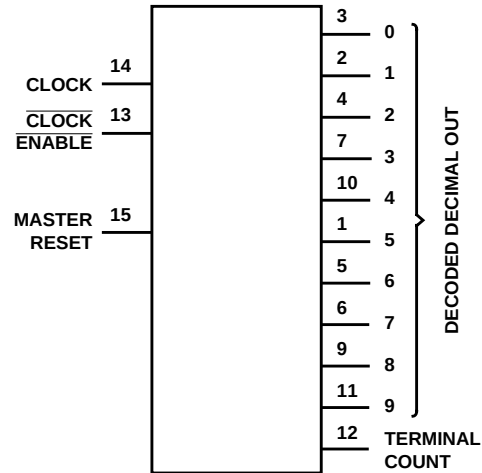
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout

CD54HC4017 (CERDIP)  
CD74HC4017 (PDIP, SOIC, SOP, TSSOP)  
TOP VIEW



## Functional Diagram



TRUTH TABLE

| CP | $\overline{CE}$ | MR | OUTPUT STATE †        |
|----|-----------------|----|-----------------------|
| L  | X               | L  | No Change             |
| X  | H               | L  | No Change             |
| X  | X               | H  | "0" = H, "1"- "9" = L |
| ↑  | L               | L  | Increments Counter    |
| ↓  | X               | L  | No Change             |
| X  | ↑               | L  | No Change             |
| H  | ↓               | L  | Increments Counter    |

H = High Level

L = Low Level

↑ = High to Low Transition

↓ = Low to High Transition

X = Don't Care.

† If  $n < 5$  TC = H, Otherwise = L

# CD54HC4017, CD74HC4017

## Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 7V  
 DC Input Diode Current,  $I_{IK}$   
     For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
     For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
     For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 25mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  .....  $\pm 50mA$

## Thermal Information

Package Thermal Impedance,  $\theta_{JA}$  (see Note 1):  
     E (PDIP) Package .....  $67^{\circ}C/W$   
     M (SOIC) Package .....  $73^{\circ}C/W$   
     NS (SOP) Package .....  $64^{\circ}C/W$   
     PW (TSSOP) Package .....  $108^{\circ}C/W$   
 Maximum Junction Temperature .....  $150^{\circ}C$   
 Maximum Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) .....  $300^{\circ}C$   
     (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range,  $T_A$  .....  $-55^{\circ}C$  to  $125^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$   
     HC Types ..... 2V to 6V  
     HCT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$   
 Input Rise and Fall Time  
     2V ..... 1000ns (Max)  
     4.5V ..... 500ns (Max)  
     6V ..... 400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |      |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|------------------------------------|---------------------|---------------------|------|------|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP  | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                   | 1.5  | -    | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                    |                     | 4.5                 | 3.15 | -    | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                    |                     | 6                   | 4.2  | -    | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                   | -    | -    | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                    |                     | 4.5                 | -    | -    | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                    |                     | 6                   | -    | -    | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -    | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                    | -0.02               | 4.5                 | 4.4  | -    | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                    | -0.02               | 6                   | 5.9  | -    | -    | 5.9           | -    | 5.9            | -    | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| -4                                      |                 |                                    | 4.5                 | 3.98                | -    | -    | 3.84 | -             | 3.7  | -              | V    |       |
| -5.2                                    |                 |                                    | 6                   | 5.48                | -    | -    | 5.34 | -             | 5.2  | -              | V    |       |
| High Level Output Voltage<br>TTL Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| 4                                       |                 |                                    | 4.5                 | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| 5.2                                     |                 |                                    | 6                   | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| 0.02                                    |                 |                                    | 4.5                 | -                   | -    | 0.1  | -    | 0.1           | -    | 0.1            | V    |       |
| 0.02                                    |                 |                                    | 6                   | -                   | -    | 0.1  | -    | 0.1           | -    | 0.1            | V    |       |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -                   | -                   | -    | -    | -    | -             | -    | -              | -    | V     |
|                                         |                 |                                    | 4                   | 4.5                 | -    | -    | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                    | 5.2                 | 6                   | -    | -    | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or GND             | -                   | 6                   | -    | -    | ±0.1 | -             | ±1   | -              | ±1   | µA    |
| Quiescent Device Current                | I <sub>CC</sub> | V <sub>CC</sub> or GND             | 0                   | 6                   | -    | -    | 8    | -             | 80   | -              | 160  | µA    |

# CD54HC4017, CD74HC4017

## Prerequisite for Switching Specifications

| PARAMETER                                 | SYMBOL           | TEST CONDITIONS | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-------------------------------------------|------------------|-----------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                           |                  |                 |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Maximum Clock Frequency                   | f <sub>MAX</sub> | -               | 2                   | 6    | -   | -   | 5             | -   | 4              | -   | MHz   |
|                                           |                  |                 | 4.5                 | 30   | -   | -   | 35            | -   | 20             | -   | MHz   |
|                                           |                  |                 | 6                   | 35   | -   | -   | 49            | -   | 23             | -   | MHz   |
| CP Pulse Width                            | t <sub>W</sub>   | -               | 2                   | 80   | -   | -   | 100           | -   | 120            | -   | ns    |
|                                           |                  |                 | 4.5                 | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                                           |                  |                 | 6                   | 14   | -   | -   | 17            | -   | 20             | -   | ns    |
| MR Pulse Width                            | t <sub>W</sub>   | -               | 2                   | 80   | -   | -   | 100           | -   | 120            | -   | ns    |
|                                           |                  |                 | 4.5                 | 16   | -   | -   | 20            | -   | 24             | -   | ns    |
|                                           |                  |                 | 6                   | 14   | -   | -   | 17            | -   | 20             | -   | ns    |
| Set-up Time, $\overline{\text{CE}}$ to CP | t <sub>SU</sub>  | -               | 2                   | 75   | -   | -   | 95            | -   | 110            | -   | ns    |
|                                           |                  |                 | 4.5                 | 15   | -   | -   | 19            | -   | 22             | -   | ns    |
|                                           |                  |                 | 6                   | 13   | -   | -   | 16            | -   | 19             | -   | ns    |
| Hold Time, $\overline{\text{CE}}$ to CP   | t <sub>H</sub>   | -               | 2                   | 0    | -   | -   | 0             | -   | 0              | -   | ns    |
|                                           |                  |                 | 4.5                 | 0    | -   | -   | 0             | -   | 0              | -   | ns    |
|                                           |                  |                 | 6                   | 0    | -   | -   | 0             | -   | 0              | -   | ns    |
| MR Removal Time                           | t <sub>REM</sub> | -               | 2                   | 5    | -   | -   | 5             | -   | 5              | -   | ns    |
|                                           |                  |                 | 4.5                 | 5    | -   | -   | 5             | -   | 5              | -   | ns    |
|                                           |                  |                 | 6                   | 5    | -   | -   | 5             | -   | 5              | -   | ns    |

## Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                               | SYMBOL                                 | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------------|----------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                         |                                        |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| Propagation Delay<br>CP to any Dec. Out | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 230 | -             | 290 | -              | 345 | ns    |
|                                         |                                        | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 46  | -             | 58  | -              | 69  | ns    |
|                                         |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 19  | -   | -             | -   | -              | -   | ns    |
|                                         |                                        | C <sub>L</sub> = 50pF | 6                   | -    | -   | 39  | -             | 49  | -              | 59  | ns    |
| CP to TC                                | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 230 | -             | 290 | -              | 345 | ns    |
|                                         |                                        | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 46  | -             | 58  | -              | 69  | ns    |
|                                         |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 19  | -   | -             | -   | -              | -   | ns    |
|                                         |                                        | C <sub>L</sub> = 50pF | 6                   | -    | -   | 39  | -             | 49  | -              | 59  | ns    |
| $\overline{\text{CE}}$ to any Dec. Out  | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 250 | -             | 315 | -              | 375 | ns    |
|                                         |                                        | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 50  | -             | 63  | -              | 75  | ns    |
|                                         |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 21  | -   | -             | -   | -              | -   | ns    |
|                                         |                                        | C <sub>L</sub> = 50pF | 6                   | -    | -   | 43  | -             | 54  | -              | 64  | ns    |
| $\overline{\text{CE}}$ to TC            | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 250 | -             | 315 | -              | 375 | ns    |
|                                         |                                        | C <sub>L</sub> = 50pF | 4.5                 | -    | -   | 50  | -             | 63  | -              | 75  | ns    |
|                                         |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 21  | -   | -             | -   | -              | -   | ns    |
|                                         |                                        | C <sub>L</sub> = 50pF | 6                   | -    | -   | 43  | -             | 54  | -              | 64  | ns    |

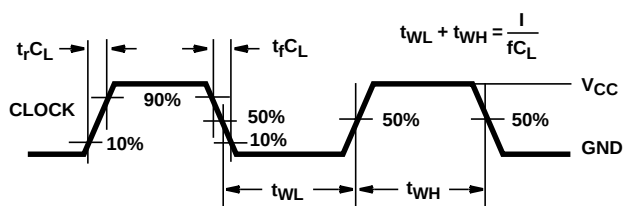
Switching Specifications Input  $t_r, t_f = 6\text{ns}$  (Continued)

| PARAMETER                                     | SYMBOL             | TEST CONDITIONS     | $V_{CC}$<br>(V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------------------|--------------------|---------------------|-----------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                               |                    |                     |                 | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| MR to any Dec. Out                            | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 2               | -    | -   | 230 | -             | 290 | -              | 345 | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 46  | -             | 58  | -              | 69  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 19  | -   | -             | -   | -              | -   | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 6               | -    | -   | 39  | -             | 49  | -              | 59  | ns    |
| MR to TC                                      | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 2               | -    | -   | 230 | -             | 290 | -              | 345 | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 46  | -             | 58  | -              | 69  | ns    |
|                                               |                    | $C_L = 15\text{pF}$ | 5               | -    | 19  | -   | -             | -   | -              | -   | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 6               | -    | -   | 39  | -             | 49  | -              | 59  | ns    |
| Transition Time TC, Dec. Out                  | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 2               | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                               |                    | $C_L = 50\text{pF}$ | 6               | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Input Capacitance                             | $C_{IN}$           | $C_L = 50\text{pF}$ | -               | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Maximum CP Frequency                          | $f_{MAX}$          | $C_L = 15\text{pF}$ | 5               | -    | 60  | -   | -             | -   | -              | -   | MHz   |
| Power Dissipation Capacitance<br>(Notes 2, 3) | $C_{PD}$           | $C_L = 15\text{pF}$ | 5               | -    | 39  | -   | -             | -   | -              | -   | pF    |

NOTES:

2.  $C_{PD}$  is used to determine the dynamic power consumption, per package.
3.  $P_D = V_{CC}^2 f_i \sum C_L V_{CC}^2 f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

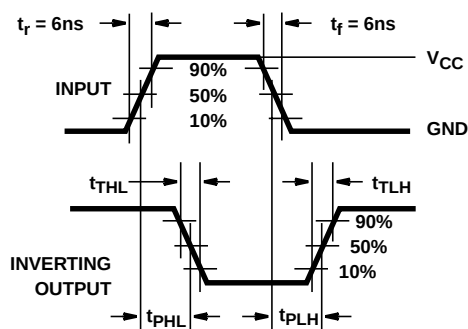


FIGURE 2. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

# Test Circuits and Waveforms (Continued)

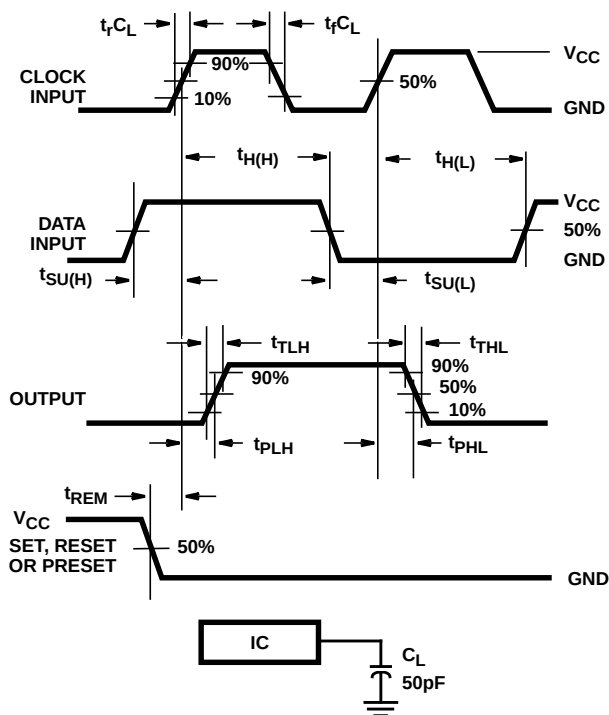


FIGURE 3. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

## Timing Diagrams

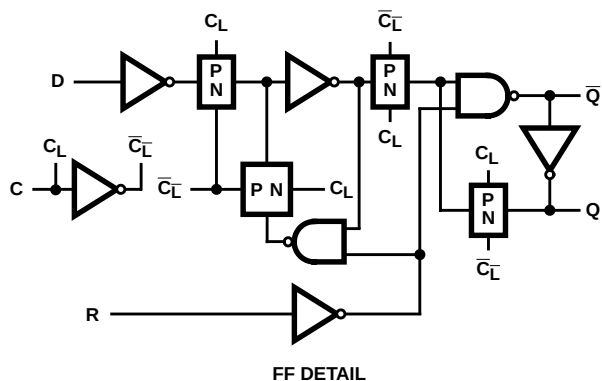


FIGURE 4.

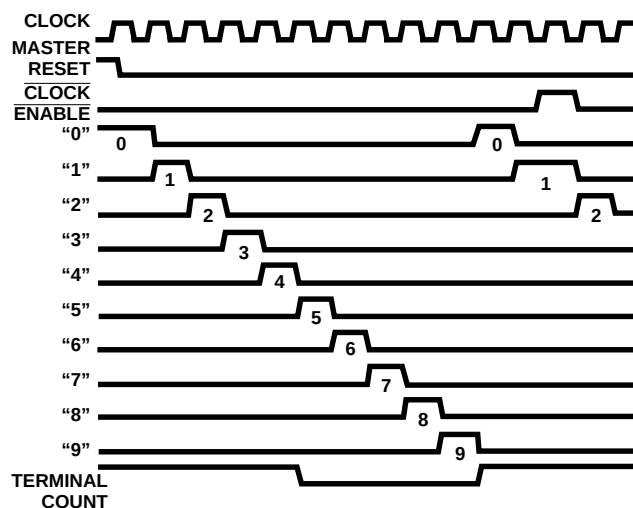


FIGURE 5.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 8601101EA        | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| CD54HC4017F3A    | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD74HC4017E      | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HC4017EE4    | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HC4017M      | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017M96    | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017M96E4  | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017M96G4  | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017ME4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017MG4    | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017MT     | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017MTE4   | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017MTG4   | ACTIVE                | SOIC         | D               | 16   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017NSR    | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017NSRE4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017NSRG4  | ACTIVE                | SO           | NS              | 16   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017PW     | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017PWE4   | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| CD74HC4017PWG4   | ACTIVE                | TSSOP        | PW              | 16   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017PWR    | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017PWRE4  | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017PWRG4  | ACTIVE                | TSSOP        | PW              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017PWT    | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017PWTE4  | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC4017PWTG4  | ACTIVE                | TSSOP        | PW              | 16   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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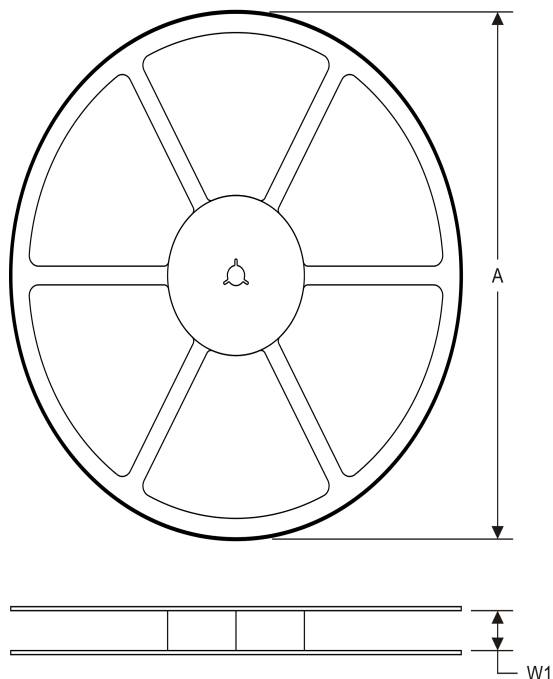
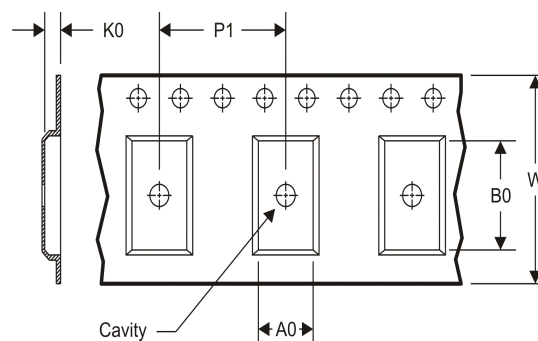
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC4017, CD74HC4017 :**

- Catalog: [CD74HC4017](#)
- Automotive: [CD74HC4017-Q1](#), [CD74HC4017-Q1](#)
- Enhanced Product: [CD74HC4017-EP](#), [CD74HC4017-EP](#)
- Military: [CD54HC4017](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


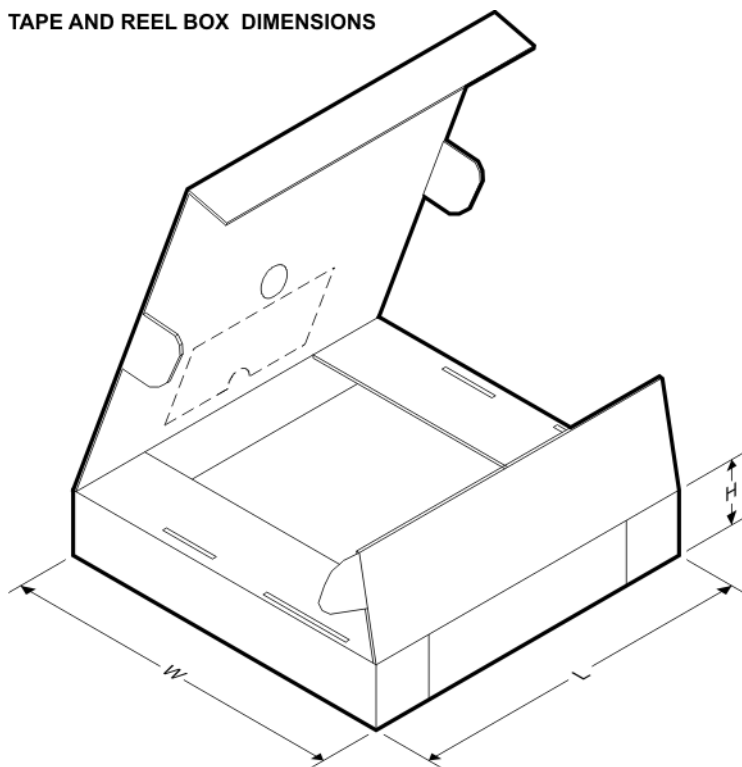
|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC4017M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC4017NSR | SO           | NS              | 16   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| CD74HC4017PWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD74HC4017PWT | TSSOP        | PW              | 16   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



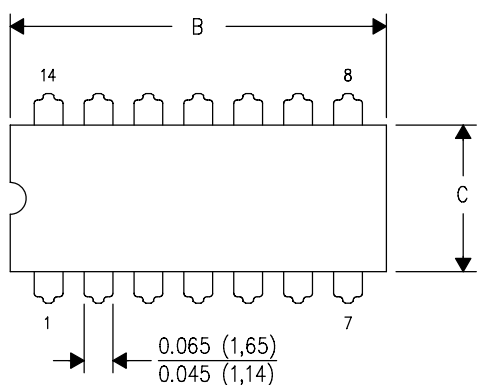
\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC4017M96 | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| CD74HC4017NSR | SO           | NS              | 16   | 2000 | 367.0       | 367.0      | 38.0        |
| CD74HC4017PWR | TSSOP        | PW              | 16   | 2000 | 367.0       | 367.0      | 35.0        |
| CD74HC4017PWT | TSSOP        | PW              | 16   | 250  | 367.0       | 367.0      | 35.0        |

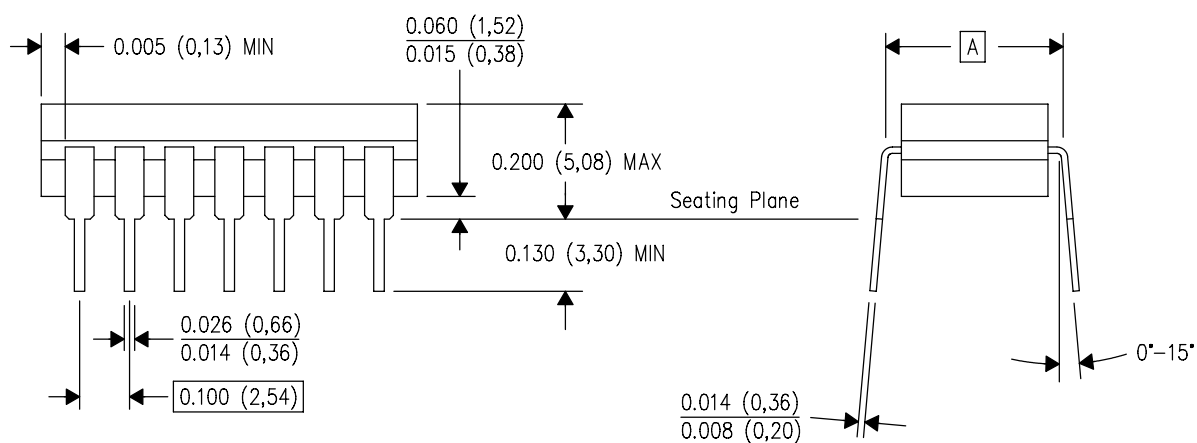
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



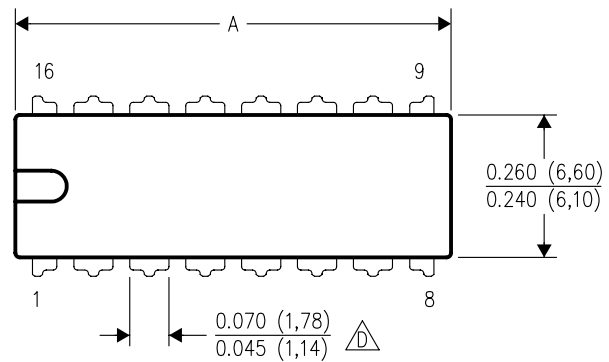
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

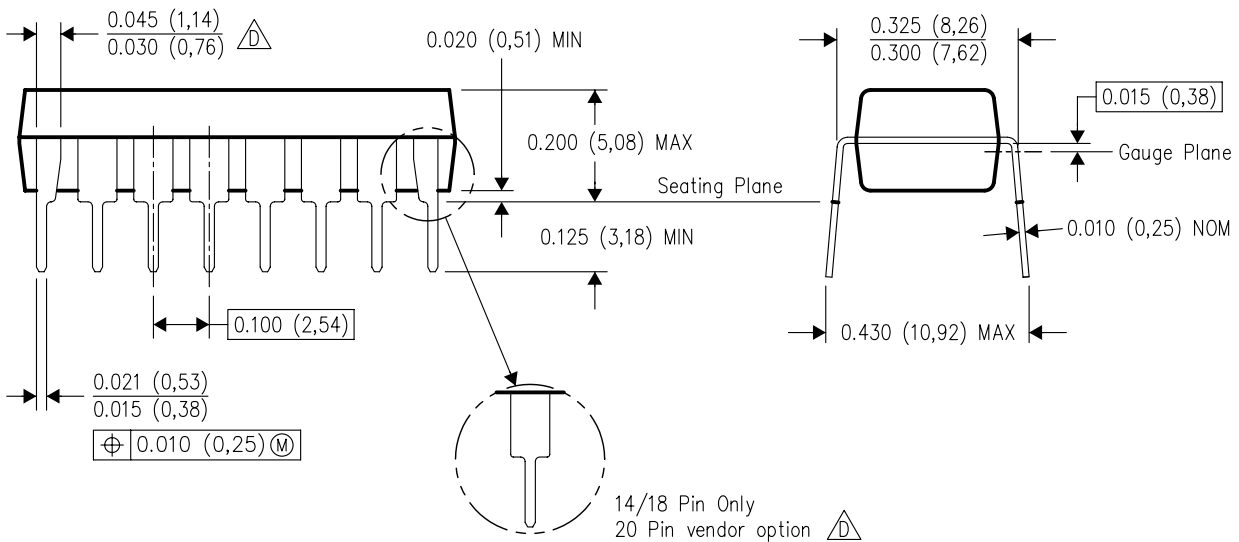
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



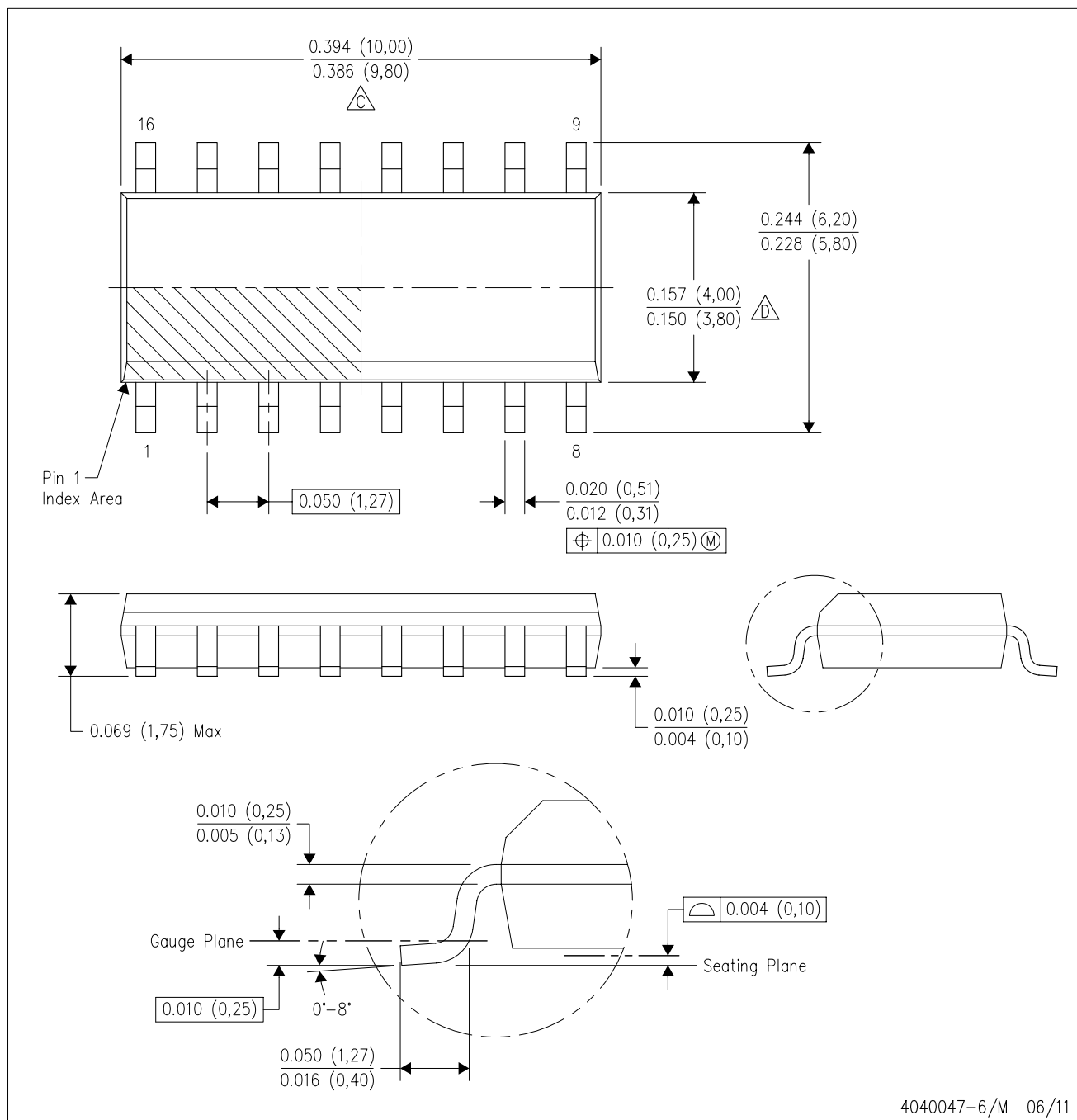
14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

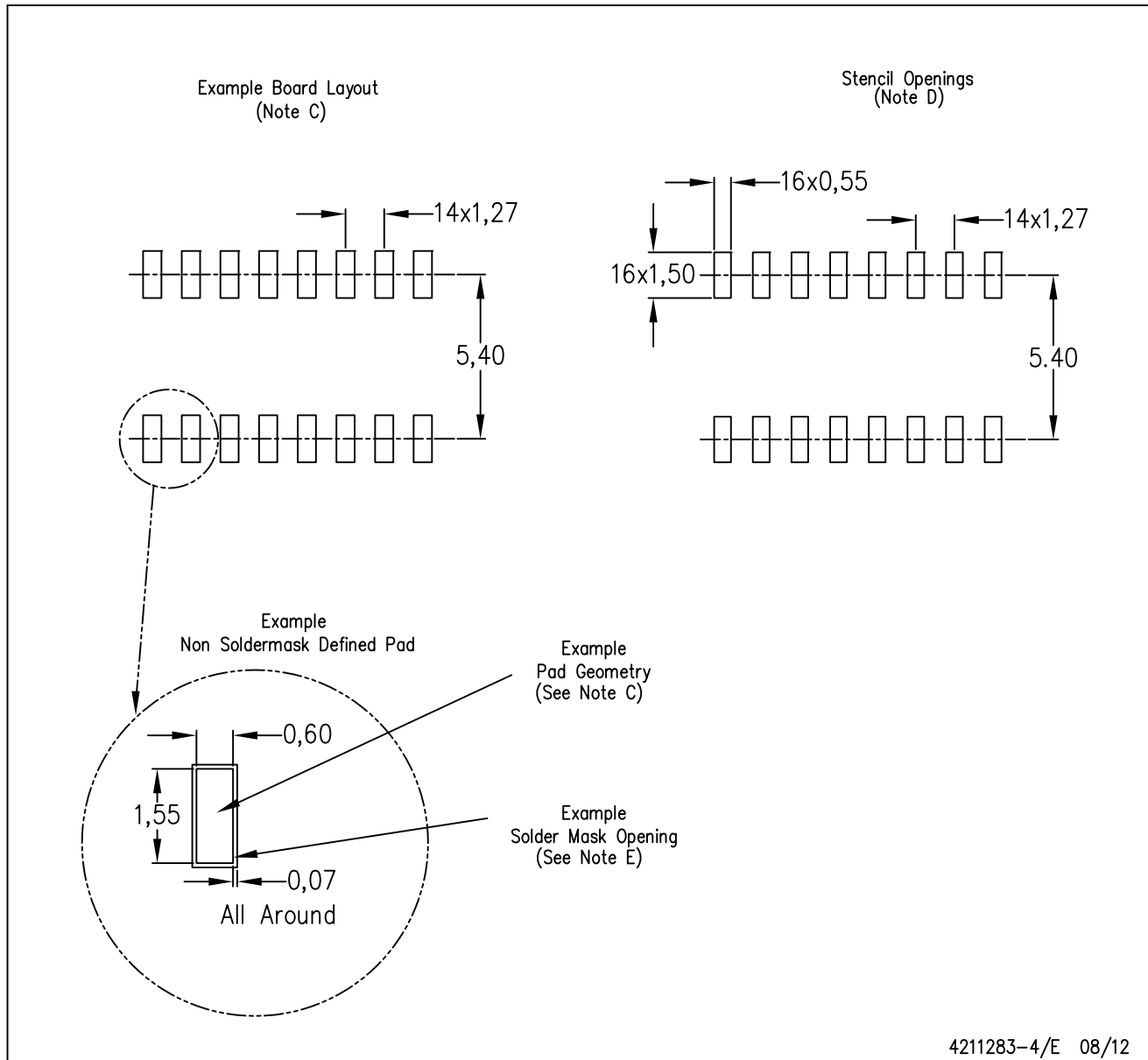


## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

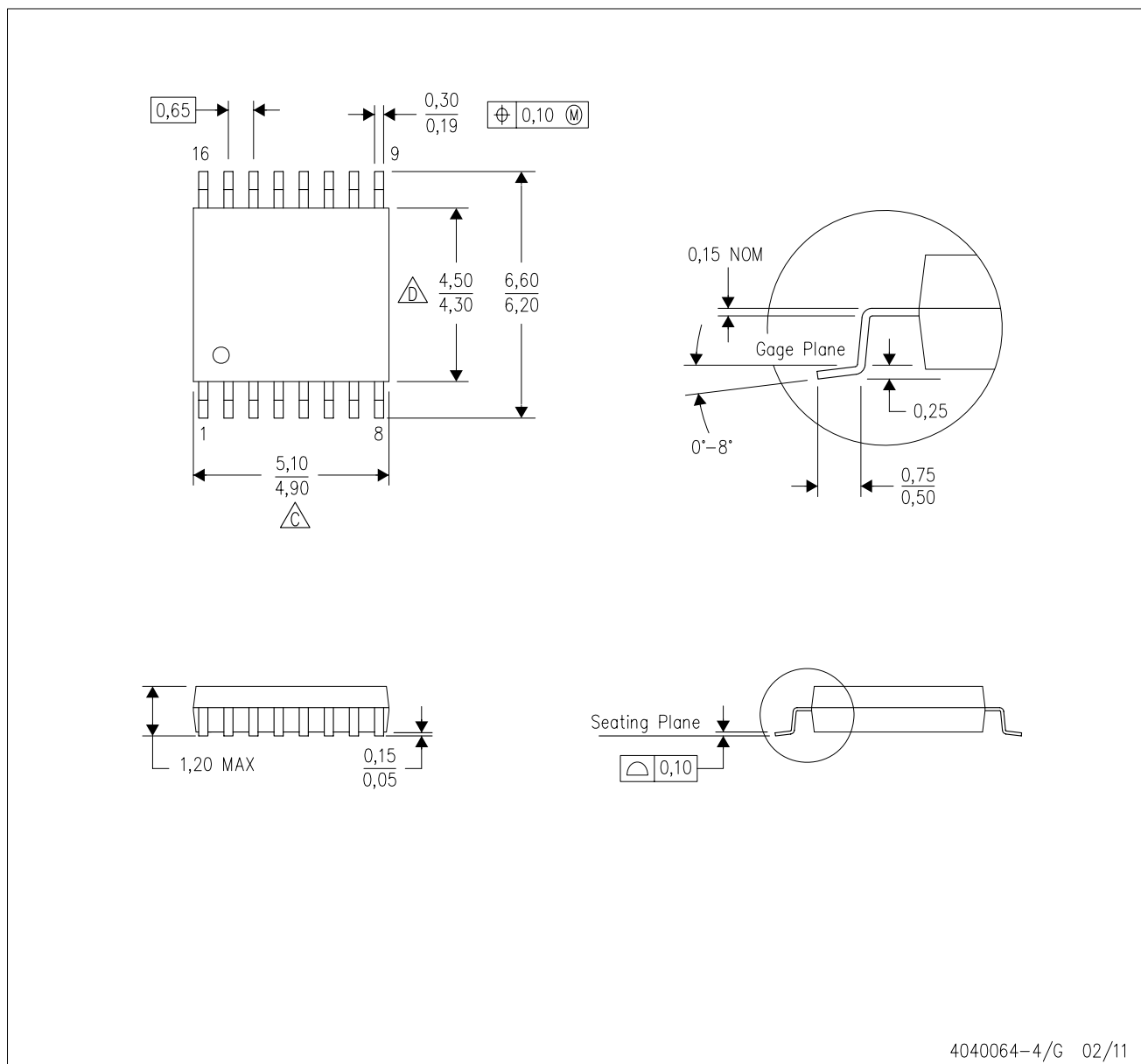
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

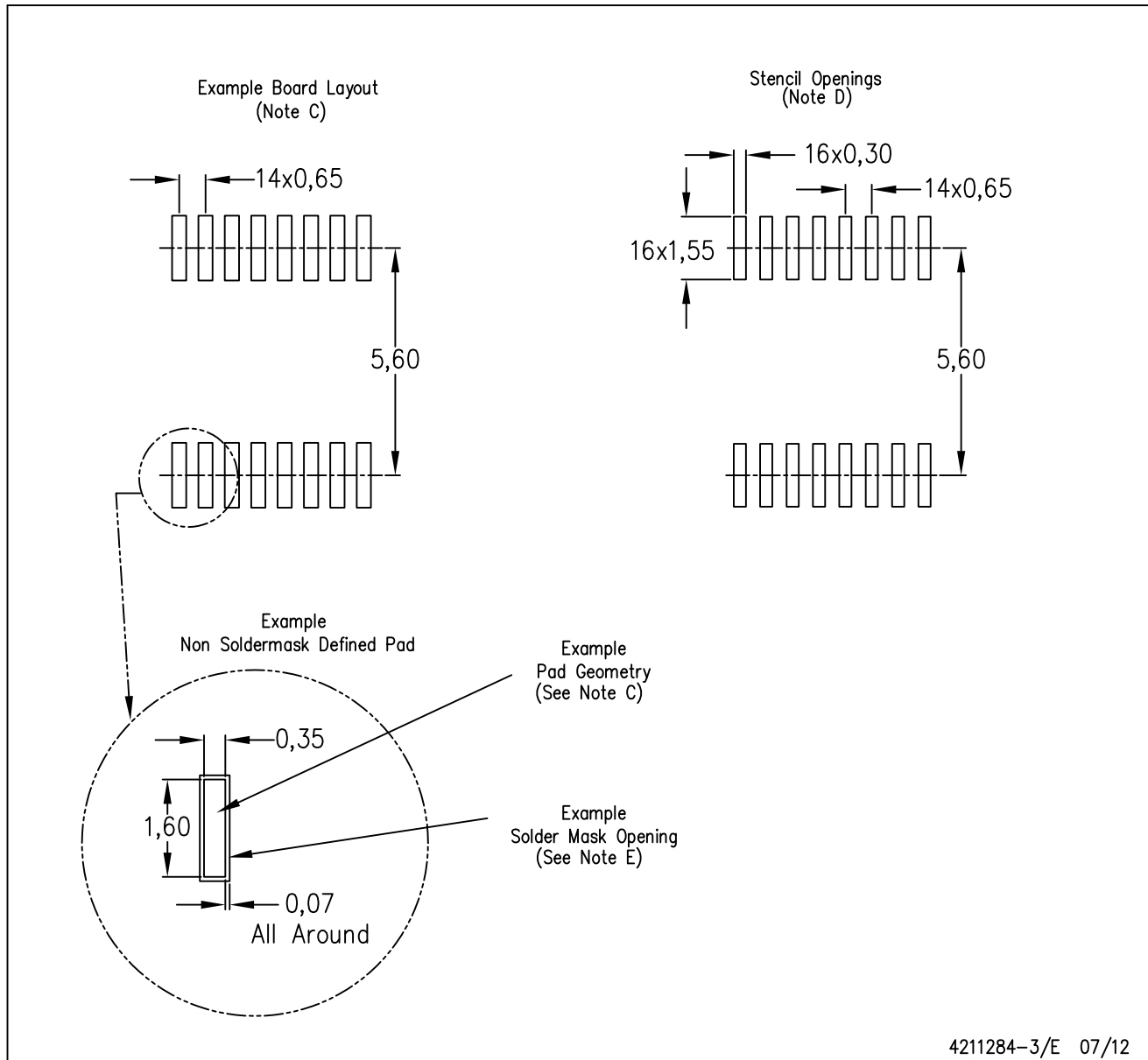


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - $\Delta$  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - $\Delta$  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



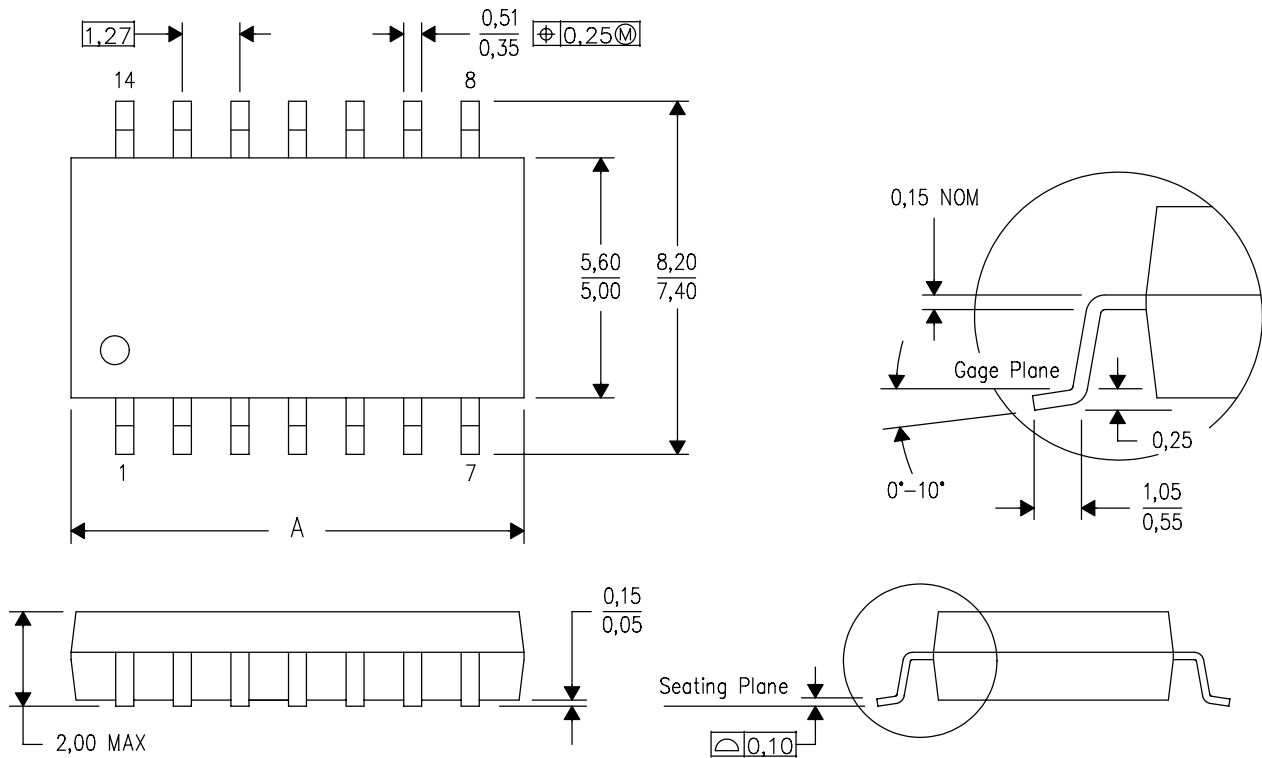
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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