

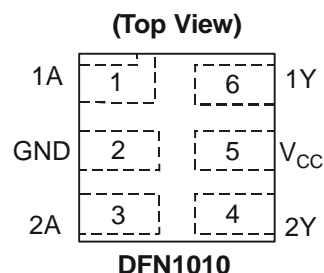
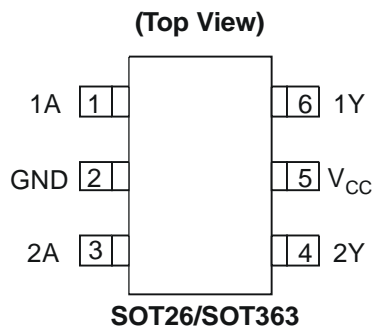
Description

The 74LVC2G14 is a dual Schmitt trigger inverter gate with standard push-pull outputs. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output preventing damaging current backflow when the device is powered down.

The gate performs the positive Boolean function:

$$Y = \overline{A}$$

Pin Assignments



Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- ±24mA Output Drive at 3.0V
- CMOS low power consumption
- IOFF Supports Partial-Power-Down Mode Operation
- Inputs accept up to 5.5V
- ESD Protection Tested per JESD 22
 - Exceeds 200-V Machine Model (A115-A)
 - Exceeds 2000-V Human Body Model (A114-A)
 - Exceeds 1000-V Charged Device Model (C101)
- Latch-Up Exceeds 100mA per JESD 78, Class II
- Range of Package Options
- SOT26, SOT363, and DFN1010 Available in “Green” Molding Compound (no Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

Applications

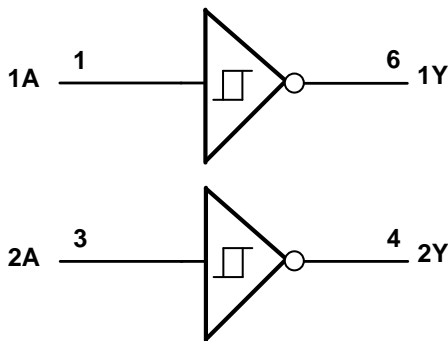
- Voltage Level Shifting
- General Purpose Logic
- Power Down Signal Isolation
- Wide array of products such as:
 - PCs, networking, notebooks, netbooks, PDAs
 - Computer peripherals, hard drives, CD/DVD ROM
 - TV, DVD, DVR, set top box
 - Cell Phones, Personal Navigation / GPS
 - MP3 players, Cameras, Video Recorders

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

Pin Descriptions

Pin Name	Pin NO.	Description
1A	1	Data Input
GND	2	Ground
2A	3	Data Input
2Y	4	Data Output
V _{CC}	5	Supply Voltage
1Y	6	Data Output

Logic Diagram



Function Table

Inputs	Output
A	Y
H	L
L	H

Absolute Maximum Ratings (Note 2)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD CDM	Charged Device Model ESD Protection	1	KV
ESD MM	Machine Model ESD Protection	200	V
V _{CC}	Supply Voltage Range	-0.5 to 6.5	V
V _I	Input Voltage Range	-0.5 to 6.5	V
V _O	Voltage applied to output in high impedance or I _{OFF} state	-0.5 to 6.5	V
V _O	Voltage applied to output in high or low state.	-0.3 to V _{CC} +0.5	V
I _{IK}	Input Clamp Current V _I <0	-50	mA
I _{OK}	Output Clamp Current	-50	mA
I _O	Continuous output current	±50	mA
	Continuous current through V _{DD} or GND	±100	mA
T _J	Operating Junction Temperature	-40 to 150	°C
T _{STG}	Storage Temperature	-65 to 150	°C

Notes: 2. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Operating Voltage	Operating	1.65	5.5	V
		Data retention only	1.5		V
V _I	Input Voltage	0	5.5	V	
V _O	Output Voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65V		-4	mA
		V _{CC} = 2.3V		-8	
		V _{CC} = 3V		-16	
		V _{CC} = 4.5V		-24	
I _{OL}	Low-level output current	V _{CC} = 1.65V		4	mA
		V _{CC} = 2.3V		8	
		V _{CC} = 3V		16	
		V _{CC} = 4.5V		24	
Δt/ΔV	Input transition rise or fall rate	V _{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V _{CC} = 3.3V ± 0.3V		10	
		V _{CC} = 5V ± 0.5V		5	
T _A	Operating free-air temperature	-40	125	°C	

Notes: 3. Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics

Symbol	Parameter	Test Conditions	V _{CC}	40°C to 85°C		-40°C to 125°C		Unit
				Min	Max	Min	Max	
V _{T+}	Positive-going input threshold Voltage		1.8V	0.70	1.50	0.70	1.70	V
			2.3V	1.00	1.80	1.00	2.00	
			3V	1.30	2.20	1.30	2.40	
			4.5V	1.90	3.10	1.90	3.30	
			5.5V	2.20	3.60	2.20	3.80	
V _{T-}	Negative-going input threshold Voltage		1.65V	0.25	0.90	0.39	1.10	V
			2.3V	0.40	1.15	0.25	0.87	
			3V	0.60	1.50	0.40	1.35	
			4.5V	1.00	2.00	0.60	1.70	
			5.5V	1.20	2.30	1.00	2.50	
ΔV _T	Hysteresis (V _{T+} - V _{T-})		1.8V	0.15	1.00	0.37	1.20	μA
			2.3V	0.25	1.10	0.15	1.30	
			3V	0.40	1.20	0.40	1.40	
			4.5V	0.60	1.50	0.60	1.70	
			5.5V	0.70	1.70	0.70	1.90	
V _{OH}	High Level Output Voltage	I _{OH} = -100 μA	1.65V to 4.5V	V _{CC} - 0.1		V _{CC} - 0.1	V	
		I _{OH} = -4 mA	1.65V	1.2		0.95		
		I _{OH} = -8 mA	2.3V	1.9		1.7		
		I _{OH} = -16 mA	3V	2.4		1.9		
		I _{OH} = -24 mA		2.3		2.0		
		I _{OH} = -32 mA	4.5V	3.8		3.4		
V _{OL}	Low-Level Output Voltage	I _{OL} = 100 μA	1.65V to 4.5V		0.1	0.10	V	
		I _{OL} = 4 mA	1.65V		0.45	0.70		
		I _{OL} = 8 mA	2.3V		0.3	0.45		
		I _{OL} = 16 mA	3V		0.4	0.60		
		I _{OL} = 24 mA			0.55	0.80		
		I _{OL} = 32 mA	4.5		0.55	0.80		
I _I	Input Current	V _I = 5.5 V or GND	0 to 5.5V		± 5	± 20	μA	
I _{OFF}	Power Down Leakage Current	V _I or V _O = 5.5V	0		± 10	± 20	μA	
I _{CC}	Supply Current	V _I = 5.5V of GND I _O =0	1.65V to 5.5V		10	40	μA	

Package Characteristics (All typical values are at $V_{CC} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Test Conditions	V_{CC}	Min	Typ.	Max	Unit
C_I	Input Capacitance	$V_I = V_{CC} - \text{or GND}$	3.3		4		pF
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT26	(Note 4)		204		$^\circ C/W$
		SOT363			371		
		DFN1010			430		
θ_{JC}	Thermal Resistance Junction-to-Case	SOT26	(Note 4)		52		$^\circ C/W$
		SOT363			143		
		DFN1010			190		

Notes: 4. Test condition for SOT26, SOT363 and DFN1010: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

Switching Characteristics

$T_A = -40^\circ C$ to $85^\circ C$, $C_L = 30$ or $50pF$ (see Figure 1)

Parameter	From (Input)	TO (OUTPUT)	$V_{CC} = 1.8V \pm 0.15V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 5V \pm 0.5V$		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	A	Y	0.5	11.0	0.5	6.5	0.5	6.0	0.5	4.3	ns

$T_A = -40^\circ C$ to $125^\circ C$, $C_L = 30$ or $50pF$ (see Figure 1)

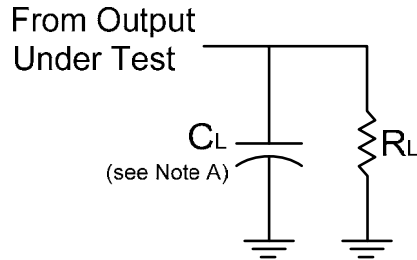
Parameter	From (Input)	TO (OUTPUT)	$V_{CC} = 1.8V \pm 0.15V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 5V \pm 0.5V$		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	A	Y	0.5	12.0	0.5	7.2	0.50	6.7	0.5	4.7	ns

Operating Characteristics

$T_A = 25^\circ C$

Parameter	Test Conditions	$V_{CC} = 1.8V$	$V_{CC} = 2.5V$	$V_{CC} = 3.3V$	$V_{CC} = 5V$	Unit
		Typ.	Typ.	Typ.	Typ.	
C_{pd}	Power dissipation capacitance $f = 10$ MHz	17	19	20	21	pF

Parameter Measurement Information



V _{CC}	Inputs		V _M	C _L	R _L
	V _I	t _r /t _f			
1.8V±0.15 V	V _{CC}	≤2ns	V _{CC} /2	30 pF	1 KΩ
2.5V±0.2 V	V _{CC}	≤2ns	V _{CC} /2	30 pF	500 Ω
3.3V±0.3 V	3 V	≤2.5ns	1.5 V	50 pF	500 Ω
5V±0.5 V	V _{CC}	≤2.5ns	V _{CC} /2	50 pF	500 Ω

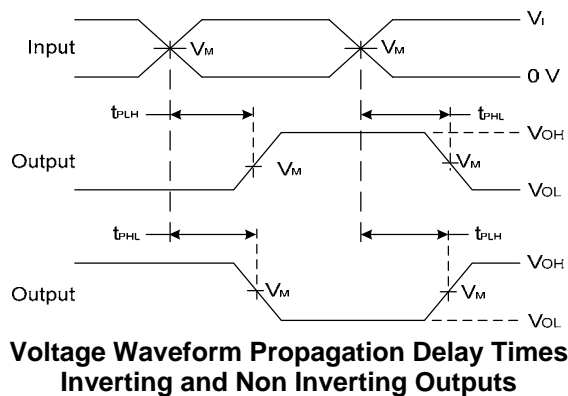
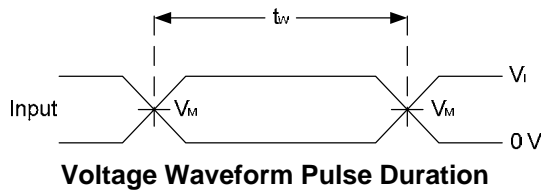
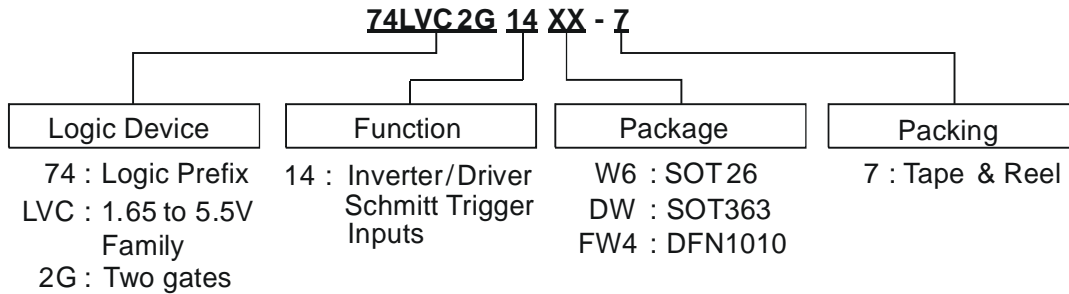


Figure 1. Load Circuit and Voltage Waveforms

- Notes:
- A. Includes test lead and test apparatus capacitance.
 - B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
 - C. Inputs are measured separately one transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{PD}.

Ordering Information

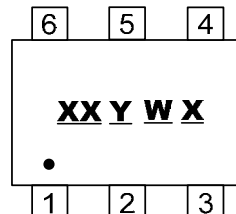


Device	Package Code	Packaging (Note 5)	7" Tape and Reel	
			Quantity	Part Number Suffix
74LVC2G14W6-7	W6	SOT26	3000/Tape & Reel	-7
74LVC2G14DW-7	DW	SOT363	3000/Tape & Reel	-7
74LVC2G14FW4-7	FW4	DFN1010	5000/Tape & Reel	-7

Notes: 5. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.
6. The taping orientation is located on our website at <http://www.diodes.com/datasheets/ap02007.pdf>

Marking Information

(1) SOT26, SOT363

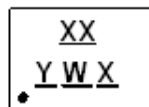


XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week
X : A~Z : Internal Code

Part Number	Package	Identification Code
74LVC2G14W6	SOT26	Z5
74LVC2G14DW	SOT363	Z5

(2) DFN1010

(Top View)

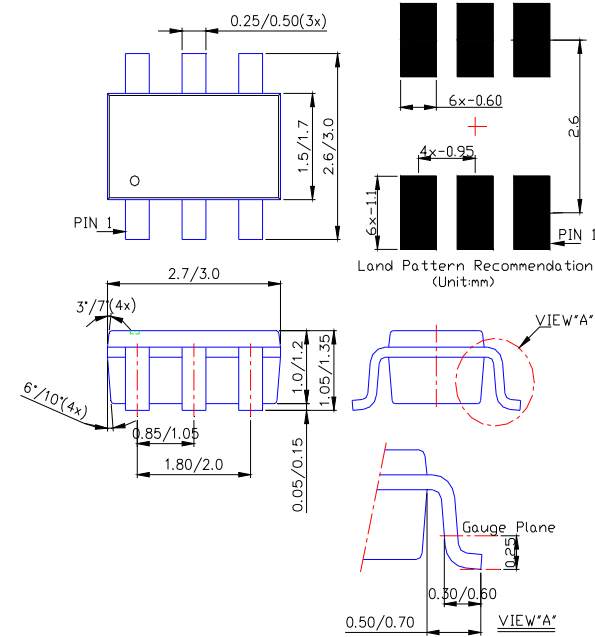


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week
X : A~Z : Internal code

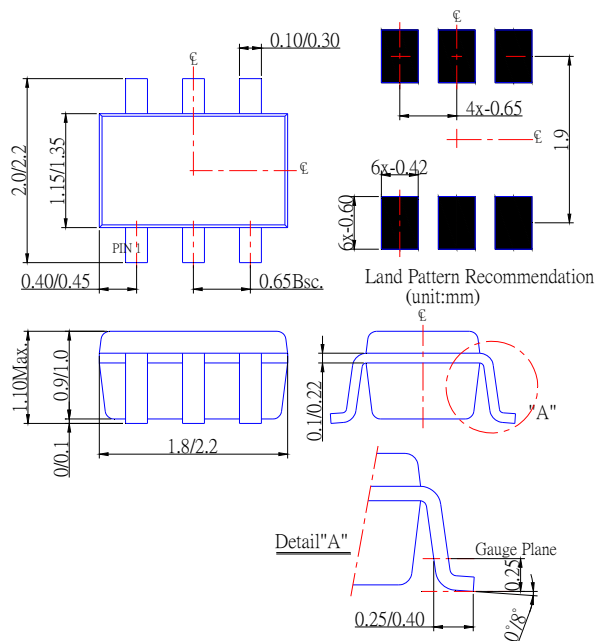
Part Number	Package	Identification Code
74LVC2G14FW4	DFN1010	Z5

Package Outline Dimensions (All Dimensions in mm)

(1) Package Type: SOT26



(2) Package Type: SOT363



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