



+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

General Description

The MAX3681 deserializer is ideal for converting 622Mbps serial data to 4-bit-wide, 155Mbps parallel data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts PECL serial clock and data inputs, and delivers low-voltage differential-signal (LVDS) clock and data outputs for interfacing with high-speed digital circuitry. It also provides an LVDS synchronization input that enables data realignment and reframing.

The MAX3681 is available in the extended-industrial temperature range (-40°C to +85°C), in a 24-pin SSOP package.

Applications

622Mbps SDH/SONET Transmission Systems
622Mbps ATM/SONET Access Nodes
Add/Drop Multiplexers
Digital Cross Connects

Features

- ◆ Single +3.3V Supply
- ◆ 622Mbps Serial to 155Mbps Parallel Conversion
- ◆ 265mW Power
- ◆ LVDS Data Outputs and Synchronization Inputs
- ◆ Synchronization Input for Data Realignment and Reframing
- ◆ Differential 3.3V PECL Clock and Data Inputs

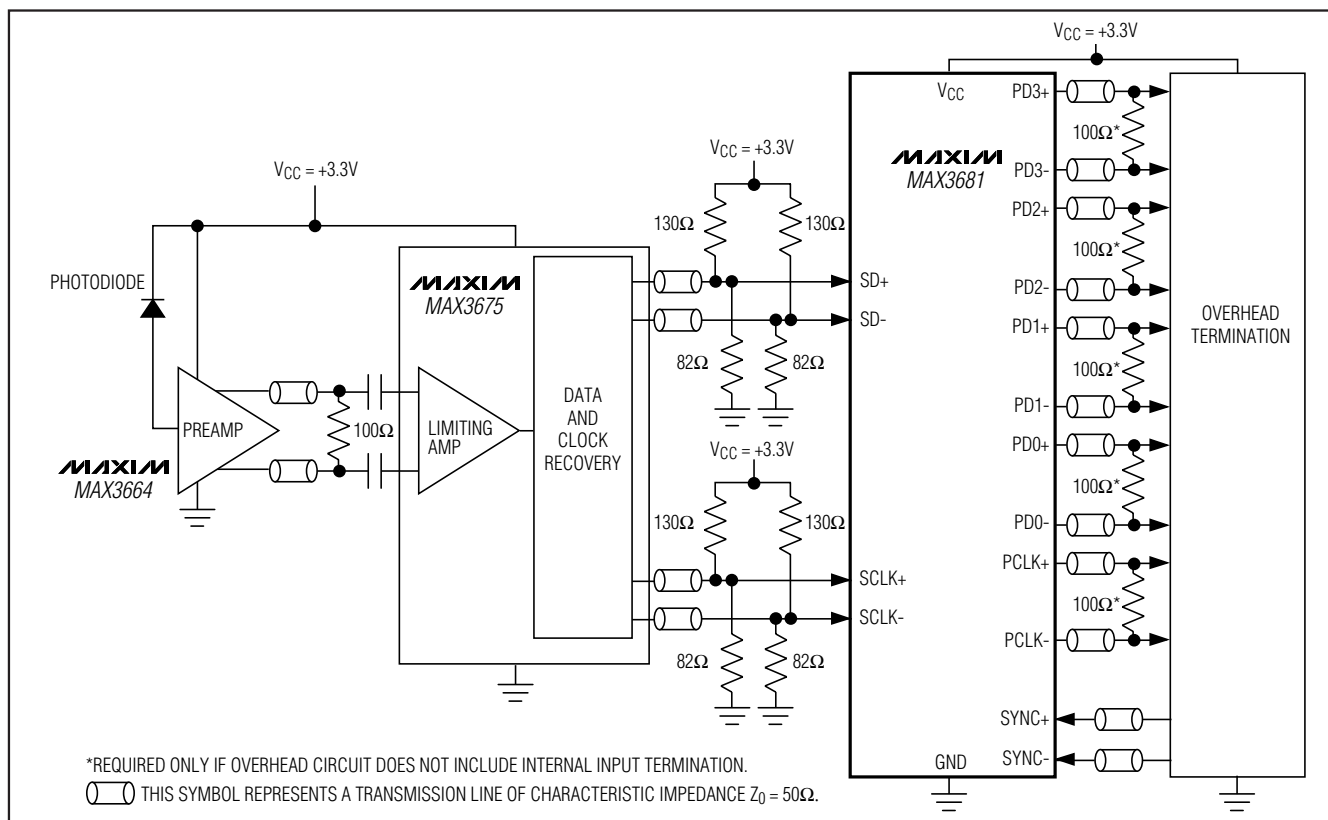
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3681EAG	-40°C to +85°C	24 SSOP
MAX3681EAG+	-40°C to +85°C	24 SSOP

+Denotes Lead Free Package

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

V_{CC} -0.5V to 5V
PECL Inputs (SD+/-, SCLK+/-) V_{CC} + 0.5V
LVDS Inputs (SYNC+/-) V_{CC} + 0.5V
Output Current, LVDS Outputs (PCLK+/-, PD+/-) 10mA

Continuous Power Dissipation (T_A = +85°C)

SSOP (derate 8.00mW/°C above +85°C) 520mW
Operating Temperature Range -40°C to +85°C
Storage Temperature Range -65°C to +160°C
Lead Temperature (soldering, 10sec) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I _{CC}		55	80	120	mA
PECL INPUTS (SD+/-, SCLK+/-)						
Input High Voltage	V _{IH}		V _{CC} - 1.16	V _{CC} - 0.88		V
Input Low Voltage	V _{IL}		V _{CC} - 1.81	V _{CC} - 1.48		V
Input High Current	I _{IH}	V _{IN} = V _{IH} (MAX)	-10		10	μA
Input Low Current	I _{IL}	V _{IN} = V _{IL} (MAX)	-10		10	μA
LVDS INPUTS AND OUTPUTS (SYNC+/-, PCLK+/-, PD+/-)						
Input Voltage Range	V _I	Differential input voltage = 100mV	0		2.4	V
Differential Input Threshold	V _{IDTH}	Common-mode voltage = 50mV	-100		100	mV
Threshold Hysteresis	V _{HYST}			70		mV
Differential Input Resistance	R _{IN}		85	100	115	Ω
Output High Voltage	V _{OH}				1.475	V
Output Low Voltage	V _{OL}		0.925			V
Differential Output Voltage	V _{OD}		250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	ΔV _{OD}				25	mV
Output Offset Voltage	V _{OS}	T _A = +25°C	1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	ΔV _{OS}				25	mV
Single-Ended Output Resistance	R _O		40	70	140	Ω
Change in Magnitude of Single-Ended Output Resistance for Complementary States	ΔR _O			±1	±10	%

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential loads = 100Ω, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Serial Clock Frequency	f _{SCLK}		622			MHz
Serial Data Setup Time	t _{SU}		800			ps
Serial Data Hold Time	t _H		50			ps
Parallel Clock to Data Output Delay	t _{CLK-Q}		200	550	900	ps

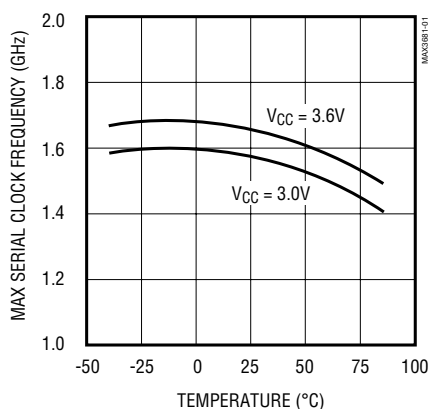
Note 1: AC Characteristics guaranteed by design and characterization.

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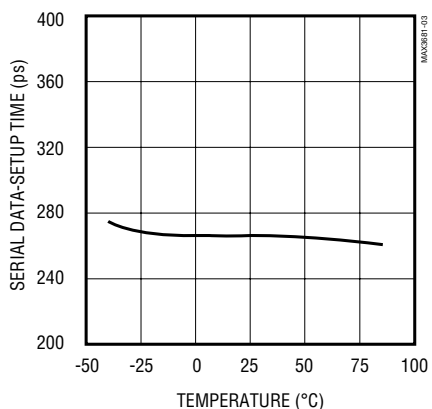
Typical Operating Characteristics

($V_{CC} = +3.0V$ to $+3.6V$, differential loads = 100Ω , unless otherwise noted.)

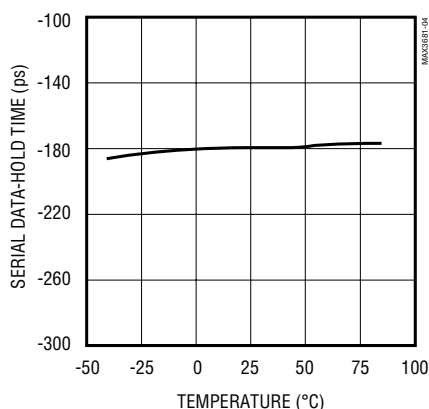
**MAXIMUM SERIAL CLOCK FREQUENCY
vs. TEMPERATURE**



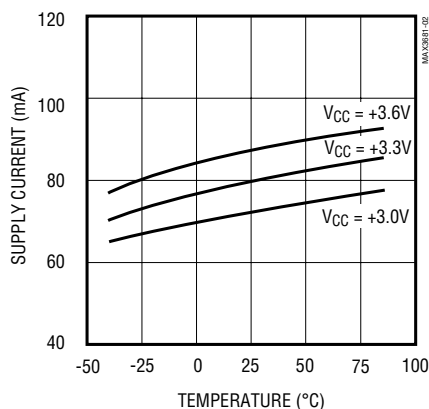
**SERIAL DATA-SETUP TIME
vs. TEMPERATURE**



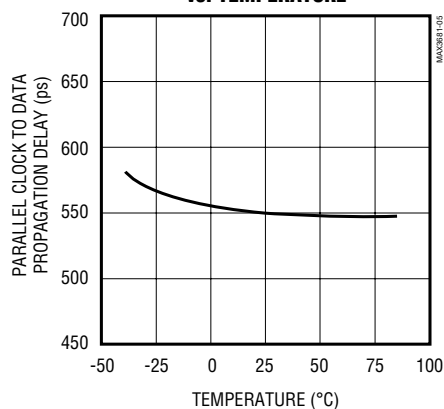
**SERIAL DATA-HOLD TIME
vs. TEMPERATURE**



**SUPPLY CURRENT
vs. TEMPERATURE**



**PARALLEL CLOCK TO DATA
OUTPUT PROPAGATION DELAY
vs. TEMPERATURE**



MAX3681

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Pin Description

PIN	NAME	FUNCTION
1, 2, 5, 8, 12	V _{CC}	+3.3V Supply Voltage
3	SD+	Noninverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
4	SD-	Inverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
6	SCLK+	Noninverting PECL Serial Clock Input
7	SCLK-	Inverting PECL Serial Clock Input
9, 15, 22	GND	Ground
10	SYNC+	Noninverting LVDS Synchronizing Pulse Input. Pulse the SYNC signal high for at least two SCLK periods to shift the data alignment by dropping one bit.
11	SYNC-	Inverting LVDS Synchronizing Pulse Input. Pulse the SYNC signal high for at least two SCLK periods to shift the data alignment by dropping one bit.
13	PCLK-	Inverting LVDS Parallel Clock Output
14	PCLK+	Noninverting LVDS Parallel Clock Output
16, 18, 20, 23	PD0- to PD3-	Inverting LVDS Parallel Data Outputs. Data is updated on the positive transition of the PCLK signal. See Figure 2 for the relationship between serial-data-bit position and output-data-bit assignment.
17, 19, 21, 24	PD0+ to PD3+	Noninverting LVDS Parallel Data Outputs. Data is updated on the positive transition of the PCLK signal. See Figure 2 for the relationship between serial-data-bit position and output-data-bit assignment.

Detailed Description

The MAX3681 deserializer uses a 4-bit shift register, 4-bit parallel output register, 2-bit counter, PECL input buffers, and low-voltage differential-signal (LVDS) input/output buffers to convert 622Mbps serial data to 4-bit-wide, 155Mbps parallel data (Figure 1).

The input shift register continuously clocks incoming data on the positive transition of the serial clock (SCLK) input signal. The 2-bit counter generates a parallel output clock (PCLK) by dividing down the serial clock frequency. The PCLK signal is used to clock the parallel output register. During normal operation, the counter divides the SCLK frequency by four, causing the output register to latch every four bits of incoming serial data.

The synchronization inputs (SYNC+, SYNC-) are used for data realignment and reframing. When the SYNC signal is pulsed high for at least two SCLK cycles, the parallel output data is delayed by one SCLK cycle. This realignment is guaranteed to occur within two PCLK cycles of the SYNC signal's positive transition. As a result, the first incoming bit of data during that PCLK cycle is dropped, shifting the alignment between PCLK and data by one bit.

See Figure 2 for the functional timing diagram and Figure 3 for the timing parameters diagram.

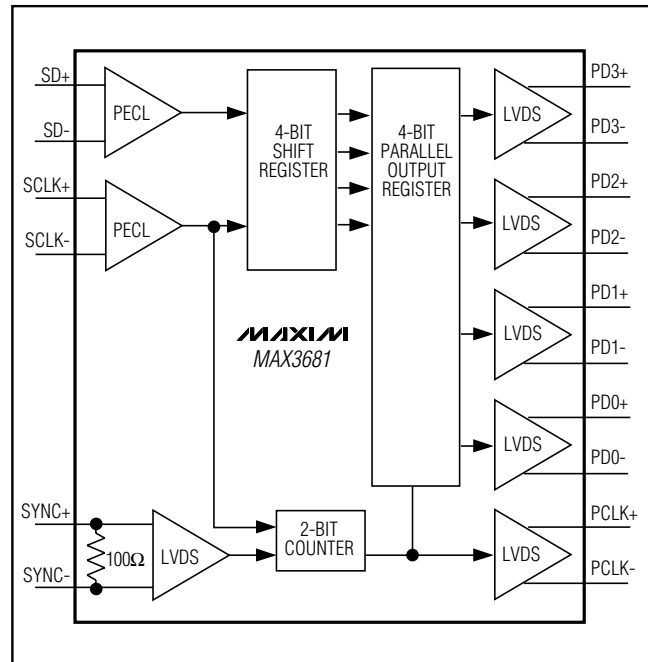


Figure 1. Functional Diagram

+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

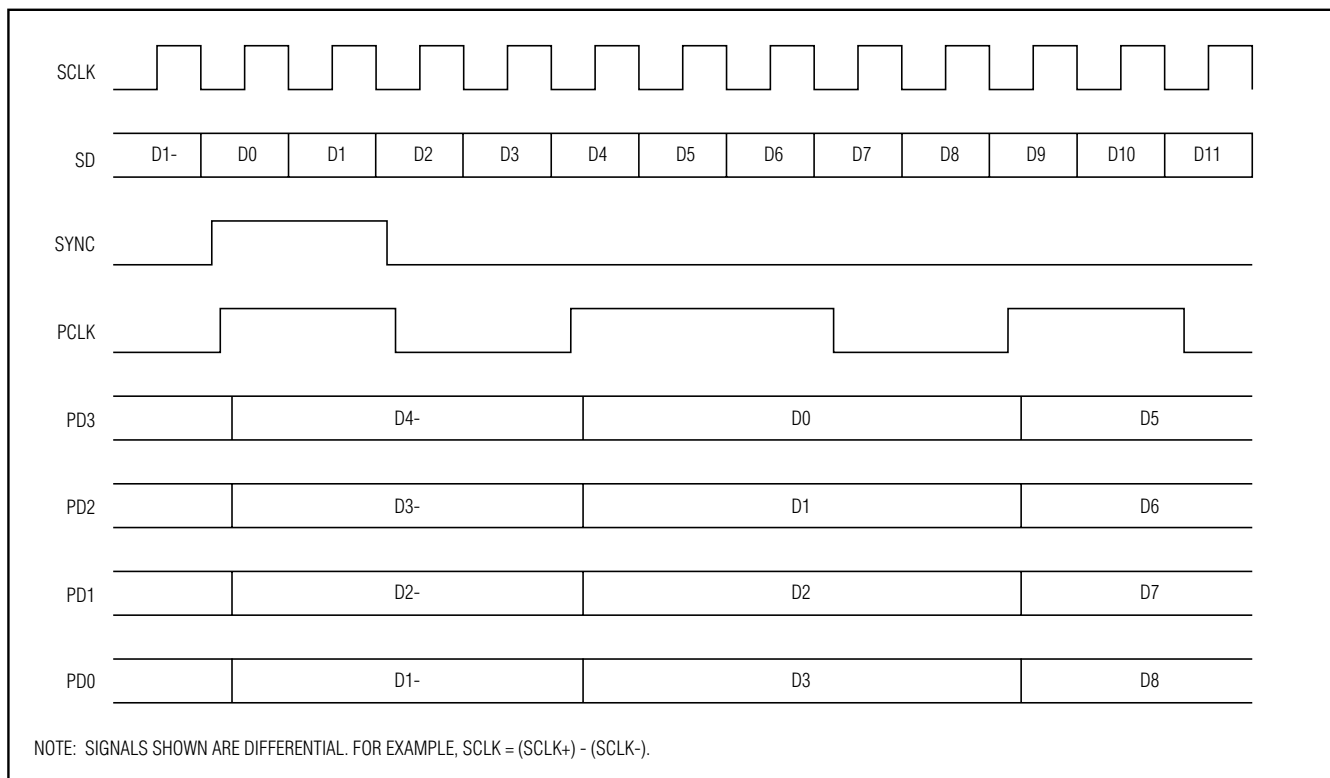


Figure 2. Functional Timing Diagram

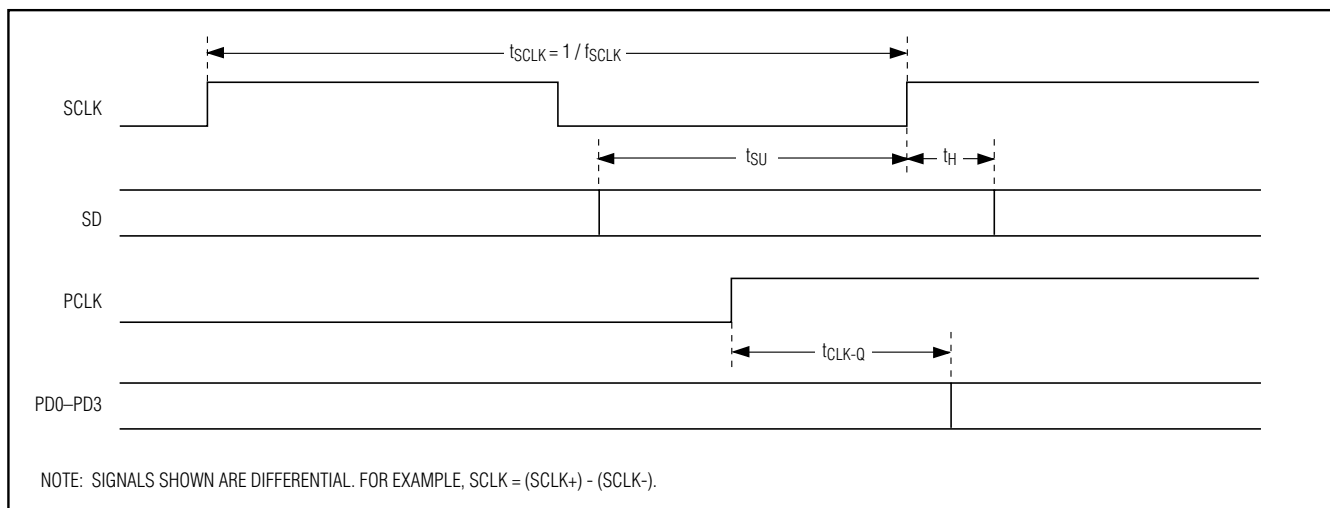


Figure 3. Timing Parameters

+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

Low-Voltage Differential-Signal (LVDS) Inputs and Outputs

The MAX3681 features LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 250mVp-p to 400mVp-p, differential low-voltage swings to achieve fast transition times, minimized power dissipation, and noise immunity.

The parallel clock and data LVDS outputs (PCLK+, PCLK-, PD_+, PD_-) require 100 Ω differential DC termination between the inverting and noninverting outputs for proper operation. Do not terminate these outputs to ground.

The synchronization LVDS inputs (SYNC+, SYNC-) are internally terminated with 100 Ω of differential input resistance, and therefore do not require external termination.

PECL Inputs

The serial data and clock PECL inputs (SD+, SD-, SCLK+, SCLK-) require 50 Ω termination to (VCC - 2V) when interfacing with a PECL source (see the *Alternative PECL Input Termination* section).

Applications Information

Alternative PECL Input Termination

Figure 4 shows alternative PECL input-termination methods. Use Thevenin-equivalent termination when a (VCC - 2V) termination voltage is not available. If AC coupling is necessary, such as when interfacing with an ECL-output device, use the ECL AC-coupling termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the MAX3681 data inputs and outputs.

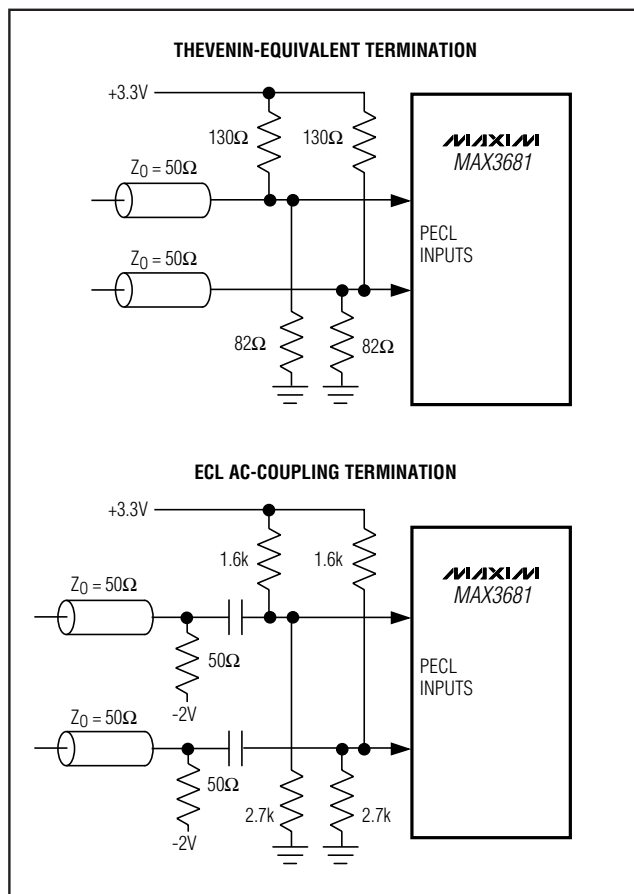
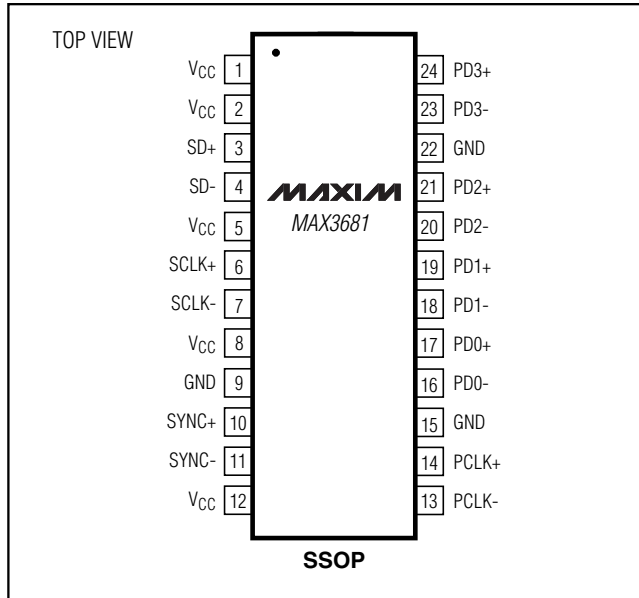


Figure 4. Alternative PECL Input Termination

+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs

Pin Configuration



Chip Information

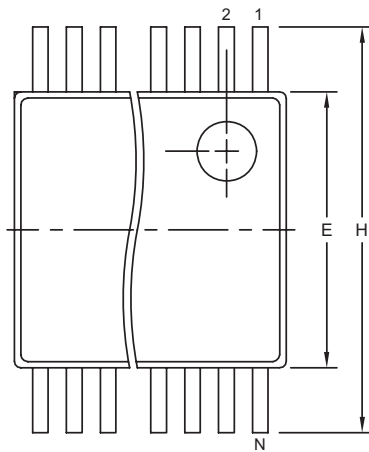
TRANSISTOR COUNT: 724

MAX3681

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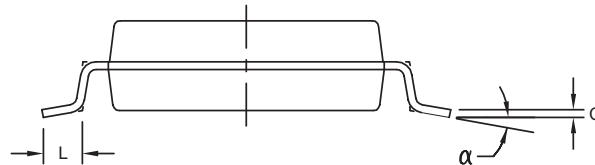
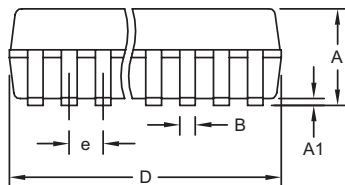
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES		MILLIMETERS		N
	MIN	MAX	MIN	MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

PROPRIETARY INFORMATION	
TITLE:	
PACKAGE OUTLINE, SSOP, 5.3 MM	
APPROVAL	DOCUMENT CONTROL NO.
	21-0056
REV.	1/1

SSOPERS

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