

## DESCRIPTION

The HF900 is a flyback regulator with an integrated 900 V MOSFET. Requiring a minimum number of external components, the HF900 provides excellent power regulation in AC/DC applications that require high reliability. These applications include smart meters, large appliances, industrial controls, and products powered by unstable AC grids.
The regulator uses peak-current-mode control to provide excellent transient response and easy loop compensation. When the output power falls below a given level, the regulator enters burst mode to lower the standby power consumption.
The MPS proprietary 900 V monolithic process enables over-temperature protection (OTP) on the same silicon of the 900 V power FET, offering precise thermal protection. Also, it offers a full suite of protection features such as $\mathrm{V}_{\mathrm{cc}}$ undervoltage lockout, over-load protection, overvoltage protection, and short-circuit protection.
The HF900 is designed to minimize electromagnetic interference for wireless communication in home and building automation applications. The operating frequency is programmed externally with a single resistor, so the power supply's radiated energy can be designed to avoid the interference with wireless communication.
In addition to the programmable frequency, the HF900 employs a frequency jittering function that not only greatly reduces the noise level but also reduces the cost of the EMI filter.

The HF900 is available in SOIC14-11 and PDIP8-7EP packages.

## FEATURES

- Internal Integrated 900V MOSFET
- Programmable Fixed Switching Frequency up to 300 kHz
- Frequency Jittering
- Current-Mode Operation
- Internal High-Voltage Current Source
- Low Standby Power Consumption via Active Burst Mode
- Internal Leading Edge Blanking
- Built-In Soft-Start Function
- Internal Slope Compensation
- Built-In Input Over-Voltage Protection
- Over-Temperature Protection (OTP)
- $V_{c c}$ Under-Voltage Lockout with Hysteresis
- Over-Voltage Protection on $\mathrm{V}_{\mathrm{cc}}$
- Time-Based Overload Protection
- Short-Circuit Protection (SCP)


## APPLICATIONS

- Smart Power Meters
- Large Appliances
- Industrial Controls
- All AC/DC Supplies Sold Where Power Grid may be Unstable

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## TYPICAL APPLICATION



ORDERING INFORMATION

| Part Number* $^{*}$ | Package | Top Marking |
| :---: | :---: | :---: |
| HF900GPR | PDIP8-7EP | See Below |
| HF900GS | SOIC14-11 | See Below |

* For Tape \& Reel, add suffix -Z (e.g. HF900GPR-Z);

TOP MARKING (PDIP8-7EP)

HF900<br>MPSYYWW<br>\section*{LLLLLLLL}

HF900: part number;
MPS: MPS prefix:
YY: year code;
WW: week code:
LLLLLLLL: lot number;

## TOP MARKING (SOIC14-11)

## MPSYYWW

HF900
LLLLLLLLL

MPS: MPS prefix:
YY: year code;
WW: week code:
HF900: part number;
LLLLLLLLLL: lot number;

## PACKAGE REFERENCE


ABSOLUTE MAXIMUM RATINGS ..... (1)
DRAIN ..... -0.3 V to 900 V
VCC ..... -0.3 V to 30 V
All other pins ..... -0.3 V to 6.5 V
Continuous power dissipation ( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ ) ..... (2)
PDIP8-7EP ..... 1.47W
SOIC14-11 ..... 1.45W
Junction temperature ..... $150^{\circ} \mathrm{C}$
Lead temperature ..... $260^{\circ} \mathrm{C}$
Storage temperature

$\qquad$
$-60^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
ESD capability human body model ..... 2.0 kV
ESD capability charged device model ..... 2.0kV
Recommended Operation Conditions ..... (3)
VCC to GND10.1 V to 24.5 V
Operating junction temp $\left(\mathrm{T}_{\mathrm{J}}\right) . .-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$
Thermal Resistance ${ }^{(4)} \quad \boldsymbol{\theta}_{J A} \quad \boldsymbol{\theta}_{J C}$PDIP8-7EP.............................. 68 ....... 7 .... ${ }^{\circ} \mathrm{C} / \mathrm{W}$SOIC14-11 .............................. 70 ...... 35 ... ${ }^{\circ} \mathrm{C} / \mathrm{W}$
NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $\mathrm{T}_{\mathrm{J}}(\mathrm{MAX})$, the junction-toambient thermal resistance $\theta_{\mathrm{JA}}$, and the ambient temperature $\mathrm{T}_{\mathrm{A}}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D}(M A X)=\left(T_{J}\right.$ $\left.(\mathrm{MAX})-\mathrm{T}_{\mathrm{A}}\right) / \theta_{\mathrm{JA}}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$\mathrm{V}_{\mathrm{cc}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=-40^{\circ} \mathrm{C} \sim 125^{\circ} \mathrm{C}$, Min \& Max are guaranteed by characterization, typical is tested under $25^{\circ} \mathrm{C}$, unless otherwise noted.

| Parameter | Symbol | Conditions |  | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Start-Up Current Source (DRAIN) |  |  |  |  |  |  |  |
| Supply current from DRAIN | $\mathrm{I}_{\text {Charge }}$ | $\mathrm{VCC}=6 \mathrm{~V}$; $\mathrm{V}_{\text {Drain }}=400 \mathrm{~V}$ |  | 1.35 | 2 | 3.1 | mA |
| Leakage current from DRAIN | $\mathrm{I}_{\text {Leak }}$ | $\mathrm{VCC}=13 \mathrm{~V} ; \mathrm{V}_{\text {Drain }}=400 \mathrm{~V}$ |  |  | 15 | 30 | $\mu \mathrm{A}$ |
| Breakdown voltage | $\mathrm{V}_{\text {(BR) }{ }^{\text {dss }}}$ | $\mathrm{l}_{\text {leakage }}=100 \mu \mathrm{~A}$ |  | 900 |  |  | V |
| On-state resistance | $\mathrm{R}_{\mathrm{DS} \text { (ON) }}$ | $\begin{aligned} & \mathrm{VCC}=10.1 \mathrm{~V} ; \\ & \mathrm{I}_{\text {Drain }}=100 \mathrm{~mA} \end{aligned}$ | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  | 13 | 17 | $\Omega$ |
|  |  |  | $\mathrm{T}_{\mathrm{J}}=125^{\circ} \mathrm{C}$ |  | 22 | 26 | $\Omega$ |
| Supply Voltage Management (VCC) |  |  |  |  |  |  |  |
| VCC upper level where the IC switches on | $\mathrm{V}_{\mathrm{CCH}}$ |  |  | 11.5 | 13.0 | 14.5 | V |
| VCC lower level where the IC switches off | $\mathrm{V}_{\text {ccl }}$ |  |  | 8.9 | 9.4 | 10.1 | V |
| VCC hysteresis | $\mathrm{V}_{\text {CC_HYS }}$ |  |  | 2.7 | 3.6 | 4.6 | V |
| VCC OVP level | Vovp |  |  | 24.5 | 26.0 | 27.3 | V |
| VCC re-charge level where the protection occurs | $\mathrm{V}_{\text {CCR }}$ |  |  | 4.5 | 5.3 | 6 | V |
| Quiescent current at protection phase | 1 Pro | $V C C=6 \mathrm{~V}$ |  |  |  | 700 | $\mu \mathrm{A}$ |
| Quiescent current | $\mathrm{I}_{\mathrm{Q}}$ | $V C C=13 \mathrm{~V}$ |  |  | 780 | 980 | $\mu \mathrm{A}$ |
| Operation current | $\mathrm{I}_{\mathrm{cc}}$ | $\mathrm{VCC}=13 \mathrm{~V} ; \mathrm{f}_{\mathrm{S}}=100 \mathrm{kHz}$ |  |  | 1.7 | 2 | mA |
| Feedback Management (FB) |  |  |  |  |  |  |  |
| Internal pull-up resistor | $\mathrm{R}_{\text {FB }}$ |  |  |  | 10 |  | k $\Omega$ |
| Internal pull-up voltage | $V_{\text {up }}$ |  |  | 3.8 | 4.1 | 4.4 | V |
| FB to current-set-point division ratio | $\mathrm{I}_{\text {div }}$ |  |  |  | 3.3 | 3.6 |  |
| Internal soft-start time | $\mathrm{T}_{\text {ss }}$ |  |  |  | 3 |  | ms |
| FB decreasing level where the regulator enters burst mode | $V_{\text {burl }}$ |  |  | 0.4 | 0.5 | 0.6 | V |
| FB increasing level where the regulator leaves burst mode | $\mathrm{V}_{\text {Burh }}$ |  |  | 0.58 | 0.70 | 0.86 | V |
| Overload set point | VoLp |  |  | 3.5 | 3.8 | 4.1 | V |
| Overload delay time | $\mathrm{T}_{\text {Delay }}$ | $\mathrm{f}_{\mathrm{S}}=100 \mathrm{kHz}$ |  |  | 82 |  | ms |
| Timing Resistor (FSET) |  |  |  |  |  |  |  |
| FSET reference voltage | $\mathrm{V}_{\text {FSET }}$ |  |  | 1.15 | 1.23 | 1.3 | V |
| Frequency spectrum jittering range in percentage of Fs | $\mathrm{R}_{\text {Jittering }}$ | Example: $\mathrm{f}_{\mathrm{S}}=$ jittering is $\pm 4 \mathrm{kH}$ | 100 kHz , then |  | $\pm 4$ |  | \% |
| Typical operating frequency | $\mathrm{f}_{\text {s }}$ | $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C} ; \mathrm{R}_{\text {FSE }}$ | $=100 \mathrm{k} \Omega$ | 90 | 104 | 118 | kHz |

## ELECTRICAL CHARACTERISTICS

$\mathrm{V}_{\mathrm{cc}}=12 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=-40^{\circ} \mathrm{C} \sim 125^{\circ} \mathrm{C}$, Min \& Max are guaranteed by characterization, typical is tested under $25^{\circ} \mathrm{C}$, unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Current Sampling Management (SOURCE) |  |  |  |  |  |  |
| Leading edge blanking for current sensor | $\mathrm{T}_{\text {LEB1 }}$ |  |  | 350 |  | ns |
| Leading edge blanking for SCP | $\mathrm{T}_{\text {LEB2 }}$ |  |  | 300 |  | ns |
| Maximum current set point | $\mathrm{V}_{\text {cs }}$ |  | 0.90 | 0.97 | 1.04 | V |
| Short-circuit protection set point | $\mathrm{V}_{\text {sc }}$ |  | 1.32 | 1.42 | 1.62 | V |
| Slope compensation ramp | $\mathrm{S}_{\text {Ramp }}$ | $\mathrm{f}_{\mathrm{S}}=100 \mathrm{kHz}$ |  | 40 |  | $\mathrm{mV} / \mathrm{\mu s}$ |
| Protection Management (PRO) |  |  |  |  |  |  |
| Protection voltage | $\mathrm{V}_{\text {PRo }}$ |  | 2.92 | 3.1 | 3.32 | V |
| Protection hysteresis | $\mathrm{V}_{\mathrm{HY}}$ |  |  | 0.2 |  | V |
| Thermal Shutdown |  |  |  |  |  |  |
| Thermal threshold ${ }^{(5)}$$\quad$ shutdown |  |  |  | 150 |  | ${ }^{\circ} \mathrm{C}$ |
| Thermal shutdown recovery hysteresis ${ }^{(5)}$ |  |  |  | 30 |  | ${ }^{\circ} \mathrm{C}$ |

## Notes:

5) Guaranteed by Design \& Characterization.

## TYPICAL CHARACTERISTICS



## TYPICAL CHARACTERISTICS (continued)

Fset Reference Voltage
vs. Temperature


Pro Protection Voltage
vs. Temperature


Max Current Set Point
vs. Temperature


TEMPERATURE $\left({ }^{\circ} \mathrm{C}\right)$

Short Circuit Protection Set Point vs. Temperature


R_ON@VCc=10.1V
vs. Temperature


BV_Drain_100 $\mu \mathrm{A}$ vs. Temperature



Typical Operating Frequency when $\mathrm{T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$


## TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. $\mathrm{V}_{\text {IN }}=230 \mathrm{~V}, \mathrm{~V}_{\text {OUT1 }}=12.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT } 2}=5 \mathrm{~V}$, Primary Inductance $=2.5 \mathrm{mH}, \mathrm{N}_{\mathrm{P}}: \mathrm{N}_{\mathrm{AUX}}: \mathrm{N}_{\mathrm{S} 1}: \mathrm{N}_{\mathrm{S} 2}=125: 14: 14: 9$, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.


Efficiency

Startup
230Vac, Full Load

$200 \mathrm{~ms} / \mathrm{div}$.

Shutdown
230Vac, No Load


EMI
230Vac, Full Load, L Line


## Shutdown

230Vac, Full Load

$200 \mathrm{~ms} / \mathrm{div}$.

SCP Entry
230Vac, Full Load

$100 \mathrm{~ms} / \mathrm{div}$.

## EMI

230Vac, Full Load, N Line


Startup
230Vac, No Load

$200 \mathrm{~ms} /$ div.

SCP Recovery
230Vac, Full Load


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Performance waveforms are tested on the evaluation board of the Design Example section. $\mathrm{V}_{\mathrm{IN}}=230 \mathrm{~V}, \mathrm{~V}_{\text {OUT } 1}=12.5 \mathrm{~V}, \mathrm{~V}_{\text {OUT } 2}=5 \mathrm{~V}$, Primary Inductance $=2.5 \mathrm{mH}, \mathrm{N}_{\mathrm{P}}: \mathrm{N}_{\mathrm{AUX}}: \mathrm{N}_{\mathrm{S} 1}: \mathrm{N}_{\mathrm{S} 2}=125: 14: 14: 9$, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.



## Stress

420Vac, Full Load

$4 \mu \mathrm{~s} / \mathrm{div}$.

SCP Entry
230Vac, No Load


Output Ripple
230Vac, Full Load


Pro Protection
230Vac, 300Vac Protection, Full Load

$40 \mathrm{~ms} / \mathrm{div}$.

SCP Recovery
230Vac, No Load


Output Ripple 230Vac, No Load


## PIN FUNCTIONS

| $\begin{array}{\|c\|} \hline \text { Pin \# } \\ \text { PDIP8-7EP } \end{array}$ | $\begin{gathered} \text { Pin \# } \\ \text { SOIC14-11 } \end{gathered}$ | Name | Description |
| :---: | :---: | :---: | :---: |
| 1 | 6 | FB | Feedback. The output voltage from the external compensation circuit is fed into this pin. FB and the current sense signal from SOURCE determines the PWM duty cycle. A feedback voltage of $\mathrm{V}_{\text {olp }}$ triggers overload protection while $\mathrm{V}_{\text {BURL }}$ triggers burst-mode operation. The regulator exits burst-mode operation and enters normal operation when the FB voltage reaches $\mathrm{V}_{\text {BURH }}$. |
| 2 | 5 | PRO | Input over-voltage protection. When voltage on PRO rises to $\mathrm{V}_{\text {PRO }}$, the IC is shut down with hysteresis. |
| 3 | 4 | FSET | Switching converter frequency set. Connect a resistor to GND to set the switching frequency up to 300 kHz . |
| 4 | 3 | VCC | Supply voltage. Connect a $22 \mu \mathrm{~F}$ bulk capacitor and a $0.1 \mu \mathrm{~F}$ ceramic capacitor for most applications. When $\mathrm{V}_{\mathrm{CC}}$ rises to $\mathrm{V}_{\mathrm{CCH}}$, the IC starts switching; when it falls below $\mathrm{V}_{\mathrm{CCL}}$, the IC stops switching. |
| 5 | 14 | DRAIN | Drain of the internal MOSFET. Input for the start-up high-voltage current source. |
| 7 | 9 | SOURCE | Source of the internal MOSFET. Input of the primary current sense signal. |
| 8 | 1,2,7,8 | GND | IC ground. |
|  | 13 | NC | Not connected. |

## FUNCTIONAL BLOCK DIAGRAM



Figure 1: Internal Function Block Diagram

## OPERATION

The HF900 integrates a 900V MOSFET for a reliable switch-mode power supply solution. It has burst-mode operation to minimize the standby power consumption at light load. Protection features such as auto-recovery for overload protection (OLP), short-circuit protection (SCP), over-voltage protection (OVP), and thermal shutdown for over-temperature protection (OTP) contribute to a safer converter design with minimal external components.

## PWM Operation

The HF900 employs peak-current-mode control. On the secondary side, the output voltage is divided by a voltage divider network. This voltage is fed back to the primary side as voltage on the FB using an optocoupler and a shunt regulator. The voltage at FB is compared to the $\mathrm{V}_{\text {Sense }}$ voltage, which measures the MOSFET switching current. The integrated MOSFET turns on at the beginning of each clock cycle. The current in the transformer magnetizing inductance increases until it reaches the value set by the FB voltage, and then the integrated MOSFET turns off.

## Start-Up and VCC UVLO

Initially, the IC is driven by the internal current source, which is drawn from the high-voltage DRAIN. The IC starts switching, and the internal high-voltage current source turns off as soon as the voltage on VCC reaches $\mathrm{V}_{\text {ссн }}$. At this point, the supply of the IC is taken over by the auxiliary winding of the transformer. When VCC falls below $\mathrm{V}_{\mathrm{CCL}}$, the regulator stops switching, and the internal high-voltage current source turns on again (see Figure 2).


Figure 2: VCC Start-Up

The lower threshold of VCC UVLO decreases from $\mathrm{V}_{\mathrm{CCL}}$ to $\mathrm{V}_{\text {CCR }}$ when fault conditions such as SCP, OLP, OVP, and OTP occur.

## Soft Start

The HF900 implements an internal soft-start circuit to reduce stress on the primary-side MOSFET and the secondary diode and smoothly establish the output voltage during start-up. The internal soft-start circuit increases the primary current sense threshold gradually, which determines the MOSFET peak current during start-up. The pulse width of the power switching device is increased progressively to establish correct operating conditions until the feedback control loop takes charge (see Figure 3).


Figure 3: Soft Start

## Switching Frequency

The switching frequency of the HF900 can be set by FSET. The frequency can be set by a resistor between FSET and GND. The oscillator frequency can be attained using Equation (1):

$$
\begin{equation*}
\mathrm{f}_{\mathrm{S}}=\frac{1}{200 \times 10^{-9}+112.5 \times 10^{-12} \times \frac{\mathrm{R}_{\text {FSET }}}{V_{\text {FST }}}} \mathrm{Hz} \tag{1}
\end{equation*}
$$

$\mathrm{V}_{\text {FST }}(1.23 \mathrm{~V})$ is the FSET pin reference voltage.

## Over-Voltage Protection (OVP)

Monitoring the VCC voltage via a $20 \mu \mathrm{~s}$ time constant filter allows the HF900 to enter OVP during an over-voltage condition, typically when $\mathrm{V}_{\mathrm{CC}}$ goes above $\mathrm{V}_{\text {ovp. }}$. The regulator will resume operation once the fault disappears.

## Overload Protection (OLP)

The HF900 shuts down when the power supply experiences an overload. OLP is achieved by monitoring the FB voltage continuously. A fault signal is triggered when FB pulls up to 3.8 V ( $\mathrm{V}_{\text {olp }}$, typical value) and after an 82 ms delay ( 8192 switching cycle, $\mathrm{f}_{\mathrm{S}}=100 \mathrm{kHz}$ ). If the fault signal is still present, the HF900 shuts down. When the fault disappears, the power supply resumes operation. The OLP delay time can be attained using Equation (2):

$$
\begin{equation*}
\mathrm{T}_{\text {Delay }}=\frac{82 \mathrm{~ms} \times 100 \mathrm{kHz}}{\mathrm{f}_{\mathrm{s}}} \tag{2}
\end{equation*}
$$

## Short-Circuit Protection (SCP)

The HF900 shuts down when voltage on CS is higher than $\mathrm{V}_{\mathrm{SC}}$, which indicates a short circuit. The HF900 enters a safe low-power mode that prevents any thermal or stress damage. As soon as the fault disappears, the power supply resumes operation.

## Thermal Shutdown (OTP)

When the junction temperature of the IC exceeds $150^{\circ} \mathrm{C}$, the over-temperature protection is activated and stops output driver switching to prevent the HF900 from any thermal damage. As soon as the junction temperature drops below $120^{\circ} \mathrm{C}$, the regulator resumes operation. During the protection period, the regulator enters autorecovery mode. The VCC voltage is discharged to $V_{C C R}$ and is re-charged to $V_{C C H}$ by the internal high-voltage current source.

## Burst Operation

To minimize standby power consumption, the HF900 implements burst mode at no load and light load. As the load decreases, the FB voltage decreases. The IC stops switching when the FB voltage drops below 0.5 V ( $\mathrm{V}_{\text {BRUL }}$, typical value). As the load power increases, the output voltage drops at a rate dependent on the load. This causes the FB voltage to rise again due to the negative feedback control loop. Once the FB voltage exceeds 0.7 V ( $\mathrm{V}_{\text {BRUH }}$, typical value), the switching pulse resumes. The FB voltage then decreases, and the whole process repeats. Burst-mode operation alternately enables and disables the switching pulse of the MOSFET. Hence switching loss at no load and light load conditions is reduced greatly.

Figure 4 shows the burst-mode operation of the HF900.


Figure 4: Burst-Mode Operation

## PRO

PRO provides extra protection against abnormal conditions. Use PRO for input OVP or other protections (input UVP, over-temperature protection for key components, etc.). If the PRO voltage exceeds 3.1 V (VPRO, typical value), the IC shuts down to enter auto-recovery mode. Once the fault disappears, the power supply resumes operation.

## Peak Current Limit

In normal operation, the primary peak current is sensed by a sensing resistor between SOURCE and GND. The turn-off threshold of the MOSFET is set by the FB voltage $\left(\mathrm{V}_{\text {Sense }}=\mathrm{V}_{\text {FB }} / I_{\text {div }}\right)$. When the sensing resistor voltage reaches $\mathrm{V}_{\text {Sense }}$, the MOSFET turns off. The $I_{\text {div }}$ is the FB to the current-set-point division ratio.

During an overload condition, the primary peak current threshold is limited internally to the maximum value of 0.97 V ( $\mathrm{V}_{\text {cs }}$, typical value), even if the $\mathrm{V}_{\mathrm{FB}}$ voltage exceeds 3.2 V , to avoid excessive output power and lower the switch voltage rating.

During the start-up period, the primary peak current threshold increases internally to the maximum current set point $\left(\mathrm{V}_{\mathrm{Cs}}\right)$ gradually.

## Leading Edge Blanking (LEB)

In order to avoid turning off the MOSFET by mistrigger spikes shortly after the switch turns
on, the IC implements leading edge blanking. During the blanking time, any trigger signal on SOURCE is blocked. An internal leading edge blanking (LEB) unit containing two LEB times is employed between SOURCE and the current comparator input to avoid premature switching pulse termination due to the parasitic capacitances. During the blanking time, the current comparator is disabled and cannot turn off the MOSFET.

Current sensor leading edge blanking inhibits the current limitation comparator for 350ns ( $\mathrm{T}_{\text {LEB1 }}$, typical value), and the SCP leading edge blanking inhibits the SCP current comparator for 300 ns ( $\mathrm{T}_{\text {LEB2 }}$, typical value). Figure 5 shows the primary current sense waveform and the leading edge blanking.


Figure 5: Leading Edge Blanking

## APPLICATION INFORMATION

## Selecting the Input Capacitor

The bulk capacitors of the rectifier bridge filter the rectified AC input, which supplies the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of a full-bridge rectifier.


Figure 6: Input Voltage Waveform
When the full-bridge rectifier is used, usually the input capacitor is set at $2 \mu \mathrm{~F} / \mathrm{W}$ for the universal input condition ( $85 \sim 265 \mathrm{~V}_{\mathrm{AC}}$ ). For high-voltage input ( $>185 \mathrm{VAC}$ ) application, cut the capacitor values in half. The input power ( $\mathrm{P}_{\text {in }}$ ) is estimated with Equation (3):

$$
\begin{equation*}
P_{\text {in }}=\frac{V_{0} \times I_{0}}{\eta} \tag{3}
\end{equation*}
$$

Where $V_{O}$ is the output voltage, $I_{O}$ is the rated output current, and $\eta$ is the estimated efficiency. Generally, $\eta$ is between 0.75 and 0.85 depending on the input range and output application.
From the waveform in Figure 6, the AC input voltage $\left(\mathrm{V}_{\mathrm{AC}}\right)$ and the DC input voltage $\left(\mathrm{V}_{\mathrm{DC}}\right)$ are calculated using Equation (4):

$$
\begin{equation*}
V_{D C}\left(V_{A C}, t\right)=\sqrt{2 \times \mathrm{V}_{A C}{ }^{2}-\frac{2 \times \mathrm{P}_{\mathrm{in}}}{\mathrm{C}_{\mathrm{in}}} \times \mathrm{t}} \tag{4}
\end{equation*}
$$

$\mathrm{V}_{\mathrm{AC}}$ starts to charge the input capacitor when the DC bus voltage reaches the minimum value ( $\mathrm{V}_{\mathrm{DC}}=\mathrm{V}_{\mathrm{AC}}$, approximately). t1 can be calculated using Equation (5):

$$
\begin{equation*}
V_{D C(\text { min })}=V_{D C}\left(V_{A C(\text { min })}, t 1\right) \tag{5}
\end{equation*}
$$

Very low DC input voltage can cause a thermal problem in a full load. It is recommended that the minimum DC voltage is higher than 70 V . Otherwise the input capacitor value should be increased.

As a 900 V offline regulator, the HF900 suits very high-voltage input applications. General input capacitors with 400 V voltage ratings cannot satisfy the safety requirement. Thus, stack capacitors can be used in very high input voltage applications such as a 420VAC input (see Figure 7).


Figure 7: Input Stack Capacitor Circuit
C1 and C2 endure half of the input DC voltage rating, respectively. R1 to R4 should use the same value resistor to equalize the C1 and C2 voltage stress. It is recommended to use a 1206 package for R1 to R4 to satisfy the safety requirement. Also, the R1 to R4 values should be large enough for energy saving. For example, the total value of R1 to R4 is $20 \mathrm{M} \Omega$, which consumes about 18 mW in 600VDC bus voltage.

## Primary-Side Inductor Design ( $\mathrm{L}_{\mathrm{m}}$ )

Normally, the converter is designed to operate in CCM with low input voltage. CCM is needed to satisfy the output energy requirement for the universal input condition. With a built-in slope compensation function, the HF900 supports CCM when the duty cycle exceeds $50 \%$. Set the ratio $\left(\mathrm{K}_{\mathrm{P}}\right)$ of the primary inductor ripple current amplitude vs. the peak current value to $0<K_{P} \leq 1$, where $K_{P}=1$ for DCM. Figure 8 shows the relevant waveforms. A larger inductor leads to a smaller $K_{P}$, which reduces RMS current but increases the transformer size. For 5 W application, an optimal $\mathrm{K}_{\mathrm{P}}$ value is between 0.8
and 1 for the universal input range and 1 for a 230VAC input range.


Figure 8: Typical Primary Current Waveform
For CCM at a minimum input, the converter duty cycle is determined using Equation (6):

$$
\begin{equation*}
D=\frac{\left(V_{O}+V_{F}\right) \times N}{\left(V_{O}+V_{F}\right) \times N+V_{D C(\text { min })}} \tag{6}
\end{equation*}
$$

Where:
$V_{F}$ is the secondary diode's forward voltage, and N is the transformer turns ratio.
The MOSFET turn-on time is calculated with Equation (7):

$$
\begin{equation*}
\mathrm{T}_{\mathrm{oN}}=\frac{\mathrm{D}}{\mathrm{f}_{\mathrm{s}}} \tag{7}
\end{equation*}
$$

Where, $\mathrm{f}_{\mathrm{S}}$ is the operating frequency.
The input average current, ripple current, peak current, and valley current of the primary side are calculated using Equation (8), Equation (9), Equation (10) and Equation (11):

$$
\begin{gather*}
\mathrm{I}_{\mathrm{AV}}=\frac{\mathrm{P}_{\text {in }}}{\mathrm{V}_{\mathrm{DC}(\text { min })}}  \tag{8}\\
\mathrm{I}_{\text {ripple }}=\mathrm{K}_{\mathrm{P}} \times \mathrm{I}_{\text {peak }}  \tag{9}\\
\mathrm{I}_{\text {peak }}=\frac{\mathrm{I}_{\mathrm{AV}}}{\left(1-\frac{\mathrm{K}_{\mathrm{P}}}{2}\right) \times \mathrm{D}}  \tag{10}\\
\mathrm{I}_{\text {valley }}=\left(1-\mathrm{K}_{\mathrm{P}}\right) \times \mathrm{I}_{\text {peak }} \tag{11}
\end{gather*}
$$

Estimate $\mathrm{L}_{\mathrm{m}}$ using Equation (12):

$$
\begin{equation*}
L_{m}=\frac{V_{\mathrm{DC}(\text { min) }} \times T_{\mathrm{oN}}}{I_{\text {ripple }}} \tag{12}
\end{equation*}
$$

## Current-Sense Resistor



Figure 9: Slope Compensation Waveform
Figure 9 shows the slope compensation waveform. When the sum of the sense resistor voltage and the slope compensation voltage reaches the peak current limit ( $\mathrm{V}_{\mathrm{Cs}}$ ), the HF900 turns off the internal MOSFET. The maximum peak current limit is $0.97 \mathrm{~V}\left(\mathrm{~V}_{\mathrm{CS}}\right.$, typical value $)$, and the slope compensation slew rate is $40 \mathrm{mV} / \mu \mathrm{s}$. Considering the margin, use $0.95 \times \mathrm{V}_{\mathrm{cs}}$ as the peak current limit at full load. The voltage on the sense resistor is given using Equation (13):

$$
\begin{equation*}
\mathrm{V}_{\text {sense }}=0.95 \times \mathrm{V}_{\text {Cs }}-\mathrm{S}_{\text {Ramp }} \times \mathrm{T}_{\text {ON }} \tag{13}
\end{equation*}
$$

The value of the sense resistor is calculated using Equation (14):

$$
\begin{equation*}
R_{\text {sense }}=\frac{V_{\text {sense }}}{I_{\text {peak }}} \tag{14}
\end{equation*}
$$

Use Equation (15) to select the current sense resistor with an appropriate power rating based on the power loss:
$P_{\text {sense }}=\left[\left(\frac{I_{\text {peak }}+I_{\text {valley }}}{2}\right)^{2}+\frac{1}{12} \times\left(I_{\text {peak }}-I_{\text {valley }}\right)^{2}\right] \times D \times R_{\text {sense }}$
PRO
Extra protection can be enabled using the HF900 PRO. A typical input over-voltage protection circuitry is shown in Figure 10.


Figure 10: Input Over-Voltage Protection Setup
The input over-voltage protection point can be calculated using Equation (16):

$$
\begin{equation*}
V_{\text {INOVP }}=V_{\text {PRO }} \times \frac{R 5+R 6+R 7+R 8}{R 8} \tag{16}
\end{equation*}
$$

For resistors R5 to R7, 1206 packages should be used for safety considerations. The total value should be larger than $10 \mathrm{M} \Omega$ for energy saving purposes.
Switching voltage noise can occur if $R \%$ to $R^{*}$ have large values, which disturbs the PRO protection action. One ceramic capacitor (around 1 nF ) should be paralleled with PRO and GND. It should be located near the IC to decouple the switching voltage noise.

## Frequency Jittering

The HF900 provides a frequency jittering function, which simplifies the input EMI filter design and decreases the system cost. The HF900 has optimized frequency jittering with a $\pm 4 \%$ frequency deviation range and a $256 \mathrm{~T}_{\mathrm{s}}$ carrier cycle that effectively improves EMI by spreading the energy dissipation over the frequency range.

## Thermal Performance Optimization

The HF900 is dedicated to high input voltage application. However, the high input voltage can cause greater switching loss on the MOSFET, especially under a high frequency, which may lead to poor thermal performance. Tests show that turn-on loss is dominant under a high input, so thermal performance optimization should focus mainly on reducing turn-on loss.
As we know that turn-on loss is caused by a turnon current spike and $\mathrm{V}_{\mathrm{DS}}$, measures should be
taken to reduce either the $\mathrm{V}_{\mathrm{Ds}}$ or the turn-on spike to get better thermal performance.
In order to reduce $\mathrm{V}_{\mathrm{DS}}$, use a small turns ratio-N to minimize the reflected output voltage on the primary MOSFET.
To suppress a turn-on spike of the MOSFET, CCM operation should be avoided, especially under a high input. The transformer structure should be designed to achieve minimum parasitic capacitance of each winding and between the primary and secondary windings.
For the HF900 PDIP8-7EP package, a heat sink can be used to further improve thermal performance in very critical applications.
In addition, choose an appropriate operating frequency for better thermal performance and EMI.

Table 1 shows the maximum output power test results of the HF900 (both packages were tested without a heat sink).

Table 1: Maximum Output Power

| Package | $\mathbf{f}_{\mathbf{s}}(\mathbf{k H z})$ | $\mathbf{P}_{\text {MAX }}(\mathbf{W})$ |
| :---: | :---: | :---: |
| PDIP8-7EP | 50 | 7 |
|  | 100 | 3 |
| SOIC14-11 | 50 | 8 |
|  | 100 | 4 |

notes:

1. The maximum output power is tested under $T_{A}=50^{\circ} \mathrm{C}$.
2. In order to reduce $V_{D S}$, the turns ratio is set to 5 .
3. $\mathrm{V}_{\text {IN }}=85 \sim 420 \mathrm{VAC}$, single output, $\mathrm{V}_{\text {OUT }}=12.5 \mathrm{~V}$.
4. PDIP8-7EP package is tested without a heat sink, and GND is connected to $2 \mathrm{~cm}^{2}$ copper areas. GND of the SOIC14-11 package is connected to $2.5 \mathrm{~cm}^{2}$ copper areas.
5. Working condition under $\mathrm{V}_{\mathrm{IN}}=85 \mathrm{VAC}$ is set to BCM .

## PCB Layout Guidelines

Efficient PCB layout is critical to achieve reliable operation, good EMI performance, and good thermal performance. For best results, refer to Figure 11 and follow the guidelines below:

1) Minimize the power stage switching stage loop area. This includes the input loop (C2-C1-T1-U1-R12/R13-C2), the auxiliary winding loop (T1-D6-C6-T1), the output loop (T1-D8-C9-T1 and T1-D7-C7-T1), and the RCD loop (T1-D5-R16/R17/C3-T1).
2) Keep the input loop, GND, and control circuit separate and only connect them at C2.
3) Connect the heat sink to the primary GND plane to improve EMI and thermal dissipation.
4) Place the control circuit capacitors (for FB, PRO, and VCC) close to the IC to decouple the switching voltage noise.
5) Enlarge the GND pad near the IC for good thermal dissipation.
6) Keep the EMI filter far away from the switching point.
7) Ensure the two outputs clearance distance satisfy the insulation requirement.

a) Top

b) Bottom

Figure 11: Recommended PCB Layout

## Design Example

Table 2 is a design example using the application guidelines for the given specifications:

Table 2: Design Example

| $\mathbf{V}_{\text {IN }}$ | 85 to 420 VAC |
| :---: | :---: |
| $\mathbf{V}_{\text {out1 }}$ | 12.5 V |
| $\mathbf{l}_{\text {OUT1 }}$ | 0.4 A |
| $\mathbf{V}_{\text {out2 }}$ | 5 V |
| $\mathbf{l}_{\text {out2 }}$ | 0.05 A |
| $\mathbf{f}_{\mathbf{s}}$ | 100 kHz |

The detailed application schematic is shown in Figure 12. The typical performance and circuit waveforms have been shown in the typical performance characteristics section. For more device applications, please refer to the related evaluation board datasheets.

## TYPICAL APPLICATION CIRCUITS



Figure 12: Typical Application Schematic


Figure 13: Transformer Structure

Table 3: Winding Order

| Tape ( T ) | Winding | Margin Wall PRI side | $\begin{gathered} \text { Terminal } \\ \text { Start—End } \end{gathered}$ | Margin Wall SEC side | Wire Size ( $\varphi$ ) | Turns ( ${ }^{\text {( }}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | N1 | 0 mm | $1 \rightarrow \mathrm{NC}$ | 0 mm | $0.18 \mathrm{~mm} * 2$ | 18 |
|  | N2 | Omm | $2 \rightarrow 1$ | 0mm | $0.18 \mathrm{mm*1}$ | 125 |
|  | N3 | Omm | $4 \rightarrow 3$ | Omm | $0.15 \mathrm{~mm}{ }^{*}$ | 14 |
|  | N4 | 0 mm | $5 \rightarrow 6$ | 0mm | $0.4 \mathrm{~mm} * 1$ | 14 |
| 3 | N5 | 3 mm | $10 \rightarrow 9$ | 3 mm | $0.2 \mathrm{~mm} * 1$ | 9 |

## FLOW CHART



## EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS



## PACKAGE INFORMATION

## PDIP8-7EP



SIDE VIEW

## NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH ,OR PROTRUSIONS.
3) JEDEC REFERENCE IS MS-001, VARIATION BA.
4) DRAWING IS NOT TO SCALE.

## SOIC14-11



## FRONT VIEW

SIDE VIEW


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

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Наши контакты:
Телефон: +7 8126271435
Электронная почта: sales@st-electron.ru
Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера H, помещение 100-Н Офис 331

