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## USB HIGH-SIDE POWER SWITCH

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NO.EA-188-150402

### OUTLINE

The R5524x is a CMOS-based high-side MOSFET switch IC which conforms to the universal serial bus (USB) standard. The device is suitable for protecting a USB power source.

By using an Nch MOSFET with low On-resistance (Typ. 100 mΩ) as a switching transistor, the device can provide low dropout voltage.

Internally, the device consists of an overcurrent limiting circuit, a thermal shutdown circuit, an undervoltage lockout (UVLO) circuit and a reverse current protection circuit. The device also consists of an internal delay circuit to prevent the output of false flag signals caused by inrush current.

To achieve simplification of layout design, the overcurrent detection accuracy has been improved.

The R5524x is offered in a 5-pin SOT-23-5 package and a 6-pin DFN(PLP)1820-6 package which achieve the smallest possible footprint solution on boards where area is limited.

### FEATURES

- N-channel MOS High-Side Switch IC
- Switch ON Resistance ..... Typ. 100 mΩ at 5 V Input
- Current Limit Threshold ..... Min. 650 mA<sup>\*1</sup>, Min. 1.25 A<sup>\*2</sup>
- Overcurrent Limit ..... Min. 550 mA
- Flag Delay Time ..... Typ. 20 ms
- Under-voltage Lockout (UVLO) Circuit
- Thermal Shutdown Circuit
- Reverse Current Protection Circuit
- Package ..... SOT-23-5, DFN(PLP)1820-6<sup>\*3</sup>

### APPLICATIONS

- PCs and PC Peripherals
- Digital Televisions (DTV)
- Set Top Boxes (STB)
- Printers
- PDA
- Game Consoles

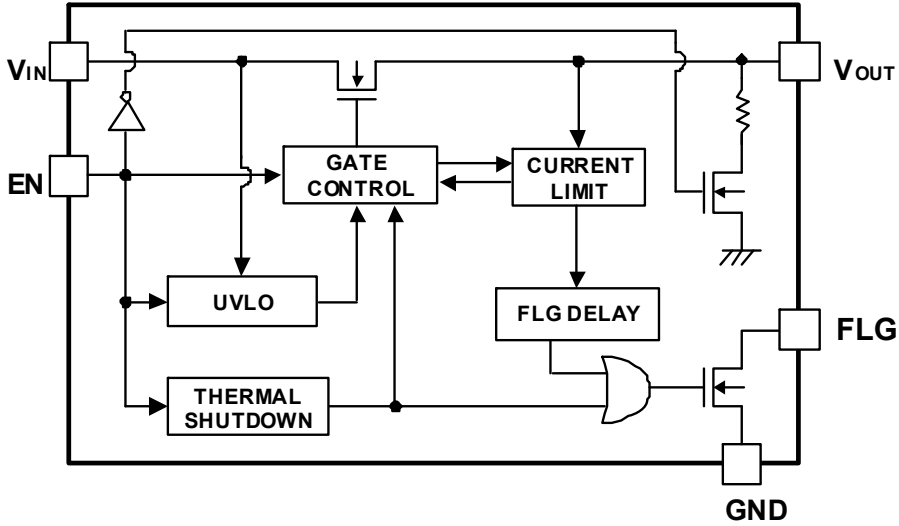
<sup>\*1</sup> only for R5524x001A/B, R5524x002A/B

<sup>\*2</sup> only for R5524N004A

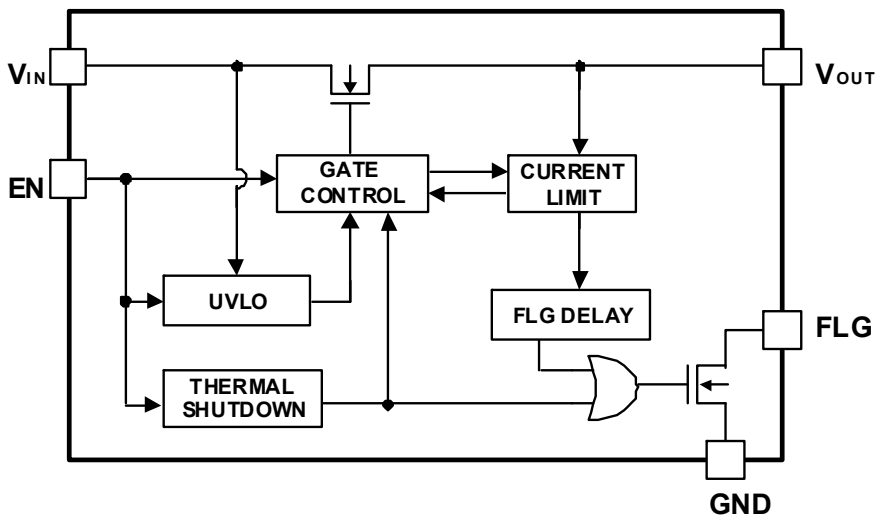
<sup>\*3</sup> only for R5524K001x, R5524K002x

**BLOCK DIAGRAMS**

**R5524xxxxA Block Diagram**



**R5524xxxxB Block Diagram**



## SELECTION GUIDE

The overcurrent limit protection type, the current limit threshold and the auto discharge options\*<sup>1</sup> for the ICs are user-selectable options.

### Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5524N00x*-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes
R5524K00x*-TR	DFN(PLP)1820-6	5,000 pcs	Yes	Yes

x: Specify the combination of Overcurrent Limit Protection type and Current Limit Threshold.

1: Latch-off Type, Current Limit Threshold: Min. 650 mA

2: Constant Current Type, Current Limit Threshold: Min. 650 mA

4: Constant Current Type, Current Limit Threshold: Min. 1.25 A\*<sup>2</sup>

\*: Specify auto-discharge options.

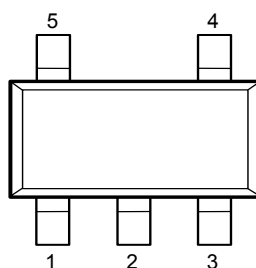
A: Auto-discharge included

B: Auto-discharge not included

\*<sup>1</sup> Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

\*<sup>2</sup> only for R5524N004A

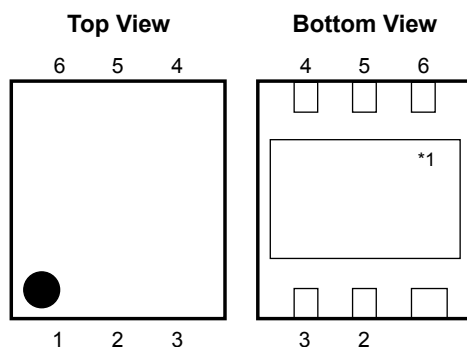
## PIN DESCRIPTIONS



SOT-23-5 Pin Configuration

### SOT23-5 Pin Description

Pin No.	Symbol	Description
1	V <sub>IN</sub>	Input Pin
2	GND	Ground Pin
3	EN	Chip Enable Pin, Active-high
4	FLG	Flag Pin, Open Drain Output
5	V <sub>OUT</sub>	Output Pin



**DFN(PLP)1820-6 Pin Configuration**

**DFN(PLP)1820-6 Pin Description**

Pin No.	Symbol	Description
1	$V_{OUT}$	Output Pin
2	NC	No Connection
3	FLG	Flag Pin, Open Drain Output
4	EN	Enable Pin, Active-high
5	GND	Ground Pin
6	$V_{IN}$	Input Pin

\*1 The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

## ABSOLUTE MAXIMUM RATINGS

### Absolute Maximum Ratings

Symbol	Item	Rating	Unit	
$V_{IN}$	Input Voltage	6.0	V	
$V_{EN}$	Enable Pin Input Voltage	-0.3 to 6.0	V	
$V_{FLG}$	Flag Pin Voltage	-0.3 to 6.0	V	
$I_{FLG}$	Flag Pin Current	14	mA	
$V_{OUT}$	Output Pin Voltage	-0.3 to 6.0	V	
$I_{OUT}$	Output Current	Internally Controlled		
$P_D$	Power Dissipation (Standard Land Pattern) <sup>*1</sup>	SOT-23-5	420	mW
		DFN(PLP)1820-6	880	mW
$T_a$	Operating Temperature Range	-40 to 85	°C	
$T_{stg}$	Storage Temperature Range	-55 to 125	°C	

<sup>\*1</sup> Refer to *PACKAGE INFORMATION* for detailed information.

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

**R5524x**

NO.EA-188-150402

**ELECTRICAL CHARACTERISTICS**The specifications surrounded by   are guaranteed by design engineering at  $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ .**Electrical Characteristics**

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
V <sub>IN</sub>	Input Voltage		2.7		5.5	V	
I <sub>DD1</sub>	Supply Current (Active Mode)	V <sub>OUT</sub> = OPEN, EN = "H", V <sub>IN</sub> = 5 V		110	180	μA	
I <sub>DD2</sub>	Supply Current (Standby Mode)	V <sub>OUT</sub> = OPEN, EN = "L", V <sub>IN</sub> = 5 V		0.1	1.0	μA	
R <sub>ON</sub>	Switch On Resistance	V <sub>IN</sub> = 5 V, I <sub>OUT</sub> = 500 mA		100	150	mΩ	
t <sub>on</sub>	Output Turn-on Delay	V <sub>IN</sub> = 5 V, R <sub>L</sub> = 60 Ω		400		μs	
t <sub>off</sub>	Output Turn-off Delay	V <sub>IN</sub> = 5V, R <sub>L</sub> = 60 Ω		50		μs	
V <sub>UVLO</sub>	UVLO Release Voltage	V <sub>IN</sub> Rising	2.3	2.5	2.7	V	
V <sub>HYS</sub>	UVLO Hysteresis Range	V <sub>IN</sub> Falling		0.1		V	
I <sub>TH</sub>	Current Limit Threshold	R5524x001A/ 001B R5524x002A/ 002B	V <sub>IN</sub> = 5 V	650	800	980	mA
		R5524N004A	V <sub>IN</sub> = 5 V	1.25	1.55	1.85	
			V <sub>IN</sub> = 5 V, Ta = 0 to 70°C	1.2	1.55	1.9	
I <sub>LIM</sub>	Overcurrent Limit	V <sub>IN</sub> = 5 V, V <sub>OUT</sub> = 0 V, after 5 ms	550	650	800	mA	
t <sub>FD</sub>	Flag Delay Time <sup>*1</sup>	V <sub>IN</sub> = 5 V, starts when overcurrent is detected and ends when FLG = "L"	7	20	30	ms	
T <sub>TSD</sub>	Thermal Shutdown Temperature	Junction Temperature		135		°C	
T <sub>TSR</sub>	Thermal Shutdown Released Temperature	Junction Temperature		120		°C	
I <sub>EN</sub>	Enable Pin Input Current			0.01	1.0	μA	
V <sub>EN1</sub>	Enable Pin Input Voltage 1	V <sub>EN</sub> Rising	2.0		6.0	V	
V <sub>EN2</sub>	Enable Pin Input Voltage 2	V <sub>EN</sub> Falling	-0.3		0.8	V	
I <sub>LO</sub>	Output Leakage Current			0.1	1.0	μA	
V <sub>LF</sub>	Flag "L" Output Voltage	I <sub>SINK</sub> = 1 mA			0.4	V	
I <sub>FOF</sub>	Flag Off Current	V <sub>FLG</sub> = 5.5 V		0.01	1.0	μA	
I <sub>REV</sub>	Reverse Leakage Current	V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 5.5 V			50	μA	
R <sub>LOW</sub>	Nch. On-resistance for Auto Discharge (R5524x00xA)			450		Ω	

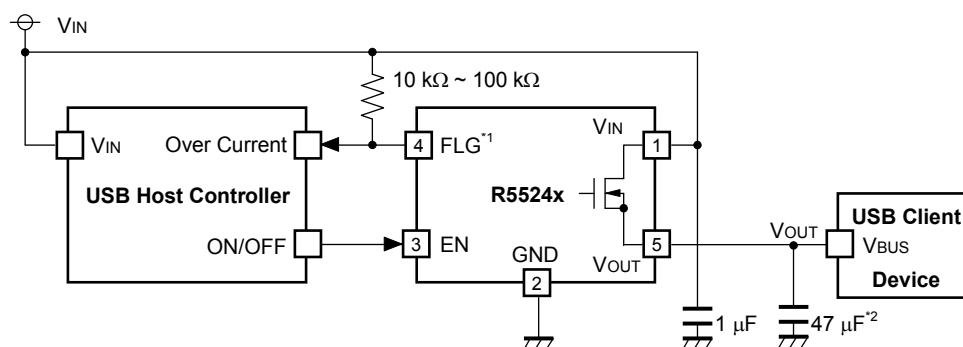
All test items listed under Electrical Characteristics are done under the pulse load condition (T<sub>j</sub> ≈ T<sub>a</sub> = 25°C) except Thermal Shutdown Temperature and Thermal Shutdown Released Temperature.

\*1 Flag Delay Time is dependent on Input Voltage.

**RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)**

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

## TYPICAL APPLICATION



R5524x Typical Application

\*1 FLG pin is Nch. Open Drain Output.

\*2 A 47  $\mu\text{F}$  or more output capacitor is recommended. According to a USB standard, a 120  $\mu\text{F}$  or more output capacitor is required.

## TECHNICAL NOTES

### Bypass Capacitor

A 0.1  $\mu\text{F}$  to 1  $\mu\text{F}$  bypass capacitor between the  $V_{\text{IN}}$  pin and the GND pin, close to the device, is recommended. This precaution reduces power supply transients that may cause ringing on the input.

### Pull-up Resistor of FLG Pin

A 10 k $\Omega$  to 100 k $\Omega$  pull-up resistor is recommended for the FLG pin.

### R5524x001A/001B

The R5524x001A/001B is equipped with a latch-off function which requires initialization before start-up.

#### Case 1: Start-up by EN Pin Control

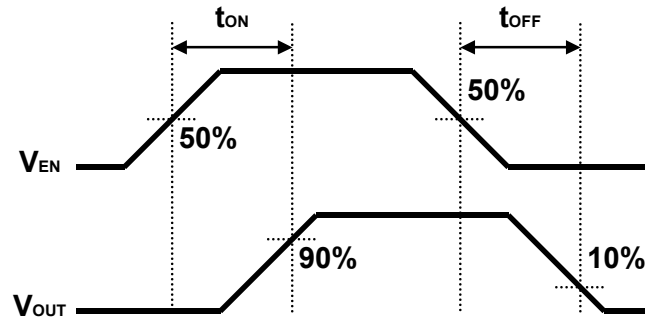
EN pin must be enabled with the delay of 10  $\mu\text{s}$  or more against 90% of  $V_{\text{IN}}$  voltage rising edge.

#### Case 2: Start-up by EN Pin Tied to $V_{\text{IN}}$ Pin

Slew rate of  $V_{\text{IN}}$  must be 40  $\mu\text{s}/\text{V}$  or slower.

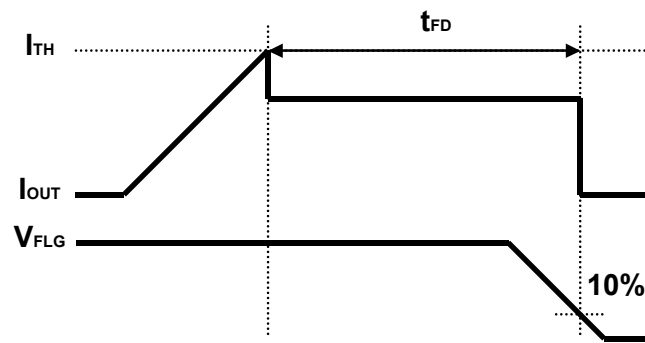
**TIMING CHART**

**Output On-time and Output Off-time**

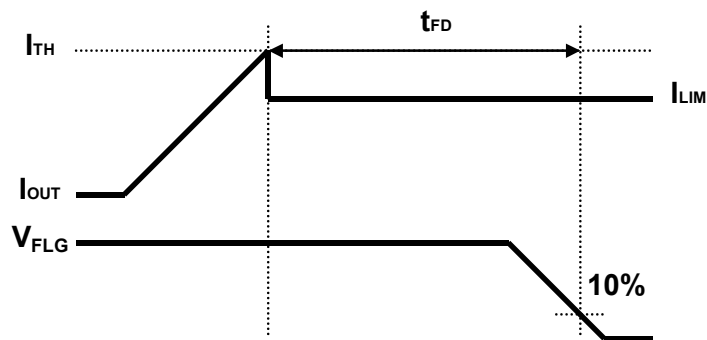


R5524x Timing Chart

**Flag Delay Time**



R5524x001A/001B Timing Chart (Latch-off Type)



R5524x002A/002B and R5524N004A Timing Chart (Constant Current Type)



## Overcurrent Limiting Function

The R5524x001A/001B has the built-in latch-off type over-current limit circuit. When the over-current is detected, the protection circuit becomes active and the switch-transistor is turned OFF. The latch function is released if the input voltage value is exceeded in the release threshold of the UVLO circuit value after when it became lower than the detection threshold of the UVLO circuit value; or the EN pin set to the enabling condition again after set to the disabling condition.

If the over current condition occurred when the input voltage value was close to the minimum operating input voltage value. Under this condition, the voltage descends by the parasitic impedance on the power supply side, and it might fall below the detection threshold of the UVLO circuit. In this case, the switch-transistor is turned OFF and because of that the voltage drop of power line's parasitic impedance stops; the latch function is released with the UVLO and it becomes the over current condition again. The switch transistor keeps continual ON and OFF until one of the following is done; increasing the input voltage value; the setting of EN pin is disabling; or reducing the value of load current.

Moreover, the supply-voltage changed by the load-current dramatically changed depends upon the parasitic impedance of the wiring on the load side or the power supply side. Due to this, decreasing the parasitic impedance by the wiring on board is recommended.

The switch transistor of the R5524x001A/001B is turned OFF when the latch-off-function operates under the condition of the load of the constant current as the load device, such as the electronic load and so on, connecting with the  $V_{OUT}$  pin of the R5524x001A/001B. Because the load device keeps the constant current, the  $V_{OUT}$  pin voltage may become negative potential. If the  $V_{OUT}$  pin is exceed the absolute maximum rating may cause the permanent damages to the device, please avoid using in this situation.

The R5524x002A/002B and R5524N004A have the built-in over current protection circuit as the constant current type. It detects as the over-current condition, if the current flows as the  $I_{TH}$  defined. Then operating the switch transistor to limit the output current to be the constant current defined by the  $I_{LIM}$ .

If the condition of the over-current limit caused by the  $V_{OUT}$  pin clamped to the GND were continued the temperature of the ICs would increase drastically. The switch-transistor is turned OFF if the temperature of the ICs becomes over 135°C (Typ.). And after this, the switch-transistor is turned ON again when the temperature of ICs decreased approximately 15°C. The switch-transistor keeps continual ON and OFF until either the switch is turned OFF or the  $V_{OUT}$  pin is removed from GND.

**PACKAGE INFORMATION**

**Power Dissipation (SOT-23-5)**

Power Dissipation ( $P_D$ ) of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement. This data is taken from a SOT-23-6 package data.

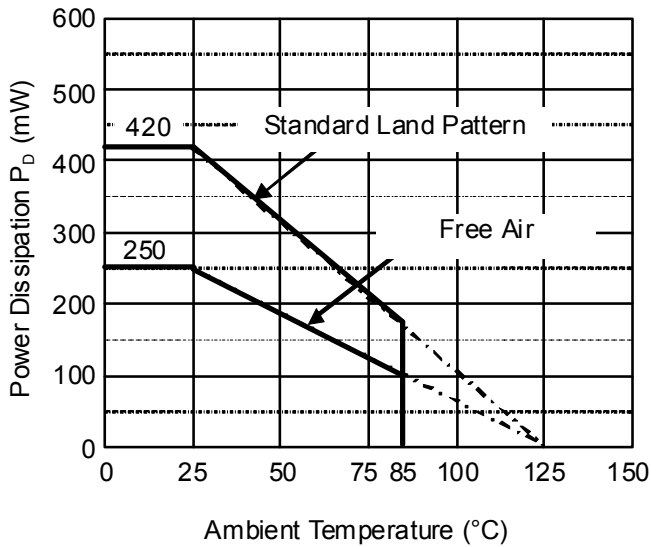
**Measurement Conditions**

	<b>Standard Land Pattern</b>
Environment	Mounting on Board (Wind Velocity = m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-sided)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top-side: Approx. 50%, Back-side: Approx. 50%
Through-holes	φ 0.5 mm × 44 pcs

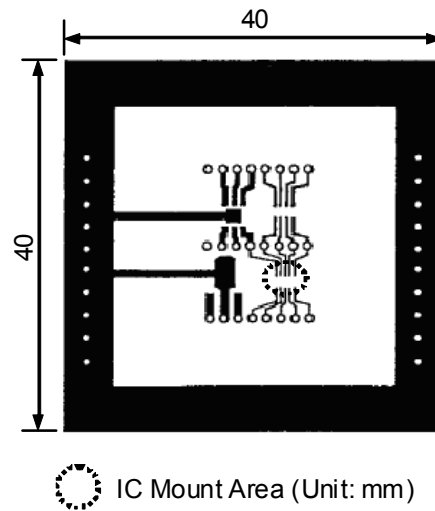
**Measurement Result**

( $T_a = 25^\circ\text{C}$ ,  $T_{j\text{max}} = 125^\circ\text{C}$ )

	<b>Standard Land Pattern</b>	<b>Free Air</b>
Power Dissipation	420 mW	250 mW
Thermal Resistance	$\Theta_{ja} = (125 - 25^\circ\text{C}) / 0.42 \text{ W} = 238^\circ\text{C/W}$	400°C/W

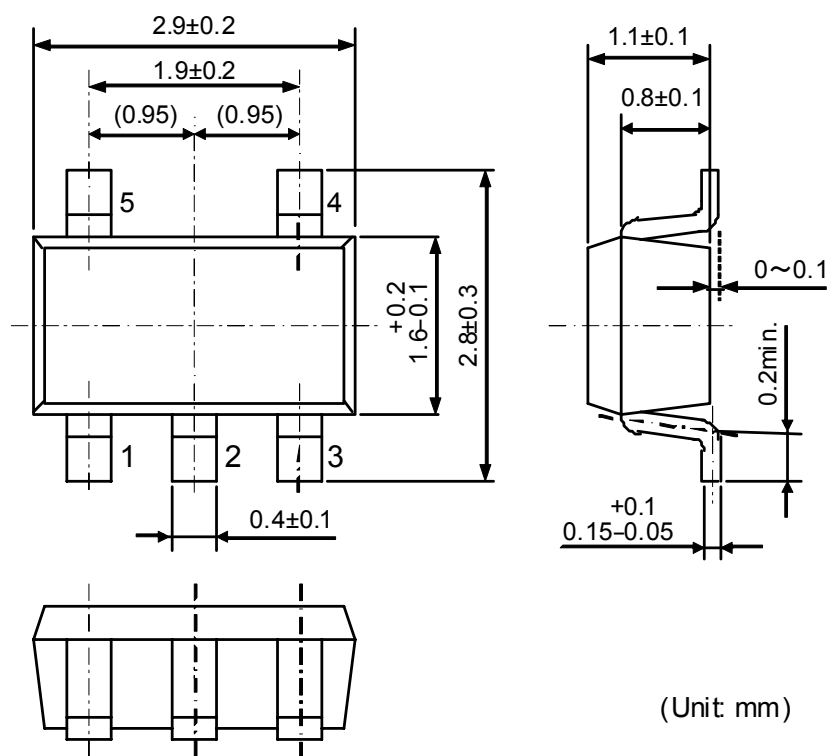


**Power Dissipation vs. Ambient Temperature**



**Measurement Board Pattern**

## PACKAGE DIMENSIONS (SOT-23-5)

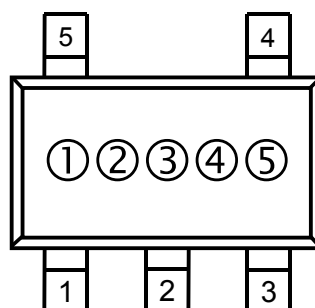


SOT-23-5 Package Dimensions

## MARK SPECIFICATION (SOT-23-5)

①②③: Product Code ... Refer to MARK SPECIFICATION TABLE (SOT-23-5)

④⑤: Lot Number ... Alphanumeric Serial Number



SOT-23-5 Mark Specification

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**R5524x**NO.EA-188-150402

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**MARK SPECIFICATION TABLE (SOT-23-5)****Mark Specification Table**

<b>Product Name</b>	<b>①②③</b>
R5524N001A	M A A
R5524N001B	M A B
R5524N002A	M A C
R5524N002B	M A D
R5524N004A	M A F

**POWER DISSIPATION (DFN(PLP)1820-6)**

Power Dissipation ( $P_D$ ) of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

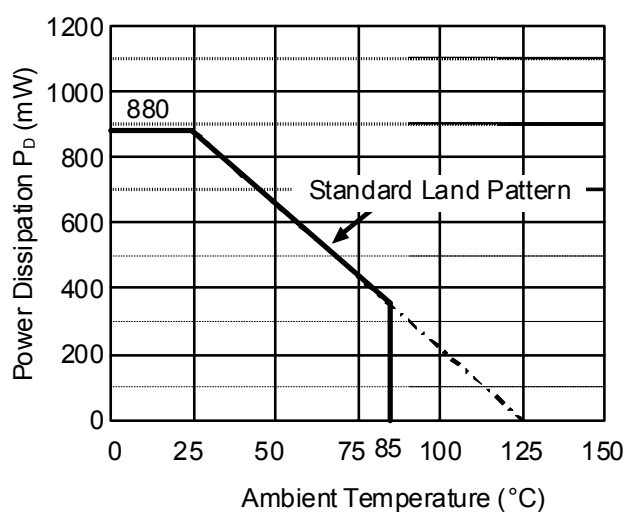
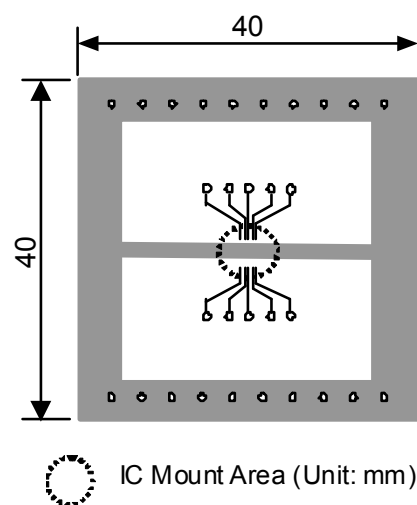
**Measurement Conditions**

	<b>Standard Land Pattern</b>
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-sided)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top-side: Approx. 50%, Back-side: Approx. 50%
Through-hole	φ 0.54 mm × 30 pcs

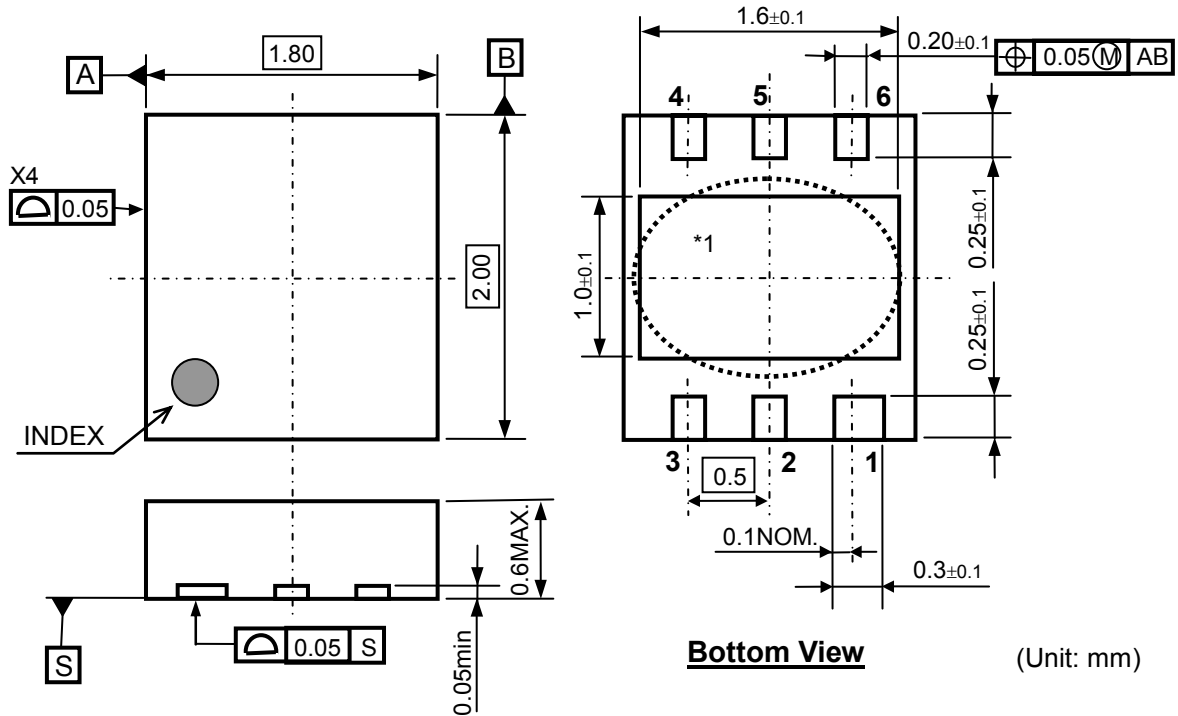
**Measurement Result**

(Ta = 25°C, Tjmax = 125°C)

	<b>Standard Land Pattern</b>
Power Dissipation	880 mW
Thermal Resistance	$\Theta_{ja} = (125 - 25^\circ\text{C}) / 0.88 \text{ W} = 114^\circ\text{C/W}$

**Power Dissipation vs. Ambient Temperature****Measurement Board Pattern**

PACKAGE DIMENSIONS (DFN(PLP)1820-6)

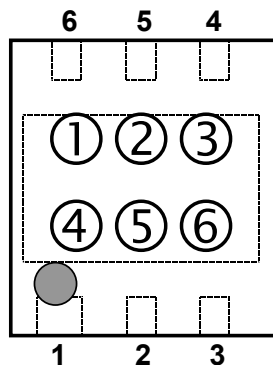


\*1 The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

DFN(PLP)1820-6 Package Dimensions

MARK SPECIFICATION (DFN(PLP)1820-6)

- ①②③④: Product Code ... Refer to **MARK SPECIFICATION TABLE (DFN(PLP)1820-6)**
- ⑤⑥: Lot Number ... Alphanumeric Serial Number

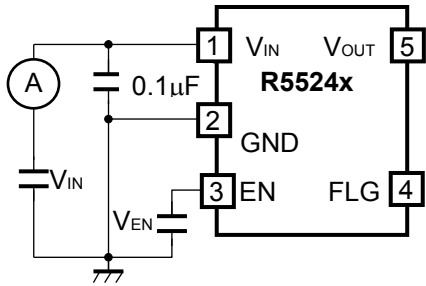


DFN(PLP)1820-6 Mark Specification

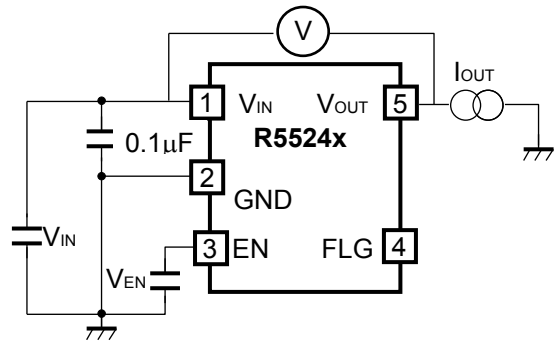
**MARK SPECIFICATION TABLE (DFN(PLP)1820-6)****Mark Specification Table**

<b>Product Name</b>	<b>①②③④</b>
R5524K001A	E J 0 0
R5524K001B	E J 0 1
R5524K002A	E J 0 2
R5524K002B	E J 0 3

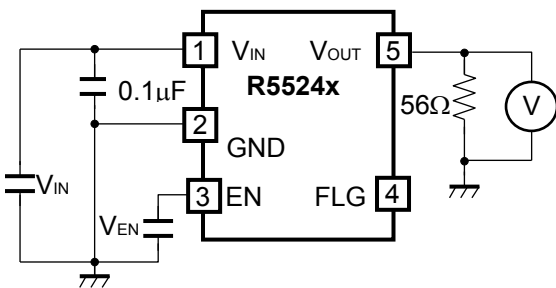
**TEST CIRCUITS**



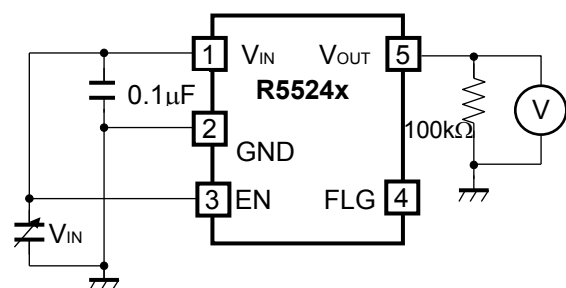
**Supply Current Test Circuit**



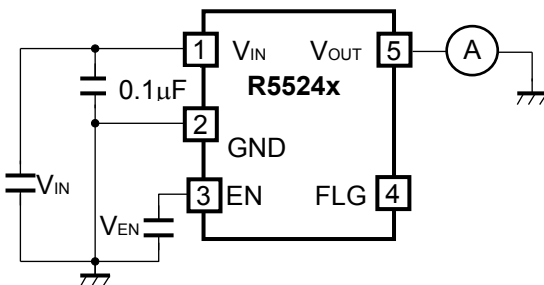
**Switch ON Resistance Test Circuit**



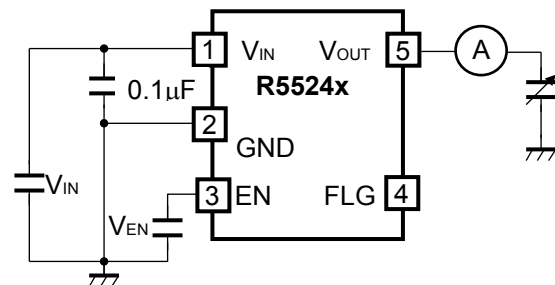
**Output ON Time/Output OFF Time Test Circuit**



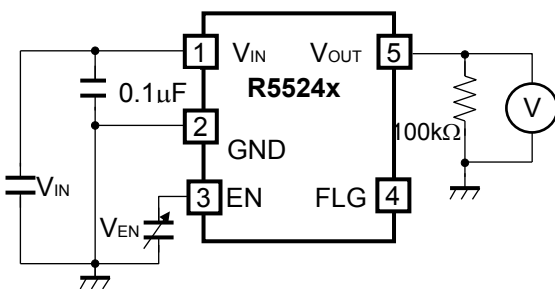
**UVLO Released Voltage Test Circuit**



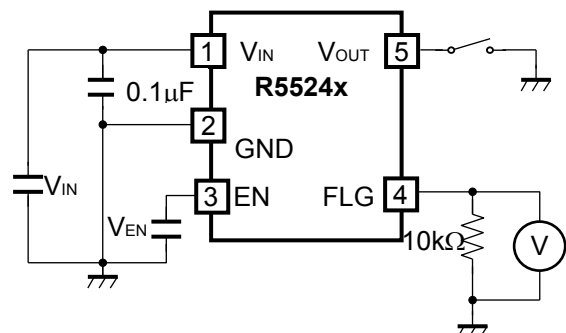
**Over current Limit Test Circuit**



**Current Limit Threshold Test Circuit**



**Enable Input Voltage Test Circuit**



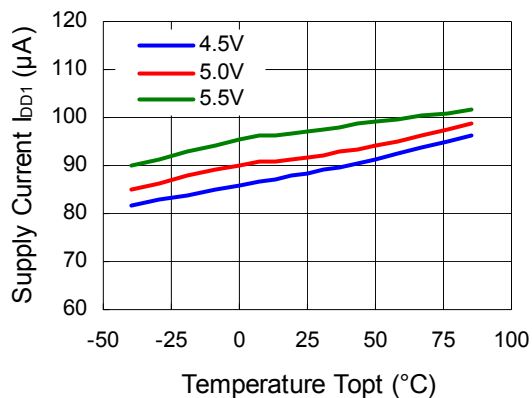
**Flag Output Delay Time Test Circuit**



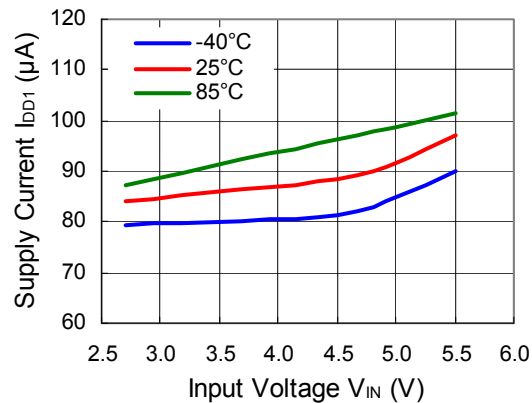
## TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

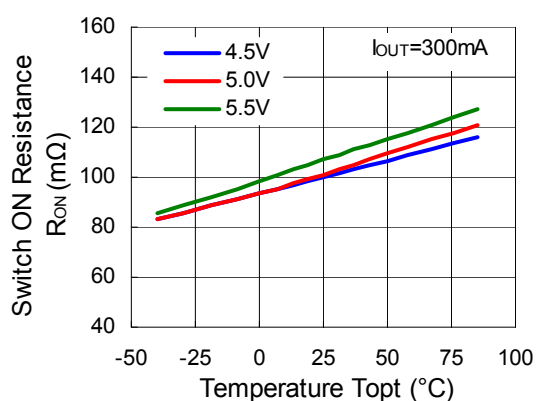
### 1) Supply Current vs. Temperature



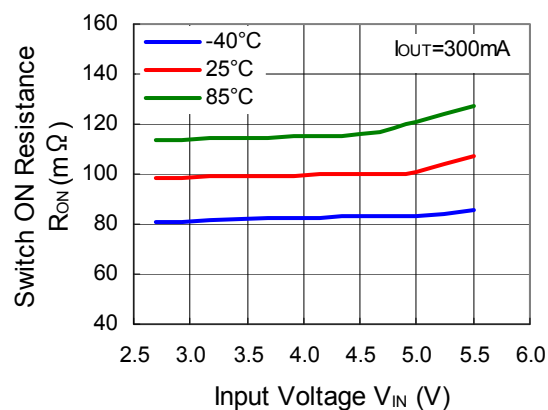
### 2) Supply Current vs. Input Voltage



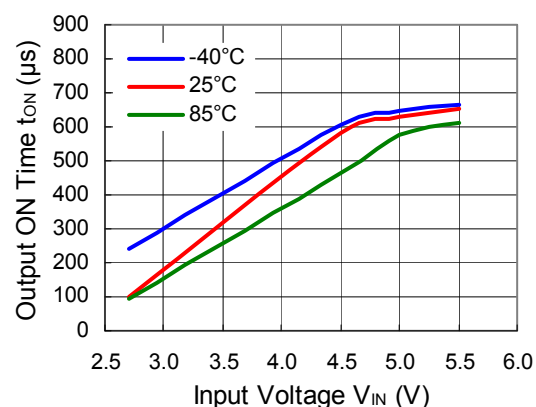
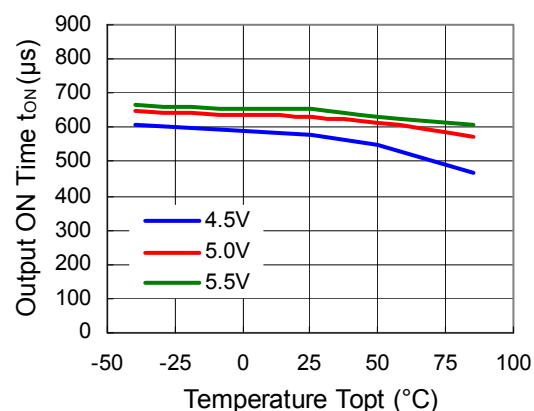
### 3) Switch ON Resistance vs. Temperature



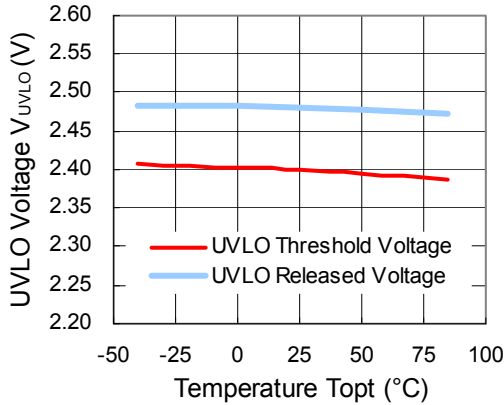
### 4) Switch ON Resistance vs. Input Voltage



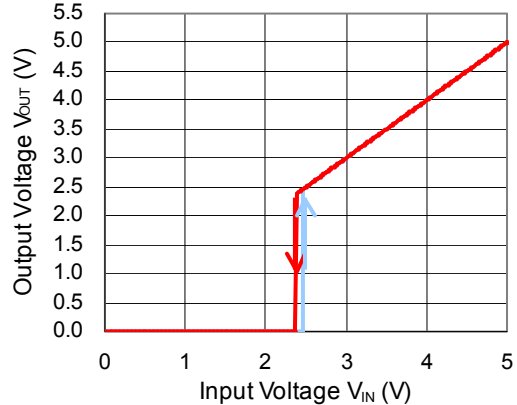
### 5) Output ON Time vs. Temperature ( $R_L = 56 \Omega$ ) 6) Output ON Time vs. Input Voltage ( $R_L = 56 \Omega$ )



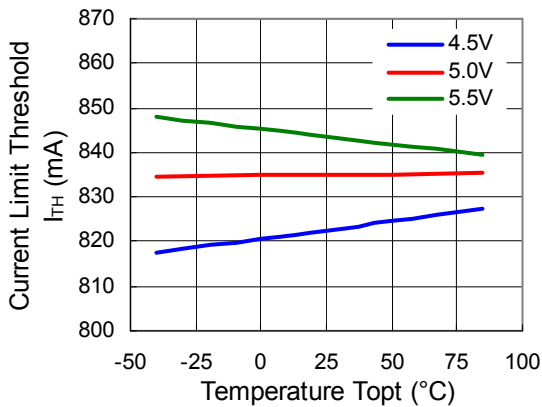
7) UVLO Voltage vs. Temperature



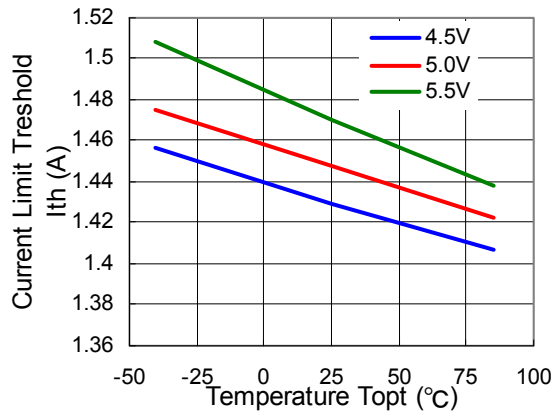
8) Output Voltage vs. Input Voltage



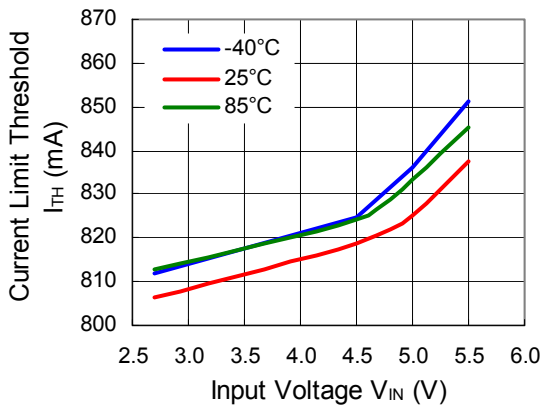
9) Current Limit Threshold vs. Temperature (001x/ 002x)



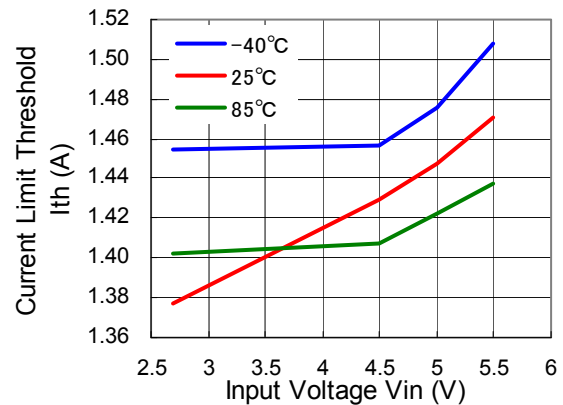
10) Current Limit Threshold vs. Temperature (004A)



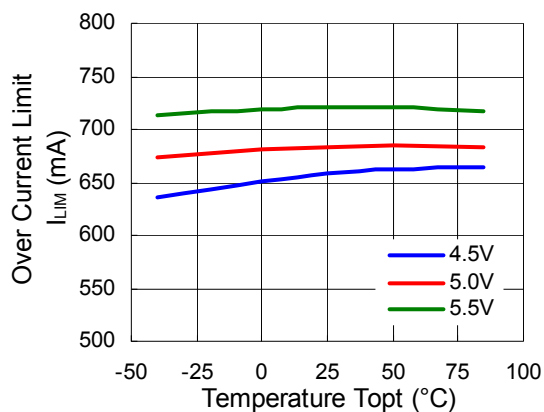
11) Current Limit Threshold vs. Input Voltage (001x/ 002x)



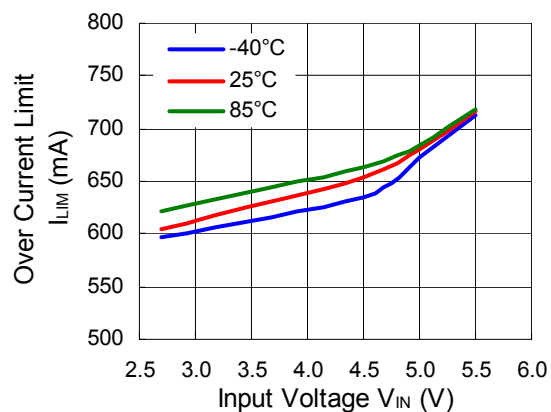
12) Current Limit Threshold vs. Input Voltage (004A)



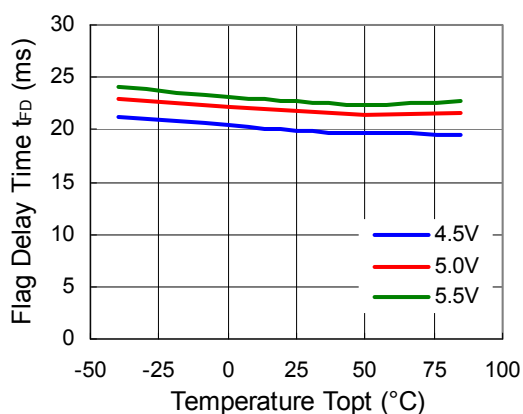
## 13) Overcurrent Limit vs. Temperature



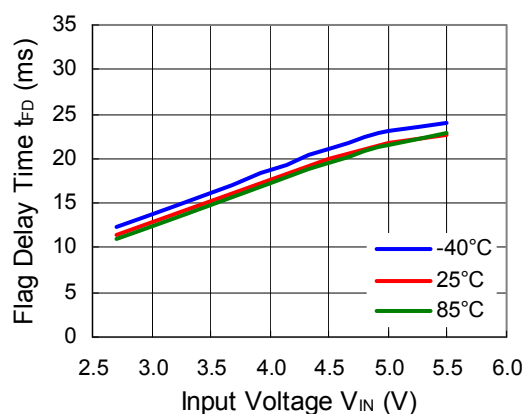
## 14) Overcurrent Limit vs. Input Voltage



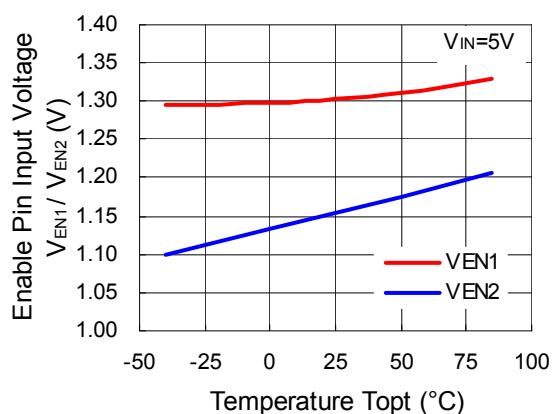
## 15) Flag Delay Time vs. Temperature



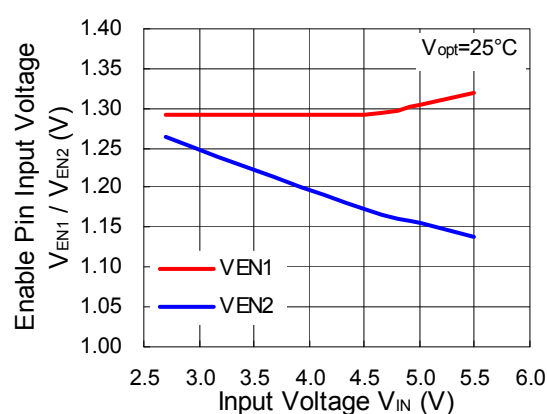
## 16) Flag Delay Time vs. Input Voltage



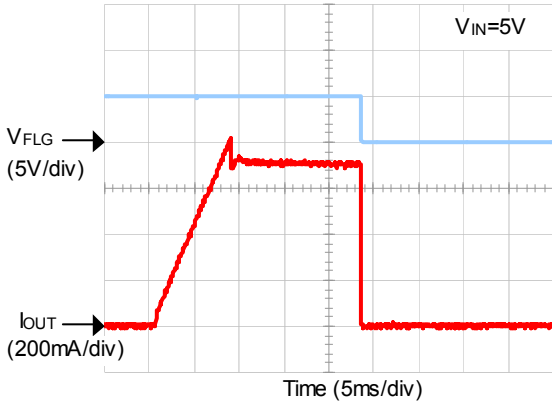
## 17) Enable Input Voltage vs. Temperature



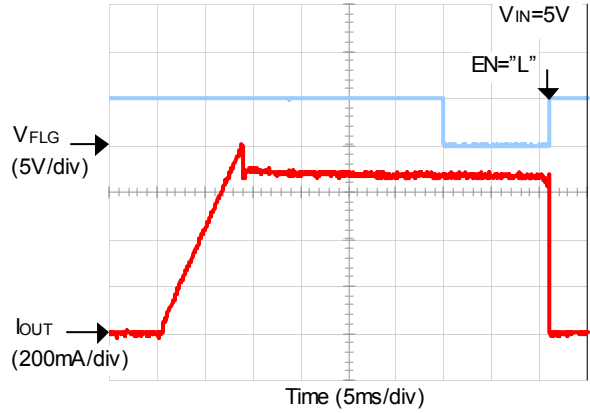
## 18) Enable Input Voltage vs. Input Voltage



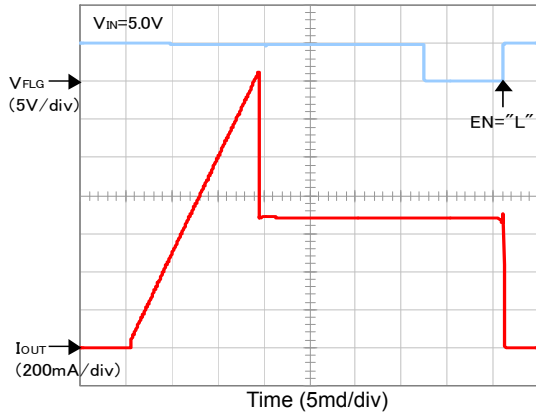
19) Overcurrent Response with Ramped Load (R5524x001x)



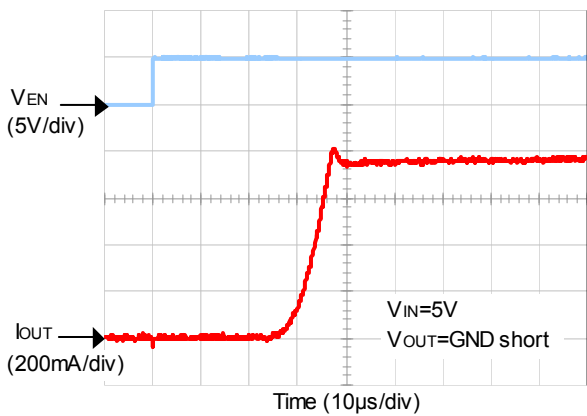
20) Overcurrent Response with Ramped Load (R5524x002x)



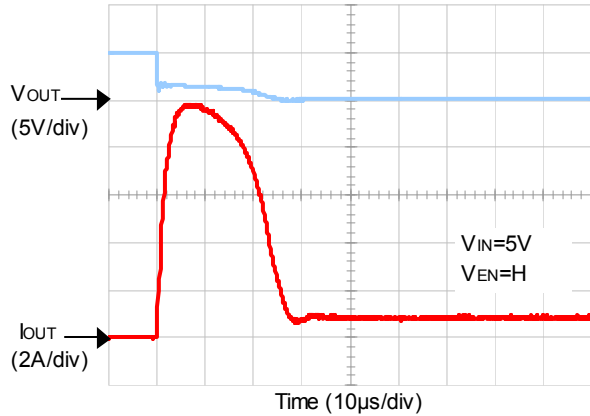
21) Overcurrent Response with Ramped Load (R5524x004A)



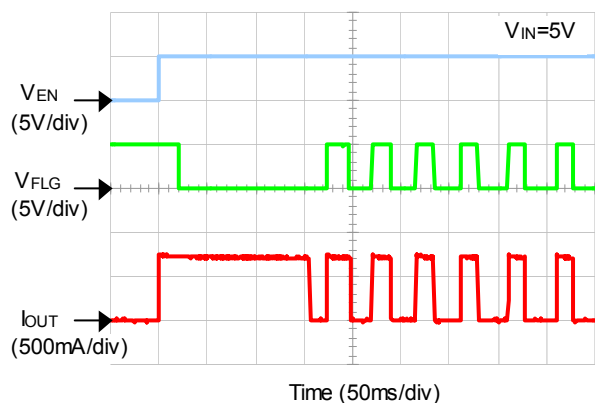
22) Overcurrent Limit Transient Response (Output short during enable "H")



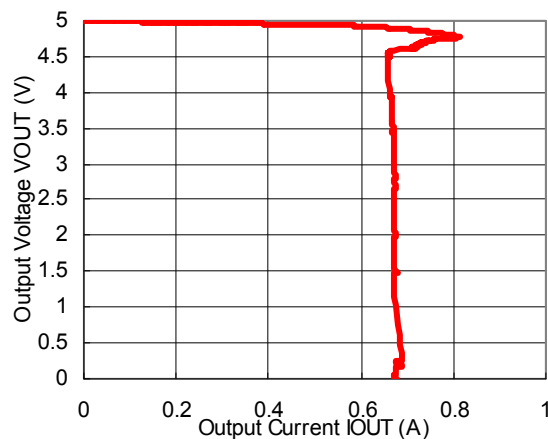
(Enable "H" during Output Short)



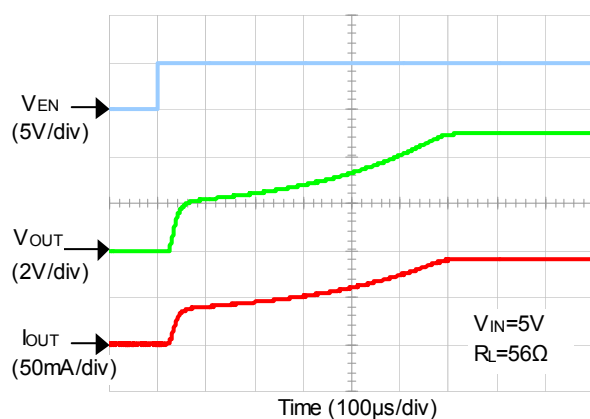
### 23) Thermal Shutdown Operation



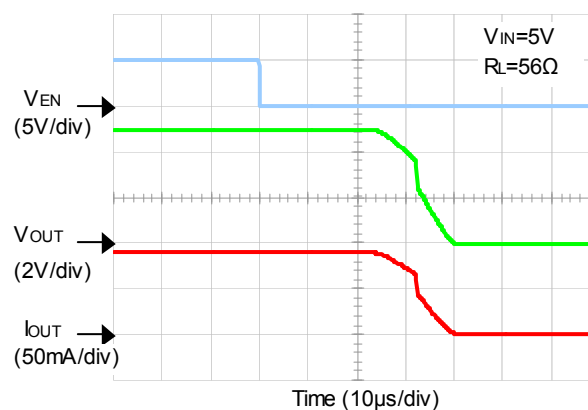
### 24) Output Voltage vs. Output Current



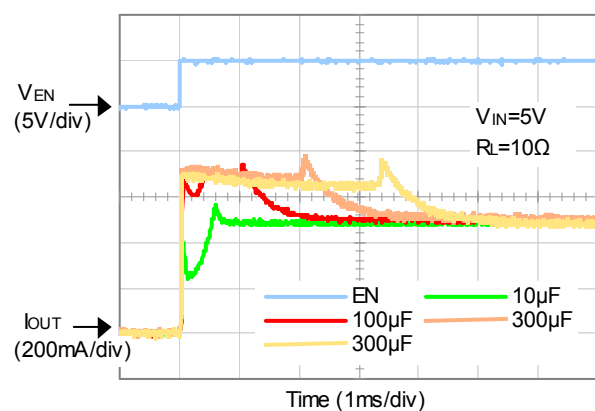
### 25) Output ON Time Response



### 26) Output OFF Time Response



### 27) Inrush current Characteristic





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