LTC6813-1

18-Cell Battery Monitor with Daisy Chain Interface

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
- **Measures Up to 18 Battery Cells in Series**
- **2.2mV Maximum Total Measurement Error**
- **Stackable Architecture for High Voltage Systems**
- **Built-In isoSPI™ Interface**
  - 1Mb Isolated Serial Communications
  - Uses a Single Twisted Pair, Up to 100 Meters
  - Low EMI Susceptibility and Emissions
  - Bidirectional for Broken Wire Protection
- 290μs to Measure All Cells in a System
- Synchronized Voltage and Current Measurement
- 16-Bit Delta-Sigma ADC with Programmable 3rd Order Noise Filter
- Engineered for ISO 26262-Compliant Systems
- Passive Cell Balancing Up to 200mA (Max) with Programmable Pulse-Width Modulation
- 9 General Purpose Digital I/O or Analog Inputs
  - Temperature or Other Sensor Inputs
  - Configurable as an I^{2}C or SPI Master
- 6μA Sleep Mode Supply Current
- 64-Lead eLQFP Package

APPLICATIONS

- Electric and Hybrid Electric Vehicles
- Backup Battery Systems
- Grid Energy Storage
- High Power Portable Equipment

DESCRIPTION

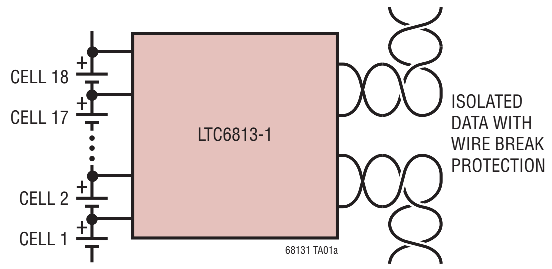
The LTC®6813-1 is a multicell battery stack monitor that measures up to 18 series connected battery cells with a total measurement error of less than 2.2mV. The cell measurement range of 0V to 5V makes the LTC6813-1 suitable for most battery chemistries. All 18 cells can be measured in 290μs, and lower data acquisition rates can be selected for high noise reduction.

Multiple LTC6813-1 devices can be connected in series, permitting simultaneous cell monitoring of long, high voltage battery strings. Each LTC6813-1 has an isoSPI interface for high speed, RF immune, long distance communications. Multiple devices are connected in a daisy chain with one host processor connection for all devices. This daisy chain can be operated bidirectionally, ensuring communication integrity, even in the event of a fault along the communication path.

The LTC6813-1 can be powered directly from the battery stack or from an isolated supply. The LTC6813-1 includes passive balancing for each cell, with individual PWM duty cycle control for each cell. Other features include an onboard 5V regulator, nine general purpose I/O lines and a sleep mode, where current consumption is reduced to 6μA.

TYPICAL APPLICATION

18-Cell Monitor and Balance IC



Cell 18 Measurement Error vs Temperature

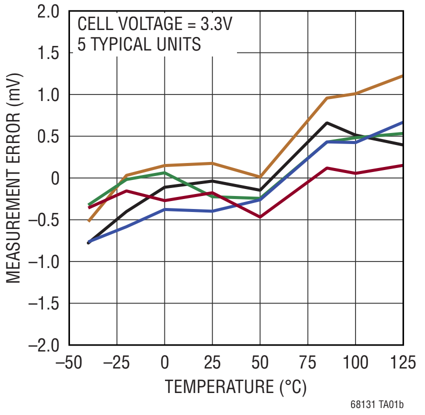


TABLE OF CONTENTS

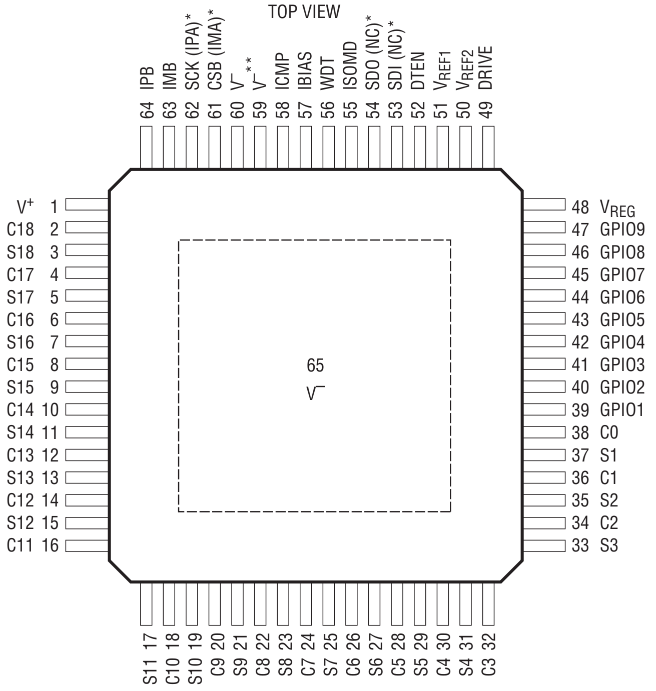
Features 1
Applications 1
Typical Application 1
Description 1
Absolute Maximum Ratings 3
Order Information 3
Pin Configuration 3
Electrical Characteristics 4
Typical Performance Characteristics 9
Pin Functions 15
Block Diagram 16
Improvements from the LTC6811-1 17
Operation 18
  State Diagram 18
  Core LTC6813-1 State Descriptions 18
  isoSPI State Descriptions 19
  Power Consumption 19
  ADC Operation 20
  Data Acquisition System Diagnostics 25
  Watchdog and Discharge Timer 32
  S Pin Pulse-Width Modulation for Cell Balancing 33
  Discharge Timer Monitor 34
  I^2C/SPI Master on LTC6813-1 Using GPIOs 34
  S Pin Pulsing Using the S Pin Control Settings 39
  S Pin Muting 40
  Serial Interface Overview 40
  4-Wire Serial Peripheral Interface (SPI) Physical Layer 40
  2-Wire Isolated Interface (isoSPI) Physical Layer 40
  Data Link Layer 51
  Network Layer 51
Applications Information 67
  Providing DC Power 67
  Internal Protection and Filtering 68
  Cell Balancing 71
  Discharge Control During Cell Measurements 72
  Digital Communications 75
  Enhanced Applications 82
  Reading External Temperature Probes 84
Package Description 86
Revision History 87
Typical Application 88
Related Parts 88

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage	
V^+ to V^-	112.5V
Supply Voltage (Relative to C12)	
V^+ to C12	50V
Input Voltage (Relative to V^-)	
C0	–0.3V to 6V
C18	–0.3V to MIN (V^+ + 5.5V, 112.5V)
C(n), S(n)	–0.3V to MIN (8 • n, 112.5V)
IPA, IMA, IPB, IMB	–0.3V to V_{REG} + 0.3V, ≤ 6V
DRIVE	–0.3V to 7V
All Other Pins	–0.3V to 6V
Voltage Between Inputs	
C(n) to C(n–1), S(n) to C(n–1)	–0.3V to 8V
C18 to C15, C15 to C12, C12 to C9, C9 to C6, C6 to C3, C3 to C0	–0.3V to 21V
Current In/Out of Pins	
All Pins Except V_{REG}, IPA, IMA, IPB, IMB, C(n), S(n)	10mA
IPA, IMA, IPB, IMB	30mA
Specified Junction Temperature Range	
LTC6813I-1	–40°C to 85°C
LTC6813H-1	–40°C to 125°C
Junction Temperature	150°C
Storage Temperature Range	–65°C to 150°C
Device HBM ESD Classification Level 1C	
Device CDM ESD Classification Level C5	

PIN CONFIGURATION



LWE PACKAGE
64-LEAD (10mm × 10mm) PLASTIC eLQFP

T_{JMAX} = 150°C, θ_{JA} = 17°C/W, θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 65) IS V^-, MUST BE SOLDERED TO PCB

*The Function of These Pins Depends on the Connection of ISOMD:
ISOMD Tied to V^-: CSB, SCK, SDI, SDO
ISOMD Tied to V_{REG}: IPA, IMA, NC, NC

**This Pin Must Be Connected to V^-

ORDER INFORMATION

AUTOMOTIVE PRODUCTS**

TRAY (160PC)	TAPE AND REEL (1500PC)	PART MARKING*	PACKAGE DESCRIPTION	MSL RATING	SPECIFIED JUNCTION TEMPERATURE RANGE
LTC6813ILWE-1#3ZZPBF	LTC6813ILWE-1#3ZZTRPBF	LTC6813LWE-1	64-Lead Plastic eLQFP	3	–40°C to 85°C
LTC6813HLWE-1#3ZZPBF	LTC6813HLWE-1#3ZZTRPBF	LTC6813LWE-1	64-Lead Plastic eLQFP	3	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #3ZZ suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 59.4V, V_{REG} = 5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC DC Specifications							
	Measurement Resolution				0.1		mV/Bit
	ADC Offset Voltage	(Note 2)			0.1		mV
	ADC Gain Error	(Note 2)			0.01		%
	Total Measurement Error (TME) in Normal Mode	C(n) to C(n–1), GPIO(n) to V^- = 0			±0.2		mV
		C(n) to C(n–1) = 2.0				±1.6	mV
		C(n) to C(n–1), GPIO(n) to V^- = 2.0, LTC6813I	●			±1.8	mV
		C(n) to C(n–1), GPIO(n) to V^- = 2.0, LTC6813H	●			±2.0	mV
		C(n) to C(n–1) = 3.3				±2.2	mV
		C(n) to C(n–1), GPIO(n) to V^- = 3.3, LTC6813I	●			±3.0	mV
		C(n) to C(n–1), GPIO(n) to V^- = 3.3, LTC6813H	●			±3.3	mV
		C(n) to C(n–1) = 4.2				±2.8	mV
		C(n) to C(n–1), GPIO(n) to V^- = 4.2, LTC6813I	●			±3.8	mV
		C(n) to C(n–1), GPIO(n) to V^- = 4.2, LTC6813H	●			±4.2	mV
		C(n) to C(n–1), GPIO(n) to V^- = 5.0			±1		mV
		Sum of Cells	●		±0.05	±0.35	%
		Internal Temperature, T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●	–1	–0.15	0	%
		V_{REF2} Pin	●	–0.05	0.05	0.20	%
		Digital Supply Voltage, V_{REGD}	●	–0.5	0.5	1.5	%
	Total Measurement Error (TME) in Filtered Mode	C(n) to C(n–1), GPIO(n) to V^- = 0			±0.1		mV
		C(n) to C(n–1) = 2.0				±1.6	mV
		C(n) to C(n–1), GPIO(n) to V^- = 2.0, LTC6813I	●			±1.8	mV
		C(n) to C(n–1), GPIO(n) to V^- = 2.0, LTC6813H	●			±2.0	mV
		C(n) to C(n–1) = 3.3				±2.2	mV
		C(n) to C(n–1), GPIO(n) to V^- = 3.3, LTC6813I	●			±3.0	mV
		C(n) to C(n–1), GPIO(n) to V^- = 3.3, LTC6813H	●			±3.3	mV
		C(n) to C(n–1) = 4.2				±2.8	mV
		C(n) to C(n–1), GPIO(n) to V^- = 4.2, LTC6813I	●			±3.8	mV
		C(n) to C(n–1), GPIO(n) to V^- = 4.2, LTC6813H	●			±4.2	mV
		C(n) to C(n–1), GPIO(n) to V^- = 5.0			±1		mV
		Sum of Cells	●		±0.05	±0.35	%
		Internal Temperature, T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●	–1	–0.15	0	%
		V_{REF2} Pin	●	–0.05	0.05	0.20	%
		Digital Supply Voltage, V_{REGD}	●	–0.5	0.8	1.5	%

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
	Total Measurement Error (TME) in Fast Mode	C(n) to C(n–1), GPIO(n) to V^- = 0				±2		mV
		C(n) to C(n–1), GPIO(n) to V^- = 2.0		●			±4	mV
		C(n) to C(n–1), GPIO(n) to V^- = 3.3		●			±6	mV
		C(n) to C(n–1), GPIO(n) to V^- = 4.2		●			±8.3	mV
		C(n) to C(n–1), GPIO(n) to V^- = 5.0				±10		mV
		Sum of Cells		●		±0.15	±0.5	%
		Internal Temperature, T = Maximum Specified Temperature				±5		°C
		V_{REG} Pin		●	–1.5	–0.15	1	%
		V_{REF2} Pin		●	–0.18	0.05	0.32	%
		Digital Supply Voltage, V_{REGD}		●	–2.5	–0.4	2	%
	Input Range	C(n) n = 1 to 18		●	C(n–1)		C(n–1) + 5	V
		C0		●	0		1	V
		GPIO(n) n = 1 to 9		●	0		5	V
I_L	Input Leakage Current When Inputs Are Not Being Measured	C(n) n = 0 to 18		●		10	±250	nA
		GPIO(n) n = 1 to 9		●		10	±250	nA
	Input Current When Inputs Are Being Measured (State: Core = MEASURE)	C(n) n = 0 to 18				±1		μA
		GPIO(n) n = 1 to 9				±1		μA
	Input Current During Open Wire Detection			●	70	100	130	μA
Voltage Reference Specifications								
V_{REF1}	1st Reference Voltage	V_{REF1} Pin, No Load		●	3.0	3.15	3.3	V
	1st Reference Voltage TC	V_{REF1} Pin, No Load				3		ppm/°C
	1st Reference Voltage Thermal Hysteresis	V_{REF1} Pin, No Load				20		ppm
	1st Reference Voltage Long Term Drift	V_{REF1} Pin, No Load				20		ppm/$\sqrt{\text{khr}}$
V_{REF2}	2nd Reference Voltage	V_{REF2} Pin, No Load		●	2.993	3	3.007	V
		V_{REF2} Pin, 5k Load to V^-		●	2.992	3	3.008	V
	2nd Reference Voltage TC	V_{REF2} Pin, No Load				10		ppm/°C
	2nd Reference Voltage Thermal Hysteresis	V_{REF2} Pin, No Load				100		ppm
	2nd Reference Voltage Long Term Drift	V_{REF2} Pin, No Load				60		ppm/$\sqrt{\text{khr}}$
General DC Specifications								
I_{VP}	V^+ Supply Current (See Figure 1: LTC6813-1 Operation State Diagram)	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 0V			6.1	11	μA
			V_{REG} = 0V	●		6.1	18	μA
			V_{REG} = 5V			3	5	μA
			V_{REG} = 5V	●		3	9	μA
		State: Core = STANDBY			9	14	22	μA
				●	6	14	28	μA
		State: Core = REFUP			0.4	0.55	0.8	mA
				●	0.375	0.55	0.825	mA
		State: Core = MEASURE			0.65	0.95	1.35	mA
				●	0.6	0.95	1.4	mA

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SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
$I_{REG(CORE)}$	V_{REG} Supply Current (See Figure 1: LTC6813-1 Operation State Diagram)	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 5V			3.1	6	μA
			V_{REG} = 5V	●		3.1	9	μA
		State: Core = STANDBY			10	35	60	μA
				●	6	35	65	μA
		State: Core = REFUP			0.4	0.9	1.4	mA
				●	0.3	0.9	1.5	mA
		State: Core = MEASURE			14	15	16	mA
				●	13.5	15	16.5	mA
$I_{REG(isoSPI)}$	Additional V_{REG} Supply Current if isoSPI in READY/ACTIVE States Note: ACTIVE State Current Assumes t_{CLK} = 1μs, (Note 3)	ISOMD = 0, R_{B1} + R_{B2} = 2k	READY	●	3.6	4.5	5.2	mA
			ACTIVE	●	5.6	6.8	8.1	mA
		ISOMD = 1, R_{B1} + R_{B2} = 2k	READY	●	4.0	5.2	6.5	mA
			ACTIVE	●	7.0	8.5	10.5	mA
		ISOMD = 0, R_{B1} + R_{B2} = 20k	READY	●	1.0	1.8	2.4	mA
			ACTIVE	●	1.3	2.3	3.3	mA
		ISOMD = 1, R_{B1} + R_{B2} = 20k	READY	●	1.6	2.5	3.5	mA
			ACTIVE	●	1.8	3.1	4.8	mA
	V^+ Supply Voltage	TME Specifications Met		●	16	60	90	V
	V^+ to C18 Voltage	TME Specifications Met		●	–0.3			V
	V^+ to C12 Voltage	TME Specifications Met		●			40	V
	C13 Voltage	TME Specifications Met		●	2.5			V
	C7 Voltage	TME Specifications Met		●	1			V
V_{REG}	V_{REG} Supply Voltage	TME Supply Rejection < 1mV/V		●	4.5	5	5.5	V
	DRIVE Output Voltage	Sourcing 1μA			5.4	5.7	5.9	V
				●	5.2	5.7	6.1	V
		Sourcing 500μA		●	5.1	5.7	6.1	V
V_{REGD}	Digital Supply Voltage			●	2.7	3	3.6	V
	Discharge Switch ON Resistance	V_{CELL} = 3.6V		●		4	10	Ω
	Thermal Shutdown Temperature					150		°C
$V_{OL(WDT)}$	Watch Dog Timer Pin Low	WDT Pin Sinking 4mA		●			0.4	V
$V_{OL(GPIO)}$	General Purpose I/O Pin Low	GPIO Pin Sinking 4mA (Used as Digital Output)		●			0.4	V
ADC Timing Specifications								
t_{CYCLE} (Figure 3, Figure 4, Figure 6)	Measurement + Calibration Cycle Time When Starting from the REFUP State in Normal Mode	Measure 18 Cells		●	2027	2343	2488	μs
		Measure 3 Cells		●	352	407	432	μs
		Measure 18 Cells and 2 GPIO Inputs		●	2717	3140	3335	μs
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Filtered Mode	Measure 18 Cells		●	174.2	201.3	213.8	ms
		Measure 3 Cells		●	29.1	33.6	35.7	ms
		Measure 18 Cells and 2 GPIO Inputs		●	232.3	268.5	285.1	ms
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Fast Mode	Measure 18 Cells		●	970	1121	1191	μs
		Measure 3 Cells		●	176	203	215	μs
		Measure 18 Cells and 2 GPIO Inputs		●	1307	1511	1605	μs
t_{SKEW1} (Figure 6)	Skew Time. The Time Difference Between Cell 18 and GPIO1 Measurements, Command = ADCVAX	Fast Mode		●	168	194	206	μs
		Normal Mode		●	470	543	577	μs

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SKEW2} (Figure 3)	Skew Time. The Time Difference Between Cell 18 and Cell 1 Measurements, Command = ADCV	Fast Mode	●	202	233	248	µs
		Normal Mode	●	580	670	711	µs
t_{WAKE}	Regulator Start-Up Time	V_{REG} Generated from DRIVE Pin (Figure 32)	●		200	400	µs
t_{SLEEP} (Figure 26)	Watchdog or Discharge Timer	DTEN Pin = 0 or DCTO[3:0] = 0000	●	1.8	2	2.2	sec
		DTEN Pin = 1 and DCTO[3:0] ≠ 0000		0.5		120	min
t_{REFUP} Figure 3 for example)	Reference Wake-Up Time. Added to t_{CYCLE} Time When Starting from the STANDBY State. t_{REFUP} = 0 When Starting from Other States.	t_{REFUP} is Independent of the Number of Channels Measured and the ADC Mode	●	2.7	3.5	4.4	ms
f_S	ADC Clock Frequency				3.3		MHz
SPI Interface DC Specifications							
$V_{IH(SPI)}$	SPI Pin Digital Input Voltage High	Pins CSB, SCK, SDI	●	2.3			V
$V_{IL(SPI)}$	SPI Pin Digital Input Voltage Low	Pins CSB, SCK, SDI	●			0.8	V
$V_{IH(CFG)}$	Configuration Pin Digital Input Voltage High	Pins ISOMD, DTEN, GPIO1 to GPIO9	●	2.7			V
$V_{IL(CFG)}$	Configuration Pin Digital Input Voltage Low	Pins ISOMD, DTEN, GPIO1 to GPIO9	●			1.2	V
$I_{LEAK(DIG)}$	Digital Input Current	Pins CSB, SCK, SDI, ISOMD, DTEN	●			±1	µA
$V_{OL(SDO)}$	Digital Output Low	Pin SDO Sinking 1mA	●			0.3	V
isoSPI DC Specifications (See Figure 17)							
V_{BIAS}	Voltage on IBIAS Pin	READY/ACTIVE State	●	1.9	2.0	2.1	V
		IDLE State			0		V
I_B	Isolated Interface Bias Current	R_{BIAS} = 2k to 20k	●	0.1		1.0	mA
A_{IB}	Isolated Interface Current Gain	$V_A = \le 1.6V$ $I_B = 1mA$	●	18	20	22	mA/mA
		$I_B = 0.1mA$	●	18	20	24.5	mA/mA
V_A	Transmitter Pulse Amplitude	$V_A = \lvert V_{IP} - V_{IM} \rvert$	●			1.6	V
V_{ICMP}	Threshold-Setting Voltage on ICMP Pin	$V_{TCMP} = A_{TCMP} \bullet V_{ICMP}$	●	0.2		1.5	V
$I_{LEAK(ICMP)}$	Input Leakage Current on ICMP Pin	V_{ICMP} = 0V to V_{REG}	●			±1	µA
$I_{LEAK(IP/IM)}$	Leakage Current on IP and IM Pins	IDLE State, V_{IP} or V_{IM}, 0V to V_{REG}	●			±1	µA
A_{TCMP}	Receiver Comparator Threshold Voltage Gain	$V_{CM} = V_{REG}/2$ to $V_{REG} - 0.2V$, V_{ICMP} = 0.2V to 1.5V	●	0.4	0.5	0.6	V/V
V_{CM}	Receiver Common Mode Bias	IP/IM Not Driving		$(V_{REG} - V_{ICMP}/3 - 167mV)$			V
R_{IN}	Receiver Input Resistance	Single-Ended to IPA, IMA, IPB, IMB	●	26	35	45	kΩ
isoSPI Idle/Wake-Up Specifications (See Figure 26)							
V_{WAKE}	Differential Wake-Up Voltage	t_{DWELL} = 240ns	●	200			mV
t_{DWELL}	Dwell Time at V_{WAKE} Before Wake Detection	V_{WAKE} = 200mV	●	240			ns
t_{READY}	Start-Up Time After Wake Detection		●			10	µs
t_{IDLE}	Idle Timeout Duration		●	4.3	5.5	6.7	ms
isoSPI Pulse Timing Specifications (See Figure 22)							
$t_{1/2PW(CS)}$	Chip-Select Half-Pulse Width	Transmitter	●	120	150	180	ns
$t_{FILT(CS)}$	Chip-Select Signal Filter	Receiver	●	70	90	110	ns
$t_{INV(CS)}$	Chip-Select Pulse Inversion Delay	Transmitter	●	120	155	190	ns
$t_{WNDW(CS)}$	Chip-Select Valid Pulse Window	Receiver	●	220	270	330	ns

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{1/2PW(D)}$	Data Half-Pulse Width	Transmitter	●	40	50	60	ns
$t_{FILT(D)}$	Data Signal Filter	Receiver	●	10	25	35	ns
$t_{INV(D)}$	Data Pulse Inversion Delay	Transmitter	●	40	55	65	ns
$t_{WNDW(D)}$	Data Valid Pulse Window	Receiver	●	70	90	110	ns
SPI Timing Requirements (See Figure 16 and Figure 25)							
t_{CLK}	SCK Period	(Note 4)	●	1			μs
t_1	SDI Setup Time before SCK Rising Edge		●	25			ns
t_2	SDI Hold Time after SCK Rising Edge		●	25			ns
t_3	SCK Low	$t_{CLK} = t_3 + t_4 \geq 1μs$	●	200			ns
t_4	SCK High	$t_{CLK} = t_3 + t_4 \geq 1μs$	●	200			ns
t_5	CSB Rising Edge to CSB Falling Edge		●	0.65			μs
t_6	SCK Rising Edge to CSB Rising Edge	(Note 4)	●	0.8			μs
t_7	CSB Falling Edge to SCK Rising Edge	(Note 4)	●	1			μs
isoSPI Timing Specifications (See Figure 25)							
t_8	SCK Falling Edge to SDO Valid	(Note 5)	●			60	ns
t_9	SCK Rising Edge to Short ±1 Transmit		●			50	ns
t_{10}	CSB Transition to Long ±1 Transmit		●			60	ns
t_{11}	CSB Rising Edge to SDO Rising	(Note 5)	●			200	ns
t_{RTN}	Data Return Delay		●	325	375	425	ns
$t_{DSY(CS)}$	Chip-Select Daisy-Chain Delay		●		120	180	ns
$t_{DSY(D)}$	Data Daisy-Chain Delay		●	200	250	300	ns
t_{LAG}	Data Daisy-Chain Lag (vs Chip-Select)	$= [t_{DSY(D)} + t_{1/2PW(D)}] – [t_{DSY(CS)} + t_{1/2PW(CS)}]$	●	0	35	70	ns
$t_{5(GOV)}$	Chip-Select High-to-Low Pulse Governor		●	0.6		0.82	μs
$t_{6(GOV)}$	Data to Chip-Select Pulse Governor		●	0.8		1.05	μs
t_{BLOCK}	isoSPI Port Reversal Blocking Window		●	2		10	μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error specification.

Note 3: The ACTIVE state current is calculated from DC measurements. The ACTIVE state current is the additional average supply current into V_{REG} when there is continuous 1MHz communications on the isoSPI ports with 50% data 1's and 50% data 0's. Slower clock rates reduce the supply current. See Applications Information section for additional details.

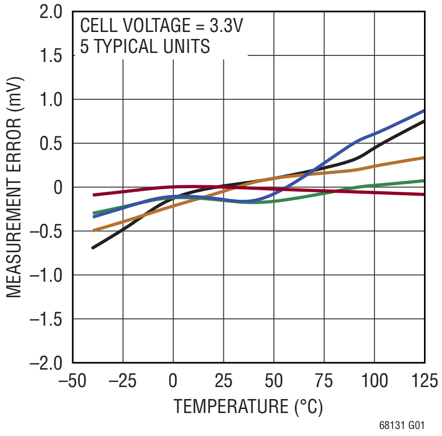
Note 4: These timing specifications are dependent on the delay through the cable, and include allowances for 50ns of delay each direction. 50ns corresponds to 10m of CAT5 cable (which has a velocity of propagation of 66% the speed of light). Use of longer cables would require derating these specs by the amount of additional delay.

Note 5: These specifications do not include rise or fall time of SDO. While fall time (typically 5ns due to the internal pull-down transistor) is not a concern, rising-edge transition time t_{RISE} is dependent on the pull-up resistance and load capacitance on the SDO pin. The time constant must be chosen such that SDO meets the setup time requirements of the MCU.

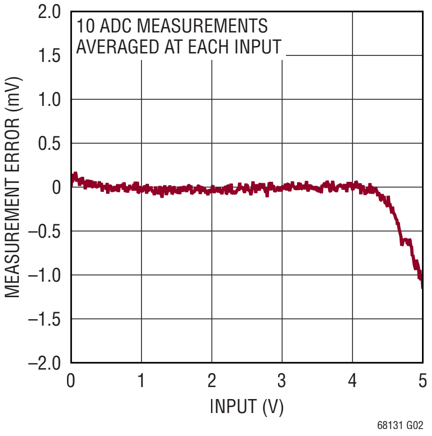
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

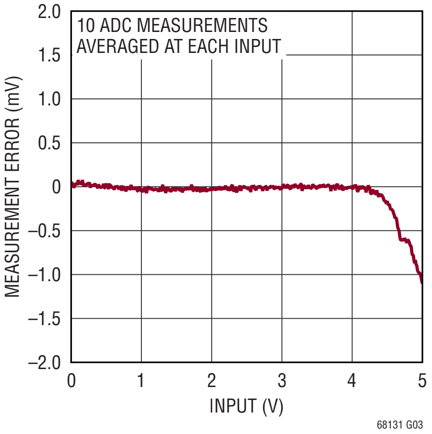
Measurement Error vs Temperature



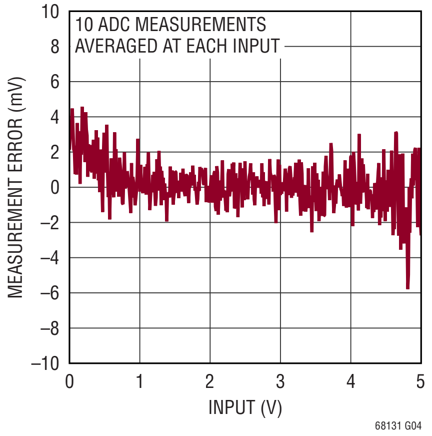
Measurement Error vs Input, Normal Mode



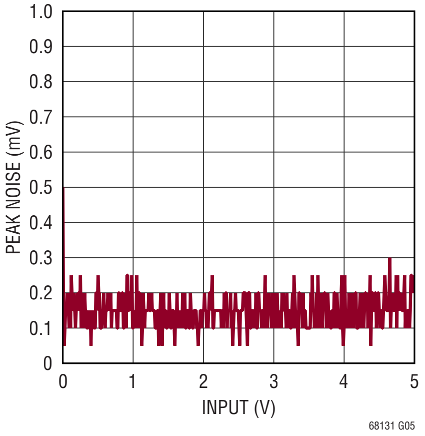
Measurement Error vs Input, Filtered Mode



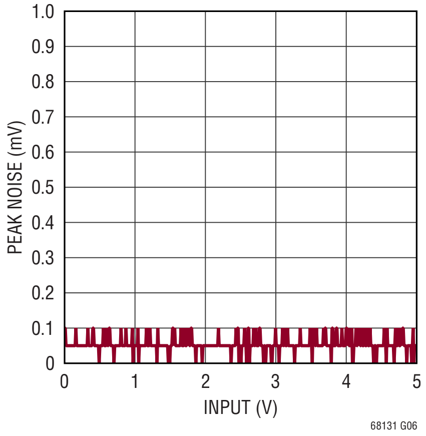
Measurement Error vs Input, Fast Mode



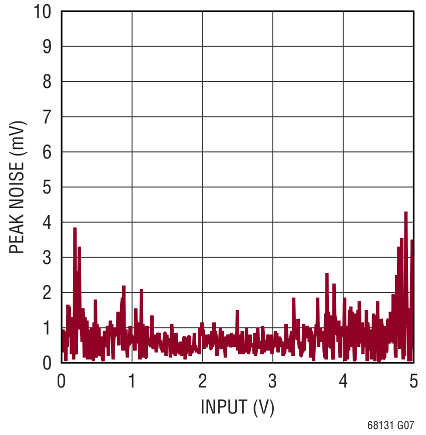
Measurement Noise vs Input, Normal Mode



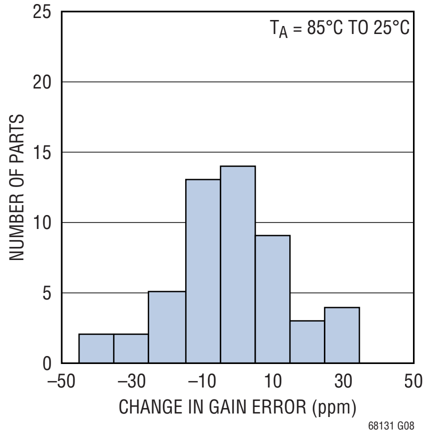
Measurement Noise vs Input, Filtered Mode



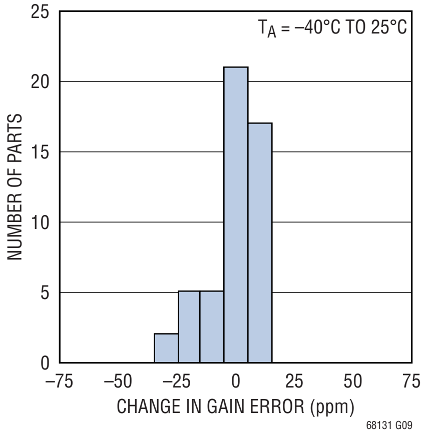
Measurement Noise vs Input, Fast Mode



Measurement Gain Error Thermal Hysteresis, Hot



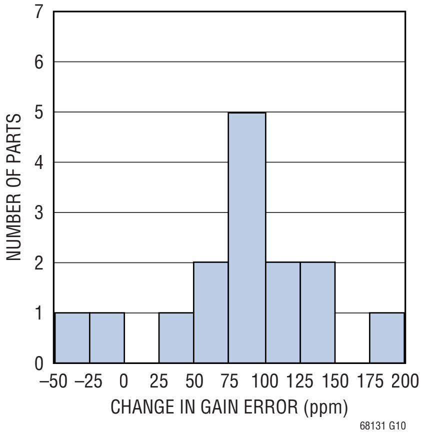
Measurement Gain Error Thermal Hysteresis, Cold



TYPICAL PERFORMANCE CHARACTERISTICS

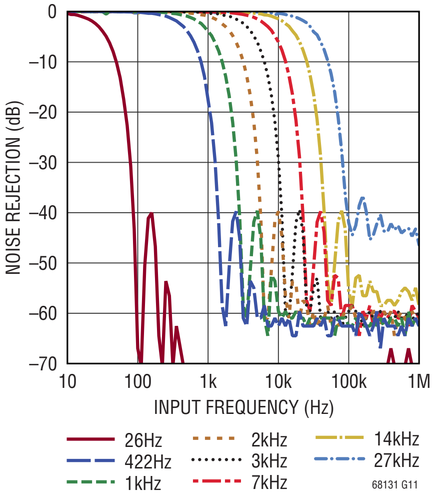
$T_A = 25°C$, unless otherwise noted.

Measurement Error Due to IR Reflow



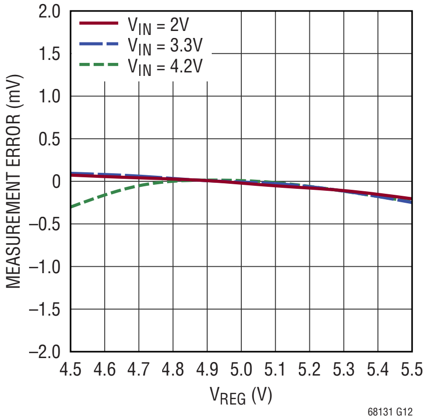
68131 G10

Noise Filter Response



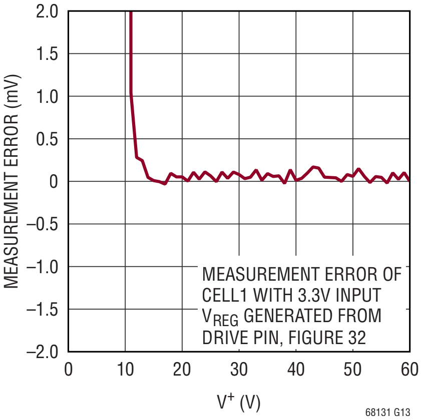
68131 G11

Measurement Error vs V_{REG}



68131 G12

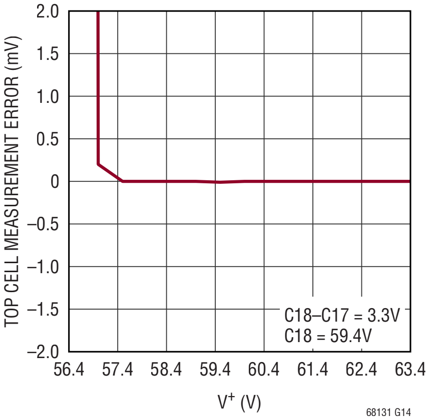
Measurement Error vs V^+



MEASUREMENT ERROR OF CELL1 WITH 3.3V INPUT V_{REG} GENERATED FROM DRIVE PIN, FIGURE 32

68131 G13

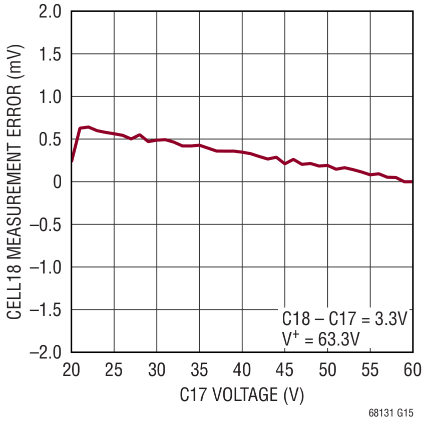
Top Cell Measurement Error vs V^+



C18–C17 = 3.3V
C18 = 59.4V

68131 G14

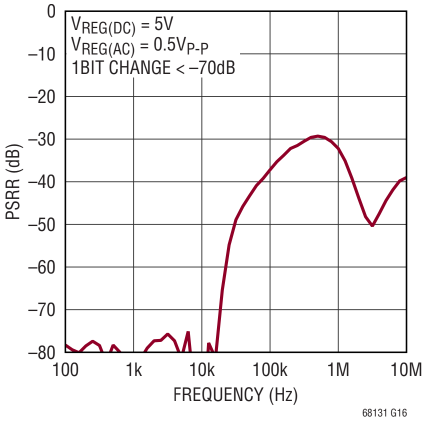
Measurement Error vs Common Mode Voltage



C18 – C17 = 3.3V
$V^+ = 63.3V$

68131 G15

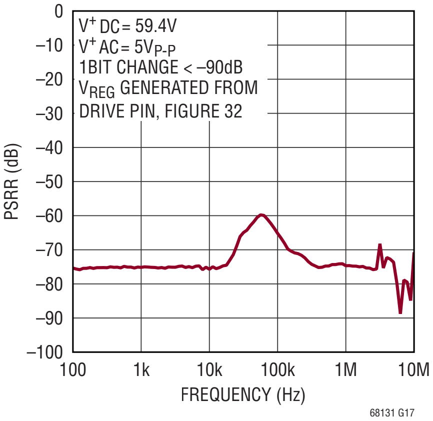
Measurement Error Due to a V_{REG} AC Disturbance



$V_{REG(DC)} = 5V$
$V_{REG(AC)} = 0.5V_{P-P}$
1BIT CHANGE < –70dB

68131 G16

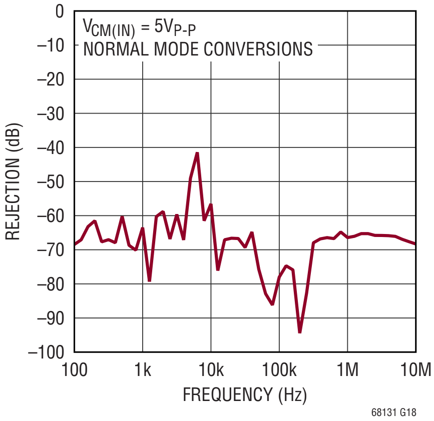
Measurement Error Due to a V^+ AC Disturbance



V^+ DC = 59.4V
V^+ AC = $5V_{P-P}$
1BIT CHANGE < –90dB
V_{REG} GENERATED FROM DRIVE PIN, FIGURE 32

68131 G17

Measurement Error CMRR vs Frequency



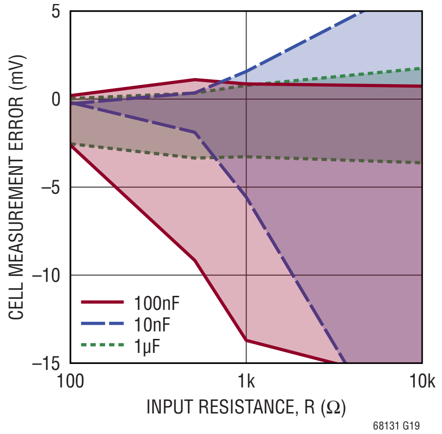
$V_{CM(IN)} = 5V_{P-P}$
NORMAL MODE CONVERSIONS

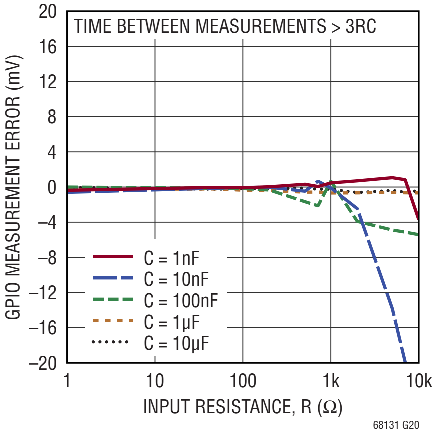
68131 G18

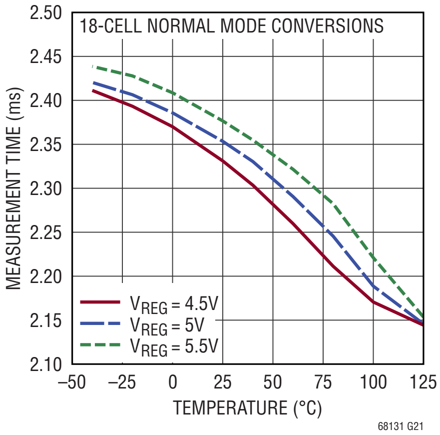
Rev. A

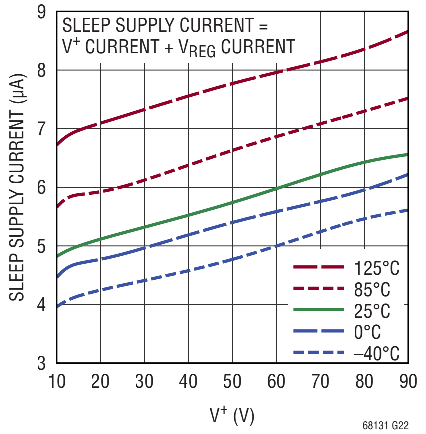
TYPICAL PERFORMANCE CHARACTERISTICS

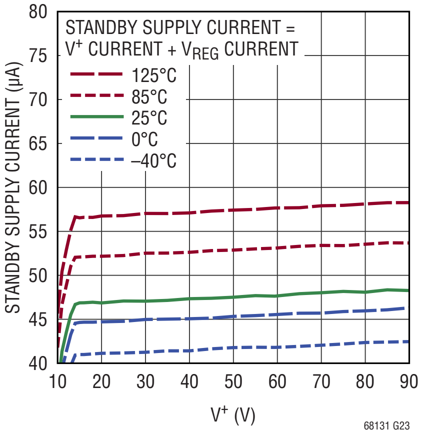
T_A = 25°C, unless otherwise noted.

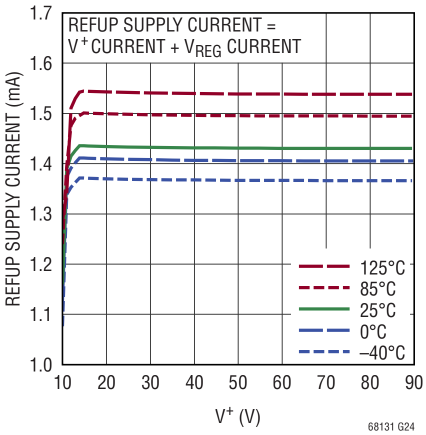

Cell Measurement Error Range vs Input RC Values

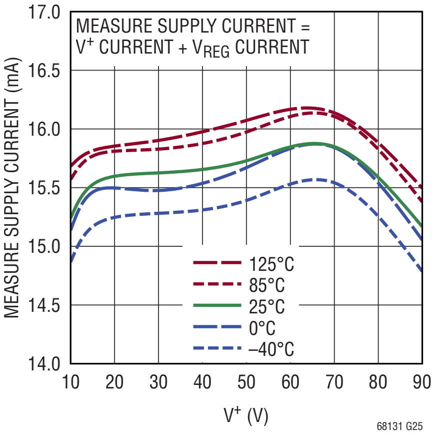

GPIO Measurement Error vs Input RC Values

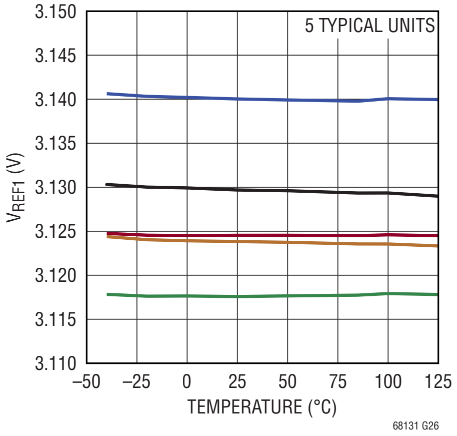

Measurement Time vs Temperature

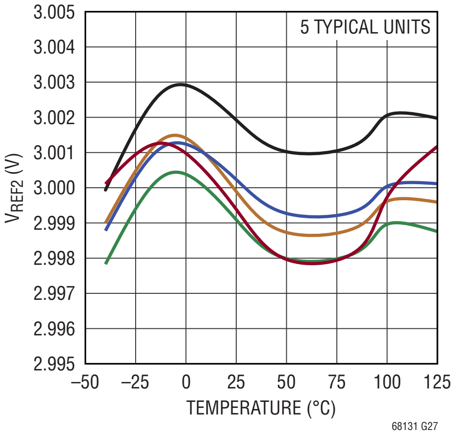

Sleep Supply Current vs V^+


Standby Supply Current vs V^+


REFUP Supply Current vs V^+


Measure Supply Current vs V^+

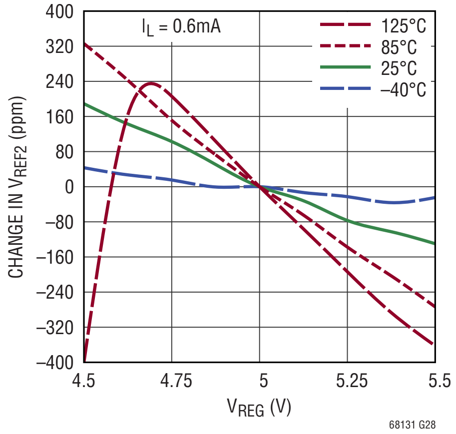

V_{REF1} vs Temperature


V_{REF2} vs Temperature

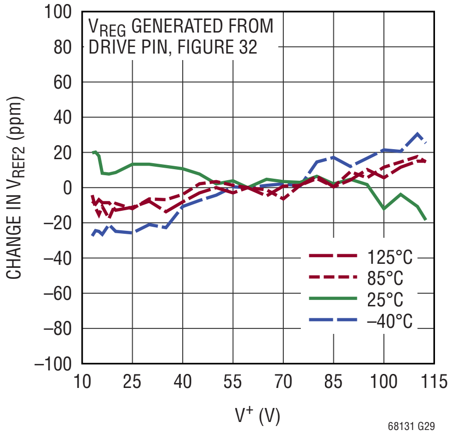
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

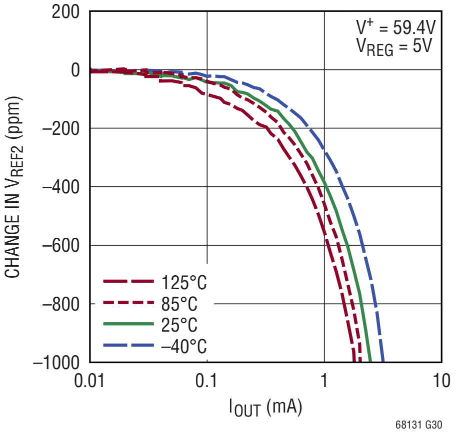
V_{REF2} V_{REG} Line Regulation



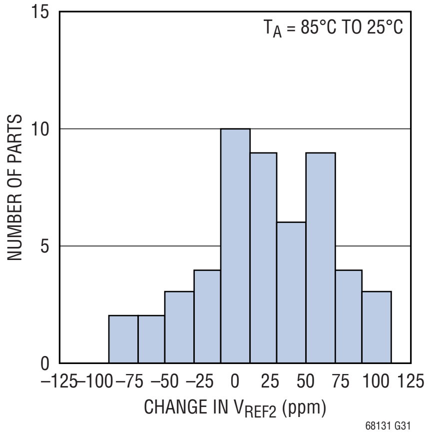
V_{REF2} V^+ Line Regulation



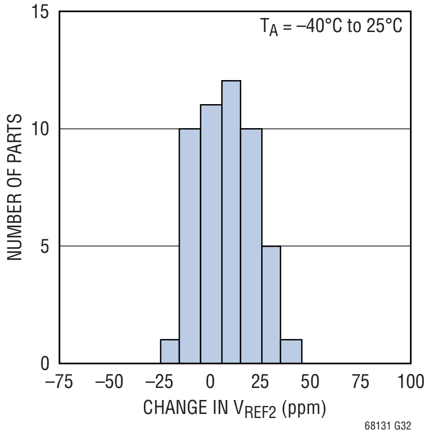
V_{REF2} Load Regulation



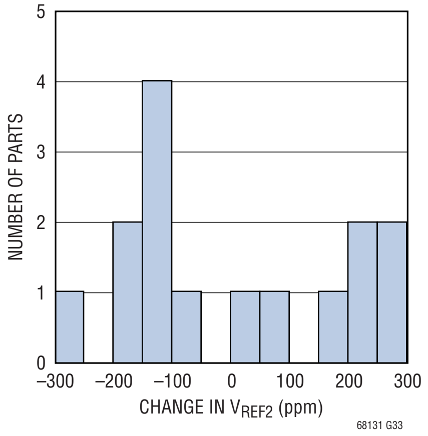
V_{REF2} Thermal Hysteresis, Hot



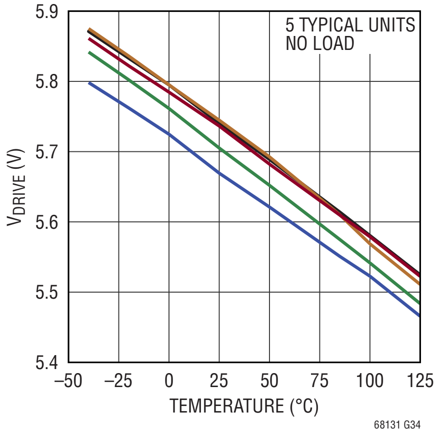
V_{REF2} Thermal Hysteresis, Cold



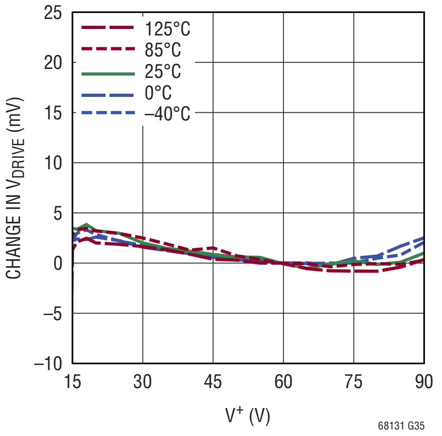
V_{REF2} Change Due to IR Reflow



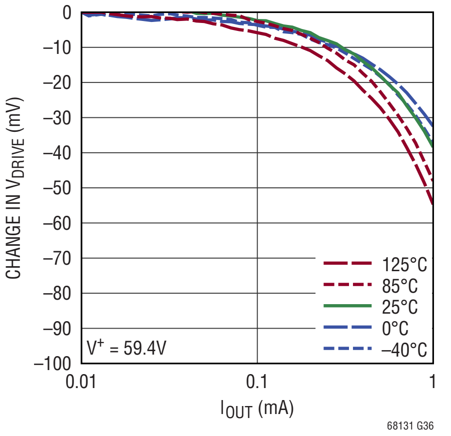
V_{DRIVE} vs Temperature



V_{DRIVE} V^+ Line Regulation



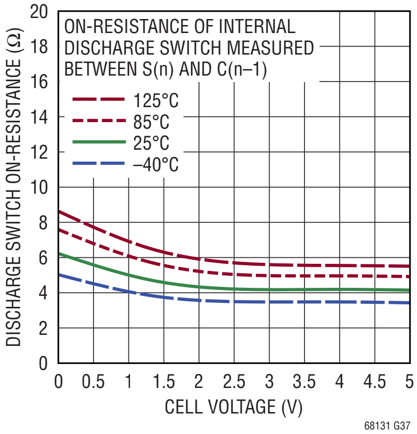
V_{DRIVE} Load Regulation



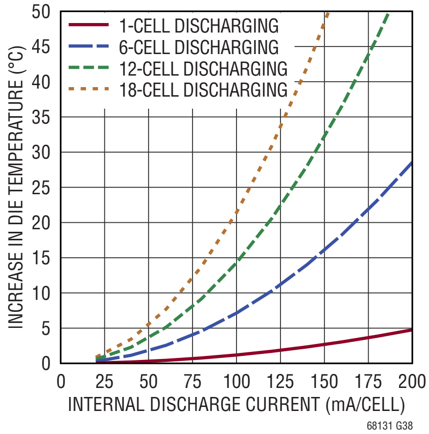
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

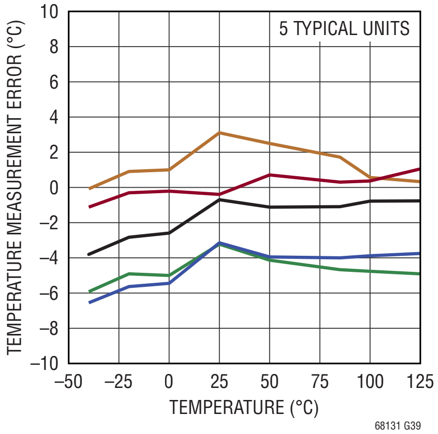
Discharge Switch On-Resistance vs Cell Voltage



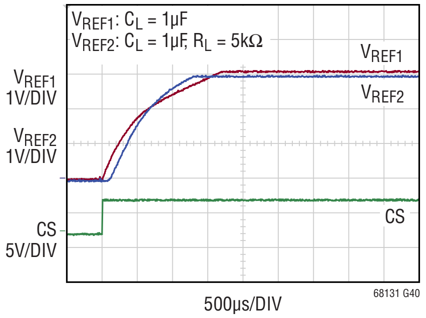
Internal Die Temperature Increase vs Discharge Current



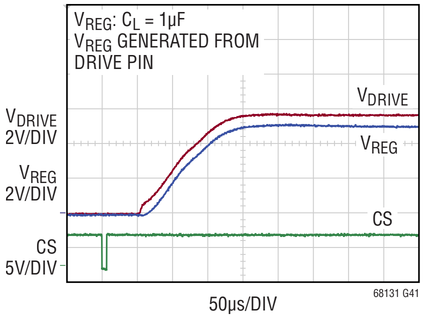
Internal Die Temperature Measurement Error vs Temperature



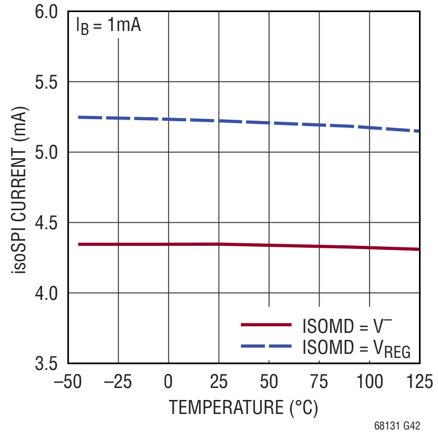
V_{REF1} and V_{REF2} Power-Up



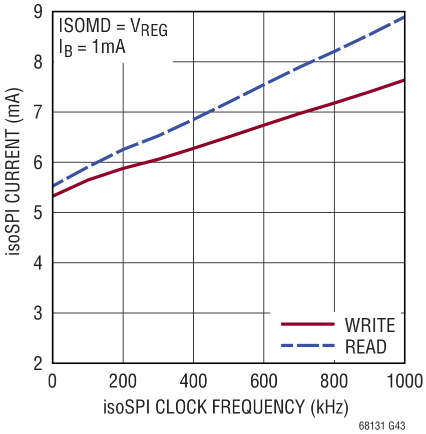
V_{REG} and V_{DRIVE} Power-Up



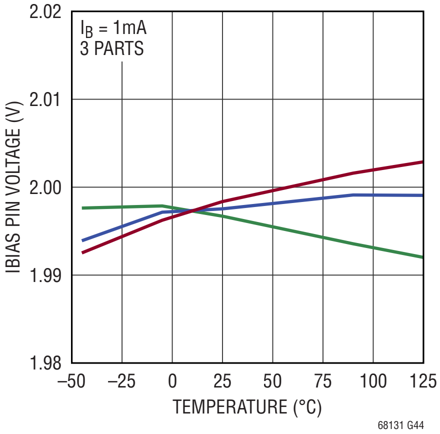
isoSPI Current (READY) vs Temperature



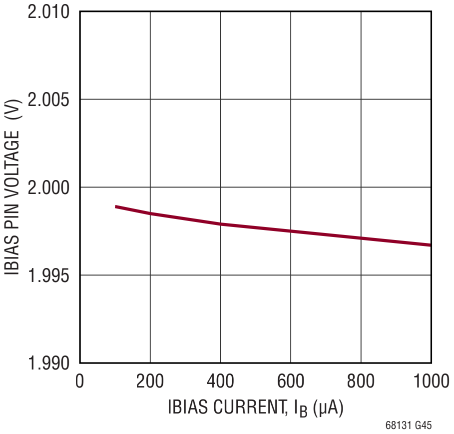
isoSPI Current (ACTIVE) vs isoSPI Clock Frequency



IBIAS Voltage vs Temperature



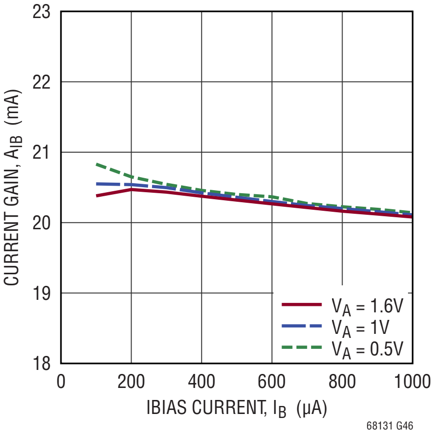
IBIAS Voltage Load Regulation



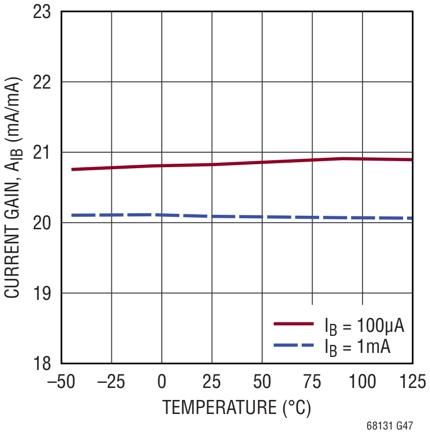
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

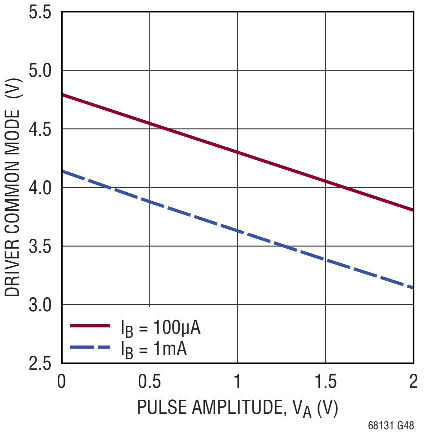
isoSPI Driver Current Gain (Port A/Port B) vs IBIAS Current



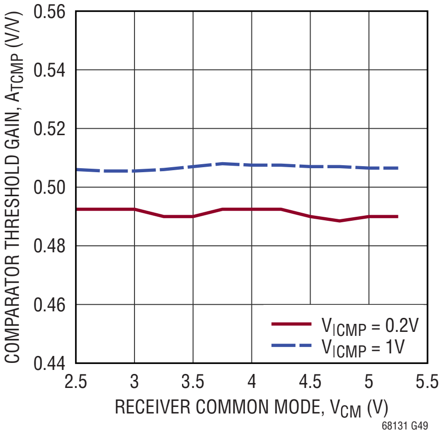
isoSPI Driver Current Gain (Port A/Port B) vs Temperature



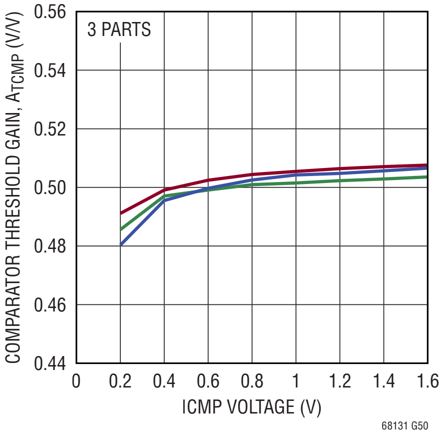
isoSPI Driver Common Mode Voltage (Port A/Port B) vs Pulse Amplitude



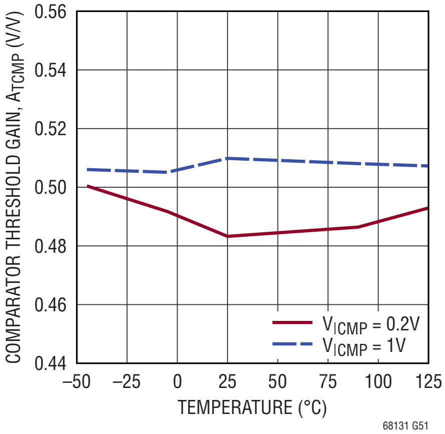
isoSPI Comparator Threshold Gain (Port A/Port B) vs Receiver Common Mode



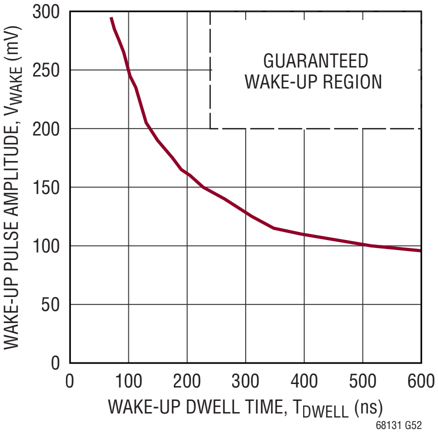
isoSPI Comparator Threshold Gain (Port A/Port B) vs ICMP Voltage



isoSPI Comparator Threshold Gain (Port A/Port B) vs Temperature



Typical Wake-Up Pulse Amplitude (Port A/Port B) vs Dwell Time



PIN FUNCTIONS

C0 to C18: Cell Inputs.

S1 to S18: Balance Inputs/Outputs. 18 internal N-MOSFETs are connected between S(n) and C(n–1) for discharging cells.

V^+: Positive Supply Pin.

$V^–$: Negative Supply Pins. The $V^–$ pins must be shorted together, external to the IC.

V_{REF2}: Buffered 2nd Reference Voltage for Driving Multiple 10k Thermistors. Bypass with an external 1µF capacitor.

V_{REF1}: ADC Reference Voltage. Bypass with an external 1µF capacitor. No DC loads allowed.

GPIO[1:9]: General Purpose I/O. Can be used as digital inputs or digital outputs, or as analog inputs with a measurement range from $V^–$ to 5V. GPIO[3:5] can be used as an I^2C or SPI port.

DTEN: Discharge Timer Enable. Connect this pin to V_{REG} to enable the Discharge Timer.

DRIVE: Connect the base of an NPN to this pin. Connect the collector to V^+ and the emitter to V_{REG}.

V_{REG}: 5V Regulator Input. Bypass with an external 1µF capacitor.

ISOMD: Serial Interface Mode. Connecting ISOMD to V_{REG} configures pins 53, 54, 61 and 62 of the LTC6813-1 for 2-wire isolated interface (isoSPI) mode. Connecting ISOMD to $V^–$ configures the LTC6813-1 for 4-wire SPI mode.

WDT: Watchdog Timer Output Pin. This is an open drain NMOS digital output. It can be left unconnected or connected with a 1M resistor to V_{REG}. If the LTC6813-1 does not receive a valid command within 2 seconds, the watchdog timer circuit will reset the LTC6813-1 and the WDT pin will go high impedance.

Serial Port Pins

	ISOMD = V_{REG}	ISOMD = $V^–$
PORT B (Pins 57, 58, 63 and 64)	IPB	IPB
	IMB	IMB
	ICMP	ICMP
	IBIAS	IBIAS
PORT A (Pins 53, 54, 61 and 62)	(NC)	SDO
	(NC)	SDI
	IPA	SCK
	IMA	CSB

CSB, SCK, SDI, SDO: 4-Wire Serial Peripheral Interface (SPI). Active low chip select (CSB), serial clock (SCK) and serial data in (SDI) are digital inputs. Serial data out (SDO) is an open drain NMOS output pin. SDO requires a 5k pull-up resistor.

IPA, IMA: Isolated 2-Wire Serial Interface Port A. IPA (plus) and IMA (minus) are a differential input/output pair.

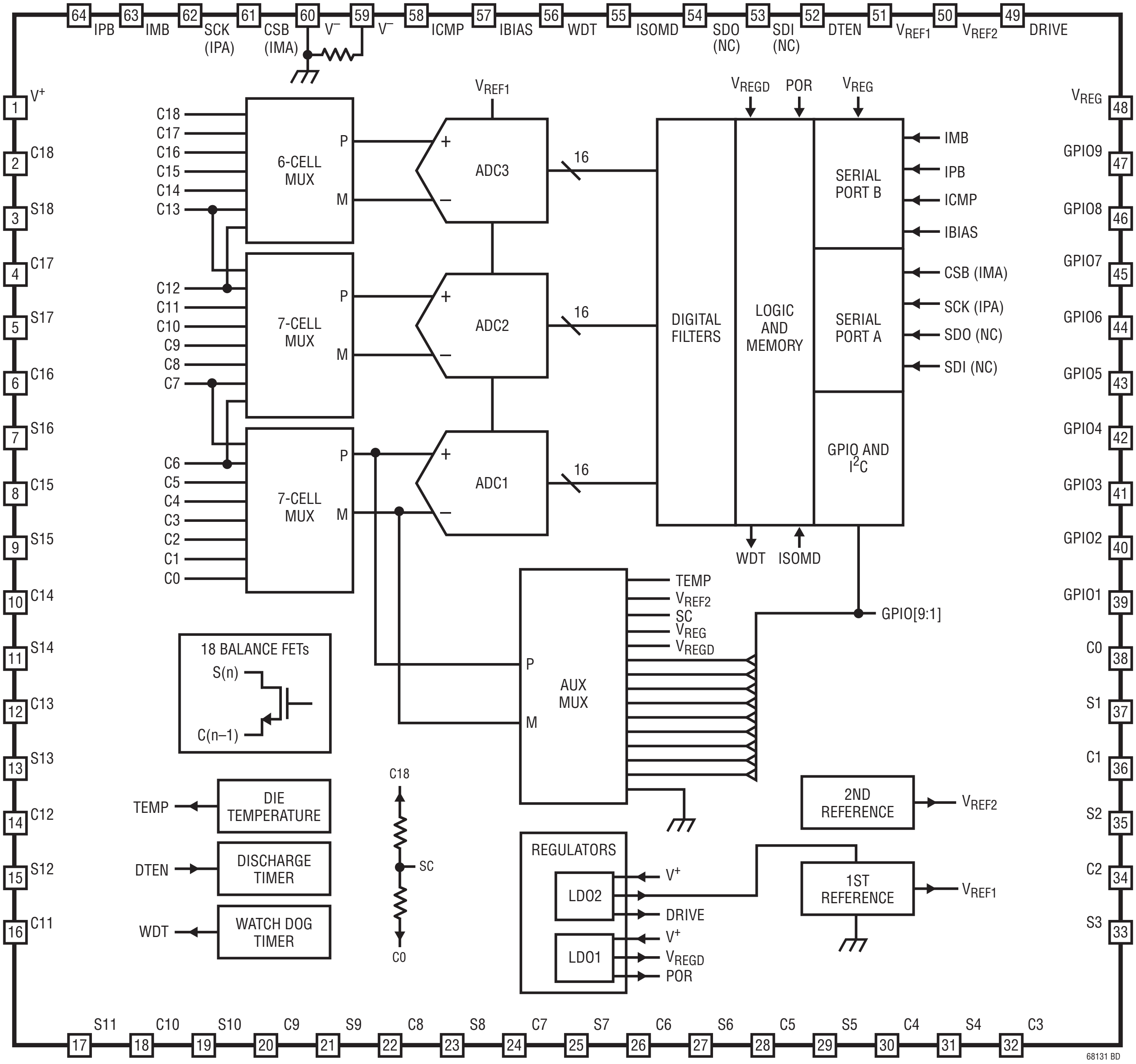
IPB, IMB: Isolated 2-Wire Serial Interface Port B. IPB (plus) and IMB (minus) are a differential input/output pair.

IBIAS: Isolated Interface Current Bias. Tie IBIAS to $V^–$ through a resistor divider to set the interface output current level. When the isoSPI interface is enabled, the IBIAS pin voltage is 2V. The IPA/IMA or IPB/IMB output current drive is set to 20 times the current, I_B, sourced from the IBIAS pin.

ICMP: Isolated Interface Comparator Voltage Threshold Set. Tie this pin to the resistor divider between IBIAS and $V^–$ to set the voltage threshold of the isoSPI receiver comparators. The comparator thresholds are set to half the voltage on the ICMP pin.

Exposed Pad: $V^–$. The Exposed Pad must be soldered to PCB.

BLOCK DIAGRAM



Rev. A

IMPROVEMENTS FROM THE LTC6811-1

The LTC6813-1 is an evolution of the LTC6811-1 design. The following table summarizes the feature changes and additions in the LTC6813-1.

ADDITIONAL LTC6813-1 FEATURES	BENEFITS	RELEVANT DATA SHEET SECTION(S)
The LTC6813-1 Has 3 ADCs Operating Simultaneously vs 2 ADCs on LTC6811-1	3 Cells Can Be Measured During Each Conversion Cycle	*ADC Operation*
In Addition to the 3 ADC Digital Filters, There Is a 4th Filter Which Is Used for Redundancy	Checks That All Digital Filters are Free of Faults	*ADC Conversion with Digital Redundancy* for a description and PS[1:0] bits in Table 10
Measure Cell 7 with ADC1 and ADC2 Simultaneously and then Measure Cell 13 with ADC2 and ADC3 Simultaneously Using the ADOL Command	Checks That ADC2 Is as Accurate as ADC1 and Also Checks That ADC3 Is as Accurate as ADC2	*Overlap Cell Measurement (ADOL Command)*
A Monitoring Feature Can Be Enabled During the Discharge Timer. The Cell Balancing Can Be Automatically Terminated When Cell Voltages Reach a Programmable Undervoltage Threshold	Improved Cell Balancing	*Discharge Timer Monitor*
The Internal Discharge MOSFETs Can Provide 200mA of Balancing Current (80mA if the die temperature is over 95°C). The Balancing Current Is Independent of Cell Voltage	Faster Cell Balancing, Especially for Low Cell Voltages	*Cell Balancing with Internal MOSFETs*
The C0 Pin Voltage Is Allowed to Range Between 0V and 1V Without Affecting Total Measurement Error (TME)	C0 Does Not Have to Connect Directly to V^-	Input Range *in Electrical Characteristics*
The MUTE and UNMUTE Commands Allow the Host to Turn Off/On the Discharge Pins (S Pins) Without Overwriting Register Values	Greater Control of Timing Between S Pins Turning Off and Cell Measurements	*S Pin Muting*
Auxiliary Measurements Have an Open-Wire Diagnostic Feature	Improved Fault Detection	*Auxiliary Open Wire Check (AXOW Command)*
Four Additional GPIO Pins Have Been Added for a Total of Nine	Increased Number of Temperature or Other Sensors That Can Be Measured	*Auxiliary (GPIO) Measurements (ADAX Command)* and *Auxiliary Open Wire Check (AXOW Command)*
A Daisy Chain of LTC6813-1s Can Operate in Both Directions (Both Ports Can Be Master or Slave)	Redundant Communication Path	*Reversible isoSPI*

OPERATION

STATE DIAGRAM

The operation of the LTC6813-1 is divided into two separate sections: the Core circuit and the isoSPI circuit. Both sections have an independent set of operating states, as well as a shutdown timeout.

CORE LTC6813-1 STATE DESCRIPTIONS

SLEEP State

The reference and ADCs are powered down. The watchdog timer (see Watchdog and Discharge Timer) has timed out. The discharge timer is either disabled or timed out. The supply currents are reduced to minimum levels. The isoSPI ports will be in the IDLE state. The DRIVE pin is 0V.

If a WAKE-UP signal is received (see Waking Up the Serial Interface), the LTC6813-1 will enter the STANDBY state.

STANDBY State

The reference and the ADCs are off. The watchdog timer and/or the discharge timer is running. The DRIVE pin powers the V_{REG} pin to 5V through an external transistor. (Alternatively, V_{REG} can be powered by an external supply).

When a valid ADC command is received or the REFON bit is set to 1 in Configuration Register Group A, the IC pauses for t_{REFUP} to allow for the reference to power up and then enters either the REFUP or MEASURE state. Otherwise, if no valid commands are received for t_{SLEEP} (when both the watchdog and discharge timer have expired), the LTC6813-1 returns to the SLEEP state. If the discharge timer is disabled, only the watchdog timer is relevant.

REFUP State

To reach this state, the REFON bit in Configuration Register Group A must be set to 1 (using the WRCFGA command, see Table 36). The ADCs are off. The reference is powered up so that the LTC6813-1 can initiate ADC conversions more quickly than from the STANDBY state.

When a valid ADC command is received, the IC goes to the MEASURE state to begin the conversion. Otherwise, the LTC6813-1 will return to the STANDBY state when the REFON bit is set to 0, either manually (using WRCFGA command) or automatically when the watchdog timer expires (the LTC6813-1 will then move straight into the SLEEP state if both timers are expired).

MEASURE State

The LTC6813-1 performs ADC conversions in this state. The reference and ADCs are powered up.

After ADC conversions are complete, the LTC6813-1 will transition to either the REFUP or STANDBY state, depending on the REFON bit. Additional ADC conversions can be

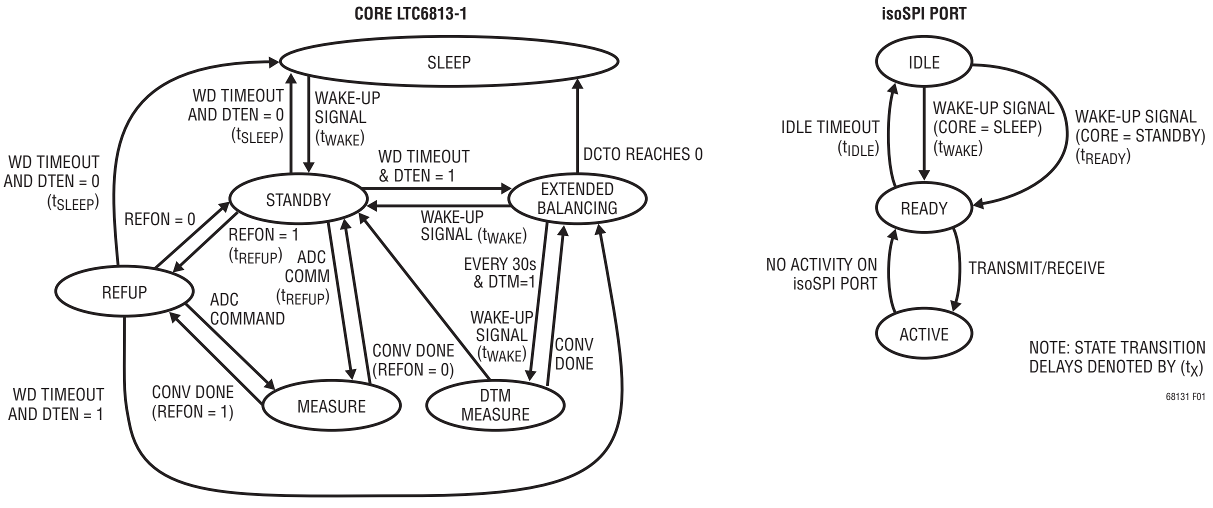


Figure 1. LTC6813-1 Operation State Diagram

initiated more quickly by setting REFON = 1 to take advantage of the REFUP state.

Note: Non-ADC commands do not cause a Core state transition. Only an ADC Conversion or diagnostic commands will place the Core in the MEASURE state.

isoSPI STATE DESCRIPTIONS

Note: The LTC6813-1 has two isoSPI ports (A and B), for daisy-chain communication.

IDLE State

The isoSPI ports are powered down.

When isoSPI Port A or Port B receives a WAKE-UP signal (see Waking Up the Serial Interface), the isoSPI enters the READY state. This transition happens quickly (within t_{READY}) if the Core is in the STANDBY state. If the Core is in the SLEEP state when the isoSPI receives a WAKE-UP signal, then it transitions to the READY state within t_{WAKE}.

READY State

The isoSPI port(s) are ready for communication. The serial interface current in this state depends on the status of the ISOMD pin and $R_{BIAS} = R_{B1} + R_{B2}$ (the external resistors tied to the IBIAS pin).

If there is no activity (i.e., no WAKE-UP signal) on Port A or Port B for greater than t_{IDLE}, the LTC6813-1 goes to the IDLE state. When the serial interface is transmitting or receiving data, the LTC6813-1 goes to the ACTIVE state.

ACTIVE State

The LTC6813-1 is transmitting/receiving data using one or both of the isoSPI ports. The serial interface consumes maximum power in this state. The supply current increases with clock frequency as the density of isoSPI pulses increases.

POWER CONSUMPTION

The LTC6813-1 is powered via two pins: V^+ and V_{REG}. The V^+ input requires voltage greater than or equal to the top cell voltage minus 0.3V, and it provides power to the high voltage elements of the Core circuits. The V_{REG} input requires 5V and provides power to the remaining Core circuits and the isoSPI circuitry. The V_{REG} input can be powered through an external transistor, driven by the regulated DRIVE output pin. Alternatively, V_{REG} can be powered by an external supply.

The power consumption varies according to the operational states. Table 1 and Table 2 provide equations to approximate the supply pin currents in each state. The V^+ pin current depends only on the Core state. However, the V_{REG} pin current depends on both the Core state and isoSPI state, and can, therefore, be divided into two components. The isoSPI interface draws current only from the V_{REG} pin.

$$I_{REG} = I_{REG(CORE)} + I_{REG(isoSPI)}$$

In the SLEEP state, the V_{REG} pin will draw approximately 3.1µA if powered by an external supply. Otherwise, the V^+ pin will supply the necessary current.

Table 1. Core Supply Current

STATE		I_{VP}	$I_{REG(CORE)}$
SLEEP	V_{REG} = 0V	6.1µA	0µA
	V_{REG} = 5V	3µA	3.1µA
STANDBY		14µA	35µA
REFUP		550µA	900µA
MEASURE		950µA	15mA

Table 2. isoSPI Supply Current Equations

isoSPI STATE	ISOMD CONNECTION	$I_{REG(isoSPI)}$
IDLE	N/A	0mA
READY	V_{REG}	$2.2mA + 3 \bullet I_B$
	V^-	$1.5mA + 3 \bullet I_B$
ACTIVE	V_{REG}	Write: $2.5mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$ Read: $2.5mA + \left(3 + 20 \bullet \frac{100ns \bullet 1.5}{t_{CLK}}\right) \bullet I_B$
	V^-	$1.8mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$

OPERATION

ADC OPERATION

There are three ADCs inside the LTC6813-1. The three ADCs operate simultaneously when measuring eighteen cells. Only one ADC is used to measure the general purpose inputs. The following discussion uses the term ADC to refer to one or all ADCs, depending on the operation being performed. The following discussion will refer to ADC1, ADC2 and ADC3 when it is necessary to distinguish between the three circuits, in timing diagrams, for example.

ADC Modes

The ADCOPT bit (CFGAR0[0]) in Configuration Register Group A and the mode selection bits MD[1:0] in the conversion command together provide eight modes of operation for the ADC which correspond to different oversampling ratios (OSR). The accuracy and timing of these modes are summarized in Table 3. In each mode, the ADC first measures the inputs, and then performs a calibration of each channel. The names of the modes are based on the –3dB bandwidth of the ADC measurement.

Mode 7kHz (Normal): In this mode, the ADC has high resolution and low TME (Total Measurement Error). This is considered the normal operating mode because of the optimum combination of speed and accuracy.

Mode 27kHz (Fast): In this mode, the ADC has maximum throughput but has some increase in TME (Total Measurement Error). So this mode is also referred to as the fast mode. The increase in speed comes from a reduction in the oversampling ratio. This results in an increase in noise and average measurement error.

Mode 26Hz (Filtered): In this mode, the ADC digital filter –3dB frequency is lowered to 26Hz by increasing the OSR. This mode is also referred to as the filtered mode due to its low –3dB frequency. The accuracy is similar to the 7kHz (Normal) mode with lower noise.

Modes 14kHz, 3kHz, 2kHz, 1kHz and 422Hz: Modes 14kHz, 3kHz, 2kHz, 1kHz and 422Hz provide additional options to set the ADC digital filter –3dB at 13.5kHz, 3.4kHz, 1.7kHz, 845Hz and 422Hz, respectively. The accuracy of the 14kHz mode is similar to the 27kHz (Fast) mode. The accuracy of 3kHz, 2kHz, 1kHz and 422Hz modes is similar to the 7kHz (Normal) mode.

The filter bandwidths and the conversion times for these modes are provided in Table 3 and Table 5. If the Core is in STANDBY state, an additional t_{REFUP} time is required to power up the reference before beginning the ADC conversions. The reference can remain powered up between ADC conversions if the REFON bit in Configuration Register Group A is set to 1 so the Core is in REFUP state after a delay t_{REFUP}. Then, the subsequent ADC commands will not have the t_{REFUP} delay before beginning ADC conversions.

Table 3. ADC Filter Bandwidth and Accuracy

MODE	–3dB FILTER BW	–40dB FILTER BW	TME SPEC AT 3.3V, 25°C	TME SPEC AT 3.3V, –40°C, 125°C
27kHz (Fast Mode)	27kHz	84kHz	±6mV	±6mV
14kHz	13.5kHz	42kHz	±6mV	±6mV
7kHz (Normal Mode)	6.8kHz	21kHz	±2.2mV	±3.3mV
3kHz	3.4kHz	10.5kHz	±2.2mV	±3.3mV
2kHz	1.7kHz	5.3kHz	±2.2mV	±3.3mV
1kHz	845Hz	2.6kHz	±2.2mV	±3.3mV
422Hz	422Hz	1.3kHz	±2.2mV	±3.3mV
26Hz (Filtered Mode)	26Hz	82Hz	±2.2mV	±3.3mV

Note: TME is the Total Measurement Error.

ADC Range and Resolution

The C inputs and GPIO inputs have the same range and resolution. The ADC inside the LTC6813-1 has an approximate range from –0.82V to +5.73V. Negative readings are rounded to 0V. The format of the data is a 16-bit unsigned integer where the LSB represents 100µV. Therefore, a reading of 0x80E8 (33,000 decimal) indicates a measurement of 3.3V.

Delta-Sigma ADCs have quantization noise which depends on the input voltage, especially at low oversampling ratios (OSR), such as in FAST mode. In some of the ADC modes, the quantization noise increases as the input voltage approaches the upper and lower limits of the ADC range. For example, the total measurement noise versus input voltage in normal and filtered modes is shown in Figure 2.

OPERATION

The specified range of the ADC is 0V to 5V. In Table 4, the precision range of the ADC is arbitrarily defined as 0.5V to 4.5V. This is the range where the quantization noise is relatively constant even in the lower OSR modes (see Figure 2). Table 4 summarizes the total noise in this range for all eight ADC operating modes. Also shown is the noise free resolution. For example, 14-bit noise free resolution in normal mode implies that the top 14 bits will be noise free with a DC input, but that the 15th and 16th Least Significant Bits (LSB) will flicker.

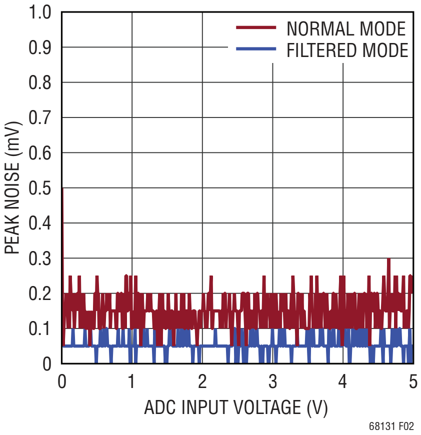


Figure 2. Measurement Noise vs Input Voltage

ADC Range vs Voltage Reference Value

Typical ADCs have a range which is exactly twice the value of the voltage reference, and the ADC measurement error is directly proportional to the error in the voltage reference. The LTC6813-1 ADC is not typical. The absolute value of V_{REF1} is trimmed up or down to compensate for gain errors in the ADC. Therefore, the ADC Total Measurement Error (TME) specifications are superior to the V_{REF1} specifications. For example, the 25°C specification of the Total Measurement Error when measuring 3.300V in 7kHz (Normal) mode is ±2.2mV and the 25°C specification for V_{REF1} is 3.150V ± 150mV.

Measuring Cell Voltages (ADCV Command)

The ADCV command initiates the measurement of the battery cell inputs, pins C0 through C18. This command has options to select the number of channels to measure and the ADC mode. See the section on Commands for the ADCV command format.

Figure 3 illustrates the timing of the ADCV command which measures all eighteen cells. After the receipt of the ADCV command to measure all 18 cells, ADC1 sequentially measures the bottom 6 cells. ADC2 measures the middle 6 cells and ADC3 measures the top 6 cells. After the cell measurements are complete, each channel is calibrated to remove any offset errors.

Table 5 shows the conversion times for the ADCV command measuring all 18 cells. The total conversion time is given by t_{6C} which indicates the end of the calibration step.

Figure 4 illustrates the timing of the ADCV command that measures only three cells.

Table 4. ADC Range and Resolution

MODE	FULL RANGE[1]	SPECIFIED RANGE	PRECISION RANGE[2]	LSB	FORMAT	MAX NOISE	NOISE FREE RESOLUTION[3]
27kHz (Fast)	–0.8192V to 5.7344V	0V to 5V	0.5V to 4.5V	100µV	Unsigned 16 Bits	±4mV_{P-P}	10 Bits
14kHz						±1mV_{P-P}	12 Bits
7kHz (Normal)						±250µV_{P-P}	14 Bits
3kHz						±150µV_{P-P}	14 Bits
2kHz						±100µV_{P-P}	15 Bits
1kHz						±100µV_{P-P}	15 Bits
422Hz						±100µV_{P-P}	15 Bits
26Hz (Filtered)						±50µV_{P-P}	16 Bits

1. Negative readings are rounded to 0V.
2. PRECISION RANGE is the range over which the noise is less than MAX NOISE.
3. NOISE FREE RESOLUTION is a measure of the noise level within the PRECISION RANGE.

OPERATION

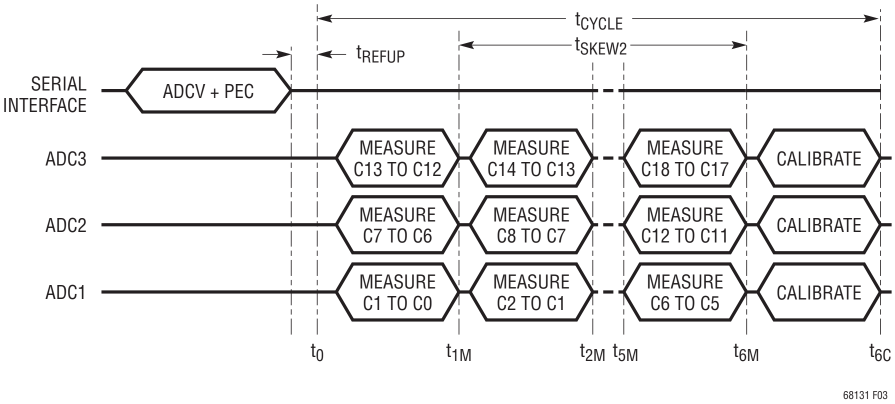


Figure 3. Timing for ADCV Command Measuring All 18 Cells

Table 5. Conversion and Synchronization Times for ADCV Command Measuring All 18 Cells in Different Modes

	CONVERSION TIMES (IN µs)						SYNCHRONIZATION TIME (IN µs)
MODE	t_0	t_{1M}	t_{2M}	t_{5M}	t_{6M}	t_{6C}	t_{SKEW2}
27kHz	0	58	104	244	291	1,121	233
14kHz	0	87	163	390	466	1,296	379
7kHz	0	145	279	681	815	2,343	670
3kHz	0	261	512	1,263	1,513	3,041	1,252
2kHz	0	494	977	2,426	2,909	4,437	2,415
1kHz	0	960	1,908	4,753	5,702	7,230	4,742
422Hz	0	1,890	3,770	9,408	11,287	12,816	9,397
26Hz	0	29,818	59,624	149,044	178,851	201,325	149,033

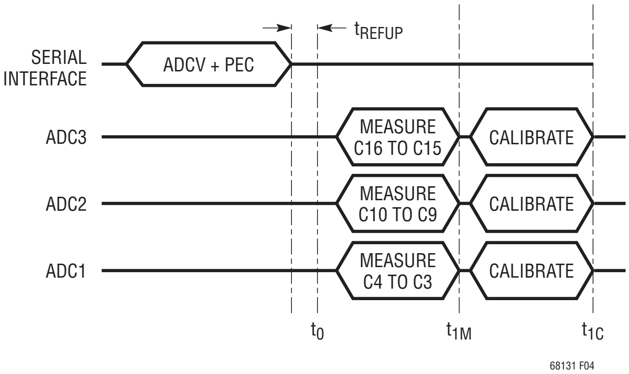


Figure 4. Timing for ADCV Command Measuring 3 Cells

OPERATION

Table 6 shows the conversion time for the ADCV command measuring only 3 cells. t_{1C} indicates the total conversion time for this command.

Table 6. Conversion Times for ADCV Command Measuring 3 Cells in Different Modes

MODE	CONVERSION TIMES (IN µs)		
	t_0	t_{1M}	t_{1C}
27kHz	0	58	203
14kHz	0	87	232
7kHz	0	145	407
3kHz	0	261	523
2kHz	0	494	756
1kHz	0	960	1,221
422Hz	0	1,890	2,152
26Hz	0	29,818	33,570

Under/Over Voltage Monitoring

Whenever the C inputs are measured, the results are compared to undervoltage and overvoltage thresholds stored in memory. If the reading of a cell is above the overvoltage limit, a bit in memory is set as a flag. Similarly, measurement results below the undervoltage limit cause a flag to be set. The overvoltage and undervoltage thresholds are stored in Configuration Register Group A. The flags are stored in Status Register Group B and Auxiliary Register Group D.

Auxiliary (GPIO) Measurements (ADAX Command)

The ADAX command initiates the measurement of the GPIO inputs. This command has options to select which GPIO input to measure (GPIO1–9) and which ADC mode to use. The ADAX command also measures the 2nd reference. There are options in the ADAX command to measure subsets of the GPIOs and the 2nd reference separately or to measure all nine GPIOs and the 2nd reference in a single command. See the section on Commands for the ADAX command format. All auxiliary measurements are relative to the V^- pin voltage. This command can be used to read external temperatures by connecting temperature sensors to the GPIOs. These sensors can be powered from the 2nd reference which is also measured by the ADAX command, resulting in precise ratiometric measurements.

Figure 5 illustrates the timing of the ADAX command measuring all GPIOs and the 2nd reference. All 10 measurements are carried out on ADC1 alone. The 2nd reference is measured after GPIO5 and before GPIO6.

Table 7 shows the conversion time for the ADAX command measuring all of the GPIOs and the 2nd reference. t_{10C} indicates the total conversion time.

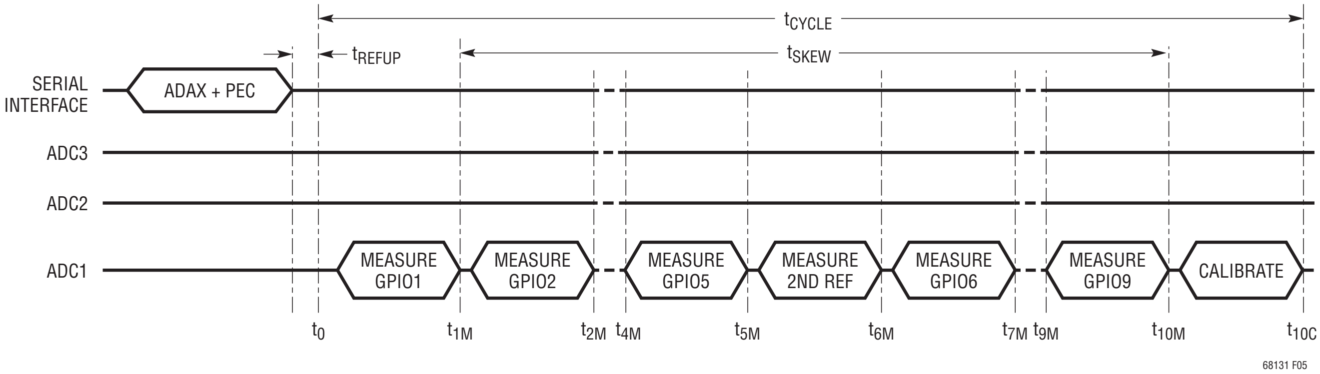


Figure 5. Timing for ADAX Command Measuring All GPIOs and 2nd Reference

OPERATION

Table 7. Conversion and Synchronization Times for ADAX Command Measuring All GPIOs and 2nd Reference in Different Modes

MODE	CONVERSION TIMES (IN µs)						SYNCHRONIZATION TIME (IN µs)
	t_0	t_{1M}	t_{2M}	t_{9M}	t_{10M}	t_{10C}	t_{SKEW}
27kHz	0	58	104	431	478	1,825	420
14kHz	0	87	163	693	769	2,116	682
7kHz	0	145	279	1,217	1,350	3,862	1,205
3kHz	0	261	512	2,264	2,514	5,025	2,253
2kHz	0	494	977	4,358	4,841	7,353	4,347
1kHz	0	960	1,908	8,547	9,496	12,007	8,536
422Hz	0	1,890	3,770	16,926	18,805	21,316	16,915
26Hz	0	29,818	59,624	268,271	298,078	335,498	268,260

Auxiliary (GPIO) Measurements with Digital Redundancy (ADAXD Command)

The ADAXD command operates similarly to the ADAX command except that an additional diagnostic is performed using digital redundancy. PS[1:0] in Configuration Register Group B must be set to 0 or 1 during ADAXD to enable redundancy. See the ADC Conversion with Digital Redundancy section.

The execution time of ADAX and ADAXD is the same.

Measuring Cell Voltages and GPIOs (ADCVAX Command)

The ADCVAX command combines eighteen cell measurements with two GPIO measurements (GPIO1 and GPIO2). This command simplifies the synchronization of battery cell voltage and current measurements when current sensors are connected to GPIO1 or GPIO2 inputs. Figure 6 illustrates the timing of the ADCVAX command. See the section on Commands for the ADCVAX command format. The synchronization of the current and voltage measurements, t_{SKEW1}, in Fast mode is within 194µs.

Table 8 shows the conversion and synchronization time for the ADCVAX command in different modes. The total conversion time for the command is given by t_{8C}.

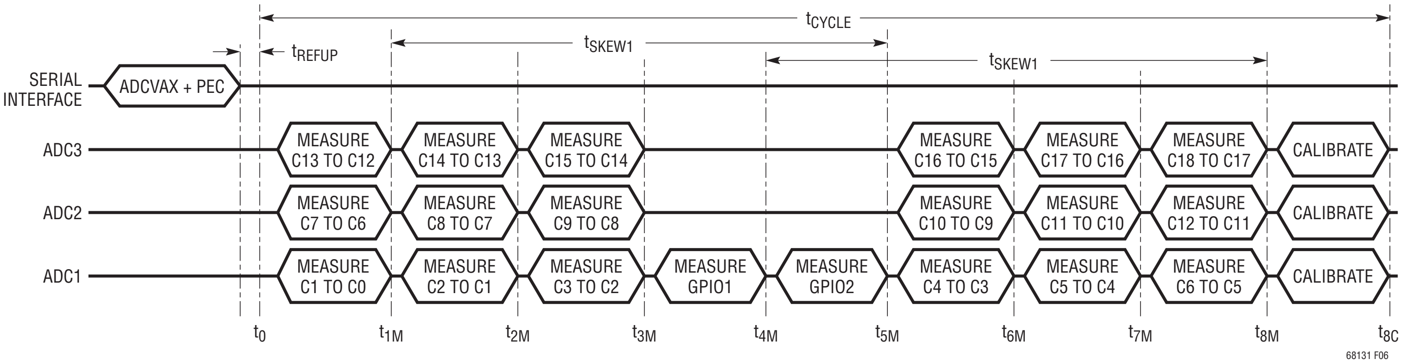


Figure 6. Timing of ADCVAX Command

Table 8. Conversion and Synchronization Times for ADCVAX Command in Different Modes

MODE	CONVERSION TIMES (IN µs)									SYNCHRONIZATION TIME (IN µs)
	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{5M}	t_{6M}	t_{7M}	t_{8M}	t_{8C}	t_{SKEW1}
27kHz	0	58	104	151	205	252	306	352	399	1,511	194
14kHz	0	87	163	238	321	397	480	556	632	1,744	310
7kHz	0	145	279	413	554	688	829	963	1,097	3,140	543
3kHz	0	261	512	762	1,020	1,270	1,527	1,778	2,028	4,071	1,008
2kHz	0	494	977	1,460	1,950	2,433	2,924	3,407	3,890	5,933	1,939
1kHz	0	960	1,908	2,857	3,812	4,761	5,717	6,665	7,613	9,657	3,801
422Hz	0	1,890	3,770	5,649	7,536	9,415	11,302	13,181	15,061	17,104	7,525
26Hz	0	29,818	59,624	89,431	119,245	149,052	178,866	208,672	238,479	268,450	119,234

DATA ACQUISITION SYSTEM DIAGNOSTICS

The battery monitoring data acquisition system is comprised of the multiplexers, ADCs, 1st reference, digital filters and memory. To ensure long term reliable performance there are several diagnostic commands which can be used to verify the proper operation of these circuits.

Measuring Internal Device Parameters (ADSTAT Command)

The ADSTAT command is a diagnostic command that measures the following internal device parameters: Sum of all Cells (SC), Internal Die Temperature (ITMP), Analog Power Supply (VA) and the Digital Power Supply (VD). These parameters are described in the section below. All the 8 ADC modes described earlier are available for these conversions. See the section on Commands for the ADSTAT command format. Figure 7 illustrates the timing of the ADSTAT command measuring all 4 internal device parameters.

Table 9 shows the conversion time of the ADSTAT command measuring all 4 internal parameters. t_{4C} indicates the total conversion time for the ADSTAT command.

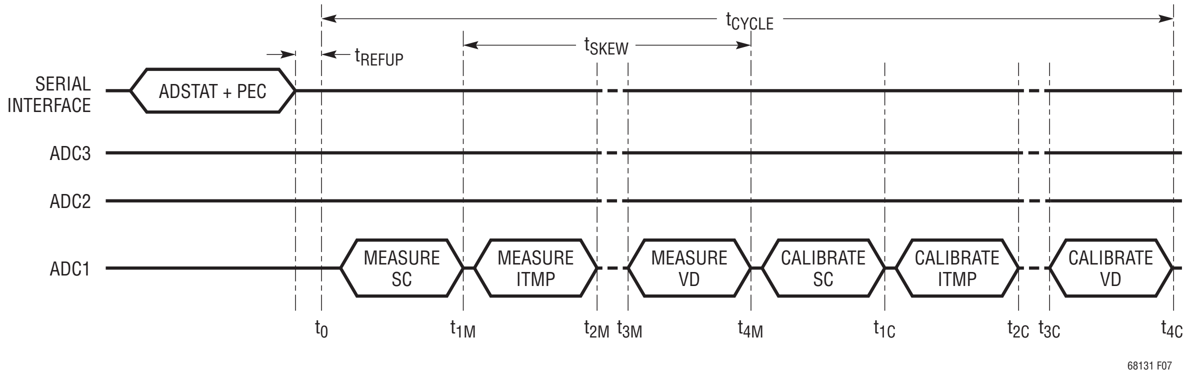


Figure 7. Timing for ADSTAT Command Measuring SC, ITMP, VA, VD

OPERATION

Table 9. Conversion and Synchronization Times for ADSTAT Command Measuring SC, ITMP, VA, VD in Different Modes

MODE	CONVERSION TIMES (IN µs)						SYNCHRONIZATION TIME (IN µs)
	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{4C}	t_{SKEW}
27kHz	0	58	104	151	198	742	140
14kHz	0	87	163	238	314	858	227
7kHz	0	145	279	413	547	1,556	402
3kHz	0	261	512	762	1,012	2,022	751
2kHz	0	494	977	1,460	1,943	2,953	1,449
1kHz	0	960	1,908	2,857	3,805	4,814	2,845
422Hz	0	1,890	3,770	5,649	7,529	8,538	5,638
26Hz	0	29,818	59,624	89,431	119,238	134,211	89,420

Sum of Cells Measurement: The Sum of All Cells measurement is the voltage between C18 and C0 with a 30:1 attenuation. The 16-bit ADC value of Sum of Cells measurement (SC) is stored in Status Register Group A. Any potential difference between the C0 and V^- pins results in an error in the SC measurement equal to this difference. From the SC value, the sum of all cell voltage measurements is given by:

$$\text{Sum of All Cells} = \text{SC} \cdot 30 \cdot 100\mu V$$

Internal Die Temperature: The ADSTAT command can measure the internal die temperature. The 16-bit ADC value of the die temperature measurement (ITMP) is stored in Status Register Group A. From ITMP, the actual die temperature is calculated using the expression:

$$\text{Internal Die Temperature (°C)} = \text{ITMP} \cdot \left(\frac{100\mu V}{7.6mV}\right)°C - 276°C$$

Power Supply Measurements: The ADSTAT command is also used to measure the Analog Power Supply (V_{REG}) and Digital Power Supply (V_{REGD}). The 16-bit ADC value of the analog power supply measurement (VA) is stored in Status Register Group A. The 16-bit ADC value of the digital power supply measurement (VD) is stored in Status Register Group B. From VA and VD, the power supply measurements are given by:

$$\text{Analog Power Supply Measurement } (V_{REG}) = V_A \cdot 100\mu V$$

$$\text{Digital Power Supply Measurement } (V_{REGD}) = V_D \cdot 100\mu V$$

The value of V_{REG} is determined by external components. V_{REG} should be between 4.5V and 5.5V to maintain accuracy. The value of V_{REGD} is determined by internal components. The normal range of V_{REGD} is 2.7V to 3.6V.

Measuring Internal Device Parameters with Digital Redundancy (ADSTATD Command)

The ADSTATD command operates similarly to the ADSTAT command except that an additional diagnostic is performed using digital redundancy. PS[1:0] in Configuration Register Group B must be set to 0 or 1 during ADSTATD to enable redundancy. See the ADC Conversion with Digital Redundancy section.

The execution time of ADSTAT and ADSTATD is the same.

ADC Conversion with Digital Redundancy

Each of the three internal ADCs contains its own digital integration and differentiation machine. The LTC6813-1 also contains a fourth digital integration and differentiation machine that is used for redundancy and error checking.

All of the ADC and self test commands, except ADAX and ADSTAT, can operate with digital redundancy. This includes ADCV, ADOW, CVST, ADOL, ADAXD, AXOW, AXST, ADSTATD, STATST, ADCVAX and ADCVSC. When performing an ADC conversion with redundancy, the analog modulator sends its bit stream to both the primary digital machine and the redundant digital machine. At the end of the conversion the results from the two machines are compared. If any mismatch occurs then a value of 0xFF0X (≥6.528V) is written to the result register. This value is

OPERATION

outside of the clamping range of the ADC and the host should identify this as a fault indication. The last four bits are used to indicate which nibble(s) of the result values did not match.

RESULT	INDICATION
0b1111_1111_0000_0XXX	No fault detected in bits 15–12
0b1111_1111_0000_1XXX	Fault detected in bits 15–12
0b1111_1111_0000_X0XX	No fault detected in bits 11–8
0b1111_1111_0000_X1XX	Fault detected in bits 11–8
0b1111_1111_0000_XX0X	No fault detected in bits 7–4
0b1111_1111_0000_XX1X	Fault detected in bits 7–4
0b1111_1111_0000_XXX0	No fault detected in bits 3–0
0b1111_1111_0000_XXX1	Fault detected in bits 3–0

Since there is a single redundant digital machine, it can apply redundancy to only one ADC at a time. By default, the LTC6813-1 will automatically select ADC path redundancy. However, the user can choose an ADC redundancy path selection by writing to the PS[1:0] bits in Configuration Register Group B.

Table 10 shows all possible ADC path redundancy selections.

When the FDRF bit in Configuration Register Group B is written to 1 it will force the digital redundancy comparison to fail during subsequent ADC conversions.

Measuring Cell Voltages and Sum of Cells (ADCVSC Command)

The ADCVSC command combines eighteen cell measurements and the measurement of Sum of Cells. This command simplifies the synchronization of the individual battery cell voltage and the total Sum of Cells measurements. Figure 8 illustrates the timing of the ADCVSC command. See the section on Commands for the ADCVSC command format. The synchronization of the cell voltage and Sum of Cells measurements, t_{SKEW}, in Fast mode is within 147µs.

Table 11 shows the conversion and synchronization time for the ADCVSC command in different modes. The total conversion time for the command is given by t_{7C}.

Table 10. ADC Path Redundancy Selection

	PS[1:0] = 00		PS[1:0] = 01		PS[1:0] = 10		PS[1:0] = 11	
MEASURE	PATH SELECT	REDUNDANT MEASURE	PATH SELECT	REDUNDANT MEASURE	PATH SELECT	REDUNDANT MEASURE	PATH SELECT	REDUNDANT MEASURE
Cells 1, 7, 13	ADC1	Cell 1	ADC1	Cell 1	ADC2	Cell 7	ADC3	Cell 13
Cells 2, 8, 14	ADC2	Cell 8	ADC1	Cell 2	ADC2	Cell 8	ADC3	Cell 14
Cells 3, 9, 15	ADC3	Cell 15	ADC1	Cell 3	ADC2	Cell 9	ADC3	Cell 15
Cells 4, 10, 16	ADC1	Cell 4	ADC1	Cell 4	ADC2	Cell 10	ADC3	Cell 16
Cells 5, 11, 17	ADC2	Cell 11	ADC1	Cell 5	ADC2	Cell 11	ADC3	Cell 17
Cells 6, 12, 18	ADC3	Cell 18	ADC1	Cell 6	ADC2	Cell 12	ADC3	Cell 18
Cell 7 (ADOL)	ADC2	Cell 7	ADC1	Cell 7	ADC2	Cell 7	ADC3	N/A
Cell 13 (ADOL)	ADC2	Cell 13	ADC1	N/A	ADC2	Cell 13	ADC3	Cell 13
GPIO[n]*	ADC1	GPIO[n]	ADC1	GPIO[n]	ADC2	N/A	ADC3	N/A
2nd Reference*	ADC1	2nd Ref	ADC1	2nd Ref	ADC2	N/A	ADC3	N/A
SC*	ADC1	SC	ADC1	SC	ADC2	N/A	ADC3	N/A
ITMP*	ADC1	ITMP	ADC1	ITMP	ADC2	N/A	ADC3	N/A
VA*	ADC1	VA	ADC1	VA	ADC2	N/A	ADC3	N/A
VD*	ADC1	VD	ADC1	VD	ADC2	N/A	ADC3	N/A

*Note that the ADAX and ADSTAT commands are identical to the ADAXD and ADSTATD commands except that ADAX and ADSTAT will not apply any digital redundancy.

OPERATION

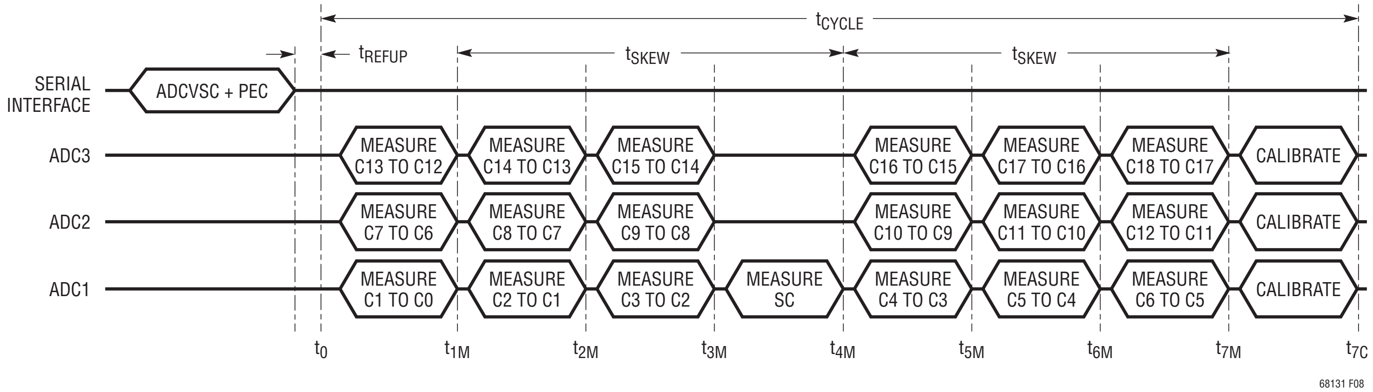


Figure 8. Timing for ADCVSC Command Measuring All 18 Cells, SC

Table 11. Conversion and Synchronization Times for ADCVSC Command in Different Modes

MODE	CONVERSION TIMES (IN µs)								SYNCHRONIZATION TIME (IN µs)
	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{5M}	t_{6M}	t_{7M}	t_{7C}	t_{SKEW}
27kHz	0	58	104	151	205	259	306	352	1,331	147
14kHz	0	87	163	238	321	404	480	556	1,534	235
7kHz	0	145	279	413	554	695	829	963	2,756	409
3kHz	0	261	512	762	1,020	1,277	1,527	1,778	3,571	758
2kHz	0	494	977	1,460	1,950	2,441	2,924	3,407	5,200	1,456
1kHz	0	960	1,908	2,857	3,812	4,768	5,717	6,665	8,458	2,853
422Hz	0	1,890	3,770	5,649	7,536	9,423	11,302	13,181	14,974	5,645
26Hz	0	29,818	59,624	89,431	119,245	149,059	178,866	208,672	234,902	89,427

OPERATION

Overlap Cell Measurement (ADOL Command)

The ADOL command first simultaneously measures Cell 7 with ADC1 and ADC2. Then it simultaneously measures Cell 13 with both ADC2 and ADC3. The host can compare the results against each other to look for inconsistencies which may indicate a fault. The result of the Cell 7 measurement from ADC2 is placed in Cell Voltage Register Group C where the Cell 7 result normally resides. The result from ADC1 is placed in Cell Voltage Register Group C where the Cell 8 result normally resides. The result of the Cell 13 measurement from ADC3 is placed in Cell Voltage Register Group E where the Cell 13 result normally resides. The result from ADC2 is placed in Cell Voltage Register Group E where the Cell 14 result normally resides. Figure 9 illustrates the timing of the ADOL command. See the section on Commands for the ADOL command format.

Table 12 shows the conversion time for the ADOL command. t_{2C} indicates the total conversion time for this command.

Accuracy Check

Measuring an independent voltage reference is the best means to verify the accuracy of a data acquisition system. The LTC6813-1 contains a 2nd reference for this purpose. The ADAX command will initiate the measurement of the 2nd reference. The results are placed in Auxiliary Register Group B. The range of the result depends on the ADC1 measurement accuracy and the accuracy of the 2nd reference, including thermal hysteresis and long term drift. Readings outside the range 2.990V to 3.014V (2.992V to 3.012V for LTC6813I) indicate the system is out of its specified tolerance. ADC2 is verified by comparing it to ADC1 using the ADOL command. ADC3 is verified by comparing it to ADC2 using the ADOL command.

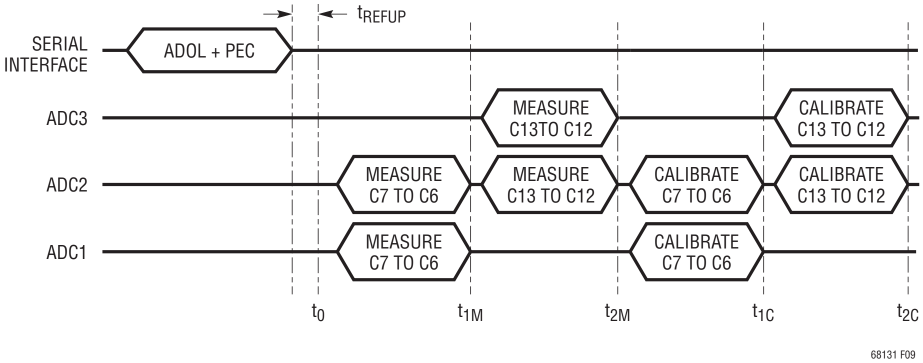


Figure 9. Timing for ADOL Command

Table 12. Conversion Times for ADOL Command

MODE	CONVERSION TIMES (IN µs)			
	t_0	t_{1M}	t_{2M}	t_{2C}
27kHz	0	58	106	384
14kHz	0	87	164	442
7kHz	0	146	281	791
3kHz	0	262	513	1,024
2kHz	0	495	979	1,490
1kHz	0	960	1,910	2,420
422Hz	0	1,891	3,772	4,282
26Hz	0	29,818	59,626	67,119

OPERATION

MUX Decoder Check

The diagnostic command DIAGN ensures the proper operation of each multiplexer channel. The command cycles through all channels and sets the MUXFAIL bit to 1 in Status Register Group B if any channel decoder fails. The MUXFAIL bit is set to 0 if the channel decoder passes the test. The MUXFAIL is also set to 1 on power-up (POR) or after a CLRSTAT command.

The DIAGN command takes about 400µs to complete if the Core is in REFUP state and about 4.5ms to complete if the Core is in STANDBY state. The polling methods described in the section Polling Methods can be used to determine the completion of the DIAGN command.

Digital Filter Check

The delta-sigma ADC is composed of a 1-bit pulse density modulator followed by a digital filter. A pulse density modulated bit stream has a higher percentage of 1s for higher analog input voltages. The digital filter converts this high frequency 1-bit stream into a single 16-bit word. This is why a delta-sigma ADC is often referred to as an oversampling converter.

The self test commands verify the operation of the digital filters and memory. Figure 10 illustrates the operation of the ADC during self test. The output of the 1-bit pulse density modulator is replaced by a 1-bit test signal. The test signal passes through the digital filter and is converted to a 16-bit value. The 1-bit test signal undergoes the same digital conversion as the regular 1-bit signal from the modulator, so the conversion time for any self test command is exactly the same as the corresponding regular ADC conversion command. The 16-bit ADC value is stored in the same register groups as the corresponding regular ADC conversion command. The test signals are designed to place alternating one-zero patterns in the registers. Table 13 provides a list of the self test commands. If the digital filters and memory are working properly, then the registers will contain the values shown in Table 13. For more details see the Commands section.

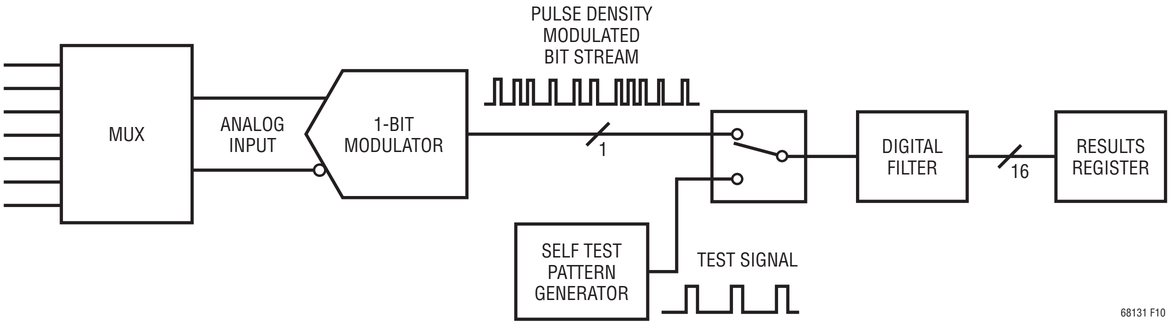


Figure 10. Operation of LTC6813-1 ADC Self Test

Table 13. Self Test Command Summary

		OUTPUT PATTERN IN DIFFERENT ADC MODES			
COMMAND	**SELF TEST OPTION**	**27kHz**	**14kHz**	**7kHz, 3kHz, 2kHz, 1kHz, 422Hz, 26Hz**	**RESULTS REGISTER GROUPS**
CVST	ST[1:0] = 01	0x9565	0x9553	0x9555	C1V to C18V (CVA, CVB, CVC, CVD, CVE, CVF)
	ST[1:0] = 10	0x6A9A	0x6AAC	0x6AAA	
AXST	ST[1:0] = 01	0x9565	0x9553	0x9555	G1V to G9V, REF (AUXA, AUXB, AUXC, AUXD)
	ST[1:0] = 10	0x6A9A	0x6AAC	0x6AAA	
STATST	ST[1:0] = 01	0x9565	0x9553	0x9555	SC, ITMP, VA, VD (STATA, STATB)
	ST[1:0] = 10	0x6A9A	0x6AAC	0x6AAA	

OPERATION

ADC Clear Commands

LTC6813-1 has 3 clear ADC commands: CLRCELL, CLRAUX and CLRSTAT. These commands clear the registers that store all ADC conversion results.

The CLRCELL command clears Cell Voltage Register Groups A, B, C, D, E and F. All bytes in these registers are set to 0xFF by CLRCELL command.

The CLRAUX command clears Auxiliary Register Groups A, B, C and D. All bytes in these registers, except the last four registers of Group D, are set to 0xFF by CLRAUX command.

The CLRSTAT command clears Status Register Groups A and B except the REV and RSVD bits in Status Register Group B. A read back of REV will return the revision code of the part. RSVD bits always read back 0s. All OV and UV flags, MUXFAIL bit, and THSD bit in Status Register Group B and also in Auxiliary Register Group D are set to 1 by CLRSTAT command. The THSD bit is set to 0 after RDSTATB command. The registers storing SC, ITMP, VA and VD are all set to 0xFF by CLRSTAT command.

Open Wire Check (ADOW Command)

The ADOW command is used to check for any open wires between the ADCs of the LTC6813-1 and the external cells. This command performs ADC conversions on the C pin inputs identically to the ADCV command, except two internal current sources sink or source current into the two C pins while they are being measured. The pull-up (PUP) bit of the ADOW command determines whether the current sources are sinking or sourcing 100µA.

The following simple algorithm can be used to check for an open wire on any of the 19 C pins:

1. Run the 18-cell command ADOW with PUP = 1 at least twice. Read the cell voltages for cells 1 through 18 once at the end and store them in array $CELL_{PU}(n)$.
2. Run the 18-cell command ADOW with PUP = 0 at least twice. Read the cell voltages for cells 1 through 18 once at the end and store them in array $CELL_{PD}(n)$.
3. Take the difference between the pull-up and pull-down measurements made in above steps for cells 2 to 18: $CELL_{\Delta}(n) = CELL_{PU}(n) – CELL_{PD}(n)$.
4. For all values of n from 1 to 17: If $CELL_{\Delta}(n+1) < –400mV$, then C(n) is open. If $CELL_{PU}(1) = 0.0000$, then C(0) is open. If $CELL_{PD}(18) = 0.0000$, then C(18) is open.

The above algorithm detects open wires using normal mode conversions with as much as 10nF of capacitance remaining on the LTC6813-1 side of the open wire. However, if more external capacitance is on the open C pin, then the length of time that the open wire conversions are ran in steps 1 and 2 must be increased to give the 100µA current sources time to create a large enough difference for the algorithm to detect an open connection. This can be accomplished by running more than two ADOW commands in steps 1 and 2, or by using filtered mode conversions instead of normal mode conversions. Use Table 14 to determine how many conversions are necessary:

Table 14.

EXTERNAL C PIN CAPACITANCE	NUMBER OF ADOW COMMANDS REQUIRED IN STEPS 1 AND 2	
	NORMAL MODE	FILTERED MODE
≤10nF	2	2
100nF	10	2
1µF	100	2
C	1 + ROUNDUP (C/10nF)	2

Auxiliary Open Wire Check (AXOW Command)

The AXOW command is used to check for any open wires between the GPIO pins of the LTC6813-1 and the external circuit. This command performs ADC conversions on the GPIO pin inputs identically to the ADAX command, except internal current sources sink or source current into each GPIO pin while it is being measured. The pull-up (PUP) bit of the AXOW command determines whether the current sources are sinking or sourcing 100µA.

Thermal Shutdown

To protect the LTC6813-1 from overheating, there is a thermal shutdown circuit included inside the IC. If the temperature detected on the die goes above approximately 150°C, the thermal shutdown circuit trips and resets the Configuration Register Groups and S Control Register Group (including S control bits in PWM/S Control Register Group B) to their default states. This turns off all

OPERATION

discharge switches. When a thermal shutdown event has occurred, the THSD bit in Status Register Group B will go high. The CLRSTAT command can also set the THSD bit high for diagnostic purposes. This bit is cleared when a read operation is performed on Status Register Group B (RDSTATB command). The CLRSTAT command sets the THSD bit high for diagnostic purposes but does not reset the Configuration Register Groups.

Revision Code

The Status Register Group B contains a 4-bit revision code (REV). If software detection of device revision is necessary, then contact the factory for details. Otherwise, the code can be ignored. In all cases, however, the values of all bits must be used when calculating the Packet Error Code (PEC) on data reads.

WATCHDOG AND DISCHARGE TIMER

When there is no valid command for more than 2 seconds, the watchdog timer expires. This resets Configuration Register bytes CFGAR0-3 and the GPIO bits in Configuration Register Group B in all cases. CFGAR4, CFGAR5, the S Control Register Group (including S control bits in PWM/S Control Register Group B) and the remainder of Configuration Register Group B are reset by the watchdog timer when the discharge timer is disabled. The WDT pin is pulled high by the external pull-up when the watchdog time elapses. The watchdog timer is always enabled and it resets after every valid command with matching command PEC.

The discharge timer is used to keep the discharge switches turned ON for programmable time duration. If the discharge timer is being used, the discharge switches are not turned OFF when the watchdog timer is activated.

To enable the discharge timer, connect the DTEN pin to V_{REG} (Figure 11). In this configuration, the discharge switches will remain ON for the programmed time duration that is determined by the DCTO value written in Configuration Register Group A. Table 15 shows the various time settings and the corresponding DCTO value.

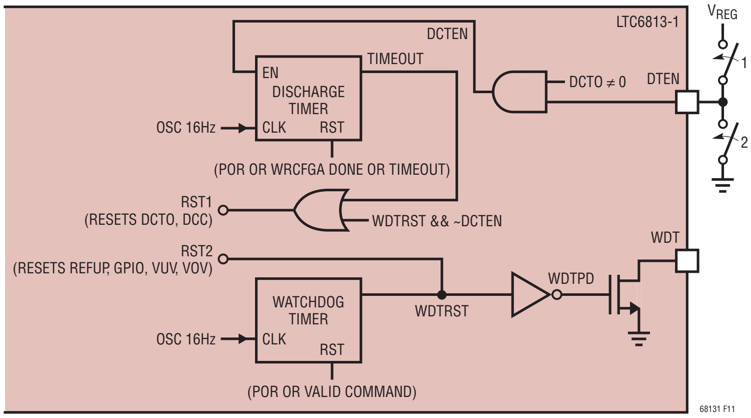


Figure 11. Watchdog and Discharge Timer

Table 15. DCTO Settings

DCTO	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
TIME (MIN)	Disabled	0.5	1	2	3	4	5	10	15	20	30	40	60	75	90	120

Table 16.

	WATCHDOG TIMER	DISCHARGE TIMER
DTEN = 0, DCTO = XXXX	Resets CFGAR0-5, CFGBR0-1 and SCTRL When It Fires	Disabled
DTEN = 1, DCTO = 0000	Resets CFGAR0-5, CFGBR0-1 and SCTRL When It Fires	Disabled
DTEN = 1, DCTO != 0000	Resets CFGAR0-3 and GPIO Bits in CFGBR0 When It Fires	Resets CFGAR4-5, SCTRL and Remainder of CFGBR0-1 When It Fires

OPERATION

Table 16 summarizes the status of the Configuration Register Groups after a watchdog timer or discharge timer event.

The status of the discharge timer can be determined by reading Configuration Register Group A using the RDCFGA command. The DCTO value indicates the time left before the discharge timer expires as shown in Table 17.

Table 17.

DCTO (READ VALUE)	DISCHARGE TIME LEFT (MIN)
0	Disabled (or) Timer Has Timed Out
1	$0 < \text{Timer} \le 0.5$
2	$0.5 < \text{Timer} \le 1$
3	$1 < \text{Timer} \le 2$
4	$2 < \text{Timer} \le 3$
5	$3 < \text{Timer} \le 4$
6	$4 < \text{Timer} \le 5$
7	$5 < \text{Timer} \le 10$
8	$10 < \text{Timer} \le 15$
9	$15 < \text{Timer} \le 20$
A	$20 < \text{Timer} \le 30$
B	$30 < \text{Timer} \le 40$
C	$40 < \text{Timer} \le 60$
D	$60 < \text{Timer} \le 75$
E	$75 < \text{Timer} \le 90$
F	$90 < \text{Timer} \le 120$

Unlike the watchdog timer, the discharge timer does not reset when there is a valid command. The discharge timer can only be reset after a valid WRCFGA (Write Configuration Register Group A) command. There is a possibility that the discharge timer will expire in the middle of some commands.

If the discharge timer activates in the middle of a WRCFGA command, the Configuration Register Groups and S Control Register Group (including S control bits in PWM/S Control Register Group B) will reset as per Table 16. However, at the end of the valid WRCFGA command, the new data is copied to Configuration Register Group A. The new configuration data is not lost when the discharge timer is activated.

If the discharge timer activates in the middle of a RDCFGA or RDCFGB command, the Configuration Register Groups reset as per Table 16. As a result, the read back data from bytes CFGAR4 and CFGAR5 and CFGBR0 and CFGBR1 could be corrupted. If the discharge timer activates in the middle of a RDSCTRL or RDPSB command, the S Control Register Group (including S control bits in PWM/S Control Register Group B) resets as per Table 16. As a result, the read back data could be corrupted.

S PIN PULSE-WIDTH MODULATION FOR CELL BALANCING

For additional control of cell discharging, the host may configure the S pins to operate using pulse-width modulation. While the watchdog timer is not expired, the DCC bits in the Configuration Register Groups control the S pins directly. After the watchdog timer expires, PWM operation begins and continues for the remainder of the selected discharge time or until a wake-up event occurs (and the watchdog timer is reset). During PWM operation, the DCC bits must be set to 1 for the PWM feature to operate.

Once PWM operation begins, the configurations in the PWM register may cause some or all S pins to be periodically de-asserted to achieve the desired duty cycle as shown in Table 18. Each PWM signal operates on a 30 second period. For each cycle, the duty cycle can be programmed from 0% to 100% in increments of 1/15 = 6.67% (2 seconds).

Each S pin PWM signal is sequenced at different intervals to ensure that no two pins switch on or off at the same time. The switching interval between channels is 62.5ms, and 1.125s is required for all eighteen pins to switch (18 • 62.5ms).

OPERATION

Table 18. S Pin Pulse-Width Modulation Settings

DCC BIT (CONFIG REGISTER GROUPS)	PWMC SETTING	ON TIME (SECONDS)	OFF TIME (SECONDS)	DUTY CYCLE (%)
0	4'bXXXX	0	Continuously Off	0
1	4'b1111	Continuously On	0	100.0
1	4'b1110	28	2	93.3
1	4'b1101	26	4	86.7
1	4'b1100	24	6	80.0
1	4'b1011	22	8	73.3
1	4'b1010	20	10	66.7
1	4'b1001	18	12	60.0
1	4'b1000	16	14	53.3
1	4'b0111	14	16	46.7
1	4'b0110	12	18	40.0
1	4'b0101	10	20	33.3
1	4'b0100	8	22	26.7
1	4'b0011	6	24	20.0
1	4'b0010	4	26	13.3
1	4'b0001	2	28	6.7
1	4'b0000	0	Continuously Off	0

The default values of the PWM control settings (located in PWM Register Group and PWM/S Control Register Group B) are all 1s. Upon entering sleep mode, the PWM control settings will be initialized to their default values.

DISCHARGE TIMER MONITOR

The LTC6813-1 has the ability to periodically monitor cell voltages while the discharge timer is active. The host should write the DTMEN bit in Configuration Register Group B to 1 to enable this feature.

When the discharge timer monitor is enabled and the watchdog timer has expired, the LTC6813-1 will perform a conversion of all cell voltages in 7kHz (Normal) mode every 30 seconds. The overvoltage and undervoltage comparisons will be performed and flags will be set if cells have crossed a threshold. For any undervoltage cells the discharge timer monitor will automatically clear the associated DCC bit in Configuration Register Group A or Configuration Register Group B so that the cell will no longer be discharged. Clearing the DCC bit will also disable PWM discharge. With this feature, the host can write the undervoltage threshold to the desired discharge level and use the discharge timer monitor to discharge all, or selected, cells (using either constant discharge or PWM discharge) down to that level.

During discharge timer monitoring, digital redundancy checking will be performed on the cell voltage measurements. If a digital redundancy failure occurs, all DCC bits will be cleared.

I^{2}C/SPI MASTER ON LTC6813-1 USING GPIOs

The I/O ports GPIO3, GPIO4 and GPIO5 on LTC6813-1 can be used as an I^{2}C or SPI master port to communicate to an I^{2}C or SPI slave. In the case of an I^{2}C master, GPIO4 and GPIO5 form the SDA and SCL ports of the I^{2}C interface, respectively. In the case of a SPI master, GPIO3, GPIO4 and GPIO5 become the CSBM, SDIOM and SCKM ports of the SPI interface respectively. The SPI master on LTC6813-1 supports SPI mode 3 (CHPA = 1, CPOL = 1).

OPERATION

The GPIOs are open-drain outputs, so an external pull-up is required on these ports to operate as an I^2C or SPI master. It is also important to write the GPIO bits to 1 in the Configuration Register Groups so these ports are not pulled low internally by the device.

COMM Register

LTC6813-1 has a 6-byte COMM register as shown in Table 19. This register stores all data and control bits required for I^2C or SPI communication to a slave. The COMM register contains three bytes of data Dn[7:0] to be transmitted to or received from the slave device. ICOMn[3:0] specify control actions before transmitting/receiving each data byte. FCOMn[3:0] specify control actions after transmitting/receiving each data byte.

If the bit ICOMn[3] in the COMM register is set to 1, the part becomes a SPI master and if the bit is set to 0, the part becomes an I^2C master.

Table 20 describes the valid write codes for ICOMn[3:0] and FCOMn[3:0] and their behavior when using the part as an I^2C master.

Table 21 describes the valid write codes for ICOMn[3:0] and FCOMn[3:0] and their behavior when using the part as a SPI master.

Table 19. COMM Register Memory Map

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMM0	RD/WR	ICOM0[3]	ICOM0[2]	ICOM0[1]	ICOM0[0]	D0[7]	D0[6]	D0[5]	D0[4]
COMM1	RD/WR	D0[3]	D0[2]	D0[1]	D0[0]	FCOM0[3]	FCOM0[2]	FCOM0[1]	FCOM0[0]
COMM2	RD/WR	ICOM1[3]	ICOM1[2]	ICOM1[1]	ICOM1[0]	D1[7]	D1[6]	D1[5]	D1[4]
COMM3	RD/WR	D1[3]	D1[2]	D1[1]	D1[0]	FCOM1[3]	FCOM1[2]	FCOM1[1]	FCOM1[0]
COMM4	RD/WR	ICOM2[3]	ICOM2[2]	ICOM2[1]	ICOM2[0]	D2[7]	D2[6]	D2[5]	D2[4]
COMM5	RD/WR	D2[3]	D2[2]	D2[1]	D2[0]	FCOM2[3]	FCOM2[2]	FCOM2[1]	FCOM2[0]

Table 20. Write Codes for ICOMn[3:0] and FCOMn[3:0] on I^2C Master

CONTROL BITS	CODE	ACTION	DESCRIPTION
ICOMn[3:0]	0110	START	Generate a START Signal on I^2C Port Followed by Data Transmission
	0001	STOP	Generate a STOP Signal on I^2C Port
	0000	BLANK	Proceed Directly to Data Transmission on I^2C Port
	0111	No Transmit	Release SDA and SCL and Ignore the Rest of the Data
FCOMn[3:0]	0000	Master ACK	Master Generates an ACK Signal on Ninth Clock Cycle
	1000	Master NACK	Master Generates a NACK Signal on Ninth Clock Cycle
	1001	Master NACK + STOP	Master Generates a NACK Signal Followed by STOP Signal

Table 21. Write Codes for ICOMn[3:0] and FCOMn[3:0] on SPI Master

CONTROL BITS	CODE	ACTION	DESCRIPTION
ICOMn[3:0]	1000	CSBM Low	Generates a CSBM Low Signal on SPI Port (GPIO3)
	1010	CSBM Falling Edge	Drives CSBM (GPIO3) High, then Low
	1001	CSBM High	Generates a CSBM High Signal on SPI Port (GPIO3)
	1111	No Transmit	Releases the SPI Port and Ignores the Rest of the Data
FCOMn[3:0]	X000	CSBM Low	Holds CSBM Low at the End of Byte Transmission
	1001	CSBM High	Transitions CSBM High at the End of Byte Transmission

OPERATION

Note that only the codes listed in Table 20 and Table 21 are valid for ICOMn[3:0] and FCOMn[3:0]. Writing any other code that is not listed in Table 20 and Table 21 to ICOMn[3:0] and FCOMn[3:0] may result in unexpected behavior on the I^2C or SPI port.

COMM Commands

Three commands help accomplish I^2C or SPI communication to the slave device: WRCOMM, STCOMM and RDCOMM.

WRCOMM Command: This command is used to write data to the COMM register. This command writes 6 bytes of data to the COMM register. The PEC needs to be written at the end of the data. If the PEC does not match, all data in the COMM register is cleared to 1s when CSB goes high. See the section Bus Protocols for more details on a write command format.

STCOMM Command: This command initiates I^2C/SPI communication on the GPIO ports. The COMM register contains 3 bytes of data to be transmitted to the slave. During this command, the data bytes stored in the COMM register are transmitted to the slave I^2C or SPI device and the data received from the I^2C or SPI device is stored in the COMM register. This command uses GPIO4 (SDA) and GPIO5 (SCL) for I^2C communication or GPIO3 (CSBM), GPIO4 (SDIOM) and GPIO5 (SCKM) for SPI communication.

The STCOMM command is to be followed by 24 clock cycles for each byte of data to be transmitted to the slave device while holding CSB low. For example, to transmit three bytes of data to the slave, send STCOMM command and its PEC followed by 72 clock cycles. Pull CSB high at the end of the 72 clock cycles of STCOMM command.

During I^2C or SPI communication, the data received from the slave device is updated in the COMM register.

RDCOMM Command: The data received from the slave device can be read back from the COMM register using the RDCOMM command. The command reads back six bytes of data followed by the PEC. See the section Bus Protocols for more details on a read command format.

Table 22 describes the possible read back codes for ICOMn[3:0] and FCOMn[3:0] when using the part as an I^2C master. Dn[7:0] contains the data byte transmitted by the I^2C slave.

Table 22. Read Codes for ICOMn[3:0] and FCOMn[3:0] on I^2C Master

CONTROL BITS	CODE	DESCRIPTION
ICOMn[3:0]	0110	Master Generated a START Signal
	0001	Master Generated a STOP Signal
	0000	Blank, SDA Was Held Low Between Bytes
	0111	Blank, SDA Was Held High Between Bytes
FCOMn[3:0]	0000	Master Generated an ACK Signal
	0111	Slave Generated an ACK Signal
	1111	Slave Generated a NACK Signal
	0001	Slave Generated an ACK Signal, Master Generated a STOP Signal
	1001	Slave Generated a NACK Signal, Master Generated a STOP Signal

In case of the SPI master, the read back codes for ICOMn[3:0] and FCOMn[3:0] are always 0111 and 1111, respectively. Dn[7:0] contains the data byte transmitted by the SPI slave.

Figure 12 illustrates the operation of LTC6813-1 as an I^2C or SPI master using the GPIOs.

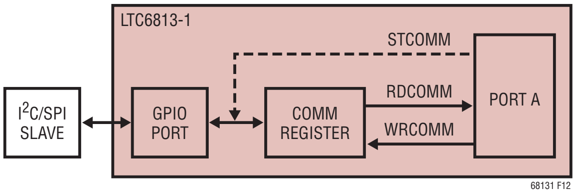


Figure 12. LTC6813-1 I^2C/SPI Master Using GPIOs

Any number of bytes can be transmitted to the slave in groups of 3 bytes using these commands. The GPIO ports will not get reset between different STCOMM commands. However, if the wait time between the commands is greater than 2s, the watchdog will time out and reset the ports to their default values.

To transmit several bytes of data using an I^2C master, a START signal is only required at the beginning of the entire data stream. A STOP signal is only required at the end of the data stream. All intermediate data groups can use a BLANK code before the data byte and an ACK/NACK signal as appropriate after the data byte. SDA and SCL will not get reset between different STCOMM commands.

OPERATION

To transmit several bytes of data using SPI master, a CSBM low signal is sent at the beginning of the 1st data byte. CSBM can be held low or taken high for intermediate data groups using the appropriate code on FCOMn[3:0]. A CSBM high signal is sent at the end of the last byte of data. CSBM, SDIOM and SCKM will not get reset between different STCOMM commands.

Figure 13 shows the 24 clock cycles following STCOMM command for an I^2C master in different cases. Note that if ICOMn[3:0] specified a STOP condition, after the STOP signal is sent, the SDA and SCL lines are held high and all data in the rest of the word is ignored. If ICOMn[3:0] is a NO TRANSMIT, both SDA and SCL lines are released, and the rest of the data in the word is ignored. This is used when a particular device in the stack does not have to communicate to a slave.

Figure 14 shows the 24 clock cycles following STCOMM command for a SPI master. Similar to the I^2C master, if ICOMn[3:0] specified a CSBM HIGH or a NO TRANSMIT condition, the CSBM, SCKM and SDIOM lines of the SPI master are released and the rest of the data in the word is ignored.

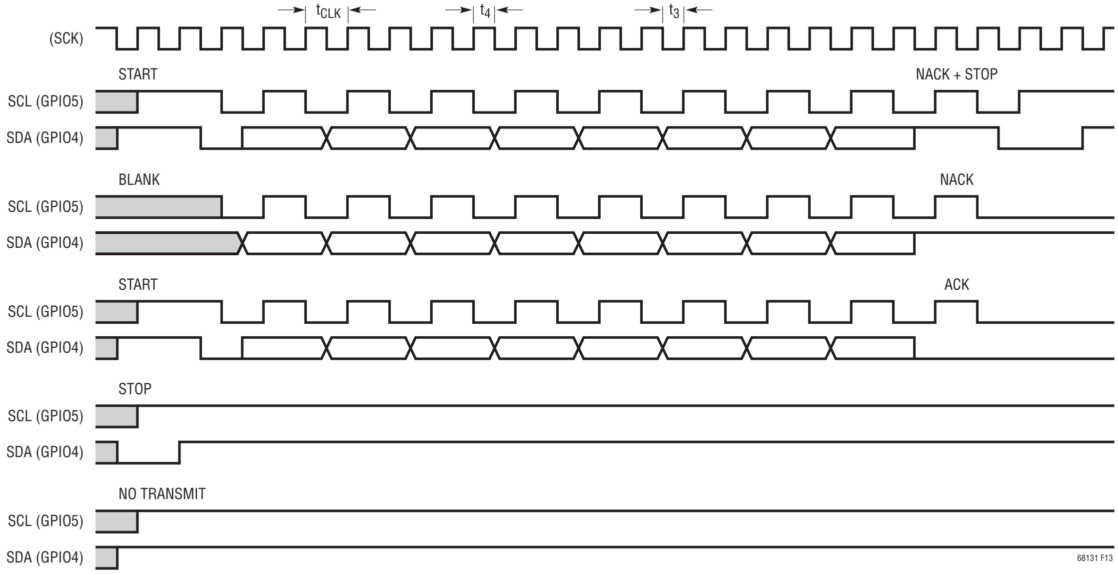


Figure 13. STCOMM Timing Diagram for an I^2C Master

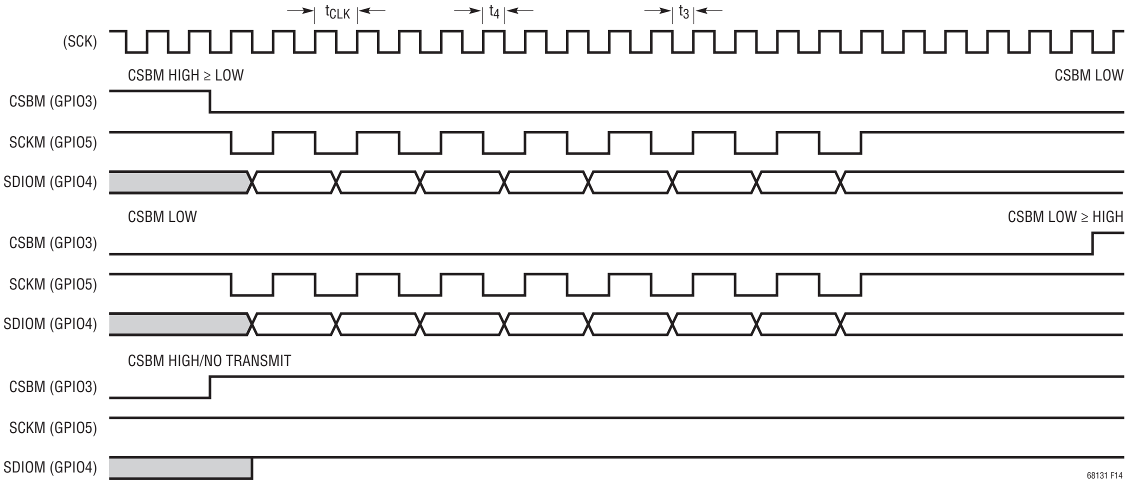


Figure 14. STCOMM Timing Diagram for a SPI Master

OPERATION

Timing Specifications of I^{2}C and SPI Master

The timing of the LTC6813-1 I^{2}C or SPI master will be controlled by the timing of the communication at the LTC6813-1's primary SPI interface. Table 23 shows the I^{2}C master timing relationship to the primary SPI clock. Table 24 shows the SPI master timing specifications.

Table 23. I^{2}C Master Timing

I^{2}C MASTER PARAMETER	TIMING RELATIONSHIP TO PRIMARY SPI INTERFACE	TIMING SPECIFICATIONS AT t_{CLK} = 1µs
SCL Clock Frequency	$1/(2 \bullet t_{CLK})$	Max 500kHz
t_{HD};STA	t_3	Min 200ns
t_{LOW}	t_{CLK}	Min 1µs
t_{HIGH}	t_{CLK}	Min 1µs
t_{SU};STA	$t_{CLK} + t_4$*	Min 1.03µs
t_{HD};DAT	t_4*	Min 30ns
t_{SU};DAT	t_3	Min 200ns
t_{SU};STO	$t_{CLK} + t_4$*	Min 1.03µs
t_{BUF}	$3 \bullet t_{CLK}$	Min 3µs

*Note: When using isoSPI, t_4 is generated internally and is a minimum of 30ns. Also, $t_3 = t_{CLK} – t_4$. When using SPI, t_3 and t_4 are the low and high times of the SCK input, each with a specified minimum of 200ns.

Table 24. SPI Master Timing

SPI MASTER PARAMETER	TIMING RELATIONSHIP TO PRIMARY SPI INTERFACE	TIMING SPECIFICATIONS AT t_{CLK} = 1µs
SDIOM Valid to SCKM Rising Setup	t_3	Min 200ns
SDIO Valid from SCKM Rising Hold	$t_{CLK} + t_4$*	Min 1.03µs
SCKM Low	t_{CLK}	Min 1µs
SCKM High	t_{CLK}	Min 1µs
SCKM Period (SCKM_Low + SCKM_High)	$2 \bullet t_{CLK}$	Min 2µs
CSBM Pulse Width	$3 \bullet t_{CLK}$	Min 3µs
SCKM Rising to CSBM Rising	$5 \bullet t_{CLK} + t_4$*	Min 5.03µs
CSBM Falling to SCKM Falling	t_3	Min 200ns
CSBM Falling to SCKM Rising	$t_{CLK} + t_3$	Min 1.2µs
SCKM Falling to SDIOM Valid	Master Requires < t_{CLK}	

*Note: When using isoSPI, t_4 is generated internally and is a minimum of 30ns. Also, $t_3 = t_{CLK} – t_4$. When using SPI, t_3 and t_4 are the low and high times of the SCK input, each with a specified minimum of 200ns.

OPERATION

S PIN PULSING USING THE S PIN CONTROL SETTINGS

The S pins of the LTC6813-1 can be used as a simple serial interface. This is particularly useful for controlling Analog Devices LT8584, a monolithic flyback DC/DC converter, designed to actively balance large battery stacks. The LT8584 has several operating modes which are controlled through a serial interface. The LTC6813-1 can communicate to an LT8584 by sending a sequence of pulses on each S pin to select a specific LT8584 mode. The S pin control settings (located in S Control Register Group and PWM/S Control Register Group B) are used to specify the behavior for each of the 18 S pins, where each nibble specifies whether the S pin should drive high, drive low, or send a pulse sequence of between 1 and 7 pulses. Table 25 shows the possible S pin behaviors that can be sent to the LT8584.

The S pin pulses occur at a pulse rate of 6.44kHz (155µs period). The pulse width will be 77.6µs. The S pin pulsing begins when the STSCTRL command is sent, after the last command PEC clock, provided that the command PEC matches. The host may then continue to clock SCK in order to poll the status of the pulsing. This polling works similarly to the ADC polling feature. The data out will remain logic low until the S pin pulsing sequence has completed.

While the S pin pulsing is in progress, new STSCTRL, WRSCTRL or WRPSB commands are ignored. The PLADC command may be used to determine when the S pin pulsing has completed.

If the WRSCTRL (or WRPSB) command and command PEC are received correctly but the data PEC does not match, then the S pin control settings will be cleared.

If a DCC bit in Configuration Register Group A or Configuration Register Group B is asserted, the LTC6813-1 will drive the selected S pin low, regardless of the S pin control settings. The host should leave the DCC bits set to 0 when using the S pin control settings.

The CLRSCTRL command can be used to quickly reset the S pin control settings to all 0s and force the pulsing machine to release control of the S pins. This command

Table 25. S Pin Pulsing Behavior

NIBBLE VALUE	S PIN BEHAVIOR
0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1XXX	

OPERATION

may be helpful in reducing the diagnostic control loop time in an automotive application.

S PIN MUTING

The S pins may be disabled by sending the MUTE command and re-enabled by sending the UNMUTE command. The MUTE and UNMUTE commands do not require any subsequent data and thus the commands will propagate quickly through a stack of LTC6813-1 devices. This allows the host to quickly (<100µs) disable and re-enable discharging without disturbing register contents. This can be useful, for instance, to allow for a specific settling time before taking cell measurements. The mute status is reported in the read-only MUTE bit in Configuration Register Group B.

SERIAL INTERFACE OVERVIEW

There are two types of serial ports on the LTC6813-1: a standard 4-wire serial peripheral interface (SPI) and a 2-wire isolated interface (isoSPI). The state of the ISOMD pin determines whether pins 53, 54, 61 and 62 are a 2-wire or 4-wire serial port.

The LTC6813-1 is used in a daisy-chain configuration. A second isoSPI interface uses pins 57, 58, 63 and 64.

4-WIRE SERIAL PERIPHERAL INTERFACE (SPI) PHYSICAL LAYER

External Connections

Connecting ISOMD to V^- configures serial Port A for 4-wire SPI. The SDO pin is an open drain output which requires a pull-up resistor tied to the appropriate supply voltage (Figure 15).

Timing

The 4-wire serial port is configured to operate in a SPI system using CPHA = 1 and CPOL = 1. Consequently, data on SDI must be stable during the rising edge of SCK. The timing is depicted in Figure 16. The maximum data rate is 1Mbps; however the device is tested at a higher data rate in production in order to guarantee operation at the maximum specified data rate.

2-WIRE ISOLATED INTERFACE (isoSPI) PHYSICAL LAYER

The 2-wire interface provides a means to interconnect LTC6813-1 devices using simple twisted pair cabling. The interface is designed for low packet error rates when the cabling is subjected to high RF fields. Isolation is achieved through an external transformer.

Standard SPI signals are encoded into differential pulses. The strength of the transmission pulse and the threshold level of the receiver are set by two external resistors. The values of the resistors allow the user to trade-off power dissipation for noise immunity.

Figure 17 illustrates how the isoSPI circuit operates. A 2V reference drives the IBIAS pin. External resistors R_{B1} and R_{B2} create the reference current I_B. This current sets the drive strength of the transmitter. R_{B1} and R_{B2} also form a voltage divider to supply a fraction of the 2V reference for the ICMP pin. The receiver circuit threshold is half of the voltage at the ICMP pin.

External Connections

The LTC6813-1 has 2 serial ports which are called Port B and Port A. Port B is always configured as a 2-wire interface. Port A is either a 2-wire or 4-wire interface, depending on the connection of the ISOMD pin.

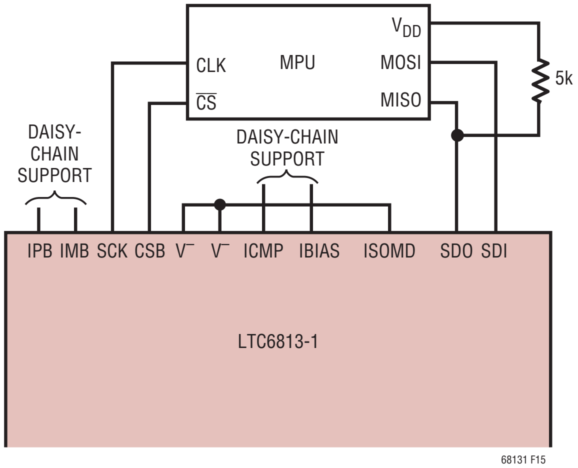


Figure 15. 4-Wire SPI Configuration

OPERATION

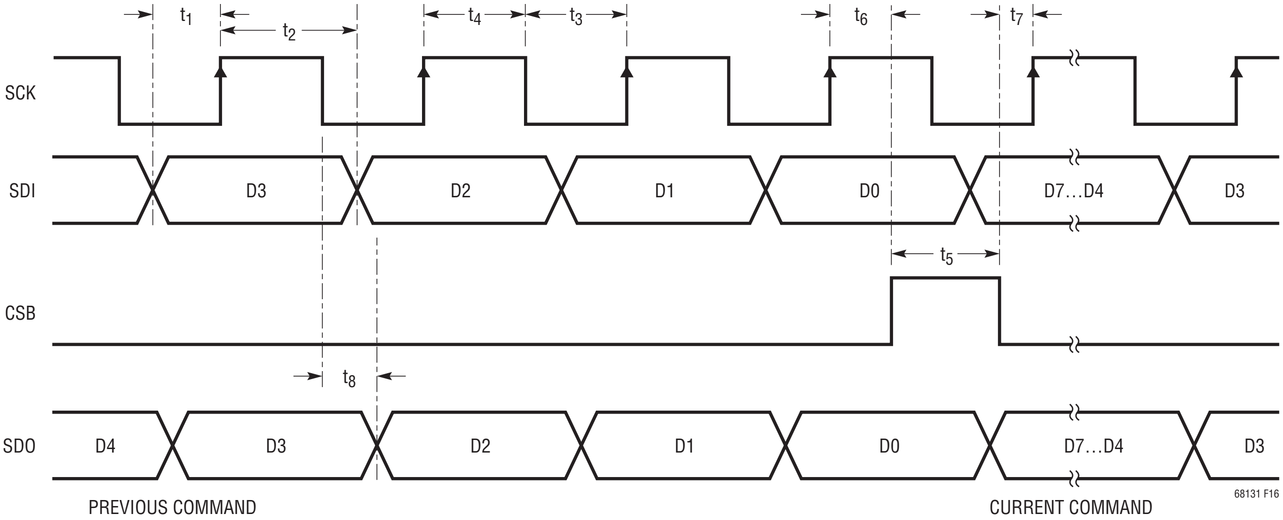


Figure 16. Timing Diagram of 4-Wire Serial Peripheral Interface

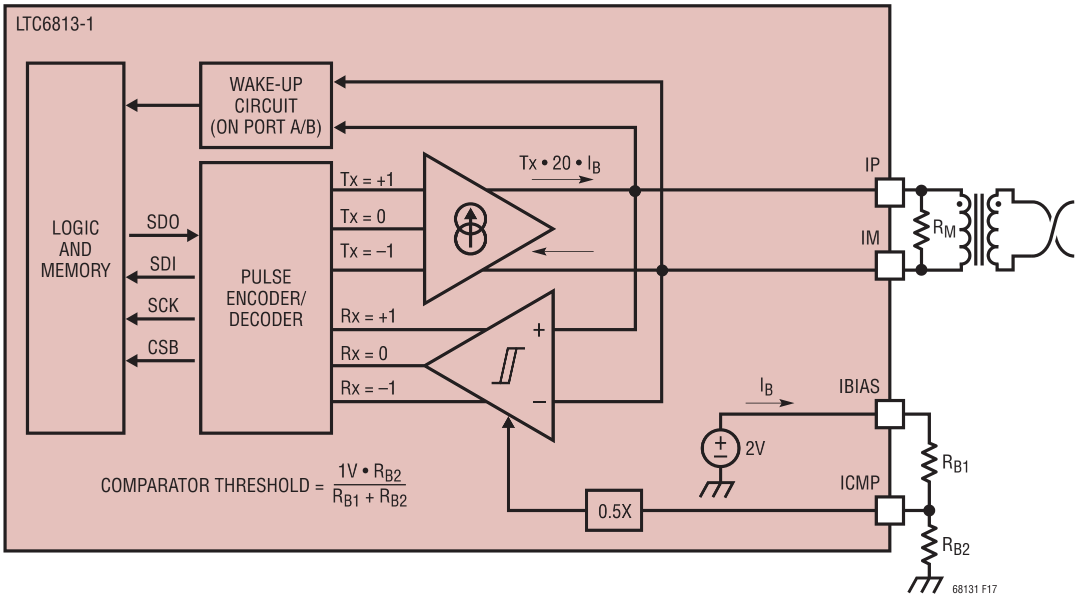


Figure 17. isoSPI Interface

OPERATION

When Port A is configured as a 4-wire interface, Port A is always the SLAVE port and Port B is the MASTER port. Communication is always initiated on Port A of the first device in the daisy-chain configuration. The final device in the daisy chain does not use Port B, and it should be terminated into R_M. Figure 18 shows the simplest port connections possible when the microprocessor and the LTC6813-1s are located on the same PCB. In this figure capacitors are used to couple signals between the LTC6813-1s.

When Port A is configured as a 2-wire interface, communication can be initiated on either Port A or Port B. If communication is initiated on Port A, LTC6813-1 configures Port A as slave and Port B as master. Likewise, if communication is initiated on Port B, LTC6813-1 configures Port B as slave and Port A as master. See the section Reversible isoSPI for a detailed description of reversible isoSPI.

Figure 19 is an example of a robust interconnection of multiple identical PCBs, each containing one LTC6813-1 configured for operation in a daisy chain. The microprocessor is located on a separate PCB. To achieve 2-wire isolation between the microprocessor PCB and the 1st LTC6813-1 PCB, use the LTC6820 support IC. The LTC6820 is functionally equivalent to the diagram in Figure 17. In this example, communication is initiated on Port A. So the LTC6813-1 configures Port A as slave and Port B as master.

Using a Single LTC6813-1

When only one LTC6813-1 is needed, it can be used as a single (non daisy-chained) device if the second isoSPI port (Port B) is properly biased and terminated, as shown in Figure 20 and Figure 21. ICMP should *not* be tied to GND, but can be tied directly to IBIAS. A bias resistance (2k to 20k) is required for IBIAS. Do *not* tie IBIAS directly to V_{REG} or V^-. Finally, IPB and IMB should be terminated into a 100Ω resistor (*not* tied to V_{REG} or V^-).

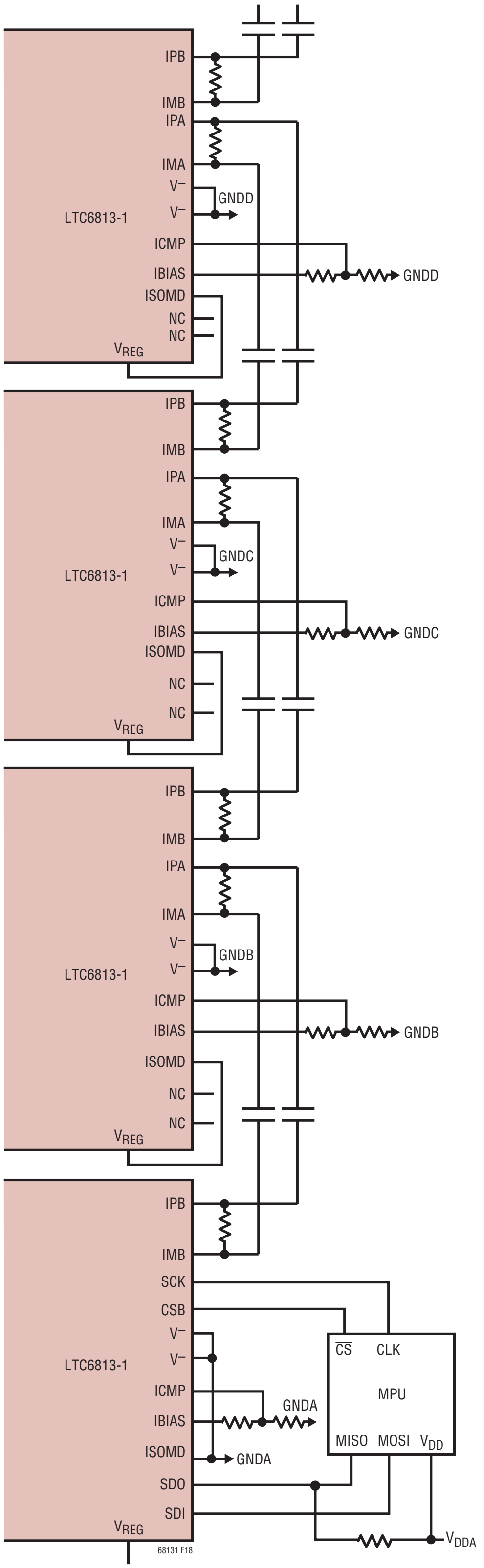


Figure 18. Capacitive-Coupled Daisy-Chain Configuration

OPERATION

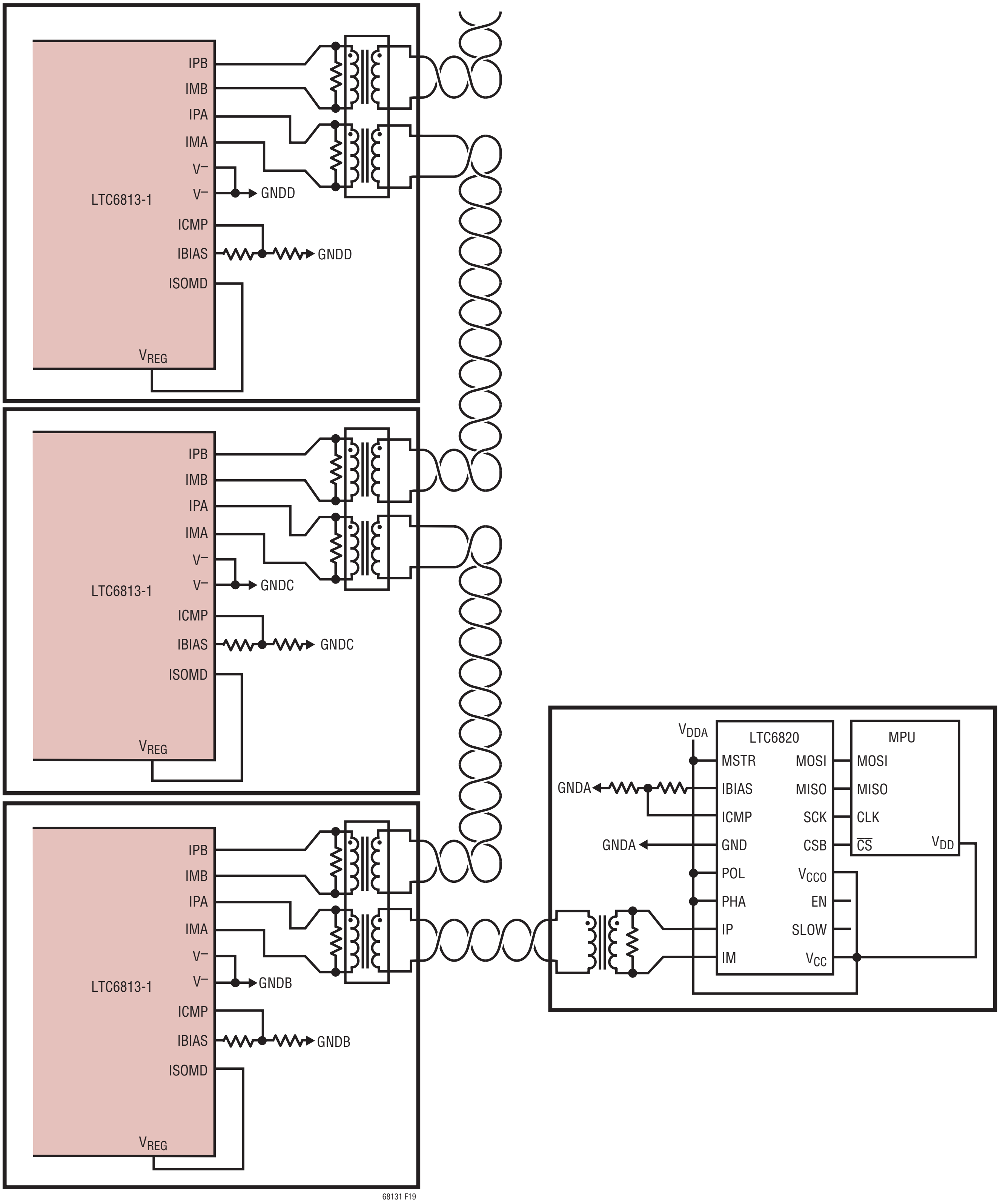


Figure 19. Transformer-Isolated Daisy-Chain Configuration

OPERATION

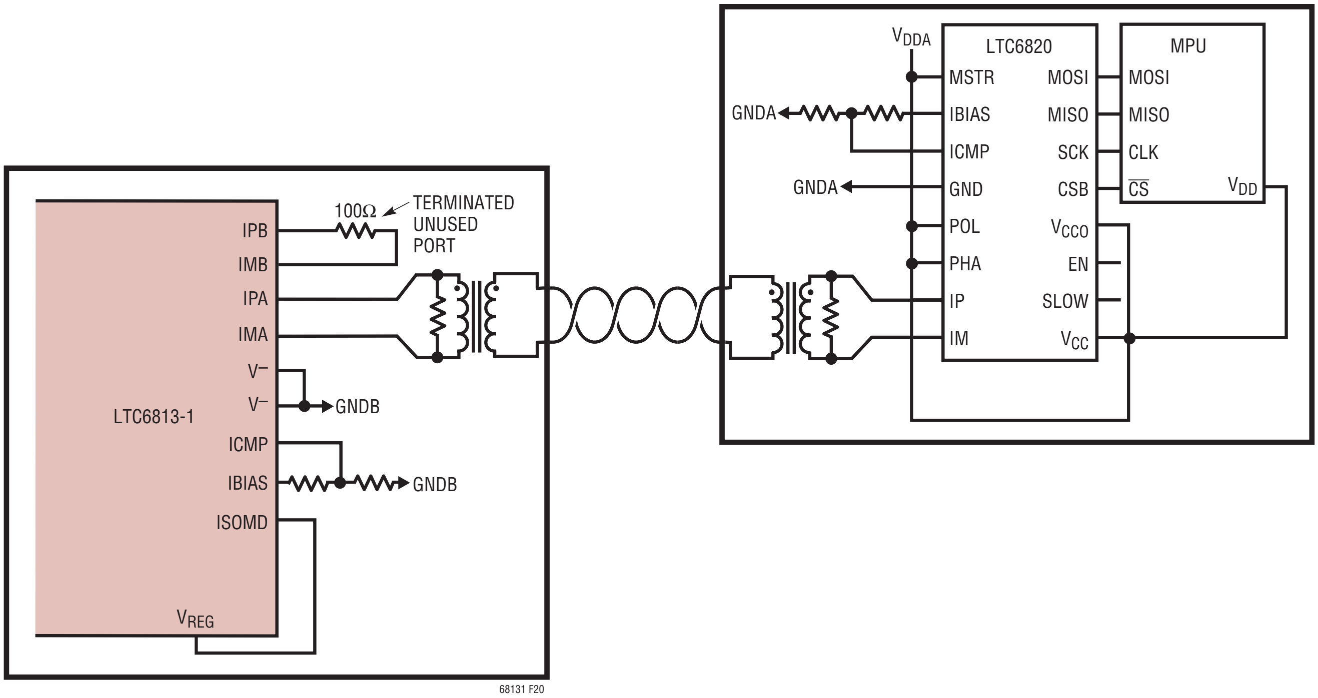


Figure 20. Single Device Using 2-Wire Port A

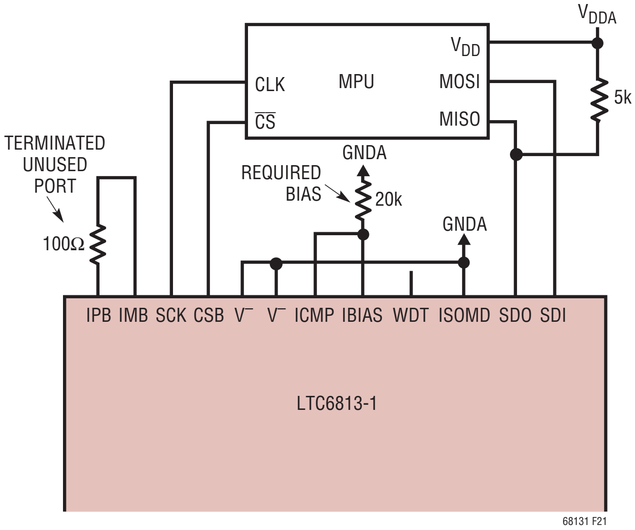


Figure 21. Single Device Using 4-Wire Port A

OPERATION

Selecting Bias Resistors

The adjustable signal amplitude allows the system to trade power consumption for communication robustness, and the adjustable comparator threshold allows the system to account for signal losses.

The isoSPI transmitter drive current and comparator voltage threshold are set by a resistor divider ($R_{BIAS} = R_{B1} + R_{B2}$) between IBIAS and $V^–$. The divided voltage is connected to the ICMP pin, which sets the comparator threshold to half of this voltage (V_{ICMP}). When either isoSPI interface is enabled (not IDLE) IBIAS is held at 2V, causing a current I_B to flow out of the IBIAS pin. The IP and IM pin drive currents are $20 \bullet I_B$.

As an example, if divider resistor R_{B1} is 2.8k and resistor R_{B2} is 1.21k (so that R_{BIAS} = 4k), then:

$$I_B = \frac{2V}{R_{B1} + R_{B2}} = 0.5mA$$

$$I_{DRV} = I_{IP} = I_{IM} = 20 \bullet I_B = 10mA$$

$$V_{ICMP} = 2V \bullet \frac{R_{B2}}{R_{B1} + R_{B2}} = I_B \bullet R_{B2} = 603mV$$

$$V_{TCMP} = 0.5 \bullet V_{ICMP} = 302mV$$

In this example, the pulse drive current I_{DRV} will be 10mA, and the receiver comparators will detect pulses with IP–IM amplitudes greater than ±302mV.

If the isolation barrier uses 1:1 transformers connected by a twisted pair and terminated with 120Ω resistors on each end, then the transmitted differential signal amplitude (±) will be:

$$V_A = I_{DRV} \bullet \frac{R_M}{2} = 0.6V$$

(This result ignores transformer and cable losses, which may reduce the amplitude).

isoSPI Pulse Detail

Two LTC6813-1 devices can communicate by transmitting and receiving differential pulses back and forth through an isolation barrier. The transmitter can output three voltage levels: $+V_A$, 0V and $–V_A$. A positive output results from IP sourcing current and IM sinking current across load resistor R_M. A negative voltage is developed by IP sinking and IM sourcing. When both outputs are off, the load resistance forces the differential output to 0V.

To eliminate the DC signal component and enhance reliability, the isoSPI uses two different pulse lengths. This allows four types of pulses to be transmitted, as shown in Table 26. A +1 pulse will be transmitted as a positive pulse followed by a negative pulse. A –1 pulse will be transmitted as a negative pulse followed by a positive pulse. The duration of each pulse is defined as $t_{1/2PW}$, since each is half of the required symmetric pair. (The total isoSPI pulse duration is $2 \bullet t_{1/2PW}$).

Table 26. isoSPI Pulse Types

PULSE TYPE	FIRST LEVEL ($t_{1/2PW}$)	SECOND LEVEL ($t_{1/2PW}$)	ENDING LEVEL
Long +1	$+V_A$ (150ns)	$–V_A$ (150ns)	0V
Long –1	$–V_A$ (150ns)	$+V_A$ (150ns)	0V
Short +1	$+V_A$ (50ns)	$–V_A$ (50ns)	0V
Short –1	$–V_A$ (50ns)	$+V_A$ (50ns)	0V

The receiver is designed to detect each of these isoSPI pulse types. For successful detection, the incoming isoSPI pulses (CSB or data) should meet the following requirements:

1. $t_{1/2PW}$ of incoming pulse > t_{FILT} of the receiver and
2. t_{INV} of incoming pulse < t_{WNDW} of the receiver

The worst-case margin (margin 1) for the first condition is the difference between minimum $t_{1/2PW}$ of the incoming pulse and maximum t_{FILT} of the receiver. Likewise, the worst-case margin (margin 2) for the second condition is the difference between minimum t_{WNDW} of the receiver and maximum t_{INV} of the incoming pulse. These timing relations are illustrated in Figure 22.

A host microcontroller does not have to generate isoSPI pulses to use this 2-wire interface. The first LTC6813-1 in the system can communicate to the microcontroller using the 4-wire SPI interface on its Port A, then daisy chain to other LTC6813-1s using the 2-wire isoSPI interface on its Port B. Alternatively, the LTC6820 can be used to translate the SPI signals into isoSPI pulses.

OPERATION

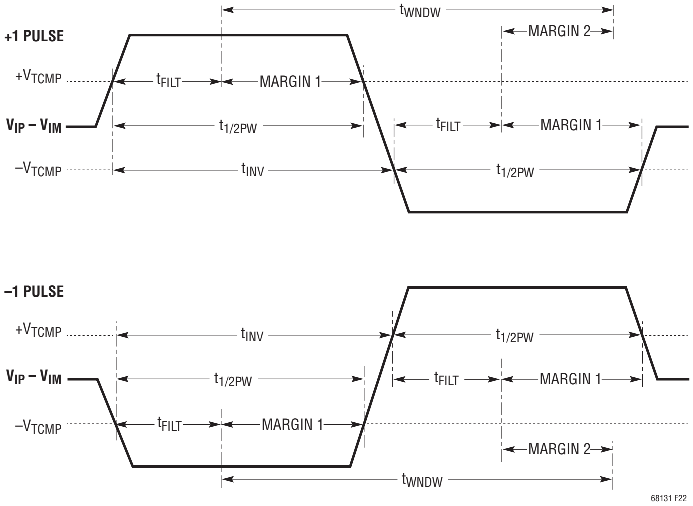


Figure 22. isoSPI Pulse Detail

Operation with Port A Configured for SPI

When the LTC6813-1 is operating with Port A as a SPI (ISOMD = $V^–$), the SPI detects one of four communication events: CSB falling, CSB rising, SCK rising with SDI = 0 and SCK rising with SDI = 1. Each event is converted into one of the four pulse types for transmission through the daisy chain. Long pulses are used to transmit CSB changes and short pulses are used to transmit data, as explained in Table 27.

Table 27. Port B (Master) isoSPI Port Function

COMMUNICATION EVENT (PORT A SPI)	TRANSMITTED PULSE (PORT B isoSPI)
CSB Rising	Long +1
CSB Falling	Long –1
SCK Rising Edge, SDI = 1	Short +1
SCK Rising Edge, SDI = 0	Short –1

Operation with Port A Configured for isoSPI

On the other side of the isolation barrier (i.e., at the other end of the cable), the 2nd LTC6813-1 will have ISOMD = V_{REG} so that its Port A is configured for isoSPI. The slave isoSPI port (Port A or B) receives each transmitted pulse and reconstructs the SPI signals internally, as shown in Table 28. In addition, during a READ command this port may transmit return data pulses.

Table 28. Port A (Slave) isoSPI Port Function

RECEIVED PULSE (PORT A isoSPI)	INTERNAL SPI PORT ACTION	RETURN PULSE
Long +1	Drive CSB High	None
Long –1	Drive CSB Low	
Short +1	1. Set SDI = 1 2. Pulse SCK	Short –1 Pulse if Reading a 0 Bit (No Return Pulse if not in READ Mode or if Reading a 1 Bit)
Short –1	1. Set SDI = 0 2. Pulse SCK	

The slave isoSPI port never transmits long (CSB) pulses. Furthermore, a slave isoSPI port will only transmit short –1 pulses, never a +1 pulse. The master port recognizes a null response as a logic 1.

Reversible isoSPI

When the LTC6813-1 is operating with Port A configured for isoSPI, communication can be initiated from either Port A or Port B. In other words, LTC6813-1 can configure either Port A or Port B as slave or master, depending on the direction of communication. The reversible isoSPI feature permits communication from both directions in a stack of daisy-chained devices. See Figure 23 for an example schematic. Figure 24 illustrates the operation of reversible isoSPI.

OPERATION

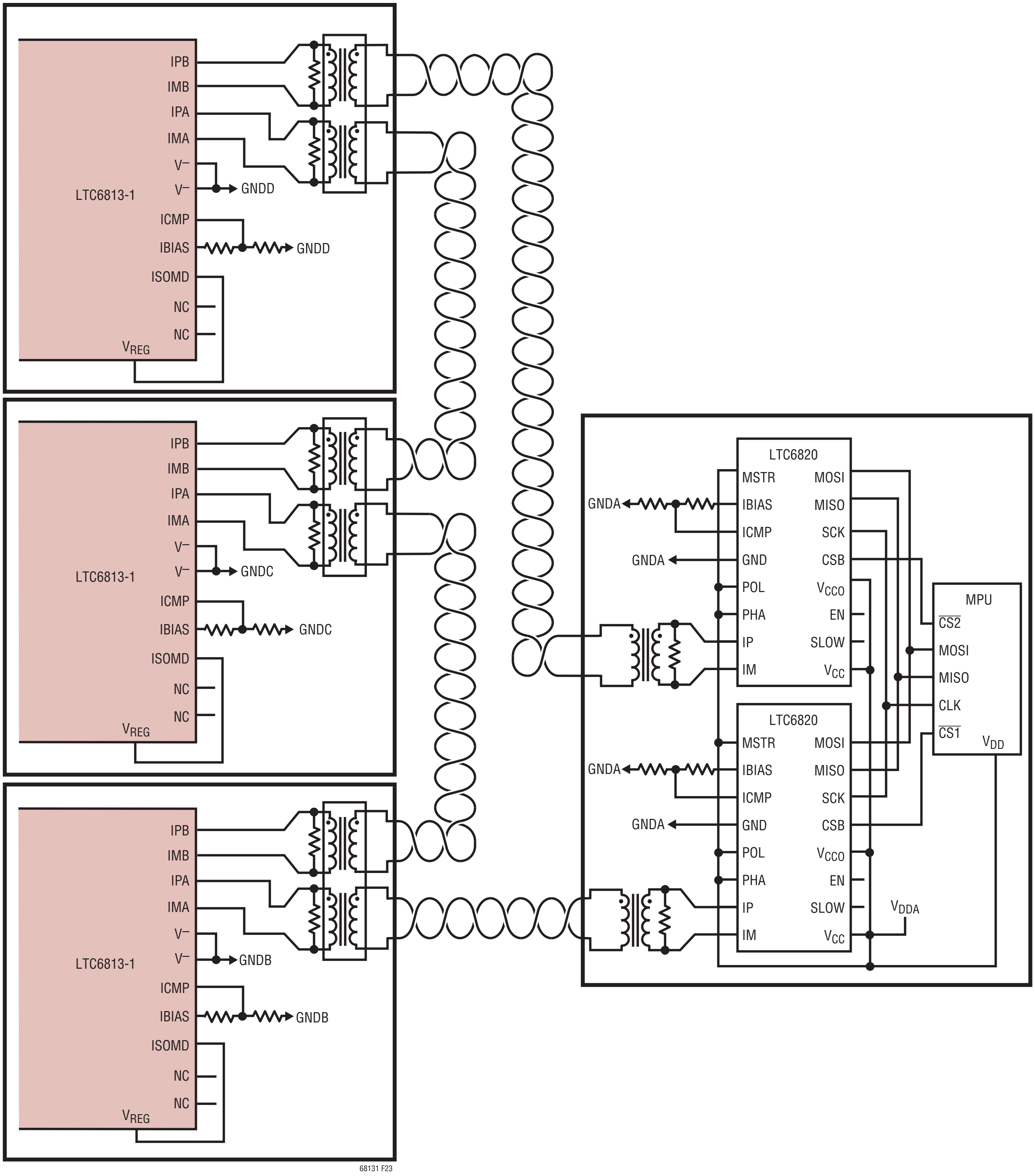


Figure 23. Reversible isoSPI Daisy Chain

OPERATION

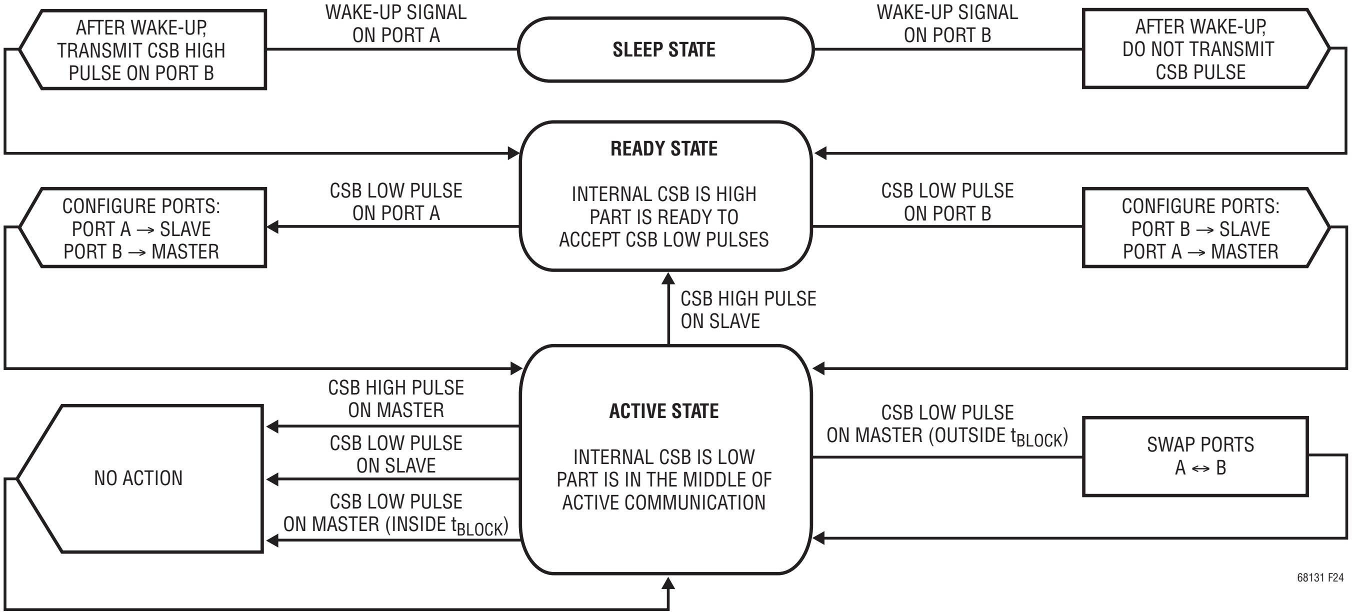


Figure 24. Reversible isoSPI State Diagram

When LTC6813-1 is in SLEEP state, it will respond to a valid WAKE-UP signal on either Port A or Port B. This is true for either configuration of the ISOMD pin.

If the WAKE-UP signal was sent on Port A, LTC6813-1 transmits a long +1 isoSPI pulse (CSB rising) on Port B after the isoSPI is powered up. If the WAKE-UP signal was sent on Port B, LTC6813-1 powers up the isoSPI but does not transmit a long +1 isoSPI pulse on Port A.

When LTC6813-1 is in READY state, communication can be initiated by sending a long –1 isoSPI pulse (CSB falling) on either Port A or Port B. The LTC6813-1 automatically configures the port that receives the long –1 isoSPI pulse as the slave and the other port is configured as the master. The isoSPI pulses are transmitted through the master port to the rest of the devices in the daisy chain.

In ACTIVE state, the LTC6813-1 is in the middle of communication and CSB of the internal SPI port is low. At the end of communication a long +1 pulse (CSB rising) on the SLAVE port returns the part to the READY state. Although it is not part of a normal communication routine, the LTC6813-1 allows ports A and B to be swapped inside the ACTIVE state. This feature is useful for the master controller to reclaim control of the slave port of LTC6813-1 irrespective of the current state of the ports. This can be done by sending a long –1 isoSPI pulse on the master port after a time delay of t_{BLOCK} from the last isoSPI signal that was transmitted by the part. Any long isoSPI pulse sent to the master port inside t_{BLOCK} is rejected by the part. This ensures the LTC6813-1 cannot switch ports because of signal reflections from poorly terminated cables (<100m cable length).

Timing Diagrams

Figure 25 shows the isoSPI timing diagram for a READ command to daisy-chained LTC6813-1 parts. The ISOMD pin is tied to V^- on the bottom part so its Port A is configured as a SPI port (CSB, SCK, SDI and SDO). The isoSPI signals of three stacked devices are shown labeled with the port (A or B) and part number. Note that ISO B1 and ISO A2 is actually the same signal, but shown on each end of the transmission cable that connects Parts 1 and 2. Likewise, ISO B2 and ISO A3 is the same signal, but with the cable delay shown between Parts 2 and 3.

Bits W_N–W_0 refer to the 16-bit command code and the 16-bit PEC of a READ command. At the end of Bit W_0, the three parts decode the READ command and begin shifting out data, which is valid on the next rising edge

OPERATION

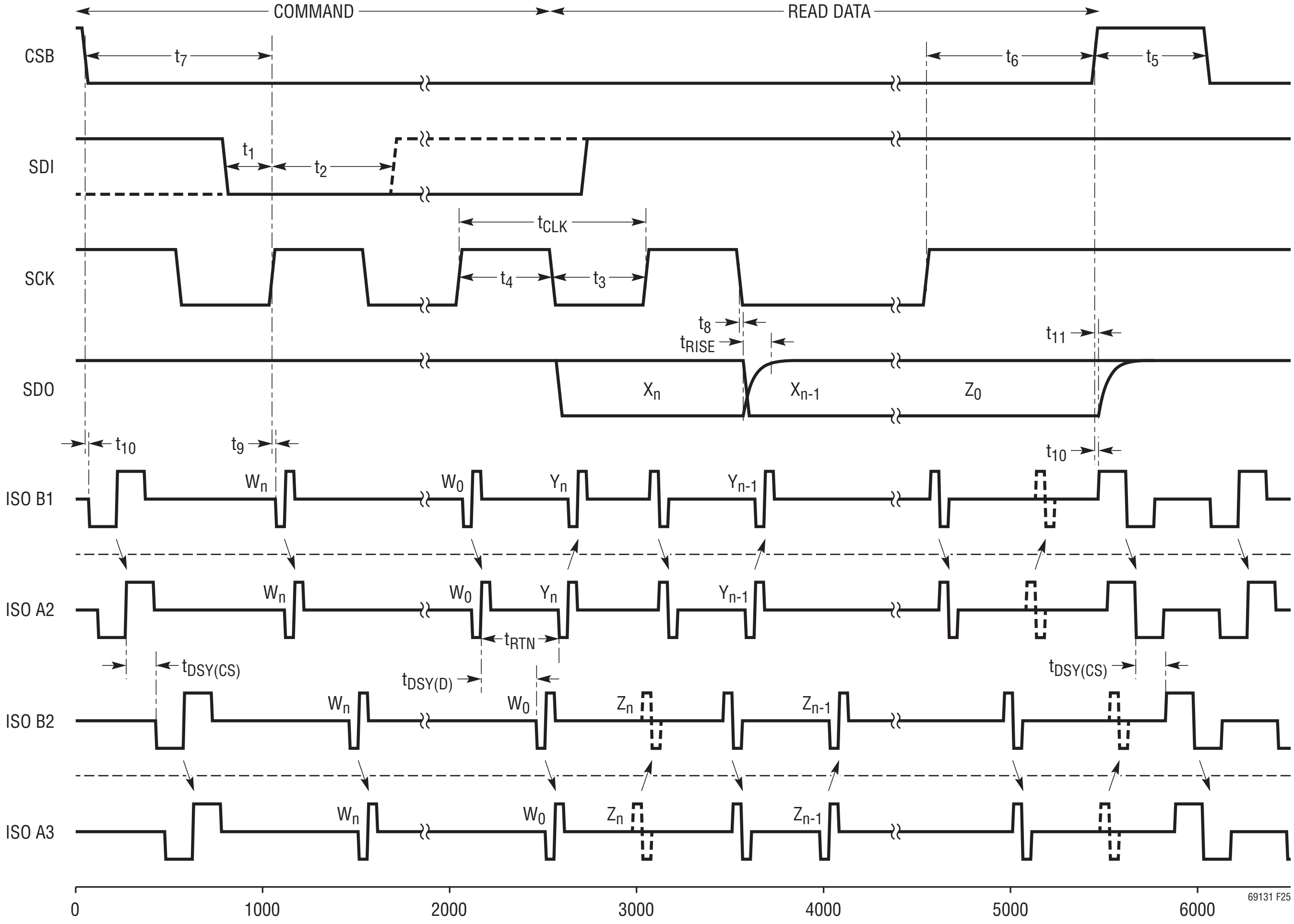


Figure 25. isoSPI Timing Diagram

OPERATION

of clock SCK. Bits X_N–X_0 refer to the data shifted out by Part 1. Bits Y_N–Y_0 refer to the data shifted out by Part 2 and bits Z_N–Z_0 refer to the data shifted out by Part 3. All this data is read back from the SDO port on Part 1 in a daisy-chained fashion.

Waking Up the Serial Interface

The serial ports (SPI or isoSPI) will enter the low power IDLE state if there is no activity on Port A or Port B for a time of t_{IDLE}. The WAKE-UP circuit monitors activity on pins 61 through 64.

If ISOMD = V^-, Port A is in SPI mode. Activity on the CSB or SCK pin will wake up the SPI interface. If ISOMD = V_{REG}, Port A is in isoSPI mode. Differential activity on IPA–IMA (or IPB–IMB) wakes up the isoSPI interface. The LTC6813-1 will be ready to communicate when the isoSPI state changes to READY within t_{WAKE} or t_{READY}, depending on the Core state (see Figure 1 and state descriptions for details).

Figure 26 illustrates the timing and the functionally equivalent circuit (only Port A shown). Common mode signals will not wake up the serial interface. The interface is designed to wake up after receiving a large signal single-ended pulse, or a low-amplitude symmetric pulse. The differential signal |SCK(IPA) – CSB(IMA)|, must be at least V_{WAKE} = 200mV for a minimum duration of t_{DWELL} = 240ns to qualify as a WAKE-UP signal that powers up the serial interface.

Waking a Daisy Chain—Method 1

The LTC6813-1 sends a long +1 pulse on Port B after it is ready to communicate. In a daisy-chained configuration, this pulse wakes up the next device in the stack which will, in turn, wake up the next device. If there are ‘N’ devices in the stack, all the devices are powered up within the time $N \bullet t_{WAKE}$ or $N \bullet t_{READY}$, depending on the Core state. For large stacks, the time $N \bullet t_{WAKE}$ may be equal to or larger than t_{IDLE}. In this case, after waiting longer than the time of $N \bullet t_{WAKE}$, the host may send another dummy byte and wait for the time $N \bullet t_{READY}$, in order to ensure that all devices are in the READY state.

Method 1 can be used when all devices on the daisy chain are in the IDLE state. This guarantees that they propagate the WAKE-UP signal up the daisy chain. However, this method will fail to wake up all devices when a device in the middle of the chain is in the READY state instead of IDLE. When this happens, the device in READY state will not propagate the wake-up pulse, so the devices above it will remain IDLE. This situation can occur when attempting to wake up the daisy chain after only t_{IDLE} of idle time (some devices may be IDLE, some may not).

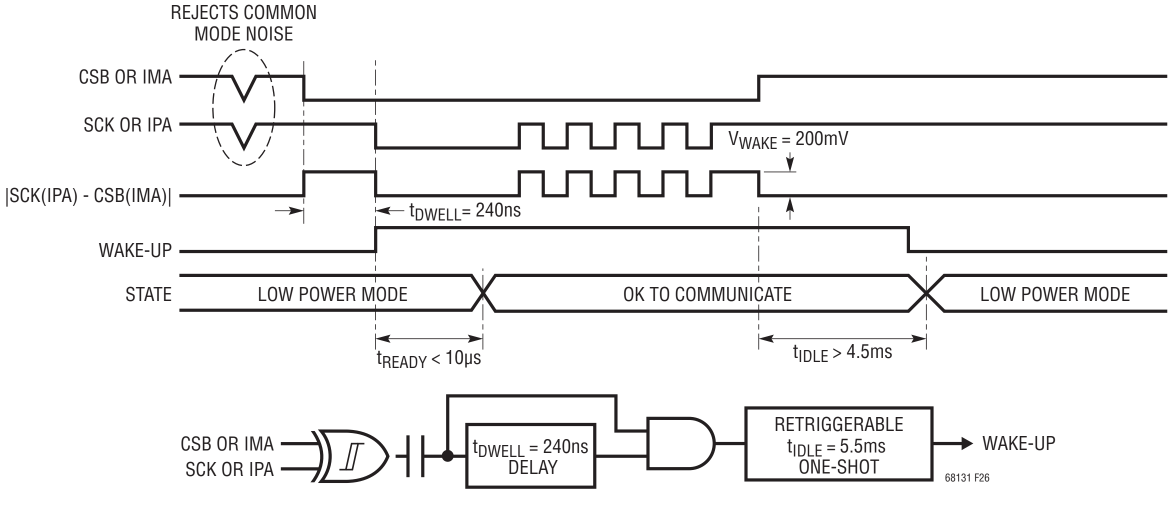


Figure 26. Wake-Up Detection and IDLE Timer

OPERATION

Waking a Daisy Chain—Method 2

A more robust wake-up method does not rely on the built-in wake-up pulse, but manually sends isoSPI traffic for enough time to wake the entire daisy chain. At minimum, a pair of long isoSPI pulses (–1 and +1) is needed for each device, separated by more than t_{READY} or t_{WAKE} (if the Core state is STANDBY or SLEEP, respectively), but less than t_{IDLE}. This allows each device to wake up and propagate the next pulse to the following device. This method works even if some devices in the chain are not in the IDLE state. In practice, implementing method 2 requires toggling the CSB pin (of the LTC6820, or bottom LTC6813-1 with ISOMD = 0) to generate the long isoSPI pulses. Alternatively, dummy commands (such as RDCFGA) can be executed to generate the long isoSPI pulses.

DATA LINK LAYER

All data transfers on LTC6813-1 occur in byte groups. Every byte consists of 8 bits. Bytes are transferred with the most significant bit (MSB) first. CSB must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. On a write command, data is latched in on the rising edge of CSB.

NETWORK LAYER

Packet Error Code

The Packet Error Code (PEC) is a 15-bit cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC value of 000000000010000 and the following characteristic polynomial: $x^{15} + x^{14} + x^{10} + x^{8} + x^{7} + x^{4} + x^{3} + 1$. To calculate the 15-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 000000000010000 (PEC is a 15-bit register group).
2. For each bit DIN coming into the PEC register group, set:
   IN0 = DIN XOR PEC[14]
   IN3 = IN0 XOR PEC[2]
   IN4 = IN0 XOR PEC[3]
   IN7 = IN0 XOR PEC[6]
   IN8 = IN0 XOR PEC[7]
   IN10 = IN0 XOR PEC[9]
   IN14 = IN0 XOR PEC[13]
3. Update the 15-bit PEC as follows:

   PEC[14] = IN14
   PEC[13] = PEC[12]
   PEC[12] = PEC[11]
   PEC[11] = PEC[10]
   PEC[10] = IN10
   PEC[9] = PEC[8]
   PEC[8] = IN8
   PEC[7] = IN7
   PEC[6] = PEC[5]
   PEC[5] = PEC[4]
   PEC[4] = IN4
   PEC[3] = IN3
   PEC[2] = PEC[1]
   PEC[1] = PEC[0]
   PEC[0] = IN0
4. Go back to step 2 until all the data is shifted. The final PEC (16 bits) is the 15-bit value in the PEC register with a 0 bit appended to its LSB.

Figure 27 illustrates the algorithm described above. An example to calculate the PEC for a 16-bit word (0x0001) is listed in Table 29. The PEC for 0x0001 is computed as 0x3D6E after stuffing a 0 bit at the LSB. For longer data streams, the PEC is valid at the end of the last bit of data sent to the PEC register.

LTC6813-1 calculates PEC for any command or data received and compares it with the PEC following the command or data. The command or data is regarded as valid only if the PEC matches. LTC6813-1 also attaches the calculated PEC at the end of the data it shifts out. Table 30 shows the format of PEC while writing to or reading from LTC6813-1.

OPERATION

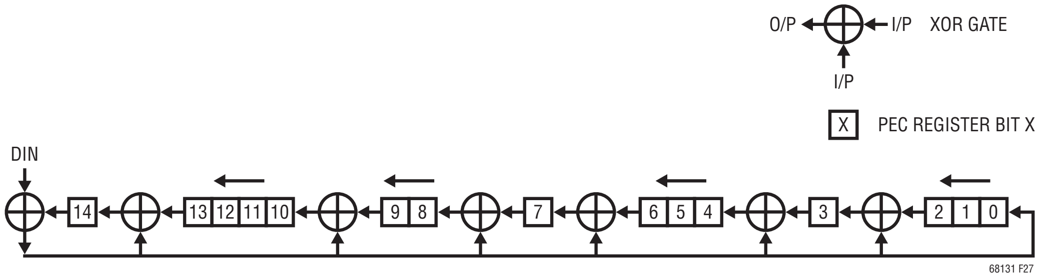


Figure 27. 15-Bit PEC Computation Circuit

Table 29. PEC Calculation for 0x0001

PEC[14]	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	**0**
PEC[13]	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	**0**
PEC[12]	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	**1**
PEC[11]	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	**1**
PEC[10]	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	**1**
PEC[9]	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[8]	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	**0**
PEC[7]	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1	**1**
PEC[6]	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**0**
PEC[5]	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[4]	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	**1**
PEC[3]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	**0**
PEC[2]	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	**1**
PEC[1]	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	**1**
PEC[0]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	**1**
IN14	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0		**0**
IN10	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1		**PEC Word**
IN8	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0		
IN7	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1		
IN4	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1		
IN3	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0		
IN0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1		
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
Clock Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Table 30. Write/Read PEC Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PEC0	RD/WR	PEC[14]	PEC[13]	PEC[12]	PEC[11]	PEC[10]	PEC[9]	PEC[8]	PEC[7]
PEC1	RD/WR	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	0

Rev. A

OPERATION

While writing any command to LTC6813-1, the command bytes CMD0 and CMD1 (see Table 37 and Table 38) and the PEC bytes PEC0 and PEC1 are sent on Port A in the following order:

CMD0, CMD1, PEC0, PEC1

After a write command to daisy-chained LTC6813-1 devices, data is sent to each device followed by the PEC. For example, when writing Configuration Register Group A to two daisy-chained devices (primary device P, stacked device S), the data will be sent to the primary device on Port A in the following order:

CFGAR0(S), … , CFGAR5(S), PEC0(S), PEC1(S),
CFGAR0(P), … , CFGAR5(P), PEC0(P), PEC1(P)

After a read command for daisy-chained devices, each device shifts out its data and the PEC that it computed for its data on Port A followed by the data received on Port B. For example, when reading Status Register Group B from two daisy-chained devices (primary device P, stacked device S), the primary device sends out data on port A in the following order:

STBR0(P), … , STBR5(P), PEC0(P), PEC1(P),
STBR0(S), … , STBR5(S), PEC0(S), PEC1(S)

See Bus Protocols for command format.

All devices in a daisy-chained configuration receive the command bytes simultaneously. For example, to initiate ADC conversions in a stack of devices, a single ADCV command is sent, and all devices will start conversions at the same time. For read and write commands, a single command is sent, and then the stacked devices effectively turn into a cascaded shift register, in which data is shifted through each device to the next higher (on a write) or the next lower (on a read) device in the stack. See the Serial Interface Overview section.

Polling Methods

The simplest method to determine ADC completion is for the controller to start an ADC conversion and wait for the specified conversion time to pass before reading the results.

If using a single LTC6813-1 that communicates in SPI mode (ISOMD pin tied low), there are two methods of polling. The first method is to hold CSB low after an ADC conversion command is sent. After entering a conversion command, the SDO line is driven low when the device is busy performing conversions. SDO is pulled high when the device completes conversions. However, SDO will also go back high when CSB goes high even if the device has not completed the conversion (Figure 28). A problem with this method is that the controller is not free to do other serial communication while waiting for ADC conversions to complete.

The next method overcomes this limitation. The controller can send an ADC start command, perform other tasks, and then send a poll ADC converter status (PLADC) command to determine the status of the ADC conversions (Figure 29). After entering the PLADC command, SDO will go low if the device is busy performing conversions. SDO is pulled high at the end of conversions. However, SDO will also go high when CSB goes high even if the device has not completed the conversion.

If using a single LTC6813-1 that communicates in isoSPI mode, the low side port transmits a data pulse only in response to a master isoSPI pulse received by it. So, after entering the command in either method of polling described above, isoSPI data pulses are sent to the part to update the conversion status. These pulses can be sent using LTC6820 by simply clocking its SCK pin. In response to this pulse, the LTC6813-1 sends back a low isoSPI pulse if it is still busy performing conversions or a high data pulse if it has completed the conversions. If a CSB high isoSPI pulse is sent to the device, it exits the polling command.

In a daisy-chained configuration of N stacked devices, the same two polling methods can be used. If the bottom device communicates in SPI mode, the SDO of the bottom device indicates the conversion status of the entire stack. i.e., SDO will remain low until all the devices in the stack have completed the conversions. In the first method of polling, after an ADC conversion command is sent, clock pulses are sent on SCK while keeping CSB low. The SDO status becomes valid only at the end of N clock pulses on SCK. During the first N clock pulses, the bottom LTC6813-1 in the daisy chain will output a 0 or a low data pulse. After N clock pulses, the output data from the bottom LTC6813-1 gets updated for every clock pulse

OPERATION

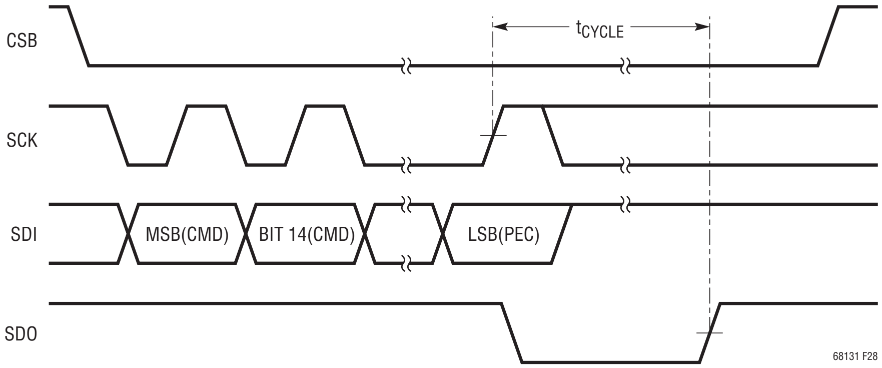


Figure 28. SDO Polling After an ADC Conversion Command (Single LTC6813-1)

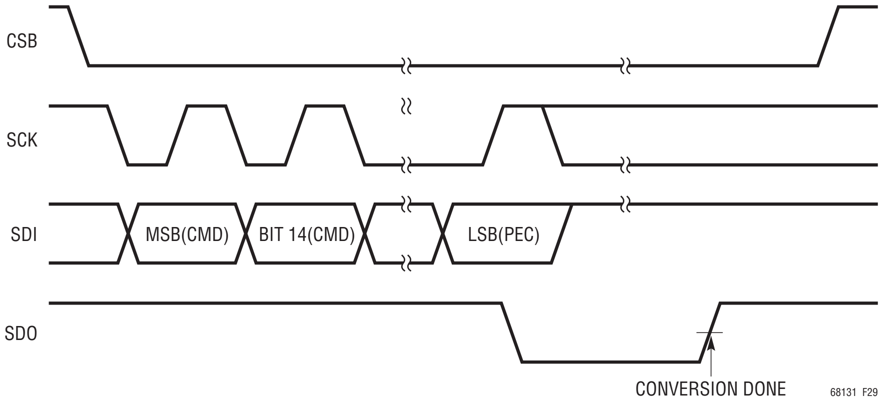


Figure 29. SDO Polling Using PLADC Command (Single LTC6813-1)

OPERATION

that follows (Figure 30). In the second method, the PLADC command is sent followed by clock pulses on SCK while keeping CSB low. Similar to the first method, the SDO status is valid only after N clock cycles on SCK and gets updated after every clock cycle that follows (Figure 31).

If the bottom device communicates in isoSPI mode, isoSPI data pulses are sent to the device to update the conversion status. Using LTC6820, this can be achieved by just clocking its SCK pin. The conversion status is valid only after the bottom LTC6813-1 device receives N isoSPI data pulses and the status gets updated for every isoSPI data pulse that follows. The device returns a low data pulse if any of the devices in the stack is busy performing conversions and returns a high data pulse if all the devices are free.

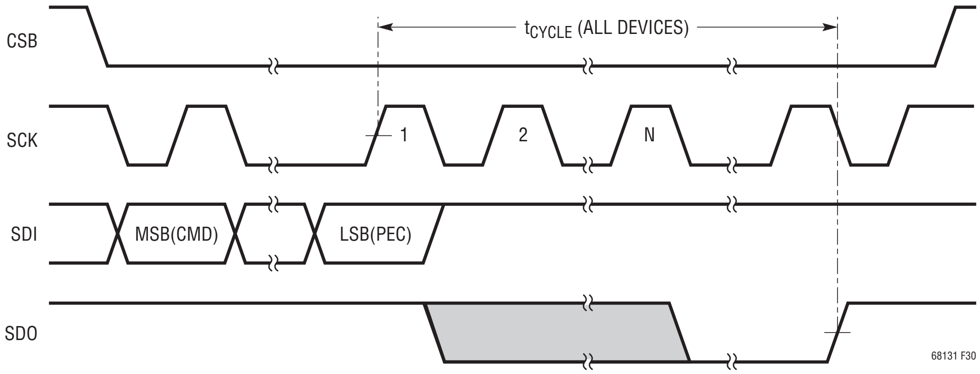


Figure 30. SDO Polling After an ADC Conversion Command (Daisy-Chain Configuration)

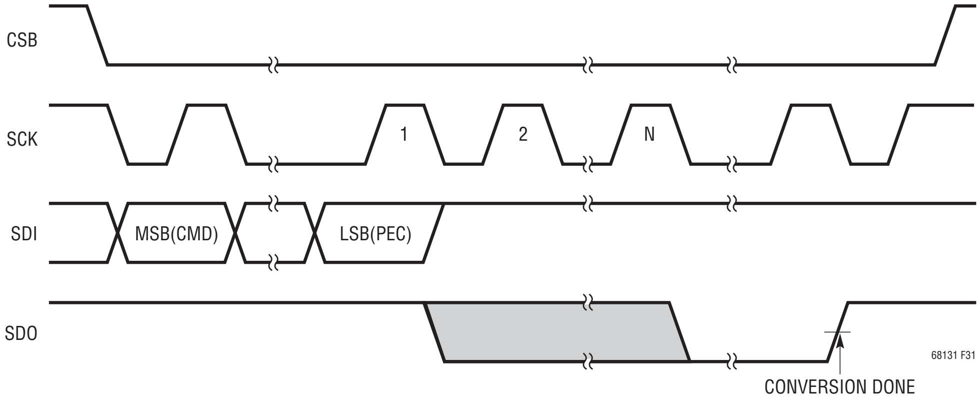


Figure 31. SDO Polling Using PLADC Command (Daisy-Chain Configuration)

Bus Protocols

Protocol Format: The protocol formats for commands are depicted in Tables 32 through 34. Table 31 is the key for reading the protocol diagrams.

Table 31. Protocol Key

CMD0	Command Byte 0 (See Table 35)
CMD1	Command Byte 1 (See Table 35)
PEC0	Packet Error Code Byte 0 (See Table 30)
PEC1	Packet Error Code Byte 1 (See Table 30)
n	Number of Bytes
…	Continuation of Protocol
	Master to Slave
▨	Slave to Master

Table 32. Poll Command

8	8	8	8	
CMD0	CMD1	PEC0	PEC1	Poll Data

Table 33. Write Command

8	8	8	8	8		8	8	8	8		8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1	Shift Byte 1	…	Shift Byte n

Table 34. Read Command

8	8	8	8	8		8	8	8	8		8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1	Shift Byte 1	…	Shift Byte n

Command Format: The format for the commands is shown in Table 35. CC[10:0] is the 11-bit command code. A list of all the command codes is shown in Table 36. All commands have a value 0 for CMD0[7] through CMD0[3]. The PEC must be computed on the entire 16-bit command (CMD0 and CMD1).

Table 35. Command Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	WR	0	0	0	0	0	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

OPERATION

Commands

Table 36 lists all the commands and their options.

Table 36. Command Codes

COMMAND DESCRIPTION	NAME	CC[10:0] – COMMAND CODE										
		10	9	8	7	6	5	4	3	2	1	0
Write Configuration Register Group A	WRCFGA	0	0	0	0	0	0	0	0	0	0	1
Write Configuration Register Group B	WRCFGB	0	0	0	0	0	1	0	0	1	0	0
Read Configuration Register Group A	RDCFGA	0	0	0	0	0	0	0	0	0	1	0
Read Configuration Register Group B	RDCFGB	0	0	0	0	0	1	0	0	1	1	0
Read Cell Voltage Register Group A	RDCVA	0	0	0	0	0	0	0	0	1	0	0
Read Cell Voltage Register Group B	RDCVB	0	0	0	0	0	0	0	0	1	1	0
Read Cell Voltage Register Group C	RDCVC	0	0	0	0	0	0	0	1	0	0	0
Read Cell Voltage Register Group D	RDCVD	0	0	0	0	0	0	0	1	0	1	0
Read Cell Voltage Register Group E	RDCVE	0	0	0	0	0	0	0	1	0	0	1
Read Cell Voltage Register Group F	RDCVF	0	0	0	0	0	0	0	1	0	1	1
Read Auxiliary Register Group A	RDAUXA	0	0	0	0	0	0	0	1	1	0	0
Read Auxiliary Register Group B	RDAUXB	0	0	0	0	0	0	0	1	1	1	0
Read Auxiliary Register Group C	RDAUXC	0	0	0	0	0	0	0	1	1	0	1
Read Auxiliary Register Group D	RDAUXD	0	0	0	0	0	0	0	1	1	1	1
Read Status Register Group A	RDSTATA	0	0	0	0	0	0	1	0	0	0	0
Read Status Register Group B	RDSTATB	0	0	0	0	0	0	1	0	0	1	0
Write S Control Register Group	WRSCTRL	0	0	0	0	0	0	1	0	1	0	0
Write PWM Register Group	WRPWM	0	0	0	0	0	1	0	0	0	0	0
Write PWM/S Control Register Group B	WRPSB	0	0	0	0	0	0	1	1	1	0	0
Read S Control Register Group	RDSCTRL	0	0	0	0	0	0	1	0	1	1	0
Read PWM Register Group	RDPWM	0	0	0	0	0	1	0	0	0	1	0
Read PWM/S Control Register Group B	RDPSB	0	0	0	0	0	0	1	1	1	1	0

OPERATION

COMMAND DESCRIPTION	NAME	CC[10:0] – COMMAND CODE										
		10	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Start S Control Pulsing and Poll Status	STSCTRL	0	0	0	0	0	0	1	1	0	0	1
Clear S Control Register Group	CLRSCTRL	0	0	0	0	0	0	1	1	0	0	0
Start Cell Voltage ADC Conversion and Poll Status	ADCV	0	1	MD[1]	MD[0]	1	1	DCP	0	CH[2]	CH[1]	CH[0]
Start Open Wire ADC Conversion and Poll Status	ADOW	0	1	MD[1]	MD[0]	PUP	1	DCP	1	CH[2]	CH[1]	CH[0]
Start Self Test Cell Voltage Conversion and Poll Status	CVST	0	1	MD[1]	MD[0]	ST[1]	ST[0]	0	0	1	1	1
Start Overlap Measurements of Cell 7 and Cell 13 Voltages	ADOL	0	1	MD[1]	MD[0]	0	0	DCP	0	0	0	1
Start GPIOs ADC Conversion and Poll Status	ADAX	1	0	MD[1]	MD[0]	1	1	0	0	CHG[2]	CHG[1]	CHG[0]
Start GPIOs ADC Conversion with Digital Redundancy and Poll Status	ADAXD	1	0	MD[1]	MD[0]	0	0	0	0	CHG[2]	CHG[1]	CHG[0]
Start GPIOs Open Wire ADC Conversion and Poll Status	AXOW	1	0	MD[1]	MD[0]	PUP	0	1	0	CHG[2]	CHG[1]	CHG[0]
Start Self Test GPIOs Conversion and Poll Status	AXST	1	0	MD[1]	MD[0]	ST[1]	ST[0]	0	0	1	1	1
Start Status Group ADC Conversion and Poll Status	ADSTAT	1	0	MD[1]	MD[0]	1	1	0	1	CHST[2]	CHST[1]	CHST[0]
Start Status Group ADC Conversion with Digital Redundancy and Poll Status	ADSTATD	1	0	MD[1]	MD[0]	0	0	0	1	CHST[2]	CHST[1]	CHST[0]
Start Self Test Status Group Conversion and Poll Status	STATST	1	0	MD[1]	MD[0]	ST[1]	ST[0]	0	1	1	1	1
Start Combined Cell Voltage and GPIO1, GPIO2 Conversion and Poll Status	ADCVAX	1	0	MD[1]	MD[0]	1	1	DCP	1	1	1	1
Start Combined Cell Voltage and SC Conversion and Poll Status	ADCVSC	1	0	MD[1]	MD[0]	1	1	DCP	0	1	1	1
Clear Cell Voltage Register Groups	CLRCELL	1	1	1	0	0	0	1	0	0	0	1
Clear Auxiliary Register Groups	CLRAUX	1	1	1	0	0	0	1	0	0	1	0
Clear Status Register Groups	CLRSTAT	1	1	1	0	0	0	1	0	0	1	1
Poll ADC Conversion Status	PLADC	1	1	1	0	0	0	1	0	1	0	0
Diagnose MUX and Poll Status	DIAGN	1	1	1	0	0	0	1	0	1	0	1
Write COMM Register Group	WRCOMM	1	1	1	0	0	1	0	0	0	0	1
Read COMM Register Group	RDCOMM	1	1	1	0	0	1	0	0	0	1	0
Start I^{2}C/SPI Communication	STCOMM	1	1	1	0	0	1	0	0	0	1	1
Mute Discharge	MUTE	0	0	0	0	0	1	0	1	0	0	0
Unmute Discharge	UNMUTE	0	0	0	0	0	1	0	1	0	0	1

OPERATION

Table 37. Command Bit Descriptions

<table>
<tr><th>NAME</th><th>DESCRIPTION</th><th colspan="10">VALUES</th></tr>
<tr><td rowspan="5">MD[1:0]</td><td rowspan="5">ADC Mode</td><td>MD</td><td colspan="3">ADCOPT(CFGAR0[0]) = 0</td><td colspan="6">ADCOPT(CFGAR0[0]) = 1</td></tr>
<tr><td>00</td><td colspan="3">422Hz Mode</td><td colspan="6">1kHz Mode</td></tr>
<tr><td>01</td><td colspan="3">27kHz Mode (Fast)</td><td colspan="6">14kHz Mode</td></tr>
<tr><td>10</td><td colspan="3">7kHz Mode (Normal)</td><td colspan="6">3kHz Mode</td></tr>
<tr><td>11</td><td colspan="3">26Hz Mode (Filtered)</td><td colspan="6">2kHz Mode</td></tr>
<tr><td rowspan="3">DCP</td><td rowspan="3">Discharge Permitted</td><td>DCP</td><td colspan="9"></td></tr>
<tr><td>0</td><td colspan="9">Discharge Not Permitted</td></tr>
<tr><td>1</td><td colspan="9">Discharge Permitted</td></tr>
<tr><td rowspan="9">CH[2:0]</td><td rowspan="9">Cell Selection for ADC Conversion</td><td colspan="2"></td><td colspan="8">Total Conversion Time in the 8 ADC Modes</td></tr>
<tr><td>CH</td><td></td><td>27kHz</td><td>14kHz</td><td>7kHz</td><td>3kHz</td><td>2kHz</td><td>1kHz</td><td>422Hz</td><td>26Hz</td></tr>
<tr><td>000</td><td>All Cells</td><td>1.1ms</td><td>1.3ms</td><td>2.3ms</td><td>3.0ms</td><td>4.4ms</td><td>7.2ms</td><td>12.8ms</td><td>201ms</td></tr>
<tr><td>001</td><td>Cells 1, 7, 13</td><td rowspan="6">203µs</td><td rowspan="6">232µs</td><td rowspan="6">407µs</td><td rowspan="6">523µs</td><td rowspan="6">756µs</td><td rowspan="6">1.2ms</td><td rowspan="6">2.2ms</td><td rowspan="6">34ms</td></tr>
<tr><td>010</td><td>Cells 2, 8, 14</td></tr>
<tr><td>011</td><td>Cells 3, 9, 15</td></tr>
<tr><td>100</td><td>Cells 4, 10, 16</td></tr>
<tr><td>101</td><td>Cells 5, 11, 17</td></tr>
<tr><td>110</td><td>Cells 6, 12, 18</td></tr>
<tr><td rowspan="3">PUP</td><td rowspan="3">Pull-Up/Pull-Down Current for Open Wire Conversions</td><td colspan="10">PUP</td></tr>
<tr><td>0</td><td colspan="9">Pull-Down Current</td></tr>
<tr><td>1</td><td colspan="9">Pull-Up Current</td></tr>
<tr><td rowspan="4">ST[1:0]</td><td rowspan="4">Self Test Mode Selection</td><td colspan="2"></td><td colspan="8">Self Test Conversion Result</td></tr>
<tr><td>ST</td><td></td><td>27kHz</td><td>14kHz</td><td>7kHz</td><td>3kHz</td><td>2kHz</td><td>1kHz</td><td>422Hz</td><td>26Hz</td></tr>
<tr><td>01</td><td>Self Test 1</td><td>0x9565</td><td>0x9553</td><td>0x9555</td><td>0x9555</td><td>0x9555</td><td>0x9555</td><td>0x9555</td><td>0x9555</td></tr>
<tr><td>10</td><td>Self test 2</td><td>0x6A9A</td><td>0x6AAC</td><td>0x6AAA</td><td>0x6AAA</td><td>0x6AAA</td><td>0x6AAA</td><td>0x6AAA</td><td>0x6AAA</td></tr>
<tr><td rowspan="9">CHG[2:0]</td><td rowspan="9">GPIO Selection for ADC Conversion</td><td colspan="2"></td><td colspan="8">Total Conversion Time in the 8 ADC Modes</td></tr>
<tr><td>CHG</td><td></td><td>27kHz</td><td>14kHz</td><td>7kHz</td><td>3kHz</td><td>2kHz</td><td>1kHz</td><td>422Hz</td><td>26Hz</td></tr>
<tr><td>000</td><td>GPIO 1–5, 2nd Reference, GPIO 6–9</td><td>1.8ms</td><td>2.1ms</td><td>3.9ms</td><td>5.0ms</td><td>7.4ms</td><td>12.0ms</td><td>21.3ms</td><td>335ms</td></tr>
<tr><td>001</td><td>GPIO 1 and GPIO 6</td><td rowspan="4">380µs</td><td rowspan="4">439µs</td><td rowspan="4">788µs</td><td rowspan="4">1.0ms</td><td rowspan="4">1.5ms</td><td rowspan="4">2.4ms</td><td rowspan="4">4.3ms</td><td rowspan="4">67.1ms</td></tr>
<tr><td>010</td><td>GPIO 2 and GPIO 7</td></tr>
<tr><td>011</td><td>GPIO 3 and GPIO 8</td></tr>
<tr><td>100</td><td>GPIO 4 and GPIO 9</td></tr>
<tr><td>101</td><td>GPIO 5</td><td rowspan="2">200µs</td><td rowspan="2">229µs</td><td rowspan="2">403µs</td><td rowspan="2">520µs</td><td rowspan="2">753µs</td><td rowspan="2">1.2ms</td><td rowspan="2">2.1ms</td><td rowspan="2">34ms</td></tr>
<tr><td>110</td><td>2nd Reference</td></tr>
<tr><td rowspan="7">CHST[2:0]*</td><td rowspan="7">Status Group Selection</td><td colspan="2"></td><td colspan="8">Total Conversion Time in the 8 ADC Modes</td></tr>
<tr><td>CHST</td><td></td><td>27kHz</td><td>14kHz</td><td>7kHz</td><td>3kHz</td><td>2kHz</td><td>1kHz</td><td>422Hz</td><td>26Hz</td></tr>
<tr><td>000</td><td>SC, ITMP, VA, VD</td><td>742µs</td><td>858µs</td><td>1.6ms</td><td>2.0ms</td><td>3.0ms</td><td>4.8ms</td><td>8.5ms</td><td>134ms</td></tr>
<tr><td>001</td><td>SC</td><td rowspan="4">200µs</td><td rowspan="4">229µs</td><td rowspan="4">403µs</td><td rowspan="4">520µs</td><td rowspan="4">753µs</td><td rowspan="4">1.2ms</td><td rowspan="4">2.1ms</td><td rowspan="4">34ms</td></tr>
<tr><td>010</td><td>ITMP</td></tr>
<tr><td>011</td><td>VA</td></tr>
<tr><td>100</td><td>VD</td></tr>
</table>

*Note: Valid options for CHST in ADSTAT command are 0–4. If CHST is set to 5/6 in ADSTAT command, the LTC6813-1 ignores the command.

OPERATION

Memory Map

Table 38. Configuration Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGAR0	RD/WR	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	REFON	DTEN	ADCOPT
CFGAR1	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGAR2	RD/WR	VOV[3]	VOV[2]	VOV[1]	VOV[0]	VUV[11]	VUV[10]	VUV[9]	VUV[8]
CFGAR3	RD/WR	VOV[11]	VOV[10]	VOV[9]	VOV[8]	VOV[7]	VOV[6]	VOV[5]	VOV[4]
CFGAR4	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGAR5	RD/WR	DCTO[3]	DCTO[2]	DCTO[1]	DCTO[0]	DCC12	DCC11	DCC10	DCC9

Table 39. Configuration Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGBR0	RD/WR	DCC16	DCC15	DCC14	DCC13	GPIO9	GPIO8	GPIO7	GPIO6
CFGBR1	RD/WR	MUTE	FDRF	PS[1]	PS[0]	DTMEN	DCC0	DCC18	DCC17
CFGBR2	RD/WR	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR3	RD/WR	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR4	RD/WR	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0
CFGBR5	RD/WR	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0	RSVD0

Table 40. Cell Voltage Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVAR0	RD	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVAR1	RD	C1V[15]	C1V[14]	C1V[13]	C1V[12]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVAR2	RD	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
CVAR3	RD	C2V[15]	C2V[14]	C2V[13]	C2V[12]	C2V[11]	C2V[10]	C2V[9]	C2V[8]
CVAR4	RD	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVAR5	RD	C3V[15]	C3V[14]	C3V[13]	C3V[12]	C3V[11]	C3V[10]	C3V[9]	C3V[8]

Table 41. Cell Voltage Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVBR0	RD	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]
CVBR1	RD	C4V[15]	C4V[14]	C4V[13]	C4V[12]	C4V[11]	C4V[10]	C4V[9]	C4V[8]
CVBR2	RD	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVBR3	RD	C5V[15]	C5V[14]	C5V[13]	C5V[12]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVBR4	RD	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]
CVBR5	RD	C6V[15]	C6V[14]	C6V[13]	C6V[12]	C6V[11]	C6V[10]	C6V[9]	C6V[8]

OPERATION

Table 42. Cell Voltage Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVCR0	RD	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVCR1	RD	C7V[15]	C7V[14]	C7V[13]	C7V[12]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVCR2*	RD	C8V[7]*	C8V[6]*	C8V[5]*	C8V[4]*	C8V[3]*	C8V[2]*	C8V[1]*	C8V[0]*
CVCR3*	RD	C8V[15]*	C8V[14]*	C8V[13]*	C8V[12]*	C8V[11]*	C8V[10]*	C8V[9]*	C8V[8]*
CVCR4	RD	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVCR5	RD	C9V[15]	C9V[14]	C9V[13]	C9V[12]	C9V[11]	C9V[10]	C9V[9]	C9V[8]

*After performing the ADOL command, CVCR2 and CVCR3 of Cell Voltage Register Group C will contain the result of measuring Cell 7 from ADC1.

Table 43. Cell Voltage Register Group D

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVDR0	RD	C10V[7]	C10V[6]	C10V[5]	C10V[4]	C10V[3]	C10V[2]	C10V[1]	C10V[0]
CVDR1	RD	C10V[15]	C10V[14]	C10V[13]	C10V[12]	C10V[11]	C10V[10]	C10V[9]	C10V[8]
CVDR2	RD	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVDR3	RD	C11V[15]	C11V[14]	C11V[13]	C11V[12]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVDR4	RD	C12V[7]	C12V[6]	C12V[5]	C12V[4]	C12V[3]	C12V[2]	C12V[1]	C12V[0]
CVDR5	RD	C12V[15]	C12V[14]	C12V[13]	C12V[12]	C12V[11]	C12V[10]	C12V[9]	C12V[8]

Table 44. Cell Voltage Register Group E

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVER0	RD	C13V[7]	C13V[6]	C13V[5]	C13V[4]	C13V[3]	C13V[2]	C13V[1]	C13V[0]
CVER1	RD	C13V[15]	C13V[14]	C13V[13]	C13V[12]	C13V[11]	C13V[10]	C13V[9]	C13V[8]
CVER2*	RD	C14V[7]*	C14V[6]*	C14V[5]*	C14V[4]*	C14V[3]*	C14V[2]*	C14V[1]*	C14V[0]*
CVER3*	RD	C14V[15]*	C14V[14]*	C14V[13]*	C14V[12]*	C14V[11]*	C14V[10]*	C14V[9]*	C14V[8]*
CVER4	RD	C15V[7]	C15V[6]	C15V[5]	C15V[4]	C15V[3]	C15V[2]	C15V[1]	C15V[0]
CVER5	RD	C15V[15]	C15V[14]	C15V[13]	C15V[12]	C15V[11]	C15V[10]	C15V[9]	C15V[8]

*After performing the ADOL command, CVER2 and CVER3 of Cell Voltage Register Group E will contain the result of measuring Cell 13 from ADC2.

Table 45. Cell Voltage Register Group F

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVFR0	RD	C16V[7]	C16V[6]	C16V[5]	C16V[4]	C16V[3]	C16V[2]	C16V[1]	C16V[0]
CVFR1	RD	C16V[15]	C16V[14]	C16V[13]	C16V[12]	C16V[11]	C16V[10]	C16V[9]	C16V[8]
CVFR2	RD	C17V[7]	C17V[6]	C17V[5]	C17V[4]	C17V[3]	C17V[2]	C17V[1]	C17V[0]
CVFR3	RD	C17V[15]	C17V[14]	C17V[13]	C17V[12]	C17V[11]	C17V[10]	C17V[9]	C17V[8]
CVFR4	RD	C18V[7]	C18V[6]	C18V[5]	C18V[4]	C18V[3]	C18V[2]	C18V[1]	C18V[0]
CVFR5	RD	C18V[15]	C18V[14]	C18V[13]	C18V[12]	C18V[11]	C18V[10]	C18V[9]	C18V[8]

OPERATION

Table 46. Auxiliary Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVAR0	RD	G1V[7]	G1V[6]	G1V[5]	G1V[4]	G1V[3]	G1V[2]	G1V[1]	G1V[0]
AVAR1	RD	G1V[15]	G1V[14]	G1V[13]	G1V[12]	G1V[11]	G1V[10]	G1V[9]	G1V[8]
AVAR2	RD	G2V[7]	G2V[6]	G2V[5]	G2V[4]	G2V[3]	G2V[2]	G2V[1]	G2V[0]
AVAR3	RD	G2V[15]	G2V[14]	G2V[13]	G2V[12]	G2V[11]	G2V[10]	G2V[9]	G2V[8]
AVAR4	RD	G3V[7]	G3V[6]	G3V[5]	G3V[4]	G3V[3]	G3V[2]	G3V[1]	G3V[0]
AVAR5	RD	G3V[15]	G3V[14]	G3V[13]	G3V[12]	G3V[11]	G3V[10]	G3V[9]	G3V[8]

Table 47. Auxiliary Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVBR0	RD	G4V[7]	G4V[6]	G4V[5]	G4V[4]	G4V[3]	G4V[2]	G4V[1]	G4V[0]
AVBR1	RD	G4V[15]	G4V[14]	G4V[13]	G4V[12]	G4V[11]	G4V[10]	G4V[9]	G4V[8]
AVBR2	RD	G5V[7]	G5V[6]	G5V[5]	G5V[4]	G5V[3]	G5V[2]	G5V[1]	G5V[0]
AVBR3	RD	G5V[15]	G5V[14]	G5V[13]	G5V[12]	G5V[11]	G5V[10]	G5V[9]	G5V[8]
AVBR4	RD	REF[7]	REF[6]	REF[5]	REF[4]	REF[3]	REF[2]	REF[1]	REF[0]
AVBR5	RD	REF[15]	REF[14]	REF[13]	REF[12]	REF[11]	REF[10]	REF[9]	REF[8]

Table 48. Auxiliary Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVCR0	RD	G6V[7]	G6V[6]	G6V[5]	G6V[4]	G6V[3]	G6V[2]	G6V[1]	G6V[0]
AVCR1	RD	G6V[15]	G6V[14]	G6V[13]	G6V[12]	G6V[11]	G6V[10]	G6V[9]	G6V[8]
AVCR2	RD	G7V[7]	G7V[6]	G7V[5]	G7V[4]	G7V[3]	G7V[2]	G7V[1]	G7V[0]
AVCR3	RD	G7V[15]	G7V[14]	G7V[13]	G7V[12]	G7V[11]	G7V[10]	G7V[9]	G7V[8]
AVCR4	RD	G8V[7]	G8V[6]	G8V[5]	G8V[4]	G8V[3]	G8V[2]	G8V[1]	G8V[0]
AVCR5	RD	G8V[15]	G8V[14]	G8V[13]	G8V[12]	G8V[11]	G8V[10]	G8V[9]	G8V[8]

Table 49. Auxiliary Register Group D

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVDR0	RD	G9V[7]	G9V[6]	G9V[5]	G9V[4]	G9V[3]	G9V[2]	G9V[1]	G9V[0]
AVDR1	RD	G9V[15]	G9V[14]	G9V[13]	G9V[12]	G9V[11]	G9V[10]	G9V[9]	G9V[8]
AVDR2	RD	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1
AVDR3	RD	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1	RSVD1
AVDR4	RD	C16OV	C16UV	C15OV	C15UV	C14OV	C14UV	C13OV	C13UV
AVDR5	RD	RSVD1	RSVD1	RSVD1	RSVD1	C18OV	C18UV	C17OV	C17UV

OPERATION

Table 50. Status Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STAR0	RD	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
STAR1	RD	SC[15]	SC[14]	SC[13]	SC[12]	SC[11]	SC[10]	SC[9]	SC[8]
STAR2	RD	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
STAR3	RD	ITMP[15]	ITMP[14]	ITMP[13]	ITMP[12]	ITMP[11]	ITMP[10]	ITMP[9]	ITMP[8]
STAR4	RD	VA[7]	VA[6]	VA[5]	VA[4]	VA[3]	VA[2]	VA[1]	VA[0]
STAR5	RD	VA[15]	VA[14]	VA[13]	VA[12]	VA[11]	VA[10]	VA[9]	VA[8]

Table 51. Status Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STBR0	RD	VD[7]	VD[6]	VD[5]	VD[4]	VD[3]	VD[2]	VD[1]	VD[0]
STBR1	RD	VD[15]	VD[14]	VD[13]	VD[12]	VD[11]	VD[10]	VD[9]	VD[8]
STBR2	RD	C4OV	C4UV	C3OV	C3UV	C2OV	C2UV	C1OV	C1UV
STBR3	RD	C8OV	C8UV	C7OV	C7UV	C6OV	C6UV	C5OV	C5UV
STBR4	RD	C12OV	C12UV	C11OV	C11UV	C10OV	C10UV	C9OV	C9UV
STBR5	RD	REV[3]	REV[2]	REV[1]	REV[0]	RSVD	RSVD	MUXFAIL	THSD

Table 52. COMM Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMM0	RD/WR	ICOM0[3]	ICOM0[2]	ICOM0[1]	ICOM0[0]	D0[7]	D0[6]	D0[5]	D0[4]
COMM1	RD/WR	D0[3]	D0[2]	D0[1]	D0[0]	FCOM0[3]	FCOM0[2]	FCOM0[1]	FCOM0[0]
COMM2	RD/WR	ICOM1[3]	ICOM1[2]	ICOM1[1]	ICOM1[0]	D1[7]	D1[6]	D1[5]	D1[4]
COMM3	RD/WR	D1[3]	D1[2]	D1[1]	D1[0]	FCOM1[3]	FCOM1[2]	FCOM1[1]	FCOM1[0]
COMM4	RD/WR	ICOM2[3]	ICOM2[2]	ICOM2[1]	ICOM2[0]	D2[7]	D2[6]	D2[5]	D2[4]
COMM5	RD/WR	D2[3]	D2[2]	D2[1]	D2[0]	FCOM2[3]	FCOM2[2]	FCOM2[1]	FCOM2[0]

Table 53. S Control Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SCTRL0	RD/WR	SCTL2[3]	SCTL2[2]	SCTL2[1]	SCTL2[0]	SCTL1[3]	SCTL1[2]	SCTL1[1]	SCTL1[0]
SCTRL1	RD/WR	SCTL4[3]	SCTL4[2]	SCTL4[1]	SCTL4[0]	SCTL3[3]	SCTL3[2]	SCTL3[1]	SCTL3[0]
SCTRL2	RD/WR	SCTL6[3]	SCTL6[2]	SCTL6[1]	SCTL6[0]	SCTL5[3]	SCTL5[2]	SCTL5[1]	SCTL5[0]
SCTRL3	RD/WR	SCTL8[3]	SCTL8[2]	SCTL8[1]	SCTL8[0]	SCTL7[3]	SCTL7[2]	SCTL7[1]	SCTL7[0]
SCTRL4	RD/WR	SCTL10[3]	SCTL10[2]	SCTL10[1]	SCTL10[0]	SCTL9[3]	SCTL9[2]	SCTL9[1]	SCTL9[0]
SCTRL5	RD/WR	SCTL12[3]	SCTL12[2]	SCTL12[1]	SCTL12[0]	SCTL11[3]	SCTL11[2]	SCTL11[1]	SCTL11[0]

Table 54. PWM Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWMR0	RD/WR	PWM2[3]	PWM2[2]	PWM2[1]	PWM2[0]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
PWMR1	RD/WR	PWM4[3]	PWM4[2]	PWM4[1]	PWM4[0]	PWM3[3]	PWM3[2]	PWM3[1]	PWM3[0]
PWMR2	RD/WR	PWM6[3]	PWM6[2]	PWM6[1]	PWM6[0]	PWM5[3]	PWM5[2]	PWM5[1]	PWM5[0]
PWMR3	RD/WR	PWM8[3]	PWM8[2]	PWM8[1]	PWM8[0]	PWM7[3]	PWM7[2]	PWM7[1]	PWM7[0]
PWMR4	RD/WR	PWM10[3]	PWM10[2]	PWM10[1]	PWM10[0]	PWM9[3]	PWM9[2]	PWM9[1]	PWM9[0]
PWMR5	RD/WR	PWM12[3]	PWM12[2]	PWM12[1]	PWM12[0]	PWM11[3]	PWM11[2]	PWM11[1]	PWM11[0]

Table 55. PWM/S Control Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PSR0	RD/WR	PWM14[3]	PWM14[2]	PWM14[1]	PWM14[0]	PWM13[3]	PWM13[2]	PWM13[1]	PWM13[0]
PSR1	RD/WR	PWM16[3]	PWM16[2]	PWM16[1]	PWM16[0]	PWM15[3]	PWM15[2]	PWM15[1]	PWM15[0]
PSR2	RD/WR	PWM18[3]	PWM18[2]	PWM18[1]	PWM18[0]	PWM17[3]	PWM17[2]	PWM7[1]	PWM17[0]
PSR3	RD/WR	SCTL14[3]	SCTL14[2]	SCTL14[1]	SCTL14[0]	SCTL13[3]	SCTL13[2]	SCTL13[1]	SCTL13[0]
PSR4	RD/WR	SCTL16[3]	SCTL16[2]	SCTL16[1]	SCTL16[0]	SCTL15[3]	SCTL15[2]	SCTL15[1]	SCTL15[0]
PSR5	RD/WR	SCTL18[3]	SCTL18[2]	SCTL18[1]	SCTL18[0]	SCTL17[3]	SCTL17[2]	SCTL17[1]	SCTL17[0]

OPERATION

Table 56. Memory Bit Descriptions

<table>
<tr><th>NAME</th><th>DESCRIPTION</th><th colspan="17">VALUES</th></tr>
<tr><td>GPIOx</td><td>GPIOx Pin Control</td><td colspan="17">Write: 0 → GPIOx Pin Pull-Down ON; 1 → GPIOx Pin Pull-Down OFF (Default)
Read: 0 → GPIOx Pin at Logic 0; 1 → GPIOx Pin at Logic 1</td></tr>
<tr><td>REFON</td><td>Reference Powered Up</td><td colspan="17">1 → Reference Remains Powered Up Until Watchdog Timeout
0 → Reference Shuts Down After Conversions (Default)</td></tr>
<tr><td>DTEN</td><td>Discharge Timer Enable (READ ONLY)</td><td colspan="17">1 → Enables the Discharge Timer for Discharge Switches
0 → Disables Discharge Timer</td></tr>
<tr><td>ADCOPT</td><td>ADC Mode Option Bit</td><td colspan="17">ADCOPT: 0 → Selects Modes 27kHz, 7kHz, 422Hz or 26Hz with MD[1:0] Bits in ADC Conversion Commands (Default)
1 → Selects Modes 14kHz, 3kHz, 1kHz or 2kHz with MD[1:0] Bits in ADC Conversion Commands</td></tr>
<tr><td>VUV</td><td>Undervoltage Comparison Voltage*</td><td colspan="17">Comparison Voltage = (VUV + 1) • 16 • 100µV
Default: VUV = 0x000</td></tr>
<tr><td>VOV</td><td>Overvoltage Comparison Voltage*</td><td colspan="17">Comparison Voltage = VOV • 16 • 100µV
Default: VOV = 0x000</td></tr>
<tr><td>DCC[x]</td><td>Discharge Cell x</td><td colspan="17">x = 1 to 18: 1 → Turn ON Shorting Switch for Cell x
0 → Turn OFF Shorting Switch for Cell x (Default)
x = 0: 1 → Turn ON GPIO9 Pull-Down
0 → Turn OFF GPIO9 Pull-Down (Default)</td></tr>
<tr><td rowspan="4">DCTO</td><td rowspan="4">Discharge Time Out Value</td><td>DCTO(Write)</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td></tr>
<tr><td>Time (Min)</td><td>Disabled</td><td>0.5</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>10</td><td>15</td><td>20</td><td>30</td><td>40</td><td>60</td><td>75</td><td>90</td><td>120</td></tr>
<tr><td>DCTO (Read)</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>F</td></tr>
<tr><td>Time Left (Min)</td><td>Disabled or Timeout</td><td>0–0.5</td><td>0.5–1</td><td>1–2</td><td>2–3</td><td>3–4</td><td>4–5</td><td>5–10</td><td>10–15</td><td>15–20</td><td>20–30</td><td>30–40</td><td>40–60</td><td>60–75</td><td>75–90</td><td>90–120</td></tr>
<tr><td>MUTE</td><td>Mute Status (READ ONLY)</td><td colspan="17">1 → Mute is Activated and Discharging is Disabled
0 → Mute is Deactivated</td></tr>
<tr><td>FDRF</td><td>Force Digital Redundancy Failure</td><td colspan="17">1 → Forces the Digital Redundancy Comparison for ADC Conversions to Fail
0 → Enables the Normal Redundancy Comparison</td></tr>
<tr><td>PS[1:0]</td><td>Digital Redundancy Path Selection</td><td colspan="17">11 → Redundancy is Applied Only to ADC3 Digital Path
10 → Redundancy is Applied Only to ADC2 Digital Path
01 → Redundancy is Applied Only to ADC1 Digital Path
00 → Redundancy is Applied Sequentially to ADC1, ADC2 and ADC3 Digital Paths During Cell Conversions and Applied to ADC1 During AUX and STATUS Conversions</td></tr>
<tr><td>DTMEN</td><td>Enable Discharge Timer Monitor</td><td colspan="17">1 → Enables the Discharge Timer Monitor Function if the DTEN Pin is Asserted
0 → Disables the Discharge Timer Monitor Function. The Normal Discharge Timer Function Will Be Enabled if the DTEN Pin is Asserted</td></tr>
<tr><td>CxV</td><td>Cell x Voltage*</td><td colspan="17">x = 1 to 18 16-Bit ADC Measurement Value for Cell x
Cell Voltage for Cell x = CxV • 100µV
CxV is Reset to 0xFFFF on Power-Up and After Clear Command</td></tr>
<tr><td>GxV</td><td>GPIO x Voltage*</td><td colspan="17">x = 1 to 9 16-Bit ADC Measurement Value for GPIOx
Voltage for GPIOx = GxV • 100µV
GxV is Reset to 0xFFFF on Power-Up and After Clear Command</td></tr>
<tr><td>REF</td><td>2nd Reference Voltage*</td><td colspan="17">16-Bit ADC Measurement Value for 2nd Reference
Voltage for 2nd Reference = REF • 100µV
Normal Range is within 2.990V to 3.014V (2.992V to 3.012V for LTC6813I), Allowing for Variations of V_{REF2} Voltage and ADC TME as Well as Additional Margin to Prevent a False Fault from Being Reported</td></tr>
<tr><td>SC</td><td>Sum of Cells Measurement*</td><td colspan="17">16-Bit ADC Measurement Value of the Sum of all Cell Voltages
Sum of all Cells Voltage = SC • 100µV • 30</td></tr>
<tr><td>ITMP</td><td>Internal Die Temperature*</td><td colspan="17">16-Bit ADC Measurement Value of Internal Die Temperature
Temperature Measurement Voltage = ITMP • 100µV/7.6mV/°C – 276°C</td></tr>
</table>

OPERATION

<table>
<tr><th>NAME</th><th>DESCRIPTION</th><th colspan="7">VALUES</th></tr>
<tr><td>VA</td><td>Analog Power Supply Voltage*</td><td></td><td colspan="6">16-Bit ADC Measurement Value of Analog Power Supply Voltage
Analog Power Supply Voltage = VA • 100μV
The Value of VA is Set by External Components and Should Be in the Range 4.5V to 5.5V for Normal Operation</td></tr>
<tr><td>VD</td><td>Digital Power Supply Voltage*</td><td></td><td colspan="6">16-Bit ADC Measurement Value of Digital Power Supply Voltage
Digital Power Supply Voltage = VD • 100μV
Normal Range is within 2.7V to 3.6V</td></tr>
<tr><td>CxOV</td><td>Cell x Over-voltage Flag</td><td>x = 1 to 18</td><td colspan="6">Cell Voltage Compared to VOV Comparison Voltage
0 → Cell x Not Flagged for Overvoltage Condition; 1 → Cell x Flagged</td></tr>
<tr><td>CxUV</td><td>Cell x Under-voltage Flag</td><td>x = 1 to 18</td><td colspan="6">Cell Voltage Compared to VUV Comparison Voltage
0 → Cell x Not Flagged for Undervoltage Condition; 1 → Cell x Flagged</td></tr>
<tr><td>REV</td><td>Revision Code</td><td colspan="7">Device Revision Code</td></tr>
<tr><td>RSVD</td><td>Reserved Bits</td><td colspan="7">Read: Read Back Value Can Be 1 or 0</td></tr>
<tr><td>RSVD0</td><td>Reserved Bits</td><td colspan="7">Read: Read Back Value is Always 0</td></tr>
<tr><td>RSVD1</td><td>Reserved Bits</td><td colspan="7">Read: Read Back Value is Always 1</td></tr>
<tr><td>MUXFAIL</td><td>Multiplexer Self Test Result</td><td colspan="7">Read: 0 → Multiplexer Passed Self Test; 1 → Multiplexer Failed Self Test</td></tr>
<tr><td>THSD</td><td>Thermal Shutdown Status</td><td colspan="7">Read: 0 → Thermal Shutdown Has Not Occurred; 1 → Thermal Shutdown Has Occurred
THSD Bit Cleared to 0 on Read of Status Register Group B</td></tr>
<tr><td>SCTLx[x]</td><td>S Pin Control Bits</td><td colspan="7">0000 – Drive S Pin High (De-Asserted)
0001 – Send 1 High Pulse on S Pin
0010 – Send 2 High Pulses on S Pin
0011 – Send 3 High Pulses on S Pin
0100 – Send 4 High Pulses on S Pin
0101 – Send 5 High Pulses on S Pin
0110 – Send 6 High Pulses on S Pin
0111 – Send 7 High Pulses on S Pin
1XXX – Drive S Pin Low (Asserted)</td></tr>
<tr><td>PWMx[x]</td><td>PWM Discharge Control</td><td colspan="7">0000 – Selects 0% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired
0001 – Selects 6.7% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired
0010 – Selects 13.3% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired
. . .
1110 – Selects 93.3% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired
1111 – Selects 100% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired</td></tr>
<tr><td rowspan="7">ICOMn</td><td rowspan="7">Initial Communication Control Bits</td><td rowspan="4">Write</td><td rowspan="2">I^{2}C</td><td>0110</td><td>0001</td><td colspan="2">0000</td><td>0111</td></tr>
<tr><td>START</td><td>STOP</td><td colspan="2">BLANK</td><td>NO TRANSMIT</td></tr>
<tr><td rowspan="2">SPI</td><td>1000</td><td>1010</td><td colspan="2">1001</td><td>1111</td></tr>
<tr><td>CSB Low</td><td>CSB Falling Edge</td><td colspan="2">CSB High</td><td>NO TRANSMIT</td></tr>
<tr><td rowspan="3">Read</td><td rowspan="2">I^{2}C</td><td>0110</td><td>0001</td><td colspan="2">0000</td><td>0111</td></tr>
<tr><td>START from Master</td><td>STOP from Master</td><td colspan="2">SDA Low Between Bytes</td><td>SDA High Between Bytes</td></tr>
<tr><td>SPI</td><td colspan="5">0111</td></tr>
<tr><td>Dn</td><td>I^{2}C/SPI Communication Data Byte</td><td colspan="7">Data Transmitted (Received) to (from) I^{2}C/SPI Slave Device</td></tr>
<tr><td rowspan="7">FCOMn</td><td rowspan="7">Final Communication Control Bits</td><td rowspan="4">Write</td><td rowspan="2">I^{2}C</td><td colspan="2">0000</td><td colspan="2">1000</td><td>1001</td></tr>
<tr><td colspan="2">Master ACK</td><td colspan="2">Master NACK</td><td>Master NACK + STOP</td></tr>
<tr><td rowspan="2">SPI</td><td colspan="3">X000</td><td colspan="2">1001</td></tr>
<tr><td colspan="3">CSB Low</td><td colspan="2">CSB High</td></tr>
<tr><td rowspan="3">Read</td><td rowspan="2">I^{2}C</td><td>0000</td><td>0111</td><td>1111</td><td>0001</td><td>1001</td></tr>
<tr><td>ACK from Master</td><td>ACK from Slave</td><td>NACK from Slave</td><td>ACK from Slave + STOP from Master</td><td>NACK from Slave + STOP from Master</td></tr>
<tr><td>SPI</td><td colspan="5">1111</td></tr>
</table>

*Voltage equations use the decimal value of registers, 0 to 4095 for 12 bits and 0 to 65535 for 16 bits.

APPLICATIONS INFORMATION

PROVIDING DC POWER

Simple Linear Regulator

The primary supply pin for the LTC6813-1 is the 5V (±0.5V) V_{REG} input pin. To generate the required 5V supply for V_{REG}, the DRIVE pin can be used to form a discrete regulator with the addition of a few external components, as shown in Figure 32. The DRIVE pin provides a 5.7V output, capable of sourcing 1mA. When buffered with an NPN transistor, this provides a stable 5V over temperature. The NPN transistor should be chosen to have a sufficient Beta over temperature (> 40) to supply the necessary supply current. The peak V_{REG} current requirement of the LTC6813-1 approaches 35mA when simultaneously communicating over isoSPI and making ADC conversions. If the V_{REG} pin is required to support any additional load, a transistor with an even higher Beta may be required.

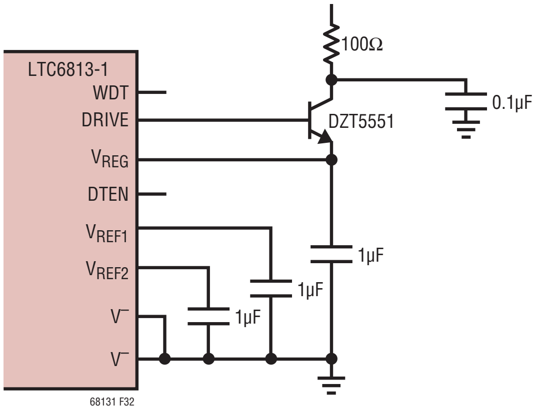


Figure 32. Simple V_{REG} Power Source Using NPN Pass Transistor

The NPN collector can be powered from any voltage source that is a minimum 6V above V^-. This includes the cells that are being monitored, or an unregulated power supply. A 100Ω/100nF RC decoupling network is recommended for the collector power connection to protect the NPN from transients. The emitter of the NPN should be bypassed with a 1µF capacitor. Larger capacitance should be avoided since this will increase the wake-up time of the LTC6813-1. Some attention should be given to the thermal characteristic of the NPN, as there can be significant heating with a high collector voltage.

Improved Regulator Power Efficiency

For improved efficiency when powering the LTC6813-1 from the cell stack, V_{REG} may be powered from a DC/DC converter, rather than the NPN pass transistor. An ideal circuit is based on Analog Devices LT8631 step-down regulator, as shown in Figure 33. A 100Ω resistor is recommended between the battery stack and the LT8631 input; this will prevent in-rush current when connecting to the stack and it will reduce conducted EMI. The EN/UVLO pin should be connected to the DRIVE pin, which will put the LT8631 into a low power state when the LTC6813-1 is in the SLEEP state.

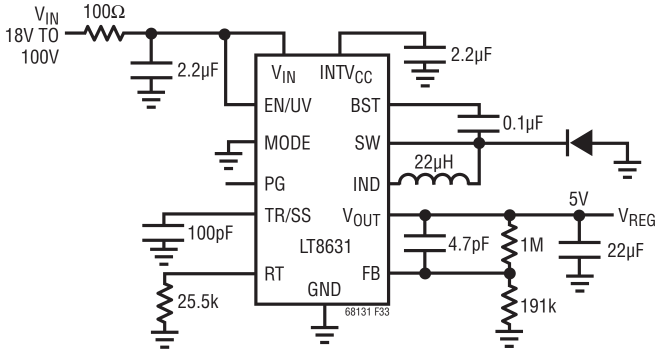


Figure 33. V_{REG} Powered From Cell Stack with High Efficiency Regulator

APPLICATIONS INFORMATION

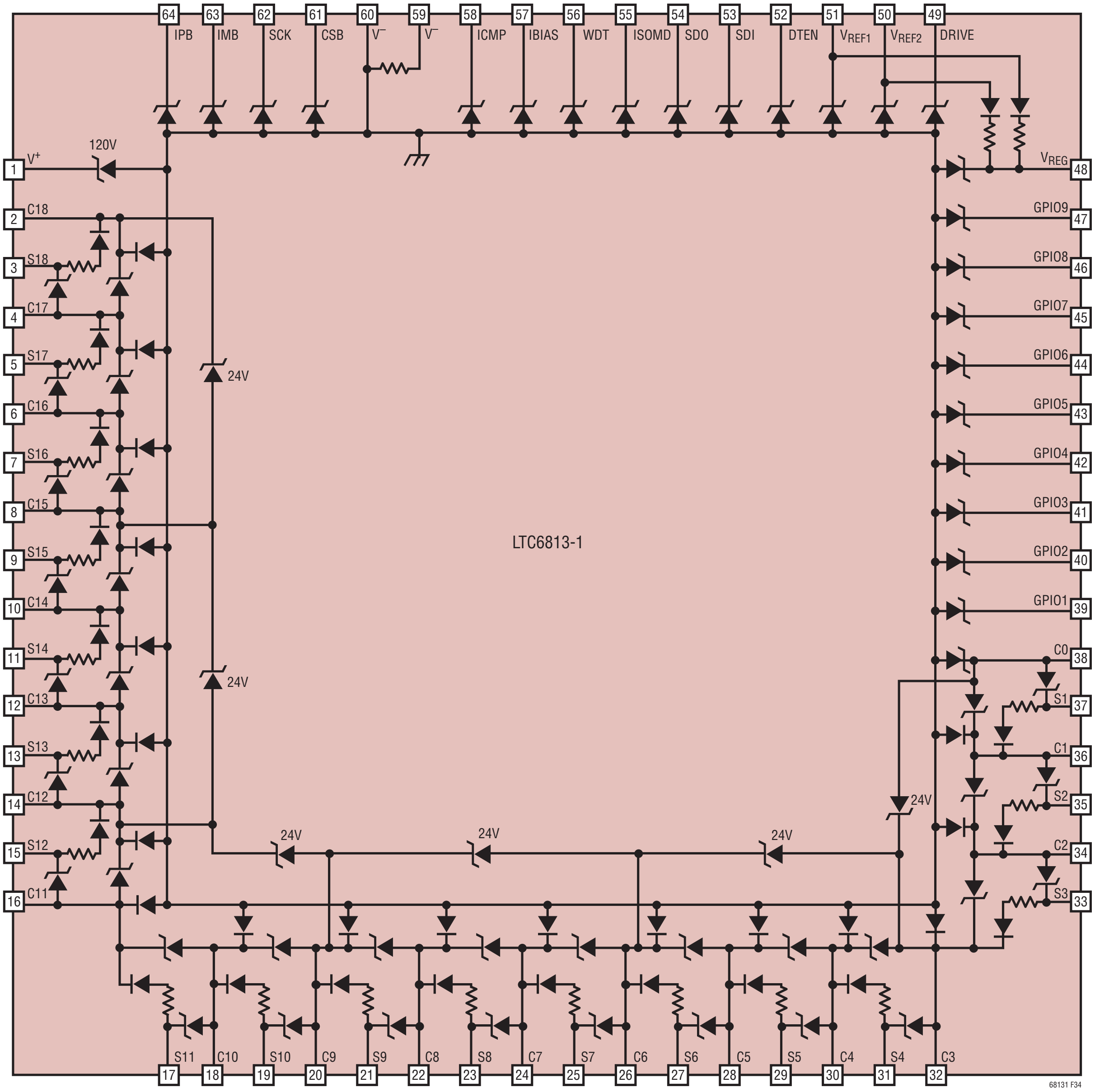
INTERNAL PROTECTION AND FILTERING

Internal Protection Features

The LTC6813-1 incorporates various ESD safeguards to ensure robust performance. An equivalent circuit showing the specific protection structures is shown in Figure 34. Zener-like suppressors are shown with their nominal clamp voltage, and the unmarked diodes exhibit standard PN junction behavior.

Filtering of Cell and GPIO Inputs

The LTC6813-1 uses a delta-sigma ADC, which includes a delta-sigma modulator followed by a SINC3 finite impulse response (FIR) digital filter. This greatly relaxes input filtering requirements. Furthermore, the programmable oversampling ratio allows the user to determine the best trade-off between measurement speed and filter cutoff frequency. Even with this high order low pass filter, fast



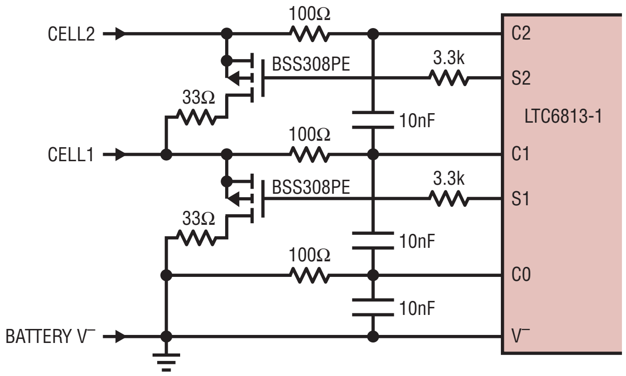
NOTE: ZENER VOLTAGE IS 8V UNLESS MARKED OTHERWISE.

Figure 34. Internal ESD Protection Structures of the LTC6813-1

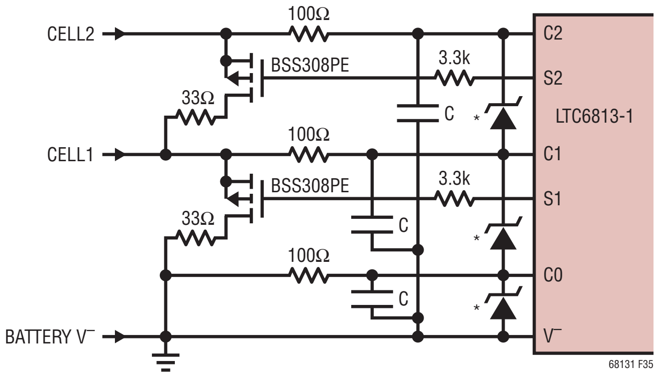
Rev. A

APPLICATIONS INFORMATION

transient noise can still induce some residual noise in measurements, especially in the faster conversion modes. This can be minimized by adding an RC low pass decoupling to each ADC input, which also helps reject potentially damaging high energy transients. Adding more than about 100Ω to the ADC inputs begins to introduce a systematic error in the measurement, which can be improved by raising the filter capacitance or mathematically compensating in software with a calibration procedure. For situations that demand the highest level of battery voltage ripple rejection, grounded capacitor filtering is recommended. This configuration has a series resistance and capacitors that decouple HF noise to V^-. In systems where noise is less periodic or higher oversample rates are in use, a differential capacitor filter structure is adequate. In this configuration there are series resistors to each input, but the capacitors connect between the adjacent C pins. However, the differential capacitor sections interact. As a result, the filter response is less consistent and results in less attenuation than predicted by the RC, by approximately a decade. Note that the capacitors only see one cell of applied voltage (thus smaller and lower cost) and tend to distribute transient energy uniformly across the IC (reducing stress events on the internal protection structure). Figure 35 shows the two methods schematically. ADC accuracy varies with R, C as shown in the Typical



(a) Differential Capacitor Filter



*6.8V ZENERS RECOMMENDED IF C ≥ 100nF

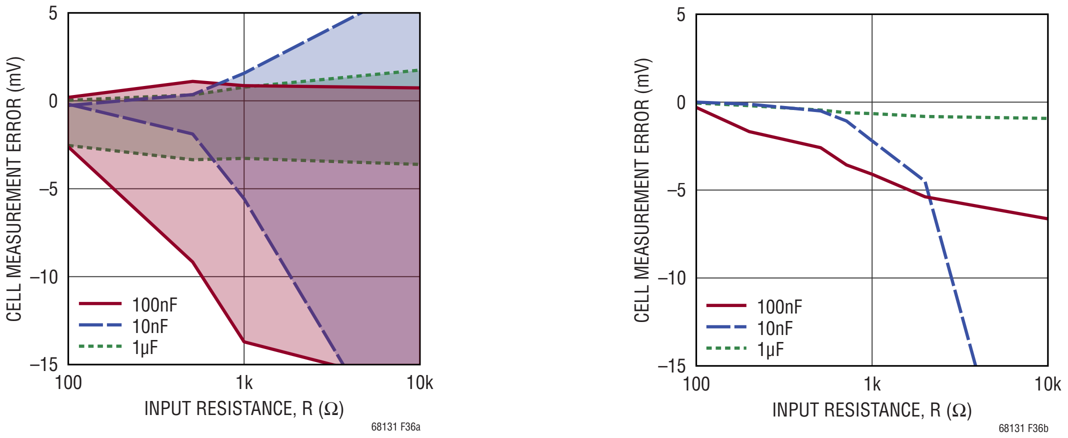
(b) Grounded Capacitor Filter

Figure 35. Input Filter Structure Configurations

Performance curves, but error is minimized if R = 100Ω and C = 10nF. The GPIO pins will always use a grounded capacitor configuration because the measurements are all with respect to V^-.

Using Nonstandard Cell Input Filters

A cell pin filter of 100Ω and 10nF is recommended for all applications. This filter provides the best combination of noise rejection and Total Measurement Error (TME) performance. In applications that use C pin RC filters larger than 100Ω/10nF there may be additional measurement error. Figure 36a shows how both total TME and TME variation increase as the RC time constant increases. The increased error is related to the MUX settling. It is possible to reduce TME levels to near data sheet specifications by implementing an extra single channel conversion before issuing a standard all channel ADCV command. Figure 37a shows the standard ADCV command sequence. Figure 37b and Figure 37c show the recommended command sequence and timing that will allow the MUX to settle. The purpose of the modified procedure is to allow the MUX to settle at C1/C7/C13 before the start of the measurement cycle. The delay between the C1/C7/C13 ADCV command and the All Channel ADCV command is dependent on the time constant of the RC being used. The general guidance is to wait 6τ between the C1/C7/C13 ADCV command and the All Channel ADCV command. Figure 36b shows the expected TME when using the recommended command sequence.



(a) Cell Measurement Error Range vs Input RC Values

(b) Cell Measurement Error vs Input RC Values (Extra Conversion and Delay Before Measurement)

Figure 36. Cell Measurement TME

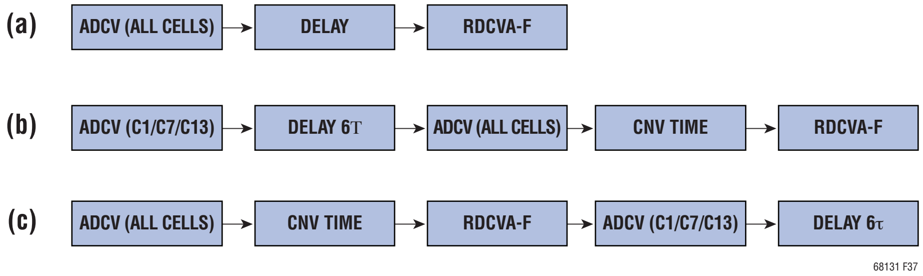


Figure 37. ADC Command Order

APPLICATIONS INFORMATION

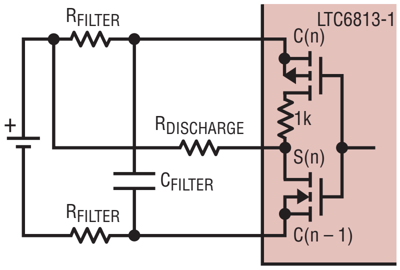
CELL BALANCING

Cell Balancing with Internal MOSFETs

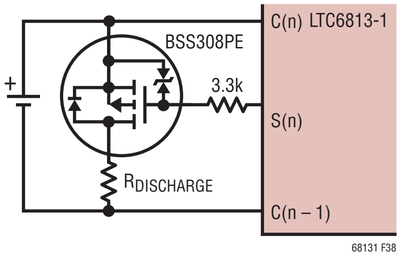
With passive balancing, if one cell in a series stack becomes overcharged, an S output can slowly discharge this cell by connecting it to a resistor. Each S output is connected to an internal N-channel MOSFET with a maximum on resistance of 10Ω. An external resistor should be connected in series with these MOSFETs to allow most of the heat to be dissipated outside of the LTC6813-1 package, as illustrated in Figure 38a.

The internal discharge switches (MOSFETs) S1 through S18 can be used to passively balance cells as shown in Figure 38a with balancing current of 200mA or less (80mA or less if the die temperature is over 95°C). Balancing current larger than 200mA is not recommended for the internal switches due to excessive die heating. When discharging cells with the internal discharge switches, the die temperature should be monitored. See the Thermal Shutdown section.

Note that the anti-aliasing filter resistor is part of the discharge path, so it should be removed or reduced. Use of an RC for added cell voltage measurement filtering is OK but the filter resistor must remain small, typically around 10Ω to reduce the effect on the balance current.



(a) Internal Discharge Circuit



(b) External Discharge Circuit

Figure 38. Internal/External Discharge Circuits

Cell Balancing with External Transistors

For applications that require balancing currents above 200mA or large cell filters, the S outputs can be used to control external transistors. The LTC6813-1 includes an internal pull-up PMOS transistor with a 1k series resistor. The S pins can act as digital outputs suitable for driving the gate of an external MOSFET as illustrated in Figure 38b. Figure 35 shows external MOSFET circuits that include RC filtering. For applications with very low cell voltages the PMOS in Figure 38b can be replaced with a PNP. When a PNP is used, the resistor in series with the base should be reduced.

Choosing a Discharge Resistor

When sizing the balancing resistor, it is important to know the typical battery imbalance and the allowable time for cell balancing. In most small battery applications, it is reasonable for the balancing circuitry to be able to correct for a 5% SOC (State of Charge) error with 5 hours of balancing. For example a 5AHr battery with a 5% SOC imbalance will have approximately 250mA Hrs of imbalance. Using a 50mA balancing current this could be corrected in 5 hours. With a 100mA balancing current, the error would be corrected in 2.5 hours. In systems with very large batteries, it becomes difficult to use passive balancing to correct large SOC imbalances in short periods of time. The excessive heat created during balancing generally limits the balancing current. In large capacity battery applications, if short balancing times are required, an active balancing solution should be considered. When choosing a balance resistor, the following equations can be used to help determine a resistor value:

$$\text{Balance Current} = \frac{\text{\%SOC\_Imbalance} \bullet \text{Battery Capacity}}{\text{Number of Hours to Balance}}$$

$$\text{Balance Resistor} = \frac{\text{Nominal Cell Voltage}}{\text{Balance Current}}$$

APPLICATIONS INFORMATION

Active Cell Balancing

Applications that require 1A or greater of cell balancing current should consider implementing an active balancing system. Active balancing allows for much higher balancing currents without the generation of excessive heat. Active balancing also allows for energy recovery since most of the balance current will be redistributed back to the battery pack. Figure 39 shows a simple active balancing implementation using Analog Devices LT8584. The LT8584 also has advanced features which can be controlled via the LTC6813-1. See S Pin Pulsing Using the S Pin Control Settings in this data sheet and the LT8584 data sheet for more details.

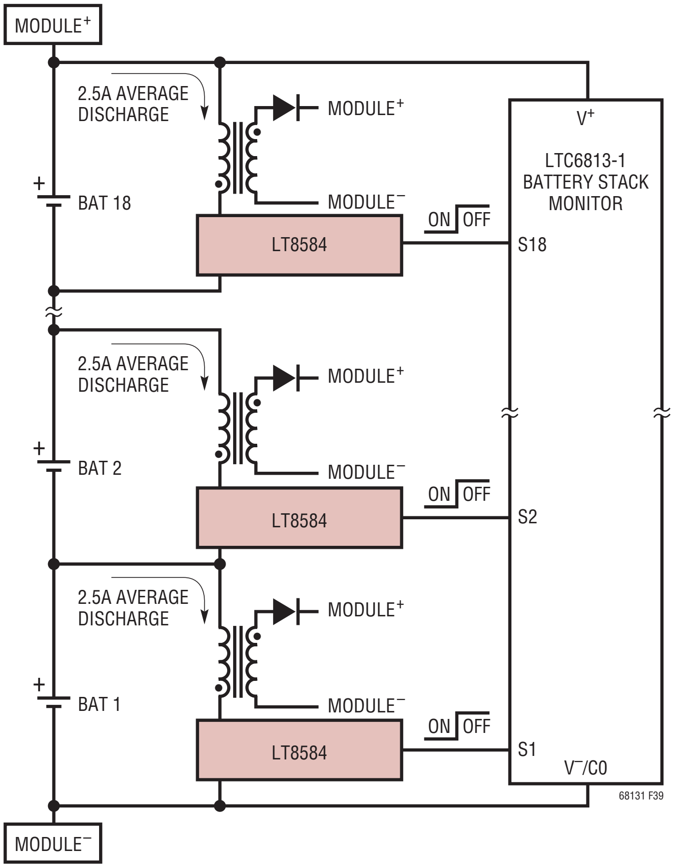


Figure 39. 18-Cell Battery Stack Module with Active Balancing

DISCHARGE CONTROL DURING CELL MEASUREMENTS

If the discharge permitted (DCP) bit is high at the time of a cell measurement command, the S pin discharge states do not change during cell measurements. If the DCP bit is low, S pin discharge states will be disabled while the corresponding cell or adjacent cells are being measured. If using an external discharge transistor, the relatively low 1kΩ impedance of the internal LTC6813-1 PMOS transistors should allow the discharge currents to fully turn off before the cell measurement. Table 57 illustrates the ADCV command with DCP = 0. In this table, OFF indicates that the S pin discharge is forced off irrespective of the state of the corresponding DCC[x] bit. ON indicates that the S pin discharge will remain on during the measurement period if it was ON prior to the measurement command.

In some cases, it is not possible for the automatic discharge control to eliminate all measurement error caused by running the discharges. This is due to the discharge transistor not turning off fast enough for the cell voltage to completely settle before the measurement starts. For the best measurement accuracy when running discharge, the MUTE and UNMUTE commands should be used. The MUTE command can be issued to temporarily disable all discharge transistors before the ADCV command is issued. After the cell conversion completes, an UNMUTE can be sent to re-enable all discharge transistors that were previously ON. Using this method maximizes the measurement accuracy with a very small time penalty.

Method to Verify Discharge Circuits

When using the internal discharge feature, the ability to verify discharge functionality can be implemented in software. In applications using an external discharge MOSFET, an additional resistor can be added between the battery cell and the source of the discharge MOSFET. This will allow the system to test discharge functionality.

APPLICATIONS INFORMATION

Table 57. Discharge Control During an ADCV Command with DCP = 0

	CELL MEASUREMENT PERIODS						CELL CALIBRATION PERIODS					
	CELL 1/7/13	CELL 2/8/14	CELL 3/9/15	CELL 4/10/16	CELL 5/11/17	CELL 6/12/18	CELL 1/7/13	CELL 2/8/14	CELL 3/9/15	CELL 4/10/16	CELL 5/11/17	CELL 6/12/18
DISCHARGE PIN	$t_0 – t_{1M}$	$t_{1M} – t_{2M}$	$t_{2M} – t_{3M}$	$t_{3M} – t_{4M}$	$t_{4M} – t_{5M}$	$t_{5M} – t_{6M}$	$t_{6M} – t_{1C}$	$t_{1C} – t_{2C}$	$t_{2C} – t_{3C}$	$t_{3C} – t_{4C}$	$t_{4C} – t_{5C}$	$t_{5C} – t_{6C}$
S1	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF
S2	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON
S3	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON
S4	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON
S5	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
S6	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
S7	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF
S8	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON
S9	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON
S10	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON
S11	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
S12	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
S13	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF
S14	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON
S15	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON
S16	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON
S17	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
S18	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF

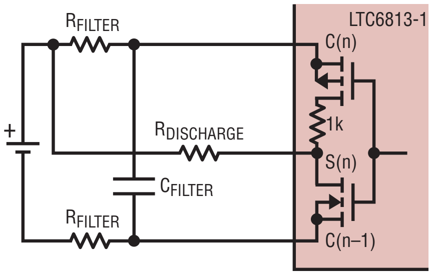
APPLICATIONS INFORMATION

Both circuits are shown in Figure 40. The functionality of the discharge circuits can be verified by conducting cell measurements and comparing measurements when the discharge is off to measurements when the discharge is on. The measurement taken when the discharge is on requires that the discharge permit bit (DCP) be set. The change in the measurement when the discharge is turned on is calculable based on the resistor values. The following algorithm can be used in conjunction with Figure 40 to verify each discharge circuit:

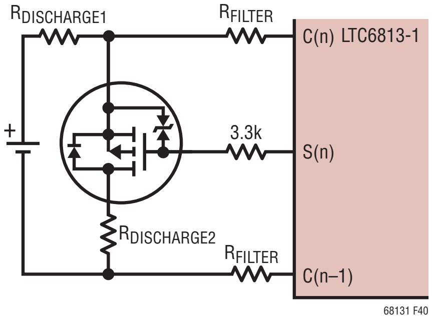
1. Measure all cells with no discharging (all S outputs off) and read and store the results.
2. Turn on S1, S7 and S13.
3. Measure C1–C0, C7–C6, C13–C12.
4. Turn off S1, S7 and S13.
5. Turn on S2, S8 and S14.
6. Measure C2–C1, C8–C7, C14–C13.
7. Turn off S2, S8 and S14.

…

17. Turn on S6, S12 and S18.
18. Measure C6–C5, C12–C11, C18–C17.
19. Turn off S6, S12 and S18.
20. Read the Cell Voltage Register Groups to get the results of Steps 2 thru 19.
21. Compare new readings with old readings. Each cell voltage reading should have decreased by a fixed percentage set by $R_{DISCHARGE}$ and R_{FILTER} for internal designs and $R_{DISCHARGE1}$ and $R_{DISCHARGE2}$ for external MOSFET designs. The exact amount of decrease depends on the resistor values and MOSFET characteristics.



(a) Internal Discharge Circuit



(b) External Discharge Circuit

Figure 40. Balancing Self Test Circuit

APPLICATIONS INFORMATION

DIGITAL COMMUNICATIONS

PEC Calculation

The Packet Error Code (PEC) can be used to ensure that the serial data read from the LTC6813-1 is valid and has not been corrupted. This is a critical feature for reliable communication, particularly in environments of high noise. The LTC6813-1 requires that a PEC be calculated for all data being read from, and written to, the LTC6813-1. For this reason it is important to have an efficient method for calculating the PEC.

The C code below provides a simple implementation of a lookup-table-derived PEC calculation method. There are two functions. The first function init_PEC15_Table() should only be called once when the microcontroller starts and will initialize a PEC15 table array called pec15Table[]. This table will be used in all future PEC calculations. The PEC15 table can also be hard coded into the microcontroller rather than running the init_PEC15_Table() function at startup. The pec15() function calculates the PEC and will return the correct 15-bit PEC for byte arrays of any given length.

```
/************************************
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USE OF SAME, INCLUDING ANY LOSS OF USE OR DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE
OR OTHER TORTUOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.
*************************************/
int16 pec15Table[256];
int16 CRC15_POLY = 0x4599;
void init_PEC15_Table()
{
for (int i = 0; i < 256; i++)
{
remainder = i << 7;
for (int bit = 8; bit > 0; --bit)
{
if (remainder & 0x4000)
{
remainder = ((remainder << 1));
remainder = (remainder ^ CRC15_POLY)
}
else
{
remainder = ((remainder << 1));
}
}
pec15Table[i] = remainder&0xFFFF;
}
}
unsigned int16 pec15 (char *data , int len)
{
int16 remainder,address;
remainder = 16;//PEC seed
for (int i = 0; i < len; i++)
{
address = ((remainder >> 7) ^ data[i]) & 0xff;//calculate PEC table address
remainder = (remainder << 8 ) ^ pec15Table[address];
}
return (remainder*2);//The CRC15 has a 0 in the LSB so the final value must be multiplied by 2
}
```

APPLICATIONS INFORMATION

isoSPI IBIAS and ICMP Setup

The LTC6813-1 allows the isoSPI links of each application to be optimized for power consumption or for noise immunity. The power and noise immunity of an isoSPI system is determined by the programmed I_B current, which controls the isoSPI signaling currents. Bias current I_B can range from 100µA to 1mA. Internal circuitry scales up this bias current to create the isoSPI signal currents equal to be 20 • I_B. A low I_B reduces the isoSPI power consumption in the READY and ACTIVE states, while a high I_B increases the amplitude of the differential signal voltage V_A across the matching termination resistor, R_M. The I_B current is programmed by the sum of the R_{B1} and R_{B2} resistors connected between the 2V IBIAS pin and GND as shown in Figure 41. The receiver input threshold is set by the ICMP voltage that is programmed with the resistor divider created by the R_{B1} and R_{B2} resistors. The receiver threshold will be half of the voltage present on the ICMP pin.

The following guidelines should be used when setting the bias current (100µA to 1mA) I_B and the receiver comparator threshold voltage $V_{ICMP}/2$:

R_M = Transmission Line Characteristic Impedance Z_0

Signal Amplitude $V_A = (20 \bullet I_B) \bullet (R_M/2)$

V_{TCMP} (Receiver Comparator Threshold) = $K \bullet V_A$

V_{ICMP} (voltage on ICMP pin) = $2 \bullet V_{TCMP}$

$R_{B2} = V_{ICMP}/I_B$

$R_{B1} = (2/I_B) - R_{B2}$

Select I_B and K (Signal Amplitude V_A to Receiver Comparator Threshold ratio) according to the application:

For lower power links: I_B = 0.5mA and K = 0.5

For full power links: I_B = 1mA and K = 0.5

For long links (>50m): I_B = 1mA and K = 0.25

For applications with little system noise, setting I_B to 0.5mA is a good compromise between power consumption and noise immunity. Using this I_B setting with a 1:1 transformer and R_M = 100Ω, R_{B1} should be set to 3.01k and R_{B2} set to 1k. With typical CAT5 twisted pair, these settings will allow for communication up to 50m. For applications in very noisy environments or that require cables longer than 50m it is recommended to increase I_B to 1mA. Higher drive current compensates for the increased insertion loss in the cable and provides high noise immunity. When using cables over 50m and a transformer with a 1:1 turns ratio and R_M = 100Ω, R_{B1} would be 1.5k and R_{B2} would be 499Ω.

The maximum clock rate of an isoSPI link is determined by the length of the isoSPI cable. For cables 10m or less, the maximum 1MHz SPI clock frequency is possible. As the length of the cable increases, the maximum possible SPI clock rate decreases. This dependence is a result of the increased propagation delays that can create possible timing violations. Figure 42 shows how the maximum data rate reduces as the cable length increases when using a CAT5 twisted pair.

Cable delay affects three timing specifications: t_{CLK}, t_6 and t_7. In the Electrical Characteristics table, each of these specifications is de-rated by 100ns to allow for 50ns

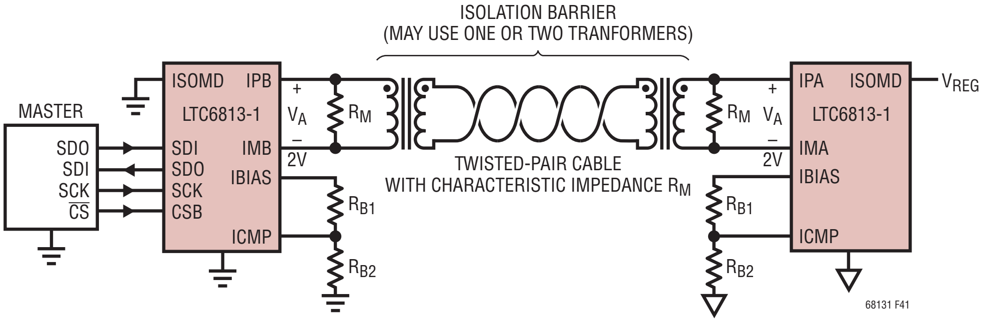


Figure 41. isoSPI Circuit

APPLICATIONS INFORMATION

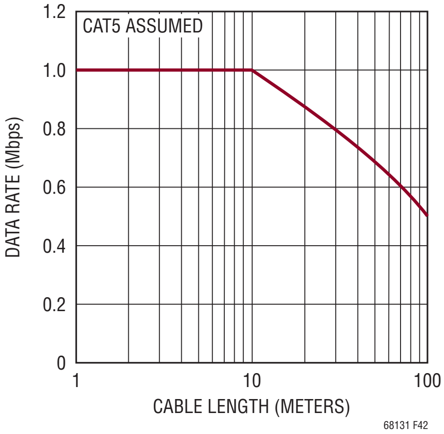


Figure 42. Data Rate vs Cable Length

of cable delay. For longer cables, the minimum timing parameters may be calculated as shown below:

t_{CLK}, t_6 and t_7 > 0.9µs + 2 • t_{CABLE} (0.2m per ns)

Implementing a Modular isoSPI Daisy Chain

The hardware design of a daisy-chain isoSPI bus is identical for each device in the network due to the daisy-chain point-to-point architecture. The simple design as shown in Figure 41 is functional, but inadequate for most designs. The termination resistor R_M should be split and bypassed with a capacitor as shown in Figure 43. This change provides both a differential and a common mode termination, and as such, increases the system noise immunity.

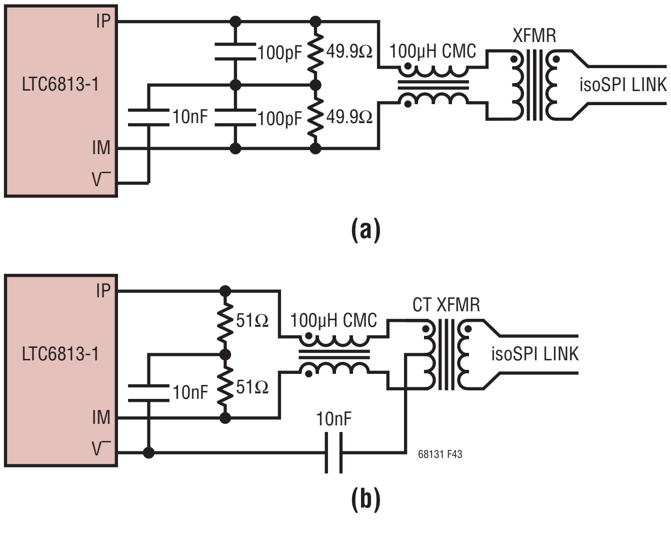


Figure 43. Daisy Chain Interface Components

The use of cables between battery modules, particularly in automotive applications, can lead to increased noise susceptibility in the communication lines. For high levels of electromagnetic interference (EMC), additional filtering is recommended. The circuit example in Figure 43 shows the use of common mode chokes (CMC) to add common mode noise rejection from transients on the battery lines. The use of a center tapped transformer will also provide additional noise performance. A bypass capacitor connected to the center tap creates a low impedance for common mode noise (Figure 43b). Since transformers without a center tap can be less expensive, they may be preferred. In this case, the addition of a split termination resistor and a bypass capacitor (Figure 43a) can enhance the isoSPI performance. Large center tap capacitors greater than 10nF should be avoided as they may prevent the isoSPI common mode voltage from settling. Common mode chokes similar to those used in Ethernet or CANbus applications are recommended. Specific examples are provided in Table 59.

An important daisy chain design consideration is the number of devices in the isoSPI network. The length of the chain determines the serial timing and affects data latency and throughput. The maximum number of devices in an isoSPI daisy chain is strictly dictated by the serial timing requirements. However, it is important to note that the serial read back time, and the increased current consumption, might dictate a practical limitation.

For a daisy chain, two timing considerations for proper operation dominate (see Figure 25):

1. t_6, the time between the last clock and the rising chip select, must be long enough.
2. t_5, the time from a rising chip select to the next falling chip select (between commands), must be long enough.

Both t_5 and t_6 must be lengthened as the number of LTC6813-1 devices in the daisy chain increases. The equations for these times are below:

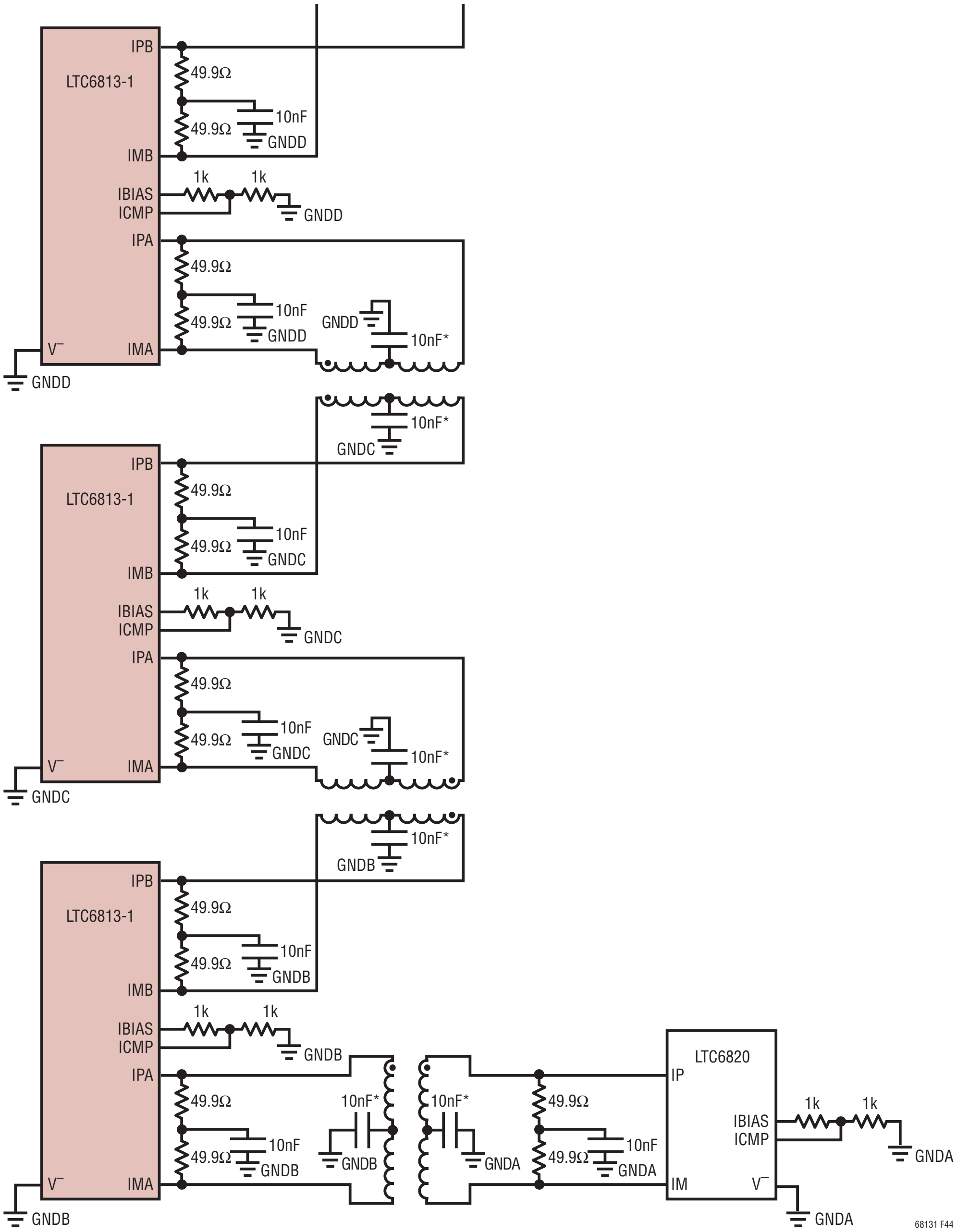
t_5 > (#devices • 70ns) + 900ns

t_6 > (#devices • 70ns) + 950ns

APPLICATIONS INFORMATION

Connecting Multiple LTC6813-1s on the Same PCB

When connecting multiple LTC6813-1 devices on the same PCB, only a single transformer is required between the LTC6813-1 isoSPI ports. The absence of the cable also reduces the noise levels on the communication lines and often only a split termination is required. Figure 44 shows an example application that has multiple LTC6813-1s on the same PCB, communicating to the bottom MCU through an LTC6820 isoSPI driver. If a transformer with a center tap is used, a capacitor can be added for better noise rejection. Additional noise filtering can be provided with discrete common mode chokes (not shown) placed to both sides of the single transformer.



* IF TRANSFORMER BEING USED HAS A CENTER TAP, IT SHOULD BE BYPASSED WITH A 10nF CAP

Figure 44. Daisy Chain Interface Components on Single Board

APPLICATIONS INFORMATION

On single board designs with low noise requirements, it is possible for a simplified capacitor-isolated coupling as shown in Figure 45 to replace the transformer.

In this circuit, the transformer is directly replaced by two 10nF capacitors. An optional common mode choke (CMC) provides noise rejection similar to application circuits usng transformers. The circuit is designed to use IBIAS/ICMP settings identical to the transformer circuit.

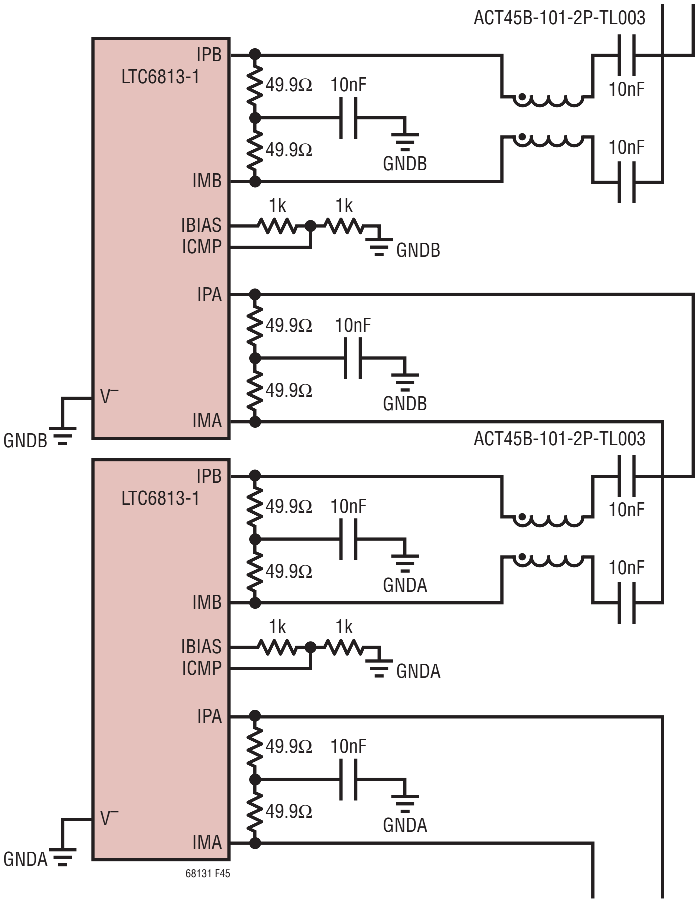


Figure 45. Capacitive Isolation Coupling for LTC6813-1s on the Same PCB

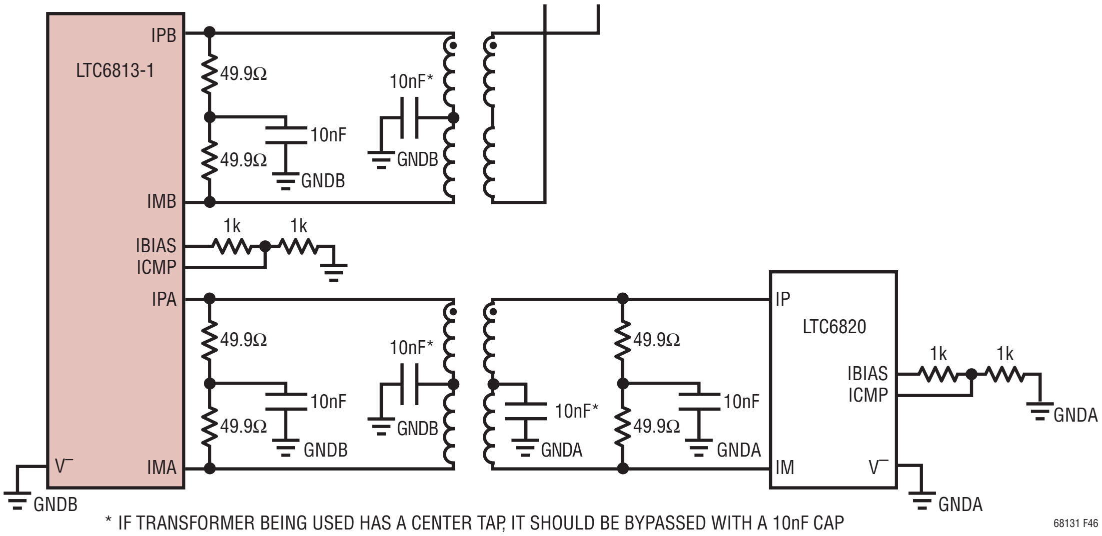
Connecting an MCU to an LTC6813-1 with an isoSPI Data Link

The LTC6820 will convert standard 4-wire SPI into a 2-wire isoSPI link that can communicate directly with the LTC6813-1. An example is shown in Figure 46. The LTC6820 can be used in applications to provide isolation between the microcontroller and the stack of LTC6813-1s. The LTC6820 also enables system configurations that have the BMS controller at a remote location relative to the LTC6813-1 devices and the battery pack.

Transformer Selection Guide

As shown in Figure 41, a transformer or pair of transformers isolates the isoSPI signals between two isoSPI ports. The isoSPI signals have programmable pulse amplitudes up to 1.6V_{P-P} and pulse widths of 50ns and 150ns. To be able to transmit these pulses with the necessary fidelity, the system requires that the transformers have primary inductances above 60µH and a 1:1 turns ratio. It is also necessary to use a transformer with less than 2.5µH of leakage inductance. In terms of pulse shape the primary inductance will mostly affect the pulse droop of the 50ns and 150ns pulses. If the primary inductance is too low, the pulse amplitude will begin to droop and decay over the pulse period. When the pulse droop is severe enough, the effective pulse width seen by the receiver will drop substantially, reducing noise margin. Some droop is acceptable as long as it is a relatively small percentage of the total pulse amplitude. The leakage inductance primarily affects the rise and fall times of the pulses. Slower rise and fall times will effectively reduce the pulse width. Pulse width is determined by the receiver as the time the signal is above the threshold set at the ICMP pin. Slow rise and fall times cut into the timing margins. Generally it is best to keep pulse edges as fast as possible. When evaluating transformers, it is also worth noting the parallel winding capacitance. While transformers have very good CMRR at low frequency, this rejection will degrade at higher frequencies, largely due to the winding to winding capacitance. When choosing a transformer, it is best to pick one with less parallel winding capacitance when possible.

When choosing a transformer, it is equally important to pick a part that has an adequate isolation rating for the application. The working voltage rating of a transformer is a key spec when selecting a part for an application. Interconnecting daisy-chain links between LTC6813-1 devices see <60V stress in typical applications; ordinary pulse and LAN type transformers will suffice. Connections to the LTC6820, in general, may need much higher



* IF TRANSFORMER BEING USED HAS A CENTER TAP, IT SHOULD BE BYPASSED WITH A 10nF CAP

Figure 46. Interfacing an LTC6813-1 with a µC Using an LTC6820 for Isolated SPI Control

APPLICATIONS INFORMATION

working voltage ratings for good long-term reliability. Usually, matching the working voltage to the voltage of the entire battery stack is conservative. Unfortunately, transformer vendors will often only specify one-second HV testing, and this is not equal to the long-term (“permanent”) rating of the part. For example, according to most safety standards a 1.5kV rated transformer is expected to handle 230V continuously, and a 3kV device is capable of 1100V long-term, though manufacturers may not always certify to those levels (refer to actual vendor data for specifics). Usually, the higher voltage transformers are called “high-isolation” or “reinforced insulation” types by the suppliers. Table 58 shows a list of transformers that have been evaluated in isoSPI links.

In most applications a common mode choke is also necessary for noise rejection. Table 59 includes a list of suitable CMCs if the CMC is not already integrated into the transformer being used.

Table 58. Recommended Transformers

SUPPLIER	PART NUMBER	TEMP RANGE	V$_{WORKING}$	V$_{HIPOT}$/60S	CT	CMC	H	L	W (W/ LEADS)	PINS	AEC-Q200
Recommended Dual Transformers											
Pulse	HX1188FNL	–40°C to 85°C	60V (est)	1.5kV$_{RMS}$	●	●	6.0mm	12.7mm	9.7mm	16SMT	–
Pulse	HX0068ANL	–40°C to 85°C	60V (est)	1.5kV$_{RMS}$	●	●	2.1mm	12.7mm	9.7mm	16SMT	–
Pulse	HM2100NL	–40°C to 105°C	1000V	4.3kVDC	–	●	3.4mm	14.7mm	14.9mm	10SMT	●
Pulse	HM2112ZNL	–40°C to 125°C	1000V	4.3kVDC	●	●	4.9mm	14.8mm	14.7mm	12SMT	●
Sumida	CLP178-C20114	–40°C to 125°C	1000V (est)	3.75kV$_{RMS}$	●	●	9mm	17.5mm	15.1mm	12SMT	–
Sumida	CLP0612-C20115		600V$_{RMS}$	3.75kV$_{RMS}$	●	–	5.7mm	12.7mm	9.4mm	16SMT	–
Wurth	7490140110	–40°C to 85°C	250V$_{RMS}$	4kV$_{RMS}$	●	●	10.9mm	24.6mm	17.0mm	16SMT	–
Wurth	7490140111	0°C to 70°C	1000V (est)	4.5kV$_{RMS}$	●	–	8.4mm	17.1mm	15.2mm	12SMT	–
Wurth	749014018	0°C to 70°C	250V$_{RMS}$	4kV$_{RMS}$	●	●	8.4mm	17.1mm	15.2mm	12SMT	–
Halo	TG110-AE050N5LF	–40°C to 85/125°C	60V (est)	1.5kV$_{RMS}$	●	●	6.4mm	12.7mm	9.5mm	16SMT	●
Recommended Single Transformers											
Pulse	PE-68386NL	–40°C to 130°C	60V (est)	1.5kVDC	–	–	2.5mm	6.7mm	8.6mm	6SMT	–
Pulse	HM2101NL	–40°C to 105°C	1000V	4.3kVDC	–	●	5.7mm	7.6mm	9.3mm	6SMT	●
Pulse	HM2113ZNL	–40°C to 125°C	1600V	4.3kVDC	●	●	3.5mm	9mm	15.5mm	6SMT	●
Wurth	750340848	–40°C to 105°C	250V	3kV$_{RMS}$	–	–	2.2mm	4.4mm	9.1mm	4SMT	–
Halo	TGR04-6506V6LF	–40°C to 125°C	300V	3kV$_{RMS}$	●	–	10mm	9.5mm	12.1mm	6SMT	–
Halo	TGR04-A6506NA6NL	–40°C to 125°C	300V	3kV$_{RMS}$	●	–	9.4mm	8.9mm	12.1mm	6SMT	●
Halo	TDR04-A550ALLF	–40°C to 105°C	1000V	5kV$_{RMS}$	●	–	6.4mm	8.9mm	16.6mm	6TH	●
TDK	ALT4532V-201-T001	–40°C to 105°C	60V (est)	~1kV	●	–	2.9mm	3.2mm	4.5mm	6SMT	●
Sumida	CEEH96BNP-LTC6804/11	–40°C to 125°C	600V	2.5kV$_{RMS}$	–	–	7mm	9.2mm	12.0mm	4SMT	–
Sumida	CEP99NP-LTC6804	–40°C to 125°C	600V	2.5kV$_{RMS}$	●	–	10mm	9.2mm	12.0mm	8SMT	–
Sumida	ESMIT-4180/A	–40°C to 105°C	250V$_{RMS}$	3kV$_{RMS}$	–	–	3.5mm	5.2mm	9.1mm	4SMT	●
TDK	VGT10/9EE-204S2P4	–40°C to 125°C	250V (est)	2.8kV$_{RMS}$	●	–	10.6mm	10.4mm	12.7mm	8SMT	–

Table 59. Recommended Common Mode Chokes

MANUFACTURER	PART NUMBER
TDK	ACT45B-101-2P
Murata	DLW43SH101XK2

APPLICATIONS INFORMATION

isoSPI Layout Guidelines

Layout of the isoSPI signal lines also plays a significant role in maximizing the noise immunity of a data link. The following layout guidelines are recommended:

1. The transformer should be placed as close to the isoSPI cable connector as possible. The distance should be kept less than 2cm. The LTC6813-1 should be placed close to but at least 1cm to 2cm away from the transformer to help isolate the IC from magnetic field coupling.
2. A V^- ground plane should not extend under the transformer, the isoSPI connector or in between the transformer and the connector.
3. The isoSPI signal traces should be as direct as possible while isolated from adjacent circuitry by ground metal or space. No traces should cross the isoSPI signal lines, unless separated by a ground plane on an inner layer.

System Supply Current

The LTC6813-1 has various supply current specifications for the different states of operation. The average supply current depends on the control loop in the system. It is necessary to know which commands are being executed each control loop cycle, and the duration of the control loop cycle. From this information it is possible to determine the percentage of time the LTC6813-1 is in the MEASURE state versus the low power SLEEP state. The amount of isoSPI or SPI communication will also affect the average supply current.

Calculating Serial Throughput

For any given LTC6813-1 the calculation to determine communication time is simple: it is the number of bits in the transmission multiplied by the SPI clock period being used. The control protocol of the LTC6813-1 is very uniform so almost all commands can be categorized as a write, read or an operation. Table 60 can be used to determine the number of bits in a given LTC6813-1 command.

ENHANCED APPLICATIONS

Using the LTC6813-1 with Fewer than 18 Cells

Cells can be connected in a conventional bottom (C1) to top (C18) sequence with all unused C inputs either shorted to the highest connected cell or left open. The unused S pins can simply be left unconnected.

Alternatively, to optimize measurement synchronization in applications with fewer than eighteen cells, the unused C pins may be equally distributed between the top of the third MUX (C18), the top of the second MUX (C12) and the top of the first MUX (C6). See Figure 47. If the number of cells being measured is not a multiple of three, the top MUX(es) should have fewer cells connected. The unused cell inputs should be tied to the other unused inputs on the same MUX and then connected to the battery stack through a 100Ω resistor. The unused inputs will result in a reading of 0.0V for those cells.

Current Measurement with a Hall-Effect Sensor

The LTC6813-1 auxiliary ADC inputs (GPIO pins) may be used for any analog signal, including active sensors with 0V to 5V analog outputs. For battery current measurements, Hall-effect sensors provide an isolated, low power solution. Figure 48 shows schematically a typical Hall-effect sensor that produces two outputs that proportion to the V_{CC} provided. The sensor in Figure 48 has two bidirectional outputs centered at half of V_{CC}. CH1 is a 0A to 50A low range and CH2 is a 0A to 200A high range. The sensor is powered from a 5V source and produces analog outputs that are connected to GPIO pins or inputs of the

Table 60. Daisy Chain Serial Time Equations

COMMAND TYPE	CMD BYTES + CMD PEC	DATA BYTES + DATA PEC PER IC	TOTAL BITS	COMMUNICATION TIME
Read	4	8	(4 + (8 • #ICs)) • 8	Total Bits • Clock Period
Write	4	8	(4 + (8 • #ICs)) • 8	Total Bits • Clock Period
Operation	4	0	4 • 8 = 32	32 • Clock Period

APPLICATIONS INFORMATION

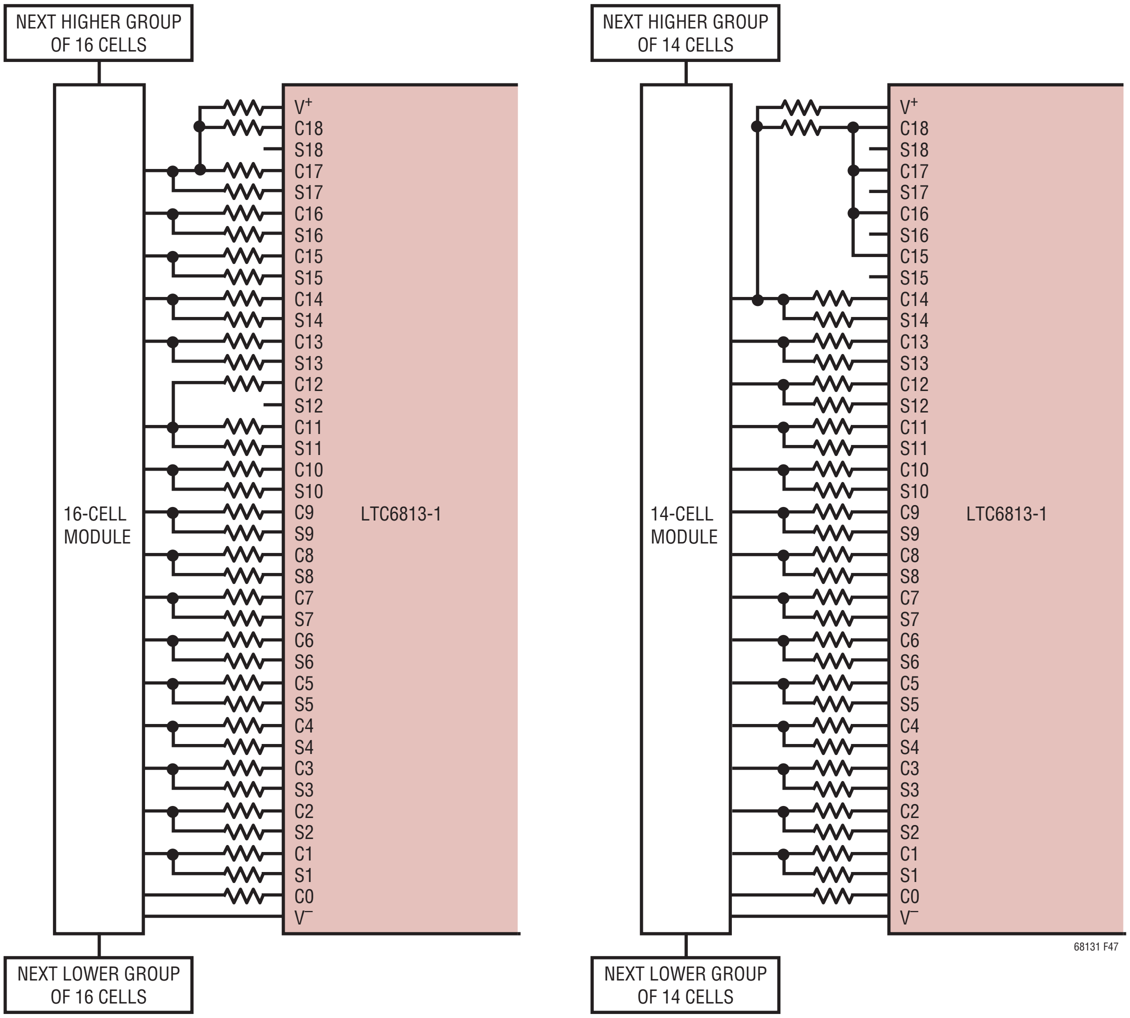


Figure 47. Cell Connection Schemes for 16 and 14 Cells

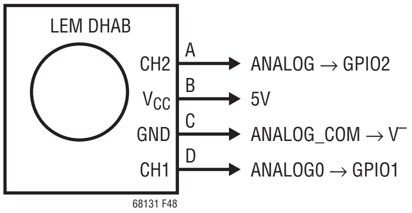


Figure 48. Interfacing a Typical Hall-Effect Battery Current Sensor to Auxiliary ADC Inputs

APPLICATIONS INFORMATION

MUX application shown in Figure 50. The use of GPIO1 and GPIO2 as the ADC inputs has the possibility of being digitized within the same conversion sequence as the cell inputs (using the ADCVAX command), thus synchronizing cell voltage and cell current measurements.

READING EXTERNAL TEMPERATURE PROBES

Figure 49 shows the typical biasing circuit for a negative temperature coefficient (NTC) thermistor. The 10k at 25°C is the most popular sensor value and the V_{REF2} output stage is designed to provide the current required to bias several of these probes. The biasing resistor is selected to correspond to the NTC value so the circuit will provide 1.5V at 25°C (V_{REF2} is 3V nominal). The overall circuit response is approximately –1%/°C in the range of typical cell temperatures, as shown in the chart of Figure 49.

Expanding the Number of Auxiliary Measurements

The LTC6813-1 has nine GPIO pins that can be used as ADC inputs. In applications that need to measure more than nine signals, a multiplexer (MUX) circuit can be implemented to expand the analog measurements to sixteen different signals (Figure 50). The GPIO1 ADC input is used for measurement and MUX control is provided by the I^2C port on GPIO 4 and 5. The buffer amplifier was selected for fast settling and will increase the usable throughput rate.

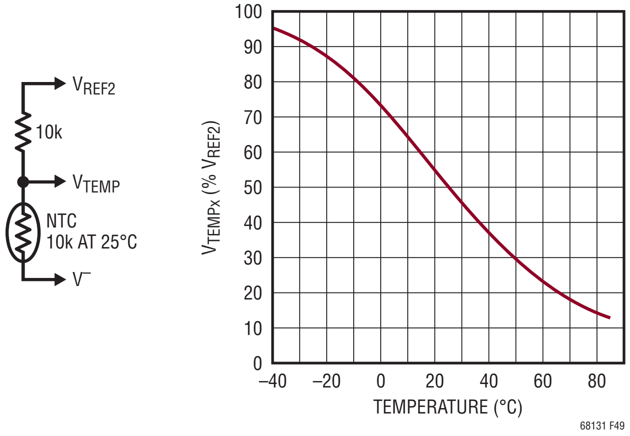


Figure 49. Typical Temperature Probe Circuit and Relative Output

APPLICATIONS INFORMATION

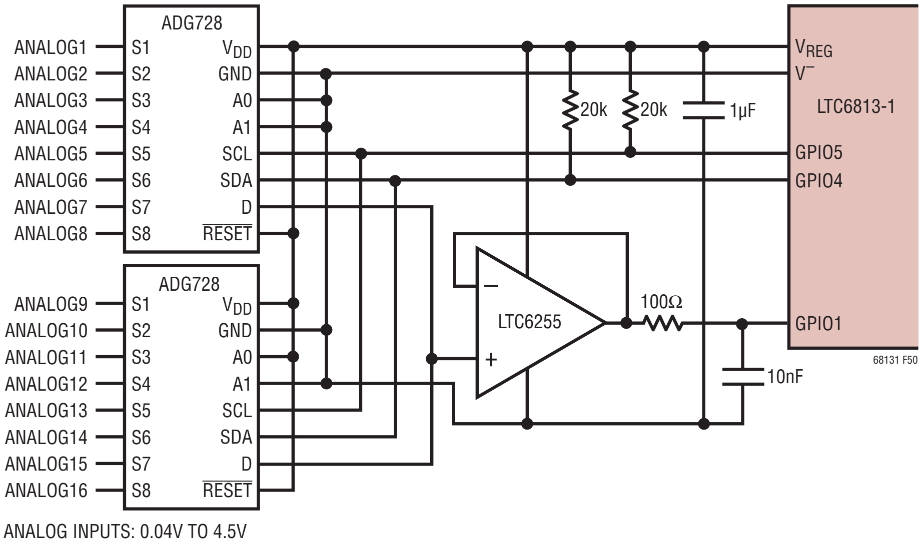
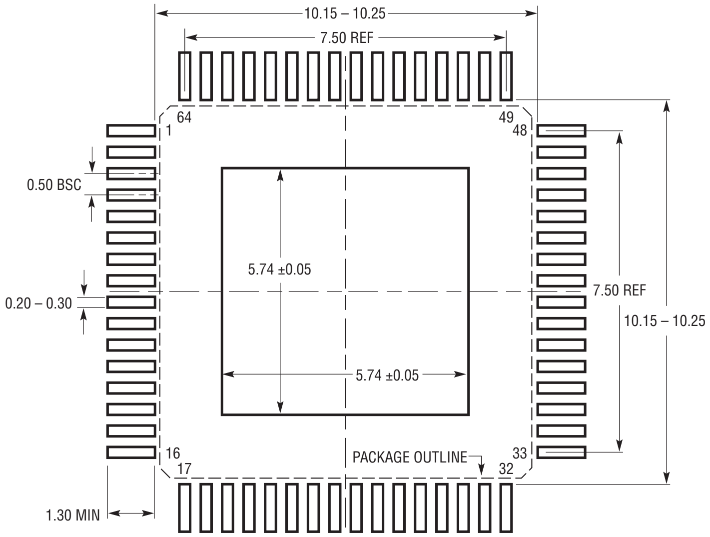


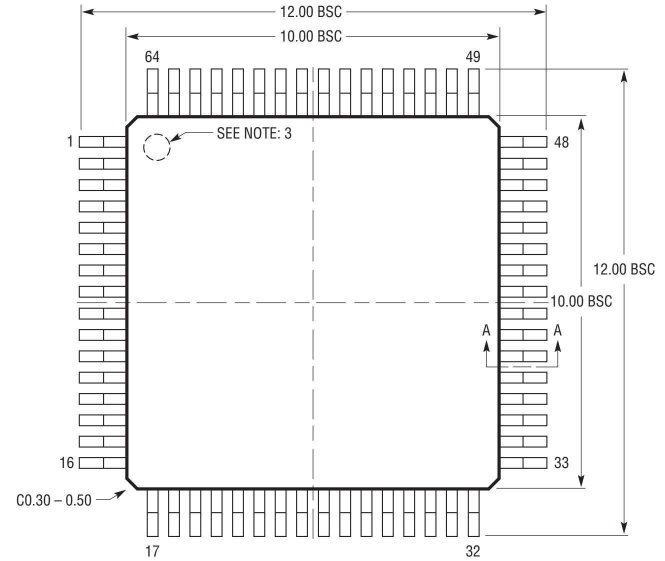
Figure 50. MUX Circuit Supports Sixteen Additional Analog Measurements

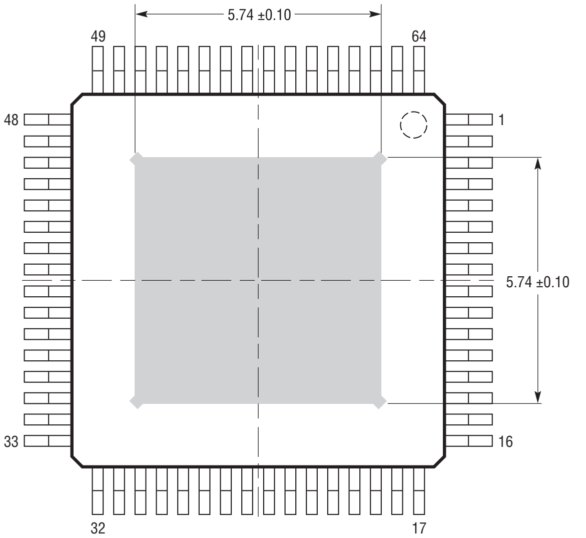
PACKAGE DESCRIPTION

LWE Package
64-Lead Plastic Exposed Pad LQFP (10mm × 10mm)
(Reference LTC DWG #05-08-1982 Rev A)

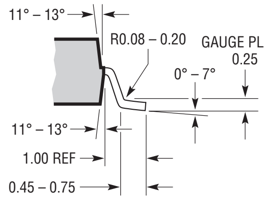


RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

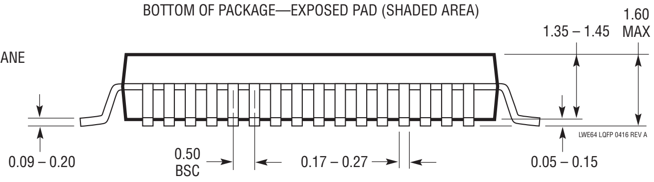




BOTTOM OF PACKAGE—EXPOSED PAD (SHADED AREA)



SECTION A – A



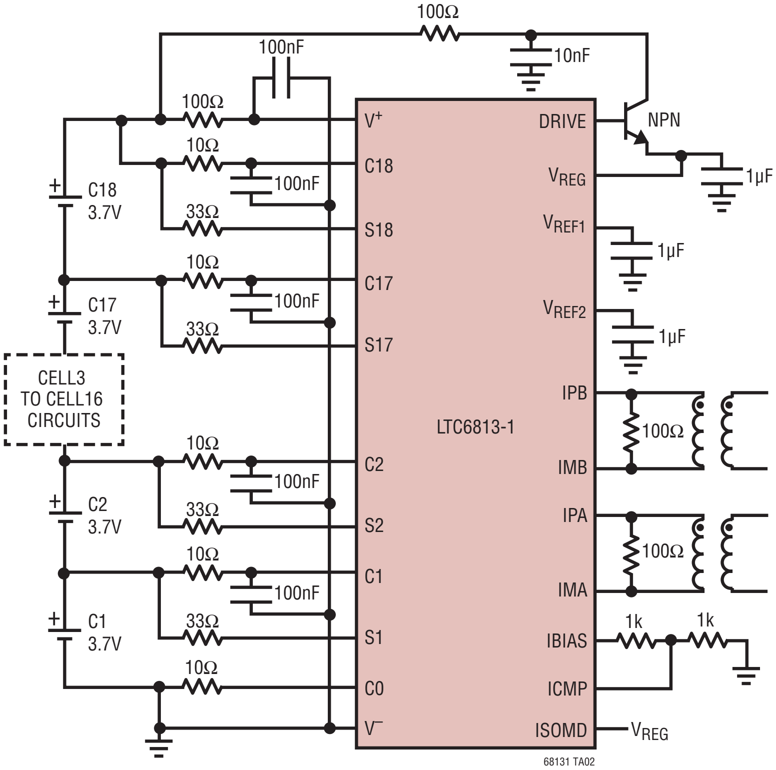
SIDE VIEW

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND MAX 0.50mm (20 MILS) ON ANY SIDE OF THE EXPOSED PAD, MAX 0.77mm (30 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
4. DRAWING IS NOT TO SCALE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/19	Title Changed	1
		Added Automotive Qualification to Front Page Features	1
		Added Order Information for Tape and Reel	3
		Added Note Regarding Automotive Products	3
		Added Plot *Measurement Error Due to IR Reflow*	10
		Added Plot V_{REF2} *Change Due to IR Reflow*	12
		Updated Figure 1 *LTC6813-1 Operation State Diagram*	18
		Voltage Range Changed from *2.988V to 3.012V* to *2.990V to 3.014V (2.992V to 3.012V for LTC6813I*) Under Accuracy Check Section	29
		Updated Figure 18 *LTC6813-1 Operation State Diagram Capacitive Coupled Daisy-Chain Configuration*	42
		Voltage Range Changed from *2.988V to 3.12V* to *2.990V to 3.014V (2.992V to 3.012V for LTC6813I)* Under REF, Table 56, Memory Bit Description	65
		Added PWMx (PWM Discharge Control) to Table 56. Memory Bit Description	66
		Rewrote the Section *Improved Regulator Power Efficiency*	67
		Updated Figure 34 *Internal ESD Protection Structures of the LTC6813-1*	68
		Updated Figure 37 *ADC Command Order*	70
		Renumbered the Steps for Discharge Verification Circuitry	74
		Updated Figure 43 *Daisy Chain Interface Components*	77
		Rewrote the Last Paragraph Section *Transformer Selection Guide*	79
		Updated Figure 45 *Capacitive Isolation Coupling for LTC6813-1x on the Same PCB*	79
		Updated Figure 47 *Cell Connection Schemes for 16 and 14 Cells*	83
		Updated Related Parts Section	88

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6811-1/ LTC6811-2	4th Generation 12-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 12 Series Battery Cells. Daisy-Chain Capability Allows Multiple Devices to Be Connected to Measure Many Battery Cells Simultaneously Via the Built-In 1MHz, 2-Wire Isolated Communication (isoSPI). Includes Capability for Passive Cell Balancing.
LTC6820	isoSPI Isolated Communications Interface	Provides an Isolated Interface for SPI Communication Up to 100 Meters, Using a Twisted Pair. Companion to the LTC6804, LTC6806, LTC6811, LTC6812 and LTC6813.
LTC6812-1	4th Generation 15-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 15 Series Battery Cells. The isoSPI Daisy-Chain Capability Allows Multiple Devices to Be Interconnected to Measure Many Battery Cells Simultaneously. The isoSPI Bus Can Operate Up to 1MHz and Can Be Operated Bidirectionally for Fault Conditions, Such As a Broken Wire or Connector. Includes Internal Passive Cell Balancing Capability of Up to 200mA.

Стандарт
Электрон
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