swissbit®

Product Data Sheet

Industrial SD Memory Card

S-200 Series

SPI, SD compliant

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made in germany

S-200 Series
Industrial SD Memory Card

1 Feature

- Custom-designed, highly-integrated memory controller
  - Fully compliant with SD Memory Card specification 2.0
  - Four integrated 4KByte Sector Buffers for fast data transfer
  - SPI Mode support
- Standard SD Memory Card form factor
  - 32.0mm x 24.0mm x 2.1mm
  - Write Protect slider
- 2.7...3.6V normal operating voltage
- 2.0...3.6V basic communication (CMD0, 15, 55 ACMD41) voltage
- Low-power CMOS technology
- Wear Leveling: equal wear leveling of static and dynamic data
  The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed.
- Patented power-off reliability
  - No data loss of older sectors
  - Max. 16 sectors data loss (old data kept) if power off during writing
- High reliability
  - Best available SLC NAND Flash technology
  - Designed for embedded market
  - MTBF: > 3,000,000 hours
  - Number of insertions: >10,000
  - Extended Temperature range -25° up to 85°C
  - Optional industrial Temperature range available -40° up to 85°C
- Hot swappable
- High performance
  - SD burst up to 25MB/s
  - SD Low speed 0...25MHz clock rate
  - SD High speed 25...50MHz clock rate
  - Flash burst up to 40MB/s
- Available densities
  - up to 2GBytes (higher densities are in the SDHC S-220 Series available up to 8GB)
- Controlled BOM
- Life Time Monitoring SD/SPI with standard or vendor commands

2 Order Information

2.1 Extended and Industrial Temperature range

Table 1: Product List for standard products

Capacity	Part Number
512MB	SFSD0512LgBN1TO-t-ME-1x1-STD
1GB	SFSD1024LgBN2TO-t-ME-1x1-STD
2GB	SFSD2048LgBN2TO-t-DF-1x1-STD

g defines the product generation
t defines the temperature range (E=-25°C to +85°C, I=-40°C to +85°C)
x defines the FW

2.2 Current product list

Table 2: General Product List

Capacity	Part Number
512MB	SFSD0512L1BN1TO-E-ME-161-STD
1GB	SFSD1024L1BN2TO-E-ME-161-STD
2GB	SFSD2048L1BN2TO-E-DF-161-STD
512MB	SFSD0512L1BN1TO-I-ME-161-STD
1GB	SFSD1024L1BN2TO-I-ME-161-STD
2GB	SFSD2048L1BN2TO-I-DF-161-STD

2.3 Offered options for customer projects

- Customer specified strings and IDs (MID, OID, PNM, PRV)
- Customer specified capacities
- Preload service
- Customized labels & lasering

Contents

3 Product Specification

The SD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The Card operates in two basic modes:

- **SD card mode**
- **SPI mode**

The SD Memory Card also supports SD **High Speed mode** with up to 50MHz clock frequency.
The cards are compliant with

- SD Memory Card Specification Part 1, Physical layer Specification V2.00
- SD Memory Card Specification Part 2, File System Specification V2.00

The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware RS-code **Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
The hardware RS-code ECC allows to detect and correct **4 symbols per 528 Bytes**.

The Card has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The power consumption is very low.
The data retention is 10 years @ life begin.
The cards are offered in 2 temperature ranges

- Extended -25°C...85°C
- Industrial -40...85°C on request

The cards are RoHS compliant and lead-free.

3.1 System Performance

Table 3: Performance

System Performance		typ	max	Unit
Burst Data transfer Rate (max clock 50MHz)			25 (166X)(1)	MB/s
Sustained Sequential Read	512MB	18.4 (1)(2)	21	
	1GB – 2GB	18.4 (1)(2)	21	
Sustained Sequential Write	512MB	6.6 (1)(2)	13	
	1GB – 2GB	12.8 (1)(2)	18	

1. All values refer to Toshiba Flash 4Gb SD Memory Card in 4bit SD mode 50MHz, cycle time 20ns, write/read file sequential.
2. Sustained Speed measured with SanDisk Mobile mate USB-SD Memory Card reader. It depends on burst speed, flash type and number, and file size

3.2 Environmental Specifications

3.2.1 Recommended Operating Conditions

Table 4: SD Memory Card Recommended Operating Conditions

Parameter	min	typ	max	Unit
Commercial Operating Temperature	0	25	70	°C
Industrial Operating Temperature	-40	25	85	°C
Power Supply VCC (3.3V)	2.7	3.3	3.6	V

Table 5: Current consumption

Current Consumption (type)	typ	max	Unit
Read	28	40	mA
Write	55	60	
Sleep Mode	0.2	0.3	

3.2.2 Recommended Storage Conditions

Table 6: SD Memory Card Recommended Storage Conditions

Parameter	min	typ	max	Unit
Commercial Storage Temperature	-40	25	85	°C
Industrial storage Temperature	-40	25	100	°C

3.2.3 Humidity & ESD

Table 7: Humidity & ESD

Parameter	Operating	Non Operating
Humidity (non-condensing)	max 95%	
ESD according to IEC61000-4-2 Human body model ±4 kV 100 pf/1.5 kOhm Machine model ±0.25 kV 200 pf/0 Ohm	**Non Contact Pads area:** ±8 kV (coupling plane discharge) ±15 kV (air discharge) Human body model according to IEC61000-4-2	**Contact Pads:** ±4 kV, Human body model according to IEC61000-4-2

3.2.4 Durability

Table 8: Durability

Parameter	Operating	Non Operating
Salt water spray	3% NaCl/35°C; 24h acc. MIL STD Method 1009	
Solar Exposure	1000W/m2 @ 400°C	
Impermeability	IP67	
UV Light Exposure	UV: 254nm, 15Ws/cm2	
Insertions	>10,000	
Drop test	1.5m free fall	
Bending	10N	
Torque	0.15Nm or ±2.5deg	
Bump	25g; 6ms; ±3 x 4000 shocks	
Shock	1000 g max.	
Vibration (peak -to-peak)	15G max.	
Minimum moving force of WP slider	0.4N	

3.3 Physical Dimensions

Table 9: Physical Dimensions

Physical Dimensions	Value	Unit
Length	32.00±0.10	mm
Width	24.00±0.10	
Thickness	2.10±0.15	
Weight (typ.)	2	g

3.4 Reliability

Table 10: Reliability

Parameter	Value
Data Retention	10 years (JEDEC47G)

4 Capacity specification

Table 11: SD Memory Card capacity specification

Capacity	Sectors_card	Total addressable capacity (Byte)
512MB	998,912	511,442,944
1GB	2,001,920	1,024,983,040
2GB	4,016,128	2,056,257,536

5 Card physical

5.1 Physical description

The SD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 1 and Figure 2 show card dimensions.

Figure 1: Mechanical Dimensions SD Memory Card

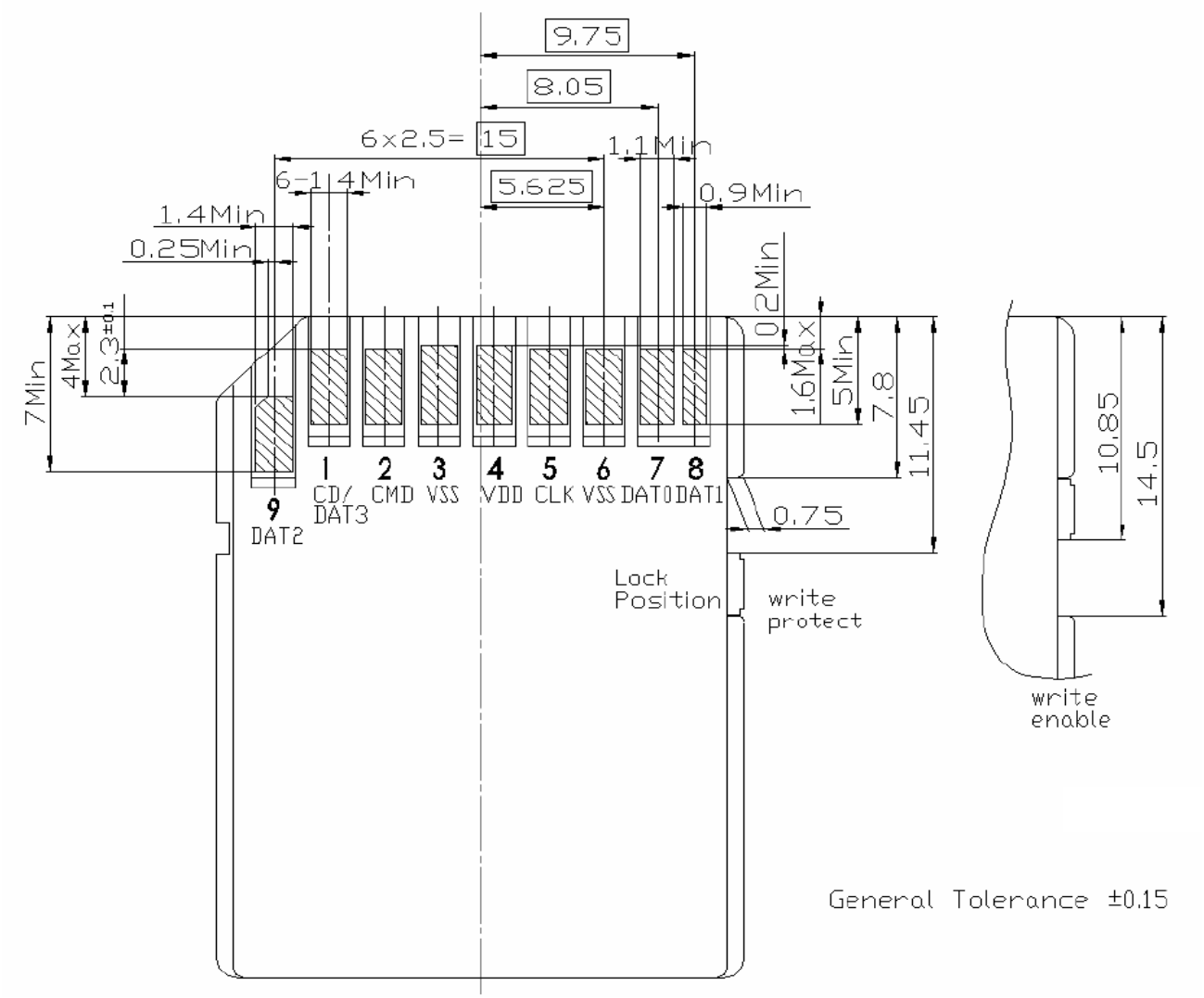
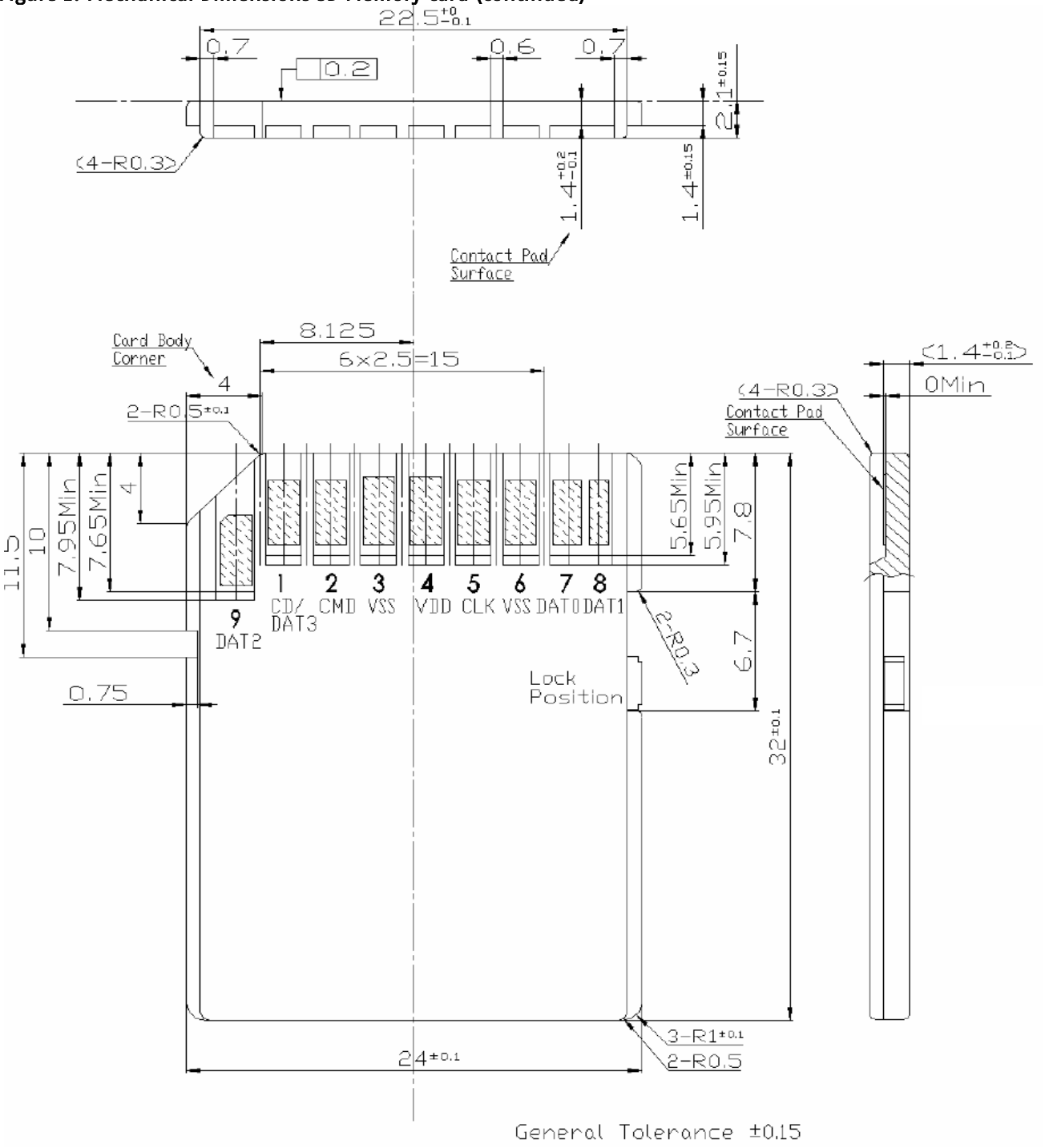


Figure 2: Mechanical Dimensions SD Memory Card (continued)



6 Electrical interface

6.1 Electrical description

Figure 3: SD Memory Card Block Diagram

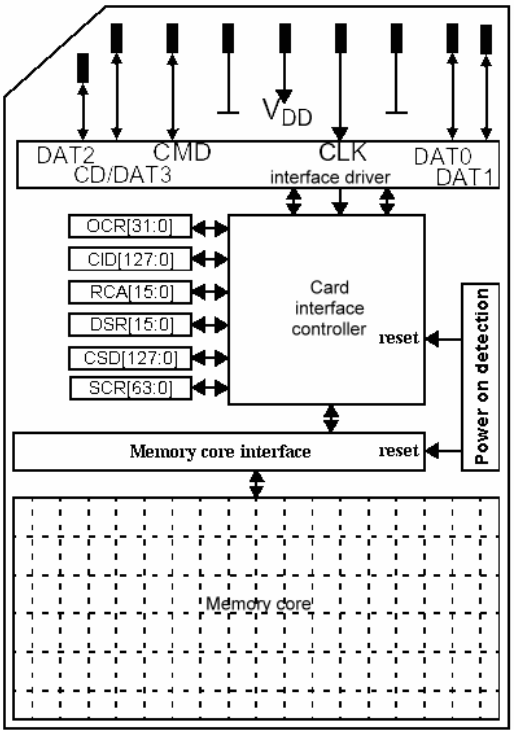


Figure 4: SD Memory Card Shape and Interface (Top View)

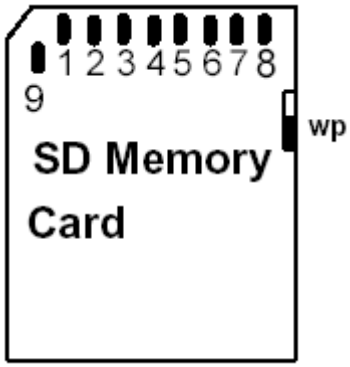


Table 12: SD Memory Card Pad Assignment

Pin #	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1[4]	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2[5]	I/O/PP	Data Line [Bit 2]	RSV		

Notes:

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50k0hm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

6.2 DC characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

Table 13: DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
	Peak Voltage on all Lines	-0.3		V_{DD}+0.3	V	
V_{OH}	Output HIGH Voltage	0.75*V_{DD}			V	at -2mA
V_{OL}	Output LOW Voltage			0.125*V_{DD}	V	at 2mA
V_{IH}	Input HIGH Voltage	0.625*V_{DD}		V_{DD}+0.3	V	
V_{IL}	Input LOW Voltage	-0.3		0.25*V_{DD}	V	
I_{DD}	Operating Current		35	50	mA	
	Pre-initialization Standby Current			3	mA	
	Post-initialization Standby Current		100	200	µA	
I_{LI}	Input Leakage Current	-10		10	µA	without pull up R
I_{LO}	Output Leakage Current	-10		10	µA	

Figure 5: Bus Signal levels

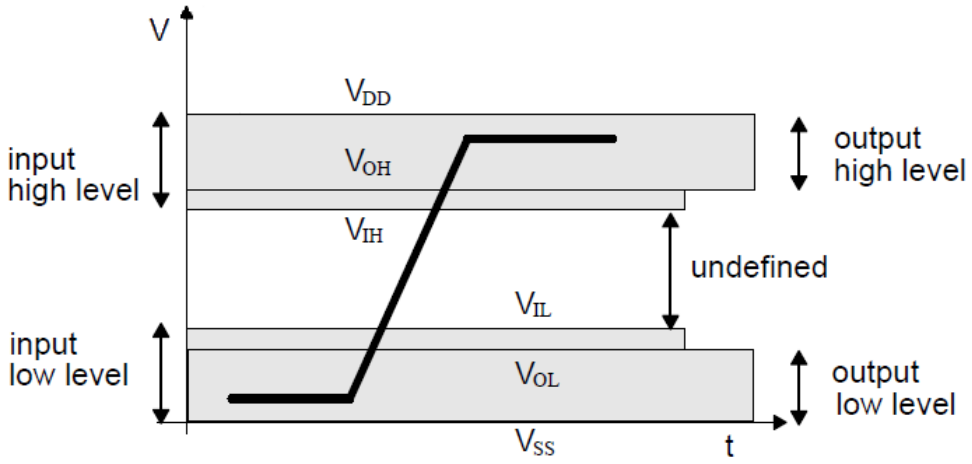


Table 14: SD Memory Card Recommended Operating Conditions

Symbol	Parameter		min	typ	max	unit
V_{DD}	Supply Voltage	Normal Operating Status	2.7	3.3	3.6	V
		Basic Communication (CMD0, CMD15, CMD55, ACMD41)	2.0	3.3	3.6	V
-	Power Up Time (from 0V to VDD min)				250	ms

6.3 Signal Loading

The total capacitance C_L is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS}, and the capacitance C_{CARD} of the card connected to the line:

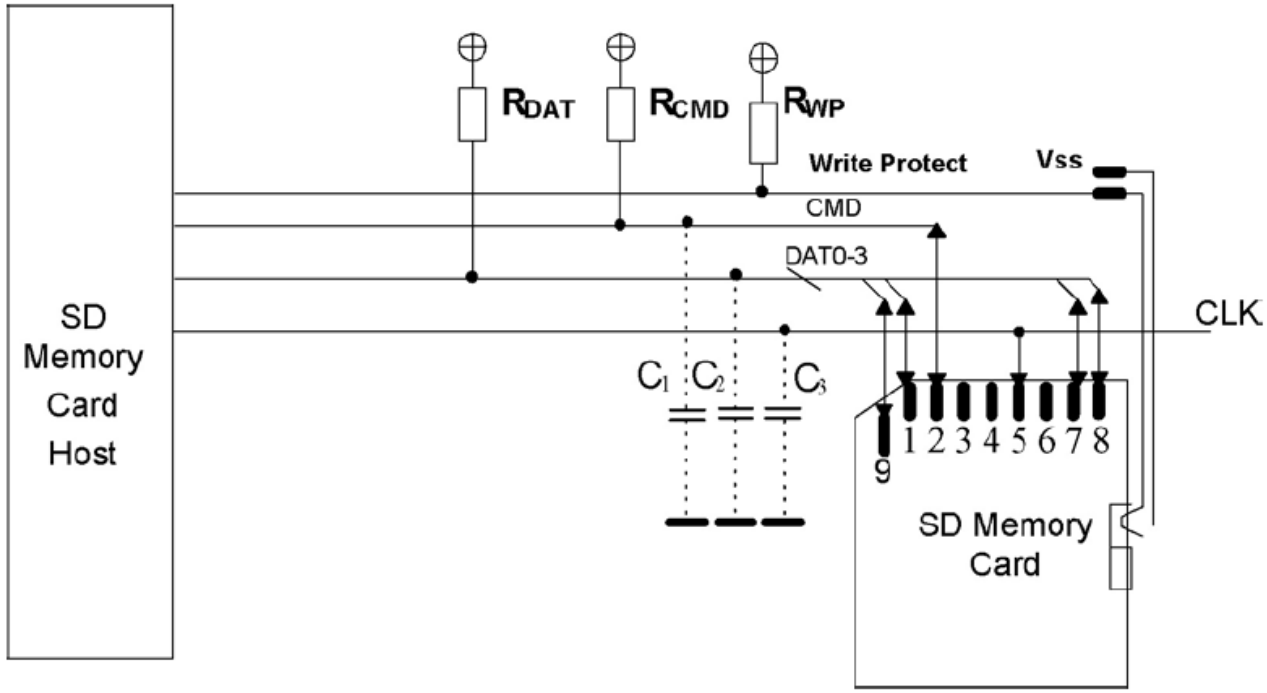
$C_L = C_{HOST} + C_{BUS} + C_{CARD}$

To allow the sum of the host and bus capacitances to be up to 20pF for the card, the following conditions in the table below are met by the card.

Table 15: Signal loading

Parameter	Symbol	Min	Max	Unit	Notes
Pull up resistance	R_{CMD},R_{DAT}	10	100	kOhm	To prevent bus floating
Pull up resistance inside card (pin1)	R_{DAT3}	10	90	kOhm	May be used for card detection
Bus signal line capacitance for each signal line	C_L		40	pF	Single card C_{HOST}+C_{BUS} shall not exceed 30pF
Signal card capacitance for each signal pin	C_{CARD}		10	pF	Single card
Signal line inductance			16	nH	f ≤ 20MHz
Capacioty Connected to Power line	C_C		5µF	µF	To prevent inrush current

Figure 6: Signal Loading



6.4 AC characteristics

6.4.1 Default Speed mode (0 – 25MHz)

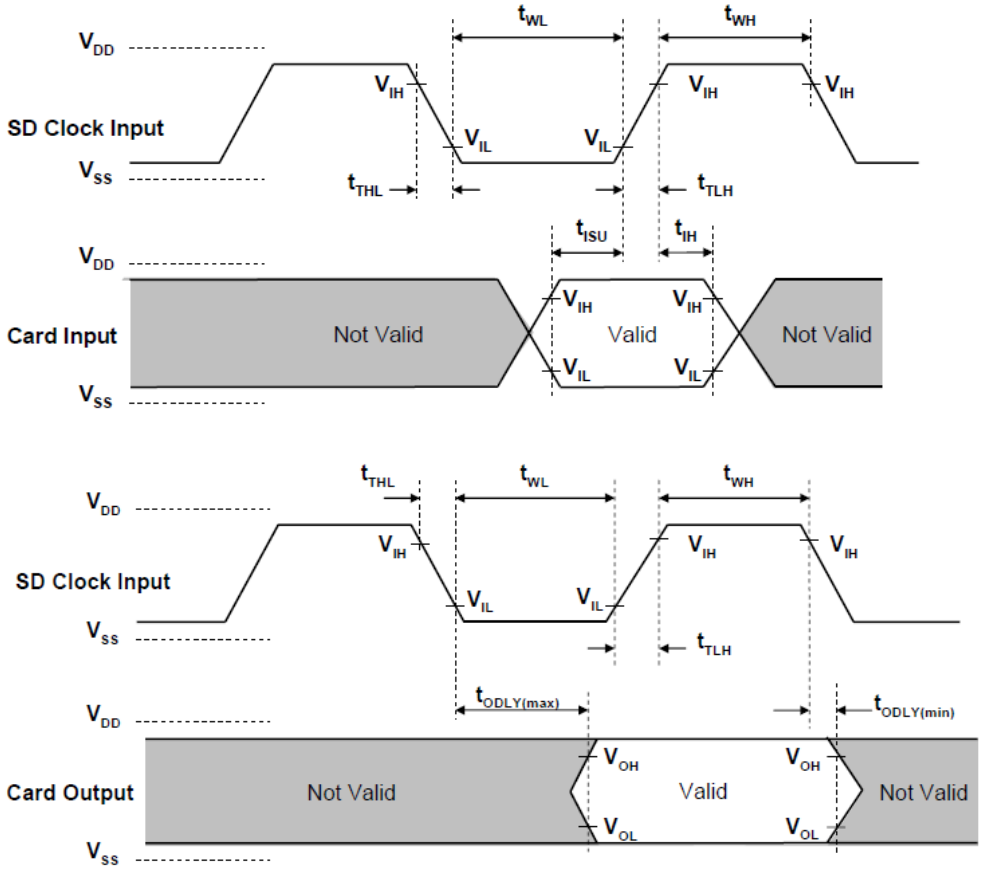
Table 16: AC Characteristics Default Speed Mode

Parameter	Symbol	Min	Max	Unit	Notes
Clock Clk All values are referred to min (VIH) and max (VIL)					
Clock frequency in data transfer mode	f_{PP}	0	25	MHz	$C_{CARD} \leq 10pF$ (1 card)
Clock frequency in card id mode	f_{OD}	0/100 1)	400	kHz	
Clock low time	t_{WL}	10		ns	
Clock high time	t_{WH}	10		ns	
Clock rise time	t_{TLH}		10	ns	
Clock fall time	t_{THL}		10	ns	
Inputs CMD, DAT (referenced to CLK)					
CMD, DAT input setup time	t_{ISU}	5		ns	$C_{CARD} \leq 10pF$ (1 card)
CMD, DAT input hold time	t_{IH}	5		ns	
Outputs CMD, DAT (referenced to CLK)					
CMD, DAT output delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$C_L \leq 40pF$ (1 card)
CMD, DAT output delay time during Identification Mode	t_{ODLY}	0	50	ns	

Notes

1. 0 kHz means to stop the clock. The minimum clock frequency should not be below 100kHz

Figure 7: AC Characteristics Default Speed Mode



6.4.2 High Speed mode (0 – 50MHz)

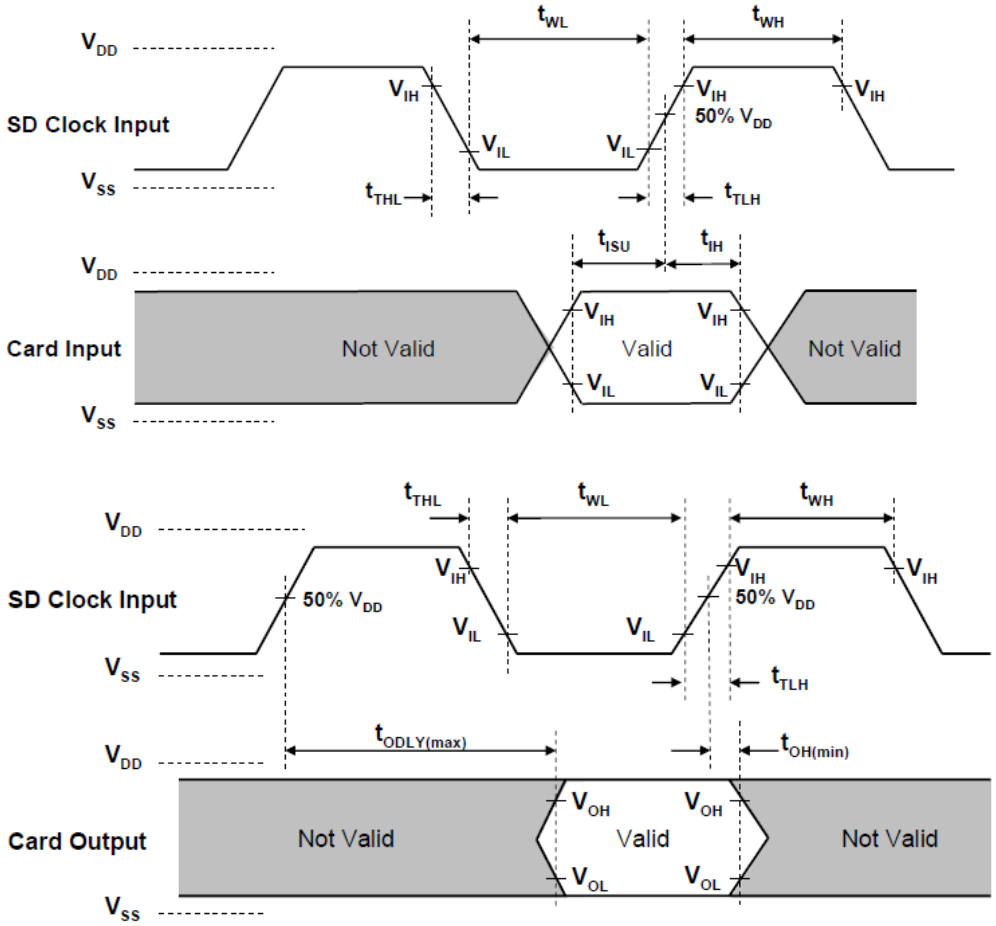
Table 17: AC Characteristics High Speed Mode

Parameter	Symbol	Min	Max	Unit	Notes
Clock Clk All values are referred to min (VIH) and max (VIL)					
Clock frequency in data transfer mode	f_{PP}	0	50	MHz	$C_{CARD} \leq 10pF$ (1 card)
Clock low time	t_{WL}	7		ns	
Clock high time	t_{WH}	7		ns	
Clock rise time	t_{TLH}		3	ns	
Clock fall time	t_{THL}		3	ns	
Inputs CMD, DAT (referenced to CLK)					
input setup time	t_{ISU}	6		ns	$C_{CARD} \leq 10pF$ (1 card)
input hold time	t_{IH}	2		ns	
Outputs CMD, DAT (referenced to CLK)					
output delay time during data transfer mode	t_{ODLY}		14	ns	$C_L \leq 40pF$ (1 card)
output hold time	t_{OH}	2.5		ns	$C_L \geq 15pF$ (1 card)

Notes

1. In order to satisfy severe timing, the host shall drive only one card with max 40pF total at each line.

Figure 8: AC Characteristics High Speed Mode



7 Host access Specification

The following chapters summarize how the host accesses the card:

- Chapter 7.1 summarizes the SD and SPI buses.
- Chapter 7.2 summarizes the registers.

7.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

7.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

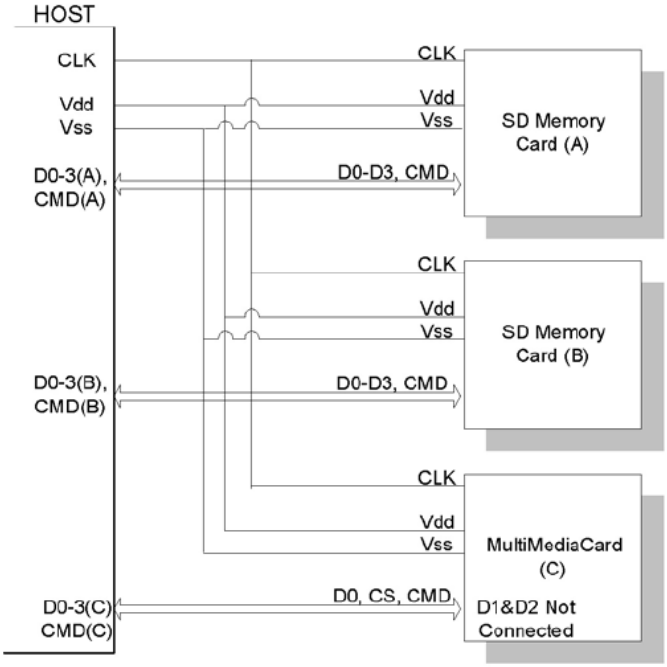
- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

The SD bus signals are listed in Table 18, and the SD bus topology is illustrated in Figure 9: SD Bus Topology.

Table 18: SD Bus Signals

Signal	Description
CLK	Host to card clock signal
CMD	Bidirectional Command/Response signal
DAT0-DAT3	4 Bidirectional data signals
Vdd, Vss	Power and Ground

Figure 9: SD Bus Topology



7.1.2 SPI Bus Mode Protocol

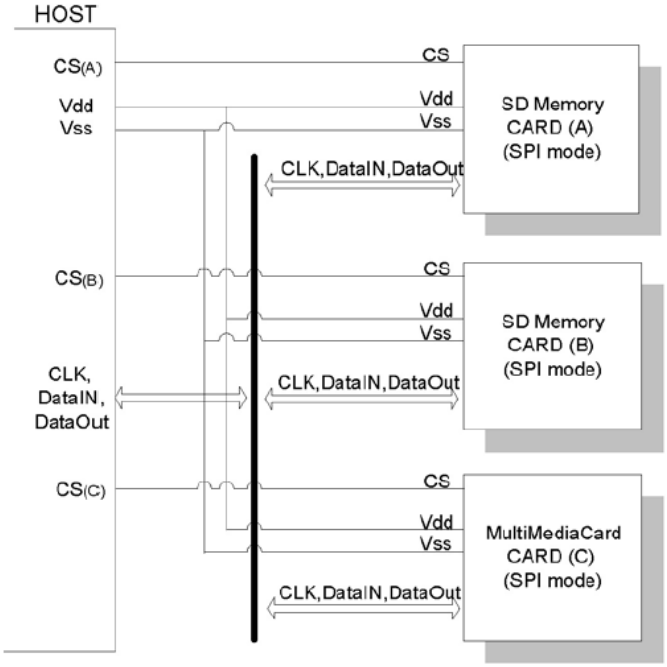
The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

The SPI bus signals are listed Table 19 and the SPI bus topology is illustrated in Figure 10.

Table 19: SPI Bus Signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

Figure 10: SPI bus topology



7.1.3 Mode Selection

The SD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in *idle_state*. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.
During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is MultiMediaCard. In that case it should re-start the card as MultiMediaCard using CMD0 and CMD1.

7.2 Card Registers

The SD Memory Card has five registers. Refer to Table 20 to Table 25 for detail.

Table 20: SD Memory Card registers

Register Name	Bit Width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA	16	Relative Card Address	This register carries the card address is SD Memory Card mode.

Table 21: CID register

Register Name	Bit Width	Description	typ. value
MID	8	Manufacture ID	0x5d
OID	16	OEM/Application ID	0x5342
PNM	40	Product Name	"LxBNc" c=number of channels
PRV	8	Product Version	0x04

			can change
PSN	32	Product Serial Number	xxxxxxxx
–	4	Reserved	0x0
MDT	12	Manufacture Date	0xyym
CRC	7	Check sum of CID contents	chksm
–	1	Not used; always=1	1

Table 22: OCR register

OCR bit position	VDD voltage window	typ. value	OCR bit position	VDD voltage window	typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24-30	Reserved	
13	2.5-2.6	0	30	Card Capacity Status (CCS)	*1)
14	2.6-2.7	0	31	0=busy; 1=ready	*2)

Notes

1. This bit is valid only when the card power up status bit is set.
2. This bit is set to LOW if the card has not finished the power up routine.

Table 23: CSD register

Register Name	First Bit	Bit Width	Description	typ. Value
CSD_STRUCTURE	127	2	CSD structure	00
–	125	6	Reserved	000000
TAAC	119	8	Data read access time 1	00001110
NSAC	111	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	103	8	Data transfer rate	00110010
CCC	95	12	Card command classes	010110110101
READ_BL_LEN	83	4	Read data block length	1001
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	1
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0
DSR_IMP	76	1	DSR implemented	0
–	75	2	Reserved	00
C_SIZE	73	12	Device size	xxx*)
VDD_R_CURR_MIN	61	3	VDD min read current	110
VDD_R_CURR_MAX	58	3	VDD max read current	110
VDD_W_CURR_MIN	55	3	VDD min write current	110
VDD_W_CURR_MAX	52	3	VDD max write current	110
C_SIZE_MULT	49	3	Device size multiplier	110*)
ERASE_BLK_EN	46	1	Erase single block enable	1
SECTOR_SIZE	45	7	Erase sector size	1111111
WP_GRP_SIZE	38	7	Write protect group size	0000001*)
WP_GRP_ENABLE	31	1	Write protect group enable	0
–	30	2	Reserved	00
R2W_FACTOR	28	3	Write speed factor	100
WRITE_BL_LEN	25	4	Write data block length	1001*)
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0
–	20	5	Reserved	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(1)
COPY	14	1	Copy flag	0 W(1)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(1)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W
FILE_FORMAT	11	2	File format	00 W(1)
–	9	2	Reserved	00 W
CRC	7	7	Checksum of CSD contents	xxxxxxx W
–	0	1	Always=1	1

*) Drive Size and block sizes vary with card capacity
memory capacity = BLOCKNR * BLOCK_LEN
Where
BLOCKNR = (C_SIZE+1) * MULT
MULT = $2^{C\_SIZE\_MULT+2}$ (C_SIZE_MULT < 8)
BLOCK_LEN = $2^{READ\_BL\_LEN}$, (READ_BL_LEN < 12)

W value can be changed with CMD27 (PROGRAM_CSD)
W(1) value can be changed ONCE with CMD27 (PROGRAM_CSD)

Table 24: SCR register

Field	Bit Width	typ Value
SCR_STRUCTURE	4	0000
SD_SPEC	4	0010
DATA_STAT_AFTER_ERASE	1	1
SD_SECURITY	3	011
SD_BUS_WIDTHS	4	0101
Reserved	16	0
Reserved	32	0

Table 25: RCA register

Field	Bit Width	typ Value
RCA	16	0x0000*)

*) After Initialization the card can change the RCA register.

8 Card Lifetime Information Data

Swissbit S-200/S-220 cards provide various lifetime monitoring information in the "reserved for manufacturer" field of the SD Status register. This data can be read out using ACMD13 (SD_STATUS) on host systems with a native SD-Interface (e.g. embedded systems, SD or SPI interface or PCI/SD-reader).

We recommend assessing the expected/guaranteed life time of Flash based devices to make sure the product life time fulfills your expectations. The real application workload should be tested in a test installation or simulation for best accuracy.
In general, calculations based on application behavior statistics are not possible as the influence of the operating systems (with the caches) and the file system have a big influence on the data actually written on the device.

This product does report the real erase cycles that the NAND Flash blocks have seen. Based on the average erase count and it's ascend in the target system, it is possible to quite simply calculate the expected life time of the product.

Bad and spare block counts can't be used for linear life time calculations. In the beginning of the device life time, only very few blocks will be needed to be replaced. Generally if a device reaches the end of the lifetime, more bad blocks will occur.

The SD Status is defined by the SD Standard and contains several status bits as well as a field for manufacturer specific data. The overall size of the SD Status is one data block of 512 bits divided into 312 reserved for manufacturer bits used for the Swissbit lifetime information and 200 bits for other purposes, defined by the SDA.

The content of the SD Status register is transmitted to the Host over the DAT bus along with a 16-bit CRC. The SD Status is sent to the host over the DAT bus as a response to ACMD13 (CMD55 followed with CMD13). ACMD13 can be sent to a card only in "tran_state" (card is selected).

Please note that it is not possible so set up the necessary command (ACMD13) through a common USB/SD-card reader/bridge. In contrast to that, a lot of embedded systems and PCIe card readers support the command.

Swissbit provides a demo code written in C for Linux systems on demand.

Table 26: SD Status and Lifetime Information sector decoding

Bits	Description (All values MSb first)
[511:312]	SD Status field as defined in the Physical Layer Specification Version 2.00 (Not relevant for Card Lifetime Info)
[311:304]	Data structure version identifier ("0" for S-200/S-220 cards)
[303:288]	Number of initial defect blocks
[287:272]	Number of initial spare blocks, 1st flash CE (across channels) big Endian
[271:256]	Number of initial spare blocks, 2nd flash CE (across channels) big Endian
[255:248]	Percentage of remaining spare blocks, first flash CE (across channels)
[247:240]	Percentage of remaining spare blocks, second flash CE (across channels)
[239:224]	(Reserved)
[223:192]	(Reserved)
[191:176]	Lowest wear level class (WL)
[175:160]	Highest wear level class (WH)
[159:144]	Wear level threshold (T)
[143:96]	Total number of block erases
[95:80]	Number of flash blocks
[79:64]	Maximum flash block erase count target, in wear level class units
[63:32]	Power on count
[31:24]	(Reserved)
[23:16]	(Reserved)
[15:8]	(Reserved)
[7:0]	(Reserved)

The lowest wear level class (WL) and highest wear level class (WH) fields give the range of wear level classes currently in use. The wear level threshold (T) gives the size of a wear level class, minus 1, in units of flash memory block erases. Thus, the number of block erases that the flash blocks have seen is between WL*(T+1) and WH*(T+1)-1.

9 RoHS and WEEE update from Swissbit

Dear Valued Customer,

We at Swissbit place great value on the environment and thus pay close attention to the diverse aspects of manufacturing environmentally and health friendly products. The European Parliament and the Council of the European Union have published two Directives defining a European standard for environmental protection. This states that CompactFlash Cards must comply with both Directives in order for them to be sold on the European market:

- **RoHS** – Restriction of Hazardous Substances
- WEEE – Waste Electrical and Electronic Equipment

Swissbit would like to take this opportunity to inform our customers about the measures we have implemented to adapt all our products to the European norms.

What is the WEEE Directive (2012/19/EU)?

The Directive covers the following points:

- Prevention of WEEE
- Recovery, recycling and other measures leading to a minimization of wastage of electronic and electrical equipment
- Improvement in the quality of environmental performance of all operators involved in the EEE life cycle, as well as measures to incorporate those involved at the EEE waste disposal points

What are the key elements?

The WEEE Directive covers the following responsibilities on the part of producers:

Producers must draft a disposal or recovery scheme to dispose of EEE correctly.
Producers must be registered as producers in the country in which they distribute the goods.
They must also supply and publish information about the EEE categories.
Producers are obliged to finance the collection, treatment and disposal of WEEE.

Inclusion of WEEE logos on devices

In reference to the Directive, the WEEE logo must be printed directly on all devices that have sufficient space. «In exceptional cases where this is necessary because of the size of the product, the symbol of the WEEE Directive shall be printed on the packaging, on the instructions of use and on the warranty»
(WEEE Directive 2012/19/EU)

When does the WEEE Directive take effect?

The Directive came into effect internationally on 13 August, 2005.

What is RoHS (2011/65/EU)?

The goals of the Directive are to:

- Place less of a burden on human health and to protect the environment by restricting the use of hazardous substances in new electrical and electronic devices
- To support the WEEE Directive (see above)

RoHS enforces the restriction of the following 6 hazardous substances in electronic and electrical devices:

- Lead (Pb) – no more than 0.1% by weight in homogeneous materials
- Mercury (Hg) – no more than 0.1% by weight in homogeneous materials
- Cadmium (Cd) – no more than 0.01% by weight in homogeneous materials
- Chromium (Cr6+) – no more than 0.1% by weight in homogeneous materials
- PBB, PBDE – no more than 0.1% by weight in homogeneous materials

Swissbit is obliged to minimize the hazardous substances in the products.

According to part of the Directive, manufacturers are obliged to make a self-declaration for all devices with RoHS. Swissbit carried out intensive tests to comply with the self-declaration. We have also already taken steps to have the analyses of the individual components guaranteed by third-party companies.

Swissbit carried out the following steps during the year with the goal of offering our customers products that are fully compliant with the RoHS Directive.

- **Preparing all far-reaching directives, logistical enhancements and alternatives regarding the full understanding and introduction of the RoHS Directive's standards**
- **Checking the components and raw materials:**
  - Replacing non-RoHS-compliant components and raw materials in the supply chain
  - Cooperating closely with suppliers regarding the certification of all components and raw materials used by Swissbit
- **Modifying the manufacturing processes and procedures**
  - Successfully adapting and optimizing the new management-free integration process in the supply chain
  - Updating existing production procedures and introducing the new procedures to support the integration process and the sorting of materials
- **Carrying out the quality process**
  - Performing detailed function and safety tests to ensure the continuous high quality of the Swissbit product line

When does the RoHS Directive take effect?

As of June 08, 2011 only new electrical and electronic devices with approved quantities of RoHS will be put on the market.

When will Swissbit be offering RoHS-approved products?

Swissbit's RoHS-approved products are available now. Please contact your Swissbit contact person to find out more about exchanging your existing products for RoHS-compliant devices.

For your attention

We understand that packaging and accessories are not EEE material and are therefore not subject to the WEEE or RoHS Directives.

Contact details:
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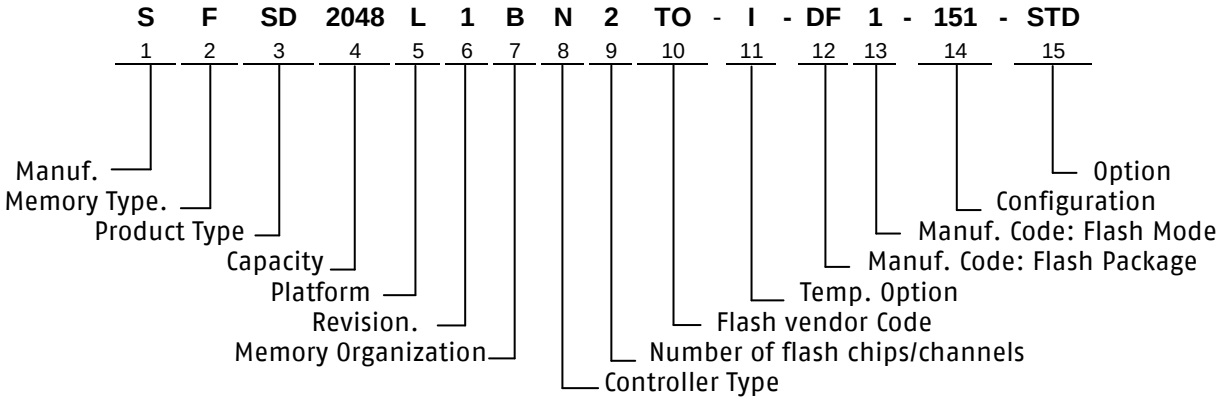
Tel: +41 71 913 03 03 – Fax: +41 71 913 03 15
E-mail: industrial@swissbit.com – Website: www.swissbit.com

10 Part Number Decoder



1. Manufacturer

Swissbit code	S

2. Memory Type

Flash	F

3. Product Type

SD Memory Card	SD

4. Capacity

512 MB	0512
1 GB	1024
2 GB	2048

5. Platform

SD Memory Card	L

6. Generation

7. Memory Organization

x8	B
x16	C

8. Technology

SD Memory Card controller	S-200	N

9. Channels

1 Flash Channel	1
2 Flash Channel	2

10. Flash Code

Samsung	SA
Micron	MT
Toshiba	TO

11. Temp. Option

Industrial Temp. Range -40°C – 85°C	I
Extended Temp. Range -25°C – 85°C	E
Standard Temp Range 0°C – 70°C	C

12. DIE Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D

13. PIN Mode

Normal nCE & R/nB	0 / E
Dual nCE & Dual R/nB	1 / F

14. Configuration XYZ

X→ Configuration

Configuration	X
default	1

Y → FW Revision

FW Revision	Y
Revision 1	1
Revision 2	2
Revision 3	3
Revision 4	4
Revision 5	5
Revision 6	6

Z → optional

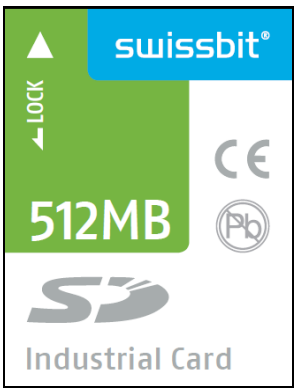
Optional	Z
optional	1

15. Option

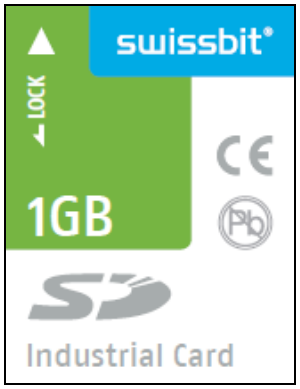
Swissbit / Standard	STD

11 Swissbit Label specification

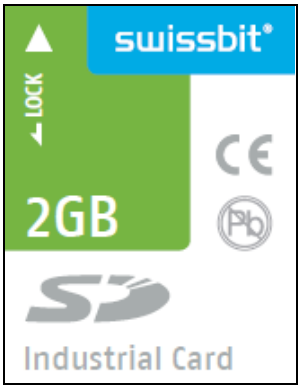
11.1 Front side label



512MB SD Memory Card



1GB SD Memory Card



2GB SD Memory Card

11.2 Back side lasering

SWISSBIT
SFSD1024L1BN2
T0-I-ME-151-STD
1012-60012345
Made in Germany
CE WEEE

Part-number
Date-Lot/Serial

Example of the back side laser marking

12 Revision History

Table 27: Document Revision History

Date	Revision	Revision Details
23-Jul-2008	1.00	Initial release
10-Dec-2008	1.02	S-200/S-210 series added, current values actualized better real speed values in CSD TAAC and R2W_Factor other CSD register corrections, document structure, new generation added
06-Mar-2009	1.03	1GB capacity corrected, FW update
04-Dec-2009	1.10	latest FW update, CMD class 7 (Lock card) added for new firmware, write CSD specified, disk size for the FW version 3 by the 1GB card adapted
28-Jul-2010	1.11	Correct High-Speed mode timing diagram, part numbers
30-Mar-2011	1.20	Samsung-NAND-Flash Versions are End of Life, and removed from Datasheet. New 512MB – 2GB Toshiba-NAND-Flash Versions added, Part number Codes updated, speed and current values updated
17-Feb-2012	1.21	Performance values updated, label and lasering update
27-Apr-2012	1.30	SDA Correction, CI update
18-June-2012	1.31	FW-Rev. 6 added
11-December-2012	1.40	New CE Declaration, new picture back side lasering
17-February-2014	1.50	DC and AC characteristics updated, CE Declaration removed
12-February-2015	1.51	Added chapter 8 "Card Lifetime Information Data"

Стандарт Электрон Связь

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