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February 2014

FDMC86259P

P-Channel PowerTrench[®] MOSFET -150 V. -13 A. 107 m Ω

Features

- Max $r_{DS(on)}$ = 107 m Ω at V_{GS} = -10 V, I_D = -3 A
- Max $r_{DS(on)}$ = 137 m Ω at V_{GS} = -6 V, I_D = -2.7 A
- Very low RDS-on mid voltage P channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL Tested
- RoHS Compliant

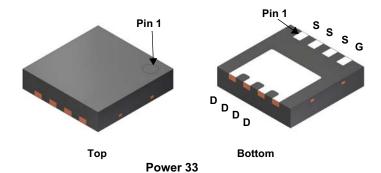


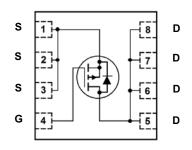
General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- Active Clamp Switch
- Load Switch





MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V _{DS}	Drain to Source Voltage			-150	V
V _{GS}	Gate to Source Voltage			±25	V
	Drain Current -Continuous	T _C = 25 °C		-13	
I _D	-Continuous	T _A = 25 °C	(Note 1a)	-3.2	Α
	-Pulsed			-20	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	181	mJ
D	Power Dissipation	T _C = 25 °C		62	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to + 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86259P	FDMC86259P	Power 33	13"	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	ncteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-150			V
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		-88		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -120 V, V _{GS} = 0 V			-1	μΑ
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \mu A$	-2	-2.8	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, referenced to 25 °C		6		mV/°C
		$V_{GS} = -10 \text{ V}, I_D = -3 \text{ A}$		87	107	
r _{DS(on)}	r _{DS(on)} Static Drain to Source On Resistance	$V_{GS} = -6 \text{ V}, I_D = -2.7 \text{ A}$		99	137	mΩ
		$V_{GS} = -10 \text{ V}, I_D = -3 \text{ A}, T_J = 125 ^{\circ}\text{C}$		145	178	
9 _{FS}	Forward Transconductance	V _{DS} = -10 V, I _D = -3 A		12		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 75 V V - 0 V		1535	2045	pF
C _{oss}	Output Capacitance	V _{DS} = -75 V, V _{GS} = 0 V, ——f = 1 MHz		125	170	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12		6	10	pF
R_q	Gate Resistance		0.1	1.4	3	Ω

Switching Characteristics

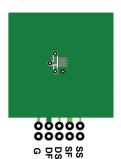
t _{d(on)}	Turn-On Delay Time		12	23	ns
t _r	Rise Time	V _{DD} = -75 V, I _D = -3 A,	3.3	10	ns
t _{d(off)}	Turn-Off Delay Time	V_{DD} = -75 V, I_{D} = -3 A, V_{GS} = -10 V, R_{GEN} = 6 Ω	22	36	ns
t _f	Fall Time		9.6	20	ns
$Q_{g(TOT)}$	Total Gate Charge	V _{GS} = 0 V to -10 V	22	32	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to -6 V}$ $V_{DD} = -75 \text{ V},$ $I_{D} = -3 \text{ A}$	14	20	nC
Q_{gs}	Total Gate Charge	I _D 3 A	5.7		nC
Q_{qd}	Gate to Drain "Miller" Charge		4.3		nC

Drain-Source Diode Characteristics

LVob Source to Drain Dioge Forward Voltage	Source to Drain Diode, Fenyard Voltage	$V_{GS} = 0 \text{ V}, I_S = -3 \text{ A}$ ((Note 2)	-0.80	-1.3	V
	$V_{GS} = 0 \text{ V}, I_S = -1.9 \text{ A}$ ((Note 2)	-0.78	-1.2	V	
t _{rr}	Reverse Recovery Time	-I _F = -3 A, di/dt = 100 A/μs		77	123	ns
Q _{rr}	Reverse Recovery Charge			208	333	nC

NOTES

^{1.} $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper

^{2.} Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.

^{3.} Starting T_J = 25 °C; P-ch: L = 3 mH, I_{AS} = -11 A, V_{DD} = -150 V, V_{GS} = -10 V. 100% test at L = 0.1 mH, I_{AS} = -34 A.

Typical Characteristics T_J = 25 °C unless otherwise noted

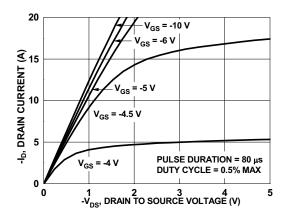


Figure 1. On Region Characteristics

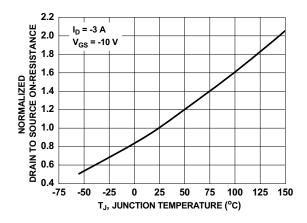


Figure 3. Normalized On Resistance vs Junction Temperature

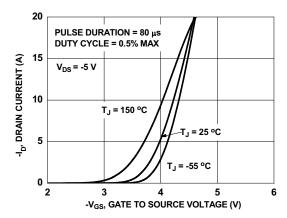


Figure 5. Transfer Characteristics

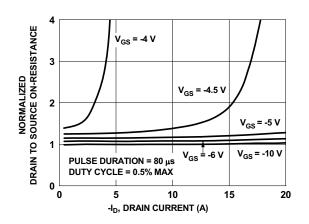


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

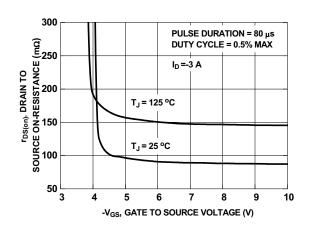


Figure 4. On-Resistance vs Gate to Source Voltage

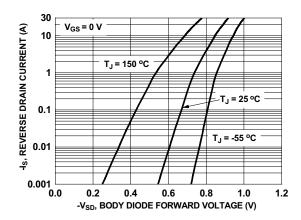


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

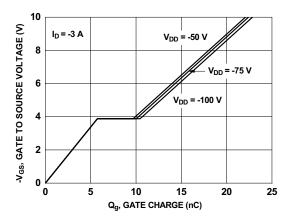


Figure 7. Gate Charge Characteristics

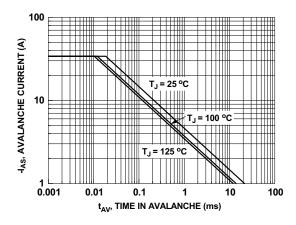


Figure 9. Unclamped Inductive Switching Capability

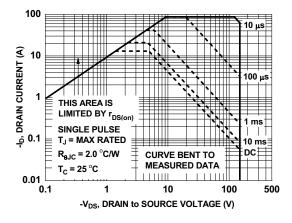


Figure 11. Forward Bias Safe Operating Area

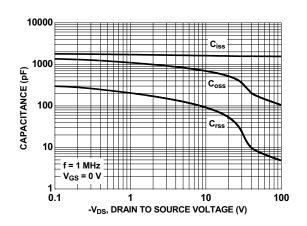


Figure 8. Capacitance vs Drain to Source Voltage

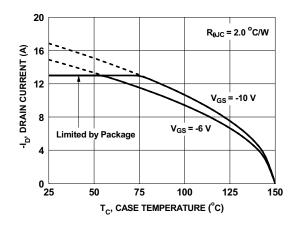


Figure 10. Maximum Continuous Drain Current vs Case Temperature

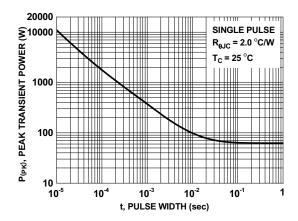


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

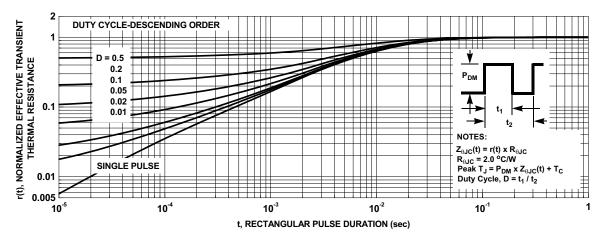
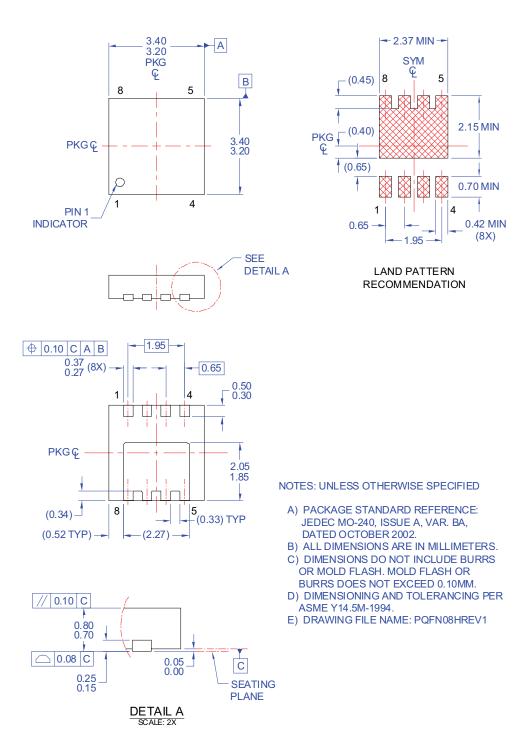


Figure 13. Junction-to-Case Transient Thermal Response Curve

Dimensional Outline and Pad Layout



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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

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Промышленная ул, дом № 19, литера Н,

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