USING THE ISOVOLT DC/DC CONVERTER REFERENCE DESIGN

1. Design Overview

The ISOvolt isolated dc/dc reference design shown in Figure 1 is a low-cost, robust, isolated dc/dc converter capable of delivering a maximum of 3 W of output power. This isolated power converter enables Silicon Labs' isolation products to be powered from a single bias supply, eliminating the need for separate supplies on both sides of the isolation device. This design features fold-back current limiting and thermal shutdown protection, low EMI operation, and high (78%) operating efficiency. Input voltage ranges are 3.3 or 4.5 Vdc to 5.5 Vdc and generate isolated output voltages of 3.3, 5.0, 7.0, or 24 V, depending on the transformer and output regulator used. Referring to Figure 1, the ISOvolt reference design is based on push-pull switching topology. The timing generator is a CT600-PX0624GM MCU, which has been factory-programmed to generate primary-side transformer switch timing.

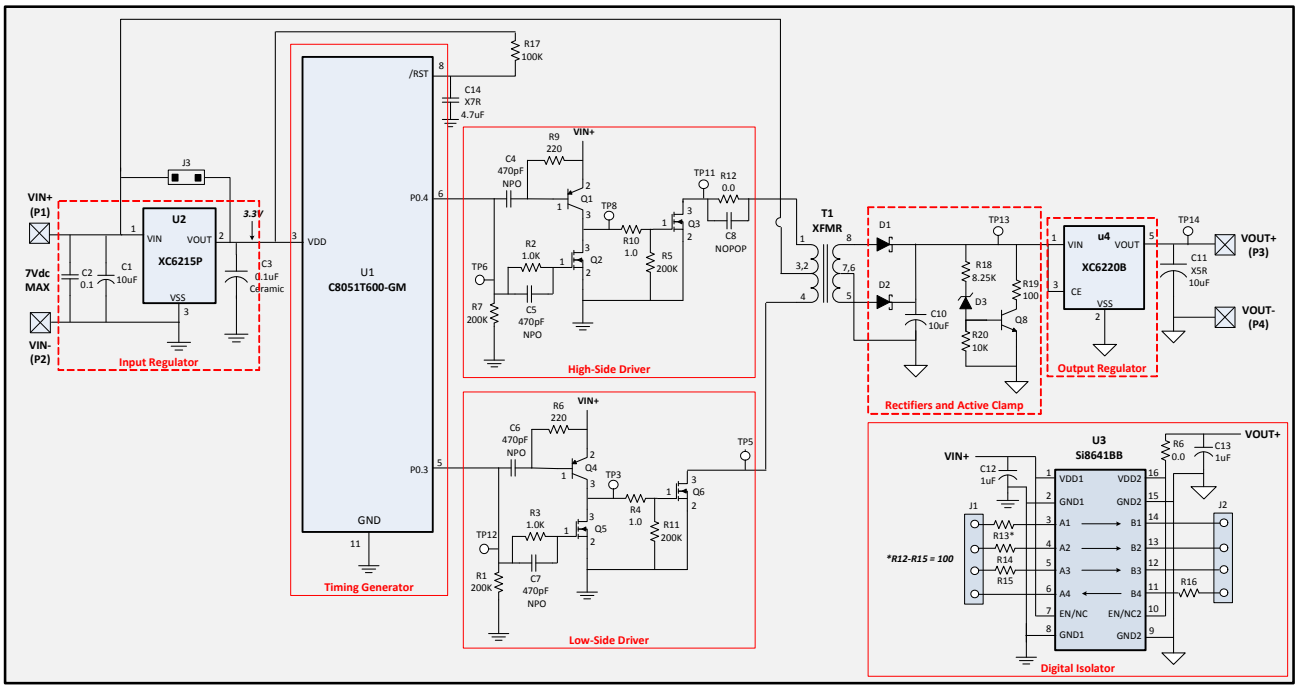

Figure 1. ISOvolt Isolated DC/DC Block Diagram

This MCU has a maximum bias voltage of 3.3 V, allowing applications having 2.7 V < VIN < 3.3 V dc. Higher values of VIN require the addition of input regulator (U2). The timing generator outputs are conditioned by high and low-side gate driver circuits, which drive the switches on transformer T1's primary at a frequency of 500 kHz. The resulting ac voltage on the secondary-side is rectified by a full-wave Schottky diode circuit and filtered by a bulk capacitor (C10). An active clamp circuit sinks current during light output loads (50 mA or less) to ensure the dc voltage stays below the maximum input voltage value of the linear output regulator. The resulting conditioned dc voltage is regulated by a linear output regulator (U4).

The ISOvolt reference design board (see Figure 4) also contains digital isolator U3 (Silicon Labs' Si864IBC with three forward channels and one reverse channel) for customer use. The combination of ISOvolt and the onboard isolator is useful in applications, such as isolated serial ports. The user can connect external signals to input blocks J1 and J2, and VOUT+ supplies bias to the output side of the isolator.

Note: U3 maximum VDD2 is 5.5 V. If VDD2 exceeds 5 V, the value of resistor R6 must be increased to ensure that U3 pin 16 does not exceed 5.5 V under any operating conditions. For BOM, schematic, and layout details, see the "Discrete ISOvolt Isolated DC-DC Converter Reference Design Users Guide".

1.1. Gate Driver Circuits

While the timing generator (U1, Figure 1) has a maximum VDD of 3.3 V, many applications will have a VIN of 4.5 V to 5.5 V dc; therefore, the gate drivers must provide a 0 to VIN output swing from a maximum input signal of 3.3 V. To meet this criterion, the discrete gate driver circuits use a bootstrap circuit to level-shift driver output swing. Referring to Figure 2, when the MCU output is low, high-side transistor Q1 is on, and bootstrap capacitor C4 charges to approximately (VIN – 0.7 V). When the MCU output transitions high, Q1 base is driven by Vboot (i.e. Vboot = MCU Vout + VIN –0.7 V ~ 7.6 V assuming VIN = 5.0 V, MCU Vout = 3.3 V, waveform “A”, Figure 2). This high-voltage swing abruptly turns high-side transistor Q1 off and low-side transistor Q2 on. Note the low-side RC circuit (C5, R2) provides “speed-up” for Q2 (Channel 2, Figure 2).

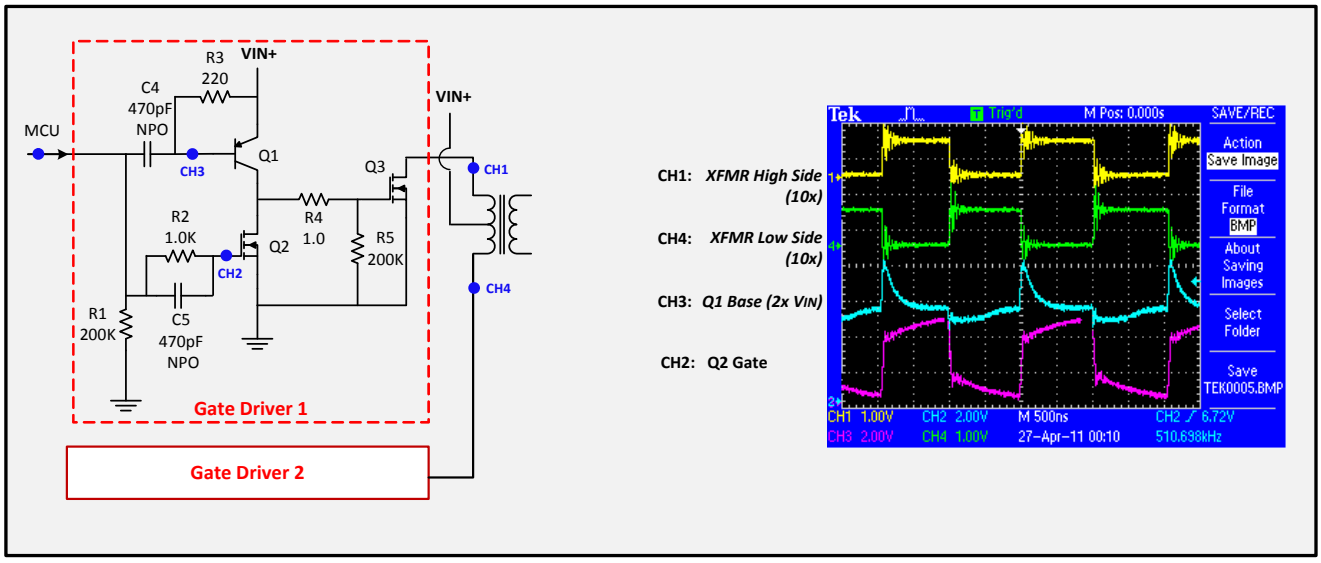

Figure 2. Bootstrap Driver Operation

The resistor, R3, helps to provide a path for pre-charging the bootstrap capacitor, C4, as well as to provide dc bias for transistor Q1. It also helps to keep the base of transistor pulled high till the microcontroller starts switching.

The value of R3 should be chosen based on minimum turn-on time (or minimum duty-cycle) of the high-side switch so that there is enough time to discharge the capacitor to bring the voltage at the base of transistor, Q1, to its normal value before the next switching cycle begins.

$$R3 \times C4 \ll t_{onQ4(min)}$$

Equation 1.

The capacitor, C4, is chosen such that the dynamic current due to change in voltage across it multiplied by the hFE of transistor Q1 should be able to charge the gate capacitor of transistor Q3 to turn it on within a short time. The base-emitter reverse bias voltage of the transistor, Q1, should not exceed vendor specifications. To prevent the base-emitter voltage from exceeding specified maximum limits during transients, use of a diode clamp between base and emitter with the anode of the diode connected to the transistor base and the cathode to the emitter is recommended. Any change in system operating frequency must also compensate the values of the RC circuits at the base of the high-side drive transistor and low-side drive MOSFET. Failure to do this can cause cross-conduction, which can lower efficiency or destroy the converter.

For best results, the layout files included in the ISOvolt Reference Design should be used. Any circuit modifications should adhere to these layout guidelines:

- The driver layout should be as tight as possible to minimize inductance.
- The driver output should be located as close to the switching transistor and transformer pads as possible to minimize inductive ringing.

1.2. Active Clamp

The active clamp shown in Figure 3 protects the linear output regulator from excessive input voltages when the converter is operating at an output current of 50 mA or less. At these low currents, the voltage at point “A” increases. The R18, D3, and R20 network provides a threshold at the base of Q8 such that, as the voltage on point A exceeds 6.8 Vdc, Q8 gradually turns-on, causing current to flow through R19 to ground and limiting the voltage excursion at point A.

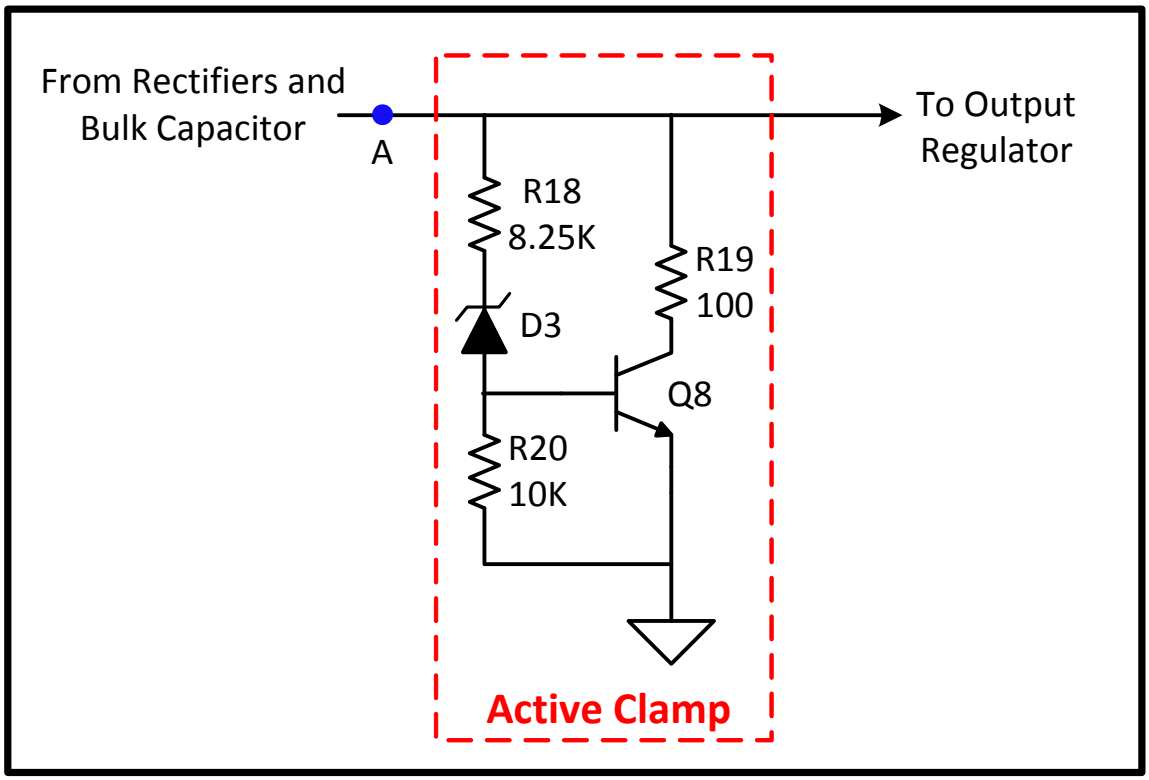

Figure 3. Active Clamp

The minimum voltage at point A must be greater than the sum of Zener voltage D3, base-emitter voltage of Q8, and the drop across resistor R18 to turn on transistor Q8 so that a minimum load current is absorbed by resistor R19 and the transistor Q8. For example, the reference design board uses the Torex XC6220B as its 5 V output linear regulator (maximum input voltage specification of 6.5 V). The active clamp is used to limit the regulator input voltage to less than 6.5 V under light load conditions. The Zener diode has a value of 5.1 V, and resistor R18 is chosen to limit the current through the Zener diode once its clamp voltage is exceeded. Current is sunk through transistor Q8 such that the voltage at the regulator input remains below 6.5 V. Resistor R19 is appropriately selected for power dissipation.

1.3. System Waveforms

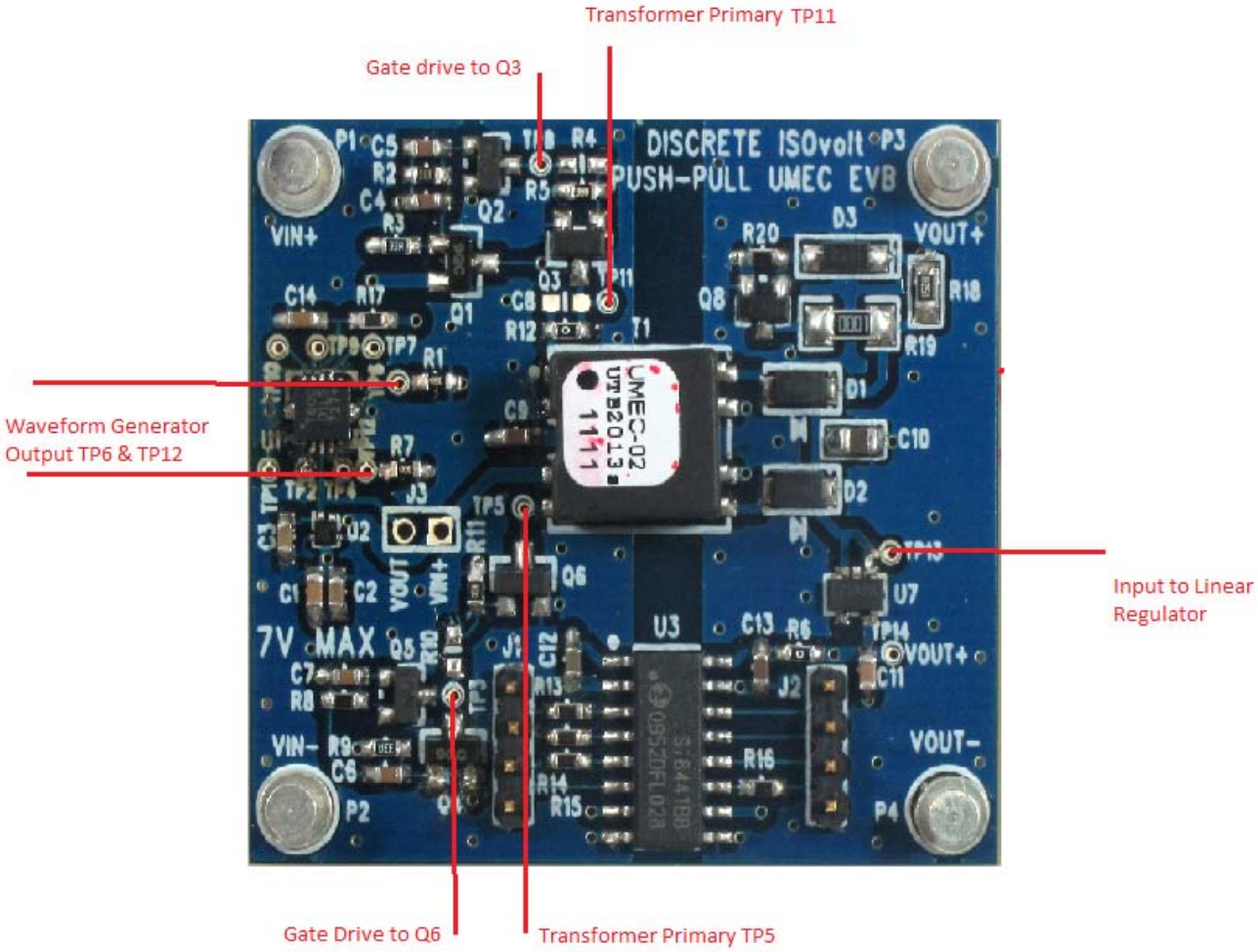

Figure 4. ISOvolt Reference Design Board

Figure 4 shows a populated ISOvolt reference design board showing the test points for waveform generator U1 outputs (TP6, TP12), gate drive to primary switching MOSFETs (TP8, TP3), primary side switch drain outputs (TP5, TP11), and the input of the linear regulator output (TP13). The corresponding waveforms at 10% and 100% load are shown in the waveforms in Figures 5 through 7.

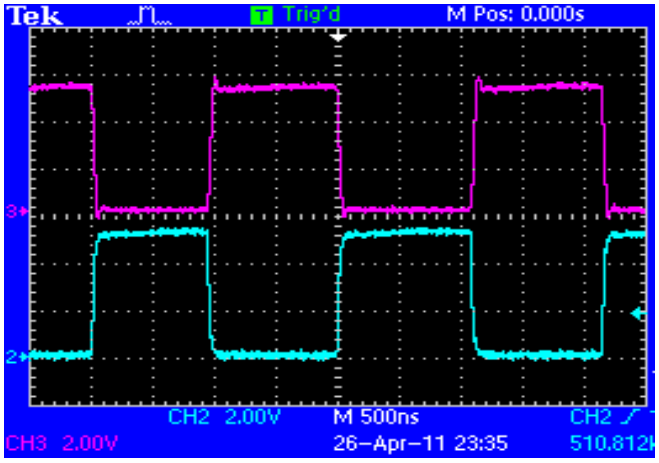

Figure 5. Gate Drive to Primary Switch TP3 and TP8

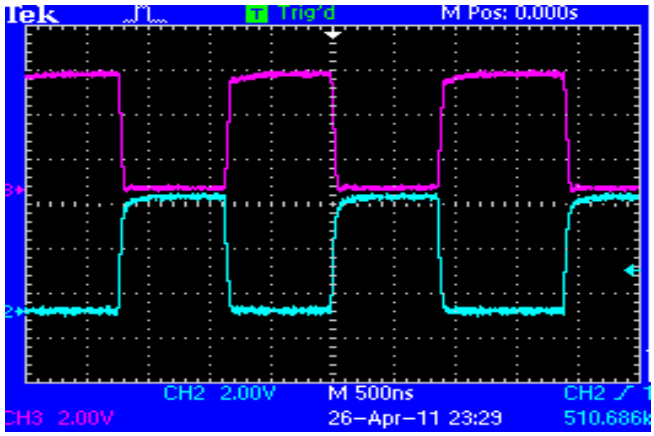

Figure 6. Waveform Generator Outputs TP6 and TP12

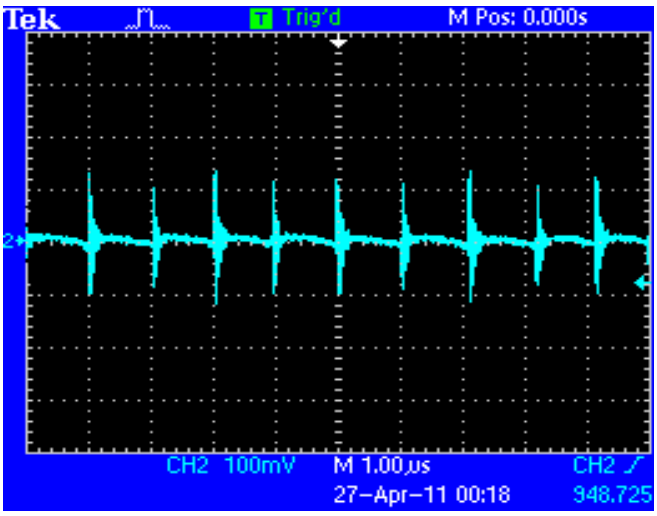

Figure 7. AC Ripple at the Cathode of the Secondary Rectifier

2. Adjusting Converter Performance

The gate driver used in this reference design is a general-purpose driver that can be used to drive any high- and low-side drive with the proper selection of components. The selection of the bootstrap capacitor and resistor is important (see "1.1. Gate Driver Circuits" on page 2 for details). Increasing the gate drive current requires higher current drive transistors (e.g. Q1 and Q2 in Figure 2).

2.1. Changing Output Voltage

The dc-dc converter can be adapted for different output voltages by modifying the turns-ratio of the isolation transformer. The secondary rectifiers (diodes D1 and D2 shown in Figure 1) should be rated for at least twice the maximum clamped voltage at the input to the linear regulator. In practice, it is recommended to use at least 50% overhead above this value to accommodate the voltage spikes due to circuit parasitics. The output filter capacitor should also be rated according to the maximum output voltage generated.

3. Performance Data

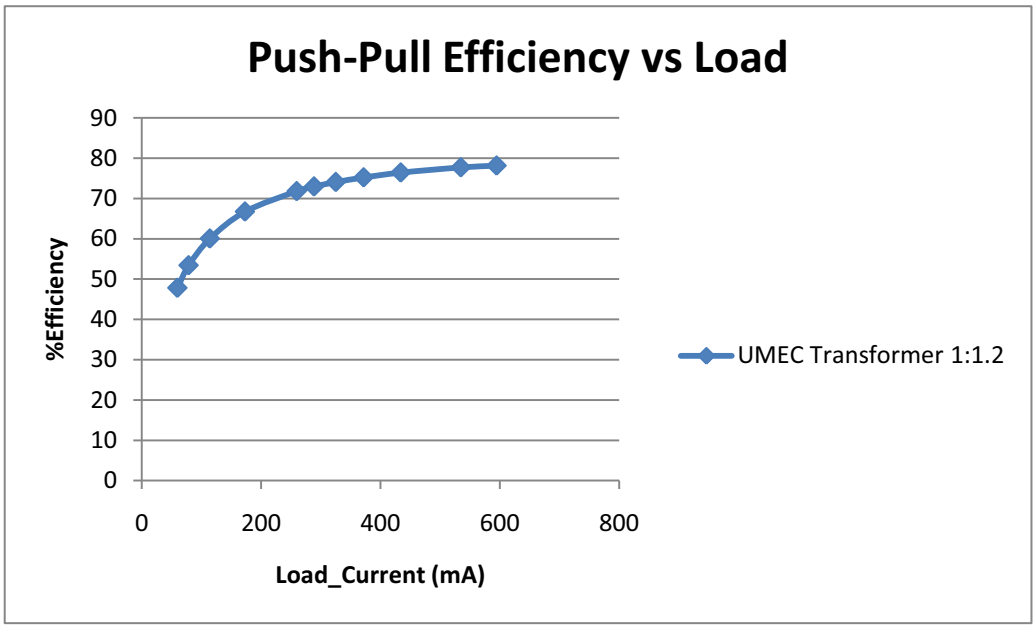

Figure 8. Efficiency vs. Load for 5 V to 5 V

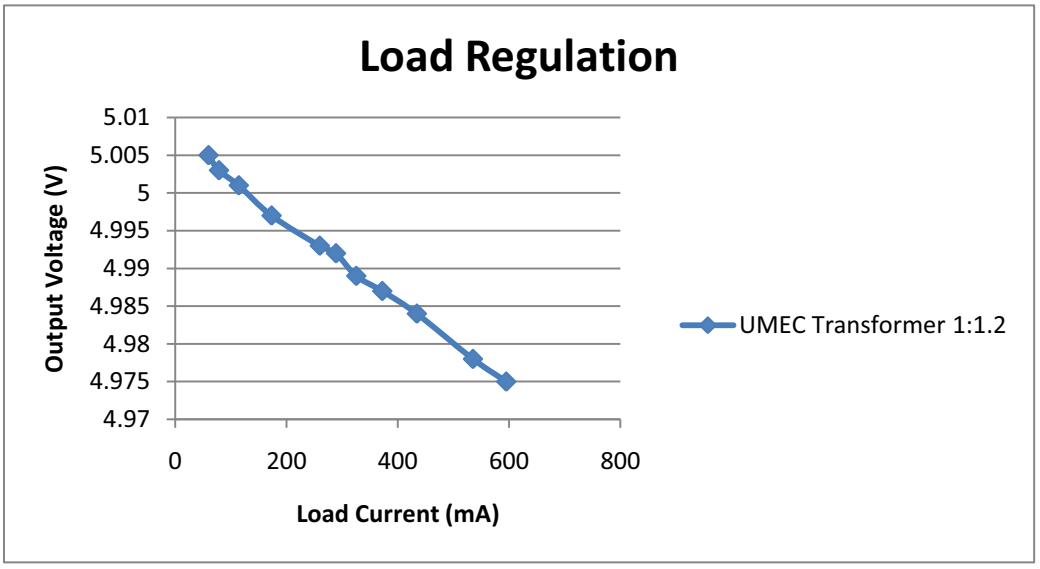

Figure 9. Load Regulation for 5 V to 5 V

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Changed “Si8441” to “Si8641” throughout.

NOTES:

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