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# ON Semiconductor®

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Aug 2015

### FDS6681Z

### 30 Volt P-Channel PowerTrench® MOSFET

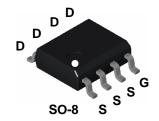
#### **General Description**

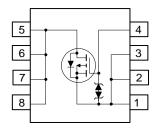
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

#### **Features**

- -20 A, -30 V.  $R_{DS(ON)} = 4.6 \text{ m}\Omega$  @  $V_{GS} = -10 \text{ V}$   $R_{DS(ON)} = 6.5 \text{ m}\Omega$  @  $V_{GS} = -4.5 \text{ V}$
- Extended V<sub>GSS</sub> range (–25V) for battery applications
- HBM ESD protection level of 8kV typical (note 3)
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS(ON)}}$
- High power and current handling capability
- Termination is Lead-free and RoHS Compliant





### $\textbf{Absolute Maximum Ratings} \quad \textit{T}_{A} = 25 \text{ $^\circ$C unless otherwise noted}$

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		-30	V
V <sub>GSS</sub>	Gate-Source Voltage		±25	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	-20	Α
	– Pulsed		-105	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1.0	
$T_J$ , $T_{STG}$	Operating and Storage Junction Temperat	ture Range	−55 to +150	°C

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

### **Package Marking and Ordering Information**

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6681Z	FDS6681Z	13"	12mm	2500 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = -250 \mu\text{A}$	-30			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu A$ , Referenced to 25°C		-26		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V},  V_{GS} = 0 \text{ V}$			-1	μА
I <sub>GSS</sub>	Gate-Body Leakage	$V_{GS} = \pm 25 \text{ V},  V_{DS} = 0 \text{ V}$			±10	μА
On Chara	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$ , Referenced to 25°C		6		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10 \text{ V},  I_D = -20 \text{ A}$ $V_{GS} = -4.5 \text{ V},  I_D = -17 \text{ A}$ $V_{GS} = -10 \text{ V},  I_D = -20 \text{ A}, T_J = 125 ^{\circ}\text{C}$		3.8 5.2 5.0	4.6 6.5 6.3	mΩ
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 \text{ V},  I_{D} = -20 \text{ A}$		79		S
Dvnamic	Characteristics	•	•			
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -15 \text{ V}.  V_{GS} = 0 \text{ V}.$		7540		pF
Coss	Output Capacitance	f = 1.0 MHz		1400		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			1120		pF
Switchin	g Characteristics (Note 2)	•	•			
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -15 \text{ V},  I_{D} = -1 \text{ A},$ $V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$		20	35	ns
t <sub>r</sub>	Turn-On Rise Time			9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	7		660	1060	ns
t <sub>f</sub>	Turn-Off Fall Time	]		380	610	ns
Q <sub>g(TOT)</sub>	Total Gate Charge at V <sub>GS</sub> = -10V	$V_{DS} = -15 \text{ V}, I_{D} = -20 \text{ A}$		185	260	nC
$Q_{g(TOT)}$	Total Gate Charge at V <sub>GS</sub> = −5V			105	150	nC
Q <sub>gs</sub>	Gate-Source Charge			26		nC
$Q_{qd}$	Gate-Drain Charge			47		nC

#### **Electrical Characteristics** $T_A = 25^{\circ}C$ unless otherwise noted **Symbol Parameter Test Conditions** Min Тур Max Units **Drain-Source Diode Characteristics and Maximum Ratings** Maximum Continuous Drain-Source Diode Forward Current -2.1 Α Drain-Source Diode Forward $V_{\text{SD}} \\$ $V_{GS} = 0 \text{ V}, \quad I_S = -2.1 \text{ A} \quad \text{(Note 2)}$ -0.7-1.2 V Voltage $I_F = -20 A$ , $t_{\mathsf{RR}}$ Reverse Recovery Time 125 ns $Q_{\mathsf{RR}}$ Reverse Recovery Charge $dI_F/dt = 100 A/\mu s$ 94 nC(Note 2)

#### Notes:

1. R<sub>8,JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>8,JC</sub> is guaranteed by design while R<sub>8CA</sub> is determined by the user's board design.



a) 50°C/W (10 sec) 62.5°C/W steady state when mounted on a 1in² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in<sup>2</sup> pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

- Scale 1:1 on letter size paper
- 2. Pulse Test: Pulse Width < 300  $\mu s, \, Duty \, Cycle < 2.0\%$
- 3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

### **Typical Characteristics**

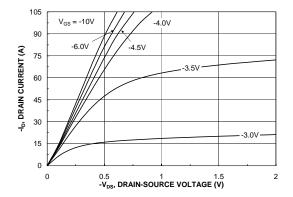


Figure 1. On-Region Characteristics.

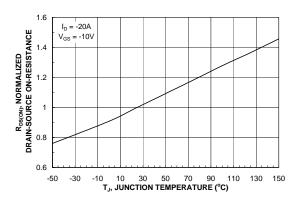


Figure 3. On-Resistance Variation with Temperature.

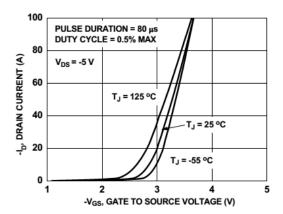


Figure 5. Transfer Characteristics.

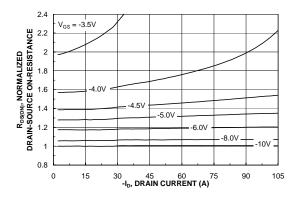


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

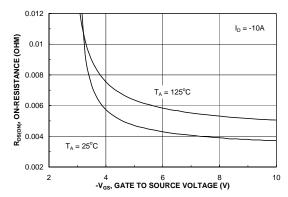


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

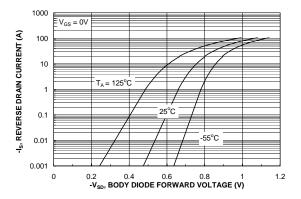
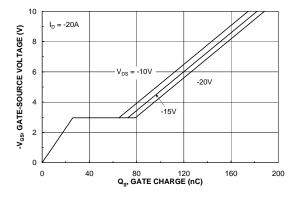


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### **Typical Characteristics**



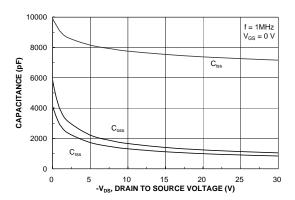
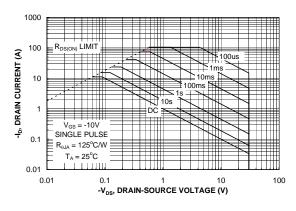


Figure 7. Gate Charge Characteristics.





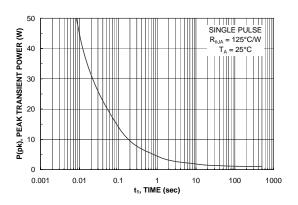


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

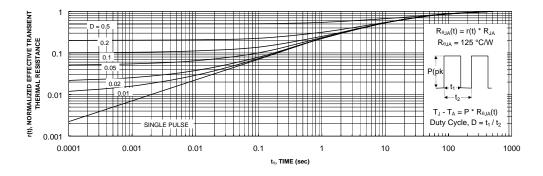
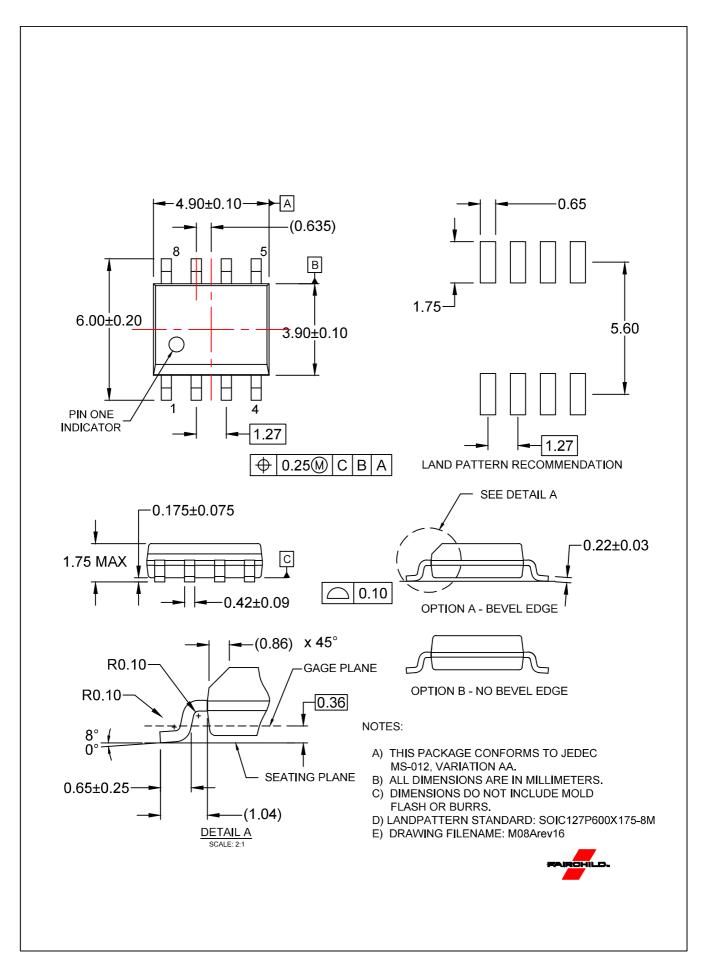


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



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