8/16-bit Atmel XMEGA Microcontroller

# ATxmega128A4U / ATxmega64A4U / ATxmega32A4U / ATxmega16A4U

## Features

- High-performance, low-power Atmel® AVR® XMEGA® 8/16-bit Microcontroller
- Nonvolatile program and data memories
  - 16K - 128KB of in-system self-programmable flash
  - 4K - 8KB boot section
  - 1K - 2KB EEPROM
  - 2K - 8KB internal SRAM
- Peripheral Features
  - Four-channel DMA controller
  - Eight-channel event system
  - Five 16-bit timer/counters
    - Three timer/counters with 4 output compare or input capture channels
    - Two timer/counters with 2 output compare or input capture channels
    - High-resolution extensions on all timer/counters
    - Advanced waveform extension (AWeX) on one timer/counter
  - One USB device interface
    - USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant
    - 32 Endpoints with full configuration flexibility
  - Five USARTs with IrDA support for one USART
  - Two Two-wire interfaces with dual address match ($I^2C$ and SMBus compatible)
  - Two serial peripheral interfaces (SPIs)
  - AES and DES crypto engine
  - CRC-16 (CRC-CCITT) and CRC-32 (IEEE® 802.3) generator
  - 16-bit real time counter (RTC) with separate oscillator
  - One twelve-channel, 12-bit, 2msps Analog to Digital Converter
  - One two-channel, 12-bit, 1msps Digital to Analog Converter
  - Two Analog Comparators with window compare function, and current sources
  - External interrupts on all general purpose I/O pins
  - Programmable watchdog timer with separate on-chip ultra low power oscillator
  - QTouch® library support
    - Capacitive touch buttons, sliders and wheels
- Special microcontroller features
  - Power-on reset and programmable brown-out detection
  - Internal and external clock options with PLL and prescaler
  - Programmable multilevel interrupt controller
  - Five sleep modes
  - Programming and debug interfaces
    - PDI (program and debug interface)
- I/O and packages
  - 34 Programmable I/O pins
  - 44 - lead TQFP
  - 44 - pad VQFN/QFN
  - 49 - ball VFBGA
- Operating voltage
  - 1.6 – 3.6V
- Operating frequency
  - 0 – 12MHz from 1.6V
  - 0 – 32MHz from 2.7V

# 1. Ordering Information

| Ordering code | Flash (bytes) | EEPROM (bytes) | SRAM (bytes) | Speed (MHz) | Power supply | Package [1][2][3] | Temp. |
|---|---|---|---|---|---|---|---|
| ATxmega128A4U-AU | 128K + 8K | 2K | 8K | 32 | 1.6 - 3.6V | 44A | -40°C - 85°C |
| ATxmega128A4U-AUR[4] | 128K + 8K | 2K | 8K | | | | |
| ATxmega64A4U-AU | 64K + 4K | 2K | 4K | | | | |
| ATxmega64A4U-AUR[4] | 64K + 4K | 2K | 4K | | | | |
| ATxmega32A4U-AU | 32K + 4K | 1K | 4K | | | | |
| ATxmega32A4U-AUR[4] | 32K + 4K | 1K | 4K | | | | |
| ATxmega16A4U-AU | 16K + 4K | 1K | 2K | | | | |
| ATxmega16A4U-AUR[4] | 16K + 4K | 1K | 2K | | | | |
| ATxmega128A4U-MH | 128K + 8K | 2K | 8K | | | PW | |
| ATxmega128A4U-MHR[4] | 128K + 8K | 2K | 8K | | | | |
| ATxmega64A4U-MH | 64K + 4K | 2K | 4K | | | | |
| ATxmega64A4U-MHR[4] | 64K + 4K | 2K | 4K | | | | |
| ATxmega32A4U-MH | 32K + 4K | 1K | 4K | | | 44M1 | |
| ATxmega32A4U-MHR[4] | 32K + 4K | 1K | 4K | | | | |
| ATxmega16A4U-MH | 16K + 4K | 1K | 2K | | | | |
| ATxmega16A4U-MHR[4] | 16K + 4K | 1K | 2K | | | | |
| ATxmega128A4U-CU | 128K + 8K | 2K | 8K | | | 49C2 | |
| ATxmega128A4U-CUR[4] | 128K + 8K | 2K | 8K | | | | |
| ATxmega64A4U-CU | 64K + 4K | 2K | 4K | | | | |
| ATxmega64A4U-CUR[4] | 64K + 4K | 2K | 4K | | | | |
| ATxmega32A4U-CU | 32K + 4K | 1K | 4K | | | | |
| ATxmega32A4U-CUR[4] | 32K + 4K | 1K | 4K | | | | |
| ATxmega16A4U-CU | 16K + 4K | 1K | 2K | | | | |
| ATxmega16A4U-CUR[4] | 16K + 4K | 1K | 2K | | | | |

| Ordering code | Flash (bytes) | EEPROM (bytes) | SRAM (bytes) | Speed (MHz) | Power supply | Package [1][2][3] | Temp. |
|---|---|---|---|---|---|---|---|
| ATxmega128A4U-AN | 128K + 8K | 2K | 8K | 32 | 1.6 - 3.6V | 44A | 0°C - 105°C |
| ATxmega128A4U-ANR[4] | 128K + 8K | 2K | 8K | | | | |
| ATxmega64A4U-AN | 64K + 4K | 2K | 4K | | | | |
| ATxmega64A4U-ANR[4] | 64K + 4K | 2K | 4K | | | | |
| ATxmega32A4U-AN | 32K + 4K | 1K | 4K | | | | |
| ATxmega32A4U-ANR[4] | 32K + 4K | 1K | 4K | | | | |
| ATxmega16A4U-AN | 16K + 4K | 1K | 2K | | | | |
| ATxmega16A4U-ANR[4] | 16K + 4K | 1K | 2K | | | | |
| ATxmega128A4U-M7 | 128K + 8K | 2K | 8K | | | PW | |
| ATxmega128A4U-M7R[4] | 128K + 8K | 2K | 8K | | | | |
| ATxmega64A4U-M7 | 64K + 4K | 2K | 4K | | | | |
| ATxmega64A4U-M7R[4] | 64K + 4K | 2K | 4K | | | | |
| ATxmega32A4U-M7 | 32K + 4K | 1K | 4K | | | 44M1 | |
| ATxmega32A4U-M7R[4] | 32K + 4K | 1K | 4K | | | | |
| ATxmega16A4U-M7 | 16K + 4K | 1K | 2K | | | | |
| ATxmega16A4U-M7R[4] | 16K + 4K | 1K | 2K | | | | |

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see "Instruction Set Summary" on page 63.
4. Tape and Reel

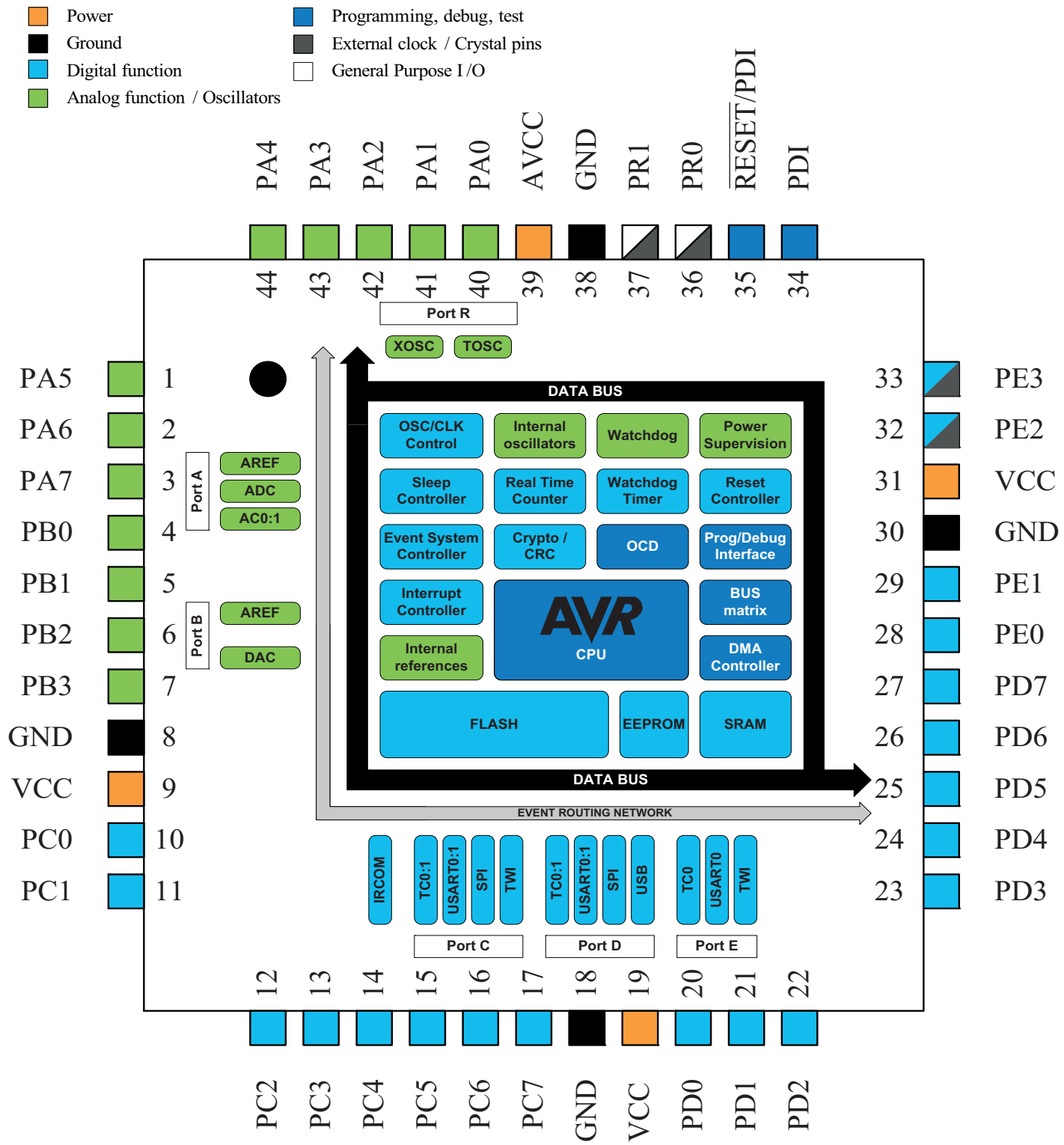
| Package Type | |
|---|---|
| 44A | 44-Lead, 10 x 10mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP) |
| 44M1 | 44-Pad, 7x7x1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN) |
| PW | 44-Pad, 7x7x1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN) |
| 49C2 | 49-Ball (7 x 7 Array), 0.65mm Pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA) |

## Typical Applications

| | | |
|---|---|---|
| Industrial control | Climate control | Low power battery applications |
| Factory automation | RF and ZigBee® | Power tools |
| Building control | USB connectivity | HVAC |
| Board control | Sensor control | Utility metering |
| White goods | Optical | Medical applications |

# 2. Pinout/Block Diagram

**Figure 2-1. Block Diagram and QFN/TQFP pinout**




Note: 1. For full details on pinout and pin functions refer to "Pinout and Pin Functions" on page 55.

**Figure 2-2. BGA pinout**

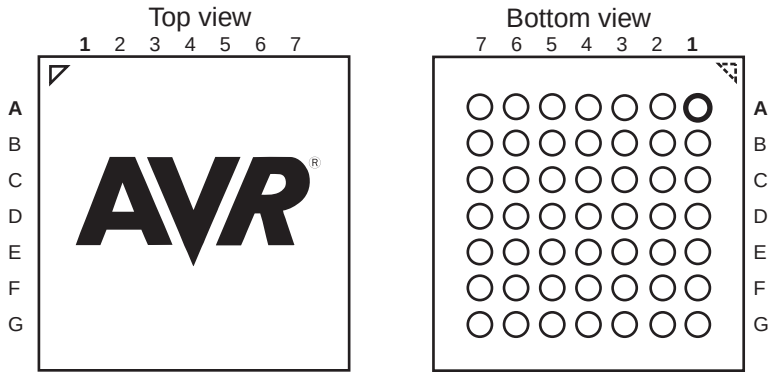



**Table 2-1. BGA pinout**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | PA3 | AVCC | GND | PR1 | PR0 | PDI_DATA | PE3 |
| B | PA4 | PA1 | PA0 | GND | RESET/ PDI_CLK | PE2 | VCC |
| C | PA5 | PA2 | PA6 | PA7 | GND | PE1 | GND |
| D | PB1 | PB2 | PB3 | PB0 | GND | PD7 | PE0 |
| E | GND | GND | PC3 | GND | PD4 | PD5 | PD6 |
| F | VCC | PC0 | PC4 | PC6 | PD0 | PD1 | PD3 |
| G | PC1 | PC2 | PC5 | PC7 | GND | VCC | PD2 |

# 3. Overview

The Atmel AVR XMEGA is a family of low power, high performance, and peripheral rich 8/16-bit microcontrollers based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the AVR XMEGA devices achieve CPU throughput approaching one million instructions per second (MIPS) per megahertz, allowing the system designer to optimize power consumption versus processing speed.

The AVR CPU combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the arithmetic logic unit (ALU), allowing two independent registers to be accessed in a single instruction, executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs many times faster than conventional single-accumulator or CISC based microcontrollers.

The AVR XMEGA A4U devices provide the following features: in-system programmable flash with read-while-write capabilities; internal EEPROM and SRAM; four-channel DMA controller, eight-channel event system and programmable multilevel interrupt controller, 34 general purpose I/O lines, 16-bit real-time counter (RTC); five flexible, 16-bit timer/counters with compare and PWM channels; five USARTs; two two-wire serial interfaces (TWIs); one full speed USB 2.0 interface; two serial peripheral interfaces (SPIs); AES and DES cryptographic engine; one twelve-channel, 12-bit ADC with programmable gain; one 2-channel 12-bit DAC; two analog comparators (ACs) with window mode; programmable watchdog timer with separate internal oscillator; accurate internal oscillators with PLL and prescaler; and programmable brown-out detection.

The program and debug interface (PDI), a fast, two-pin interface for programming and debugging, is available.

The ATx devices have five software selectable power saving modes. The idle mode stops the CPU while allowing the SRAM, DMA controller, event system, interrupt controller, and all peripherals to continue functioning. The power-down mode saves the SRAM and register contents, but stops the oscillators, disabling all other functions until the next TWI, USB resume, or pin-change interrupt, or reset. In power-save mode, the asynchronous real-time counter continues to run, allowing the application to maintain a timer base while the rest of the device is sleeping. In standby mode, the external crystal oscillator keeps running while the rest of the device is sleeping. This allows very fast startup from the external crystal, combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run. To further reduce power consumption, the peripheral clock to each individual peripheral can optionally be stopped in active mode and idle sleep mode.

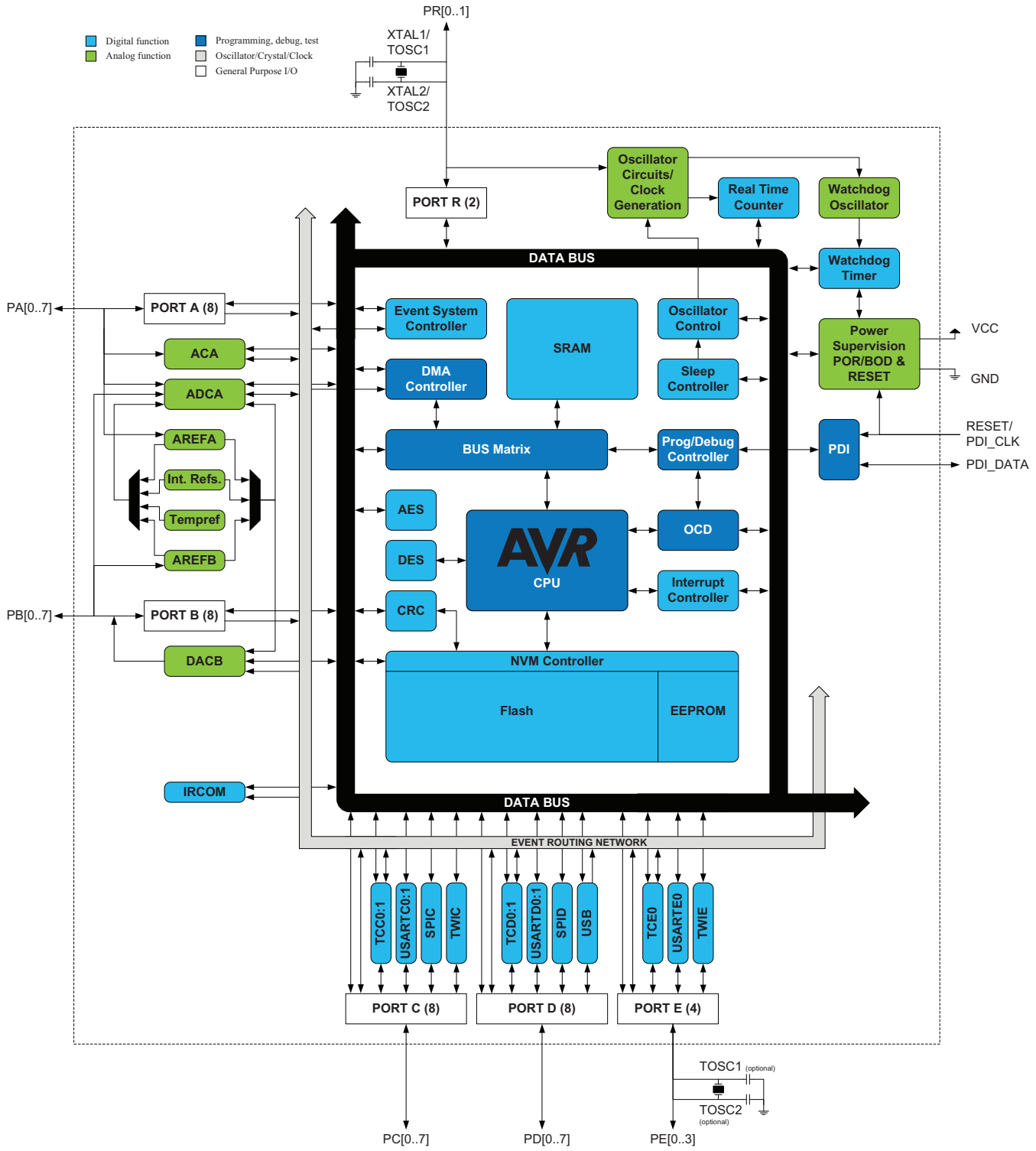
Atmel offers a free QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers.

The devices are manufactured using Atmel high-density, nonvolatile memory technology. The program flash memory can be reprogrammed in-system through the PDI. A boot loader running in the device can use any interface to download the application program to the flash memory. The boot loader software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8/16-bit RISC CPU with in-system, self-programmable flash, the AVR XMEGA is a powerful microcontroller family that provides a highly flexible and cost effective solution for many embedded applications.

All Atmel AVR XMEGA devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers, and evaluation kits.

## 3.1 Block Diagram

**Figure 3-1. XMEGA A4U Block Diagram**



# 4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

## 4.1 Recommended reading

- Atmel AVR XMEGA AU manual
- XMEGA application notes

This device data sheet only contains part specific information with a short description of each peripheral and module. The XMEGA AU manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

All documentation are available from www.atmel.com/avr.

# 5. Capacitive touch sensing

The Atmel QTouch library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the QTouch library user guide - also available for download from the Atmel website.

# 6. AVR CPU

## 6.1 Features

- 8/16-bit, high-performance Atmel AVR RISC CPU
  - 142 instructions
  - Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in RAM
- Stack pointer accessible in I/O memory space
- Direct addressing of up to 16MB of program memory and 16MB of data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Efficient support for 8-, 16-, and 32-bit arithmetic
- Configuration change protection of system-critical features

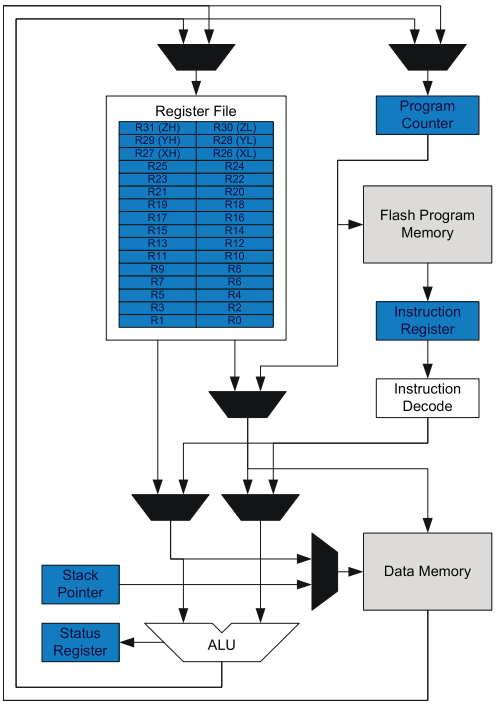
## 6.2 Overview

All Atmel AVR XMEGA devices use the 8/16-bit AVR CPU. The main function of the CPU is to execute the code and perform all calculations. The CPU is able to access memories, perform calculations, control peripherals, and execute the program in the flash memory. Interrupt handling is described in a separate section, refer to "Interrupts and Programmable Multilevel Interrupt Controller" on page 29.

## 6.3 Architectural Overview

In order to maximize performance and parallelism, the AVR CPU uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This enables instructions to be executed on every clock cycle. For details of all AVR instructions, refer to http://www.atmel.com/avr.

**Figure 6-1. Block diagram of the AVR CPU architecture.**




The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers, SRAM, and external RAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for safe storing of nonvolatile data in the program memory.

## 6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general

purpose registers. In a single clock cycle, arithmetic operations between general purpose registers or between a register and an immediate are executed and the result is stored in the register file. After an arithmetic or logic operation, the status register is updated to reflect information about the result of the operation.

ALU operations are divided into three main categories – arithmetic, logical, and bit functions. Both 8- and 16-bit arithmetic is supported, and the instruction set allows for efficient implementation of 32-bit aritmetic. The hardware multiplier supports signed and unsigned multiplication and fractional format.

### 6.4.1 Hardware Multiplier

The multiplier is capable of multiplying two 8-bit numbers into a 16-bit result. The hardware multiplier supports different variations of signed and unsigned integer and fractional numbers:

- Multiplication of unsigned integers
- Multiplication of signed integers
- Multiplication of a signed integer with an unsigned integer
- Multiplication of unsigned fractional numbers
- Multiplication of signed fractional numbers
- Multiplication of a signed fractional number with an unsigned one

A multiplication takes two CPU clock cycles.

## 6.5 Program Flow

After reset, the CPU starts to execute instructions from the lowest address in the flash programmemory ‘0.’ The program counter (PC) addresses the next instruction to be fetched.

Program flow is provided by conditional and unconditional jump and call instructions capable of addressing the whole address space directly. Most AVR instructions use a 16-bit word format, while a limited number use a 32-bit format.

During interrupts and subroutine calls, the return address PC is stored on the stack. The stack is allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. After reset, the stack pointer (SP) points to the highest address in the internal SRAM. The SP is read/write accessible in the I/O memory space, enabling easy implementation of multiple stacks or stack areas. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR CPU.

## 6.6 Status Register

The status register (SREG) contains information about the result of the most recently executed arithmetic or logic instruction. This information can be used for altering program flow in order to perform conditional operations. Note that the status register is updated after all ALU operations, as specified in the instruction set reference. This will in many cases remove the need for using the dedicated compare instructions, resulting in faster and more compact code.

The status register is not automatically stored when entering an interrupt routine nor restored when returning from an interrupt. This must be handled by software.

The status register is accessible in the I/O memory space.

## 6.7 Stack and Stack Pointer

The stack is used for storing return addresses after interrupts and subroutine calls. It can also be used for storing temporary data. The stack pointer (SP) register always points to the top of the stack. It is implemented as two 8-bit registers that are accessible in the I/O memory space. Data are pushed and popped from the stack using the PUSH and POP instructions. The stack grows from a higher memory location to a lower memory location. This implies that pushing data onto the stack decreases the SP, and popping data off the stack increases the SP. The SP is automatically loaded after reset, and the initial value is the highest address of the internal SRAM. If the SP is changed, it must be set to point above address 0x2000, and it must be defined before any subroutine calls are executed or before interrupts are enabled.

During interrupts or subroutine calls, the return address is automatically pushed on the stack. The return address can be two or three bytes, depending on program memory size of the device. For devices with 128KB or less of program memory, the return address is two bytes, and hence the stack pointer is decremented/incremented by two. For devices with more than 128KB of program memory, the return address is three bytes, and hence the SP is decremented/incremented by three. The return address is popped off the stack when returning from interrupts using the RETI instruction, and from subroutine calls using the RET instruction.

The SP is decremented by one when data are pushed on the stack with the PUSH instruction, and incremented by one when data is popped off the stack using the POP instruction.

To prevent corruption when updating the stack pointer from software, a write to SPL will automatically disable interrupts for up to four instructions or until the next I/O memory write.

After reset the stack pointer is initialized to the highest address of the SRAM. See Figure 7-1 on page 16.

## 6.8 Register File

The register file consists of 32 x 8-bit general purpose working registers with single clock cycle access time. The register file supports the following input/output schemes:

- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for lookup tables in flash program memory.

# 7. Memories

## 7.1 Features

- Flash program memory
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support
  - Application section for application code
  - Application table section for application code or data storage
  - Boot section for application code or boot loader code
  - Separate read/write protection lock bits for all sections
  - Built in fast CRC check of a selectable flash program memory section
- Data memory
  - One linear address space
  - Single-cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O memory
    - Configuration and status registers for all peripherals and modules
    - 16 bit-accessible general purpose registers for global variables or flags
  - Bus arbitration
    - Deterministic priority handling between CPU, DMA controller, and other bus masters
  - Separate buses for SRAM, EEPROM and I/O memory
    - Simultaneous bus access for CPU and DMA controller
- Production signature row memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User signature row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

## 7.2 Overview

The Atmel AVR architecture has two main memory spaces, the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

The available memory size configurations are shown in "Ordering Information" on page 2. In addition, each device has a Flash memory signature row for calibration data, device identification, serial number etc.

## 7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

**Table 7-1. Flash Program Memory (Hexadecimal address).**

| Word Address | | | | |
|---|---|---|---|---|
| **ATxmega128A4U** | **ATxmega64A4U** | **ATxmega32A4U** | **ATxmega16A4U** | |
| 0 | 0 | 0 | 0 | Application Section (128K/64K/32K/16K) |
| | | | | ... |
| EFFF / | 77FF / | 37FF / | 17FF | |
| F000 / | 7800 / | 3800 / | 1800 | Application Table Section (8K/4K/4K/4K) |
| FFFF / | 7FFF / | 3FFF / | 1FFF | |
| 10000 / | 8000 / | 4000 / | 2000 | Boot Section (8K/4K/4K/4K) |
| 10FFF / | 87FF / | 47FF / | 27FF | |

### 7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

### 7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

### 7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

### 7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to "Electrical Characteristics" on page 72.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-2.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

**Table 7-2. Device ID bytes for Atmel AVR XMEGA A4U devices.**

| Device | Device ID bytes | | |
|---|---|---|---|
| | Byte 2 | Byte 1 | Byte 0 |
| ATxmega16A4U | 41 | 94 | 1E |
| ATxmega32A4U | 41 | 95 | 1E |
| ATxmega64A4U | 46 | 96 | 1E |
| ATxmega128A4U | 46 | 97 | 1E |

### 7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

## 7.4 Fuses and Lock bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, and startup configuration.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

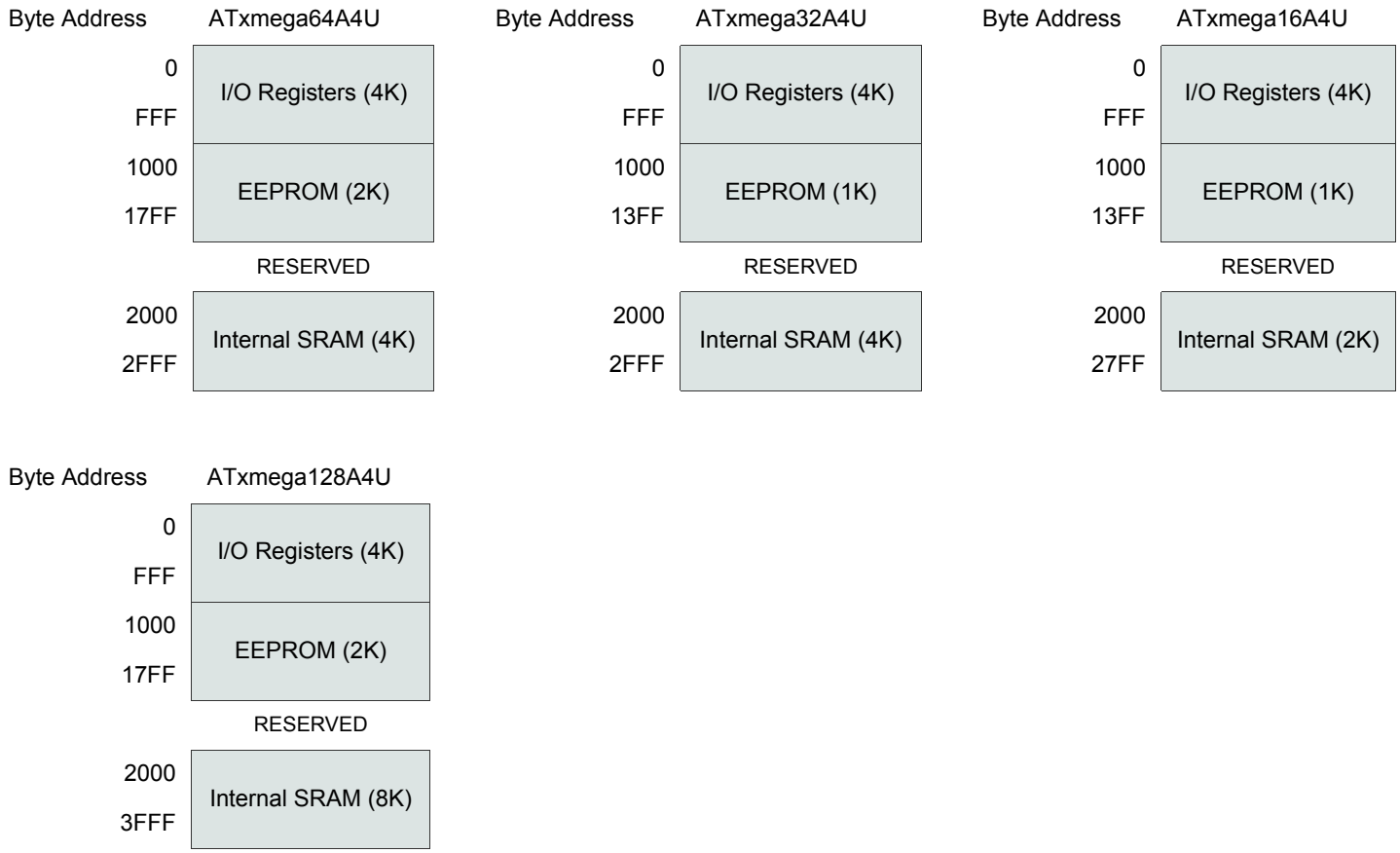
An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

## 7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-1. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

**Figure 7-1. Data memory map (Hexadecimal address).**




## 7.6 EEPROM

All devices have EEPROM for nonvolatile data storage. It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space. The EEPROM supports both byte and page access. Memory mapped EEPROM allows highly efficient EEPROM reading and EEPROM buffer loading. When doing this, EEPROM is accessible using load and store instructions. Memory mapped EEPROM will always start at hexadecimal address 0x1000.

## 7.7 I/O Memory

The status and configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations. All I/O locations can be accessed by the load (LD/LDS/LDD) and store (ST/STS/STD) instructions, which are used to transfer data between the 32 registers in the register file and the I/O memory. The IN and OUT instructions can address I/O memory locations in the range of 0x00 to 0x3F directly. In the address range 0x00 - 0x1F, single-cycle instructions for manipulation and checking of individual bits are available.

The I/O memory address for all peripherals and modules in XMEGA A4U is shown in the "Peripheral Module Address Map" on page 61.

### 7.7.1 General Purpose I/O Registers

The lowest 16 I/O memory addresses are reserved as general purpose I/O registers. These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions.

## 7.8 Data Memory and Bus Arbitration

Since the data memory is organized as four separate sets of memories, the different bus masters (CPU, DMA controller read and DMA controller write, etc.) can access different memory sections at the same time.

## 7.9 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. For burst read (DMA), new data are available every cycle. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

## 7.10 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

## 7.11 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

## 7.12 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-3 on page 17 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

**Table 7-3. Number of words and pages in the flash.**

| Devices | PC size | Flash size | Page Size | FWORD | FPAGE | Application | | Boot | |
|---|---|---|---|---|---|---|---|---|---|
| | bits | bytes | words | | | Size | No of pages | Size | No of pages |
| ATxmega16A4U | 14 | 16K + 4K | 128 | Z[6:0] | Z[13:7] | 16K | 64 | 4K | 16 |
| ATxmega32A4U | 15 | 32K + 4K | 128 | Z[6:0] | Z[14:7] | 32K | 128 | 4K | 16 |
| ATxmega64A4U | 16 | 64K + 4K | 128 | Z[6:0] | Z[15:7] | 64K | 256 | 4K | 16 |
| ATxmega128A4U | 17 | 128K + 8K | 128 | Z[6:0] | Z[16:7] | 128K | 512 | 8K | 32 |

Table 7-4 shows EEPROM memory organization for the Atmel AVR XMEGA A4U devices. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

**Table 7-4. Number of bytes and pages in the EEPROM.**

| Devices | EEPROM | Page Size | E2BYTE | E2PAGE | No of Pages |
|---|---|---|---|---|---|
| | Size | bytes | | | |
| ATxmega16A4U | 1K | 32 | ADDR[4:0] | ADDR[10:5] | 32 |
| ATxmega32A4U | 1K | 32 | ADDR[4:0] | ADDR[10:5] | 32 |
| ATxmega64A4U | 2K | 32 | ADDR[4:0] | ADDR[10:5] | 64 |
| ATxmega128A4U | 2K | 32 | ADDR[4:0] | ADDR[10:5] | 64 |

# 8. DMAC – Direct Memory Access Controller

## 8.1 Features

- Allows high speed data transfers with minimal CPU intervention
  - from data memory to data memory
  - from data memory to peripheral
  - from peripheral to data memory
  - from peripheral to peripheral
- Four DMA channels with separate
  - transfer triggers
  - interrupt vectors
  - addressing modes
- Programmable channel priority
- From 1 byte to 16MB of data in a single transaction
  - Up to 64KB block transfers with repeat
  - 1, 2, 4, or 8 byte burst transfers
- Multiple addressing modes
  - Static
  - Incremental
  - Decremental
- Optional reload of source and destination addresses at the end of each
  - Burst
  - Block
  - Transaction
- Optional interrupt on end of transaction
- Optional connection to CRC generator for CRC on DMA data

## 8.2 Overview

The four-channel direct memory access (DMA) controller can transfer data between memories and peripherals, and thus offload these tasks from the CPU. It enables high data transfer rates with minimum CPU intervention, and frees up CPU time. The four DMA channels enable up to four independent and parallel transfers.

The DMA controller can move data between SRAM and peripherals, between SRAM locations and directly between peripheral registers. With access to all peripherals, the DMA controller can handle automatic transfer of data to/from communication modules. The DMA controller can also read from memory mapped EEPROM.

Data transfers are done in continuous bursts of 1, 2, 4, or 8 bytes. They build block transfers of configurable size from 1 byte to 64KB. A repeat counter can be used to repeat each block transfer for single transactions up to 16MB. Source and destination addressing can be static, incremental or decremental. Automatic reload of source and/or destination addresses can be done after each burst or block transfer, or when a transaction is complete. Application software, peripherals, and events can trigger DMA transfers.

The four DMA channels have individual configuration and control settings. This include source, destination, transfer triggers, and transaction sizes. They have individual interrupt settings. Interrupt requests can be generated when a transaction is complete or when the DMA controller detects an error on a DMA channel.

To allow for continuous transfers, two channels can be interlinked so that the second takes over the transfer when the first is finished, and vice versa.

# 9. Event System

## 9.1 Features

- System for direct peripheral-to-peripheral communication and signaling
- Peripherals can directly send, receive, and react to peripheral events
  - CPU and DMA controller independent operation
  - 100% predictable signal timing
  - Short and guaranteed response time
- Eight event channels for up to eight different and parallel signal routing configurations
- Events can be sent and/or used by most peripherals, clock system, and software
- Additional functions include
  - Quadrature decoders
  - Digital filtering of I/O pin state
- Works in active mode and idle sleep mode

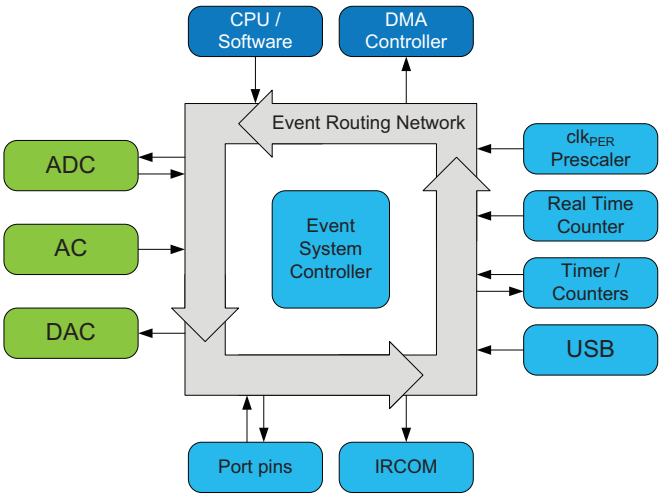
## 9.2 Overview

The event system enables direct peripheral-to-peripheral communication and signaling. It allows a change in one peripheral's state to automatically trigger actions in other peripherals. It is designed to provide a predictable system for short and predictable response times between peripherals. It allows for autonomous peripheral control and interaction without the use of interrupts, CPU, or DMA controller resources, and is thus a powerful tool for reducing the complexity, size and execution time of application code. It also allows for synchronized timing of actions in several peripheral modules.

A change in a peripheral's state is referred to as an event, and usually corresponds to the peripheral's interrupt conditions. Events can be directly passed to other peripherals using a dedicated routing network called the event routing network. How events are routed and used by the peripherals is configured in software.

Figure 9-1 on page 20 shows a basic diagram of all connected peripherals. The event system can directly connect together analog and digital converters, analog comparators, I/O port pins, the real-time counter, timer/counters, IR communication module (IRCOM), and USB interface. It can also be used to trigger DMA transactions (DMA controller). Events can also be generated from software and the peripheral clock.

**Figure 9-1. Event system overview and connected peripherals.**




The event routing network consists of eight software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to eight parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

# 10. System Clock and Clock options

## 10.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated and tuneable oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Internal and external clock options and 1x to 31x multiplication
  - Lock detector
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

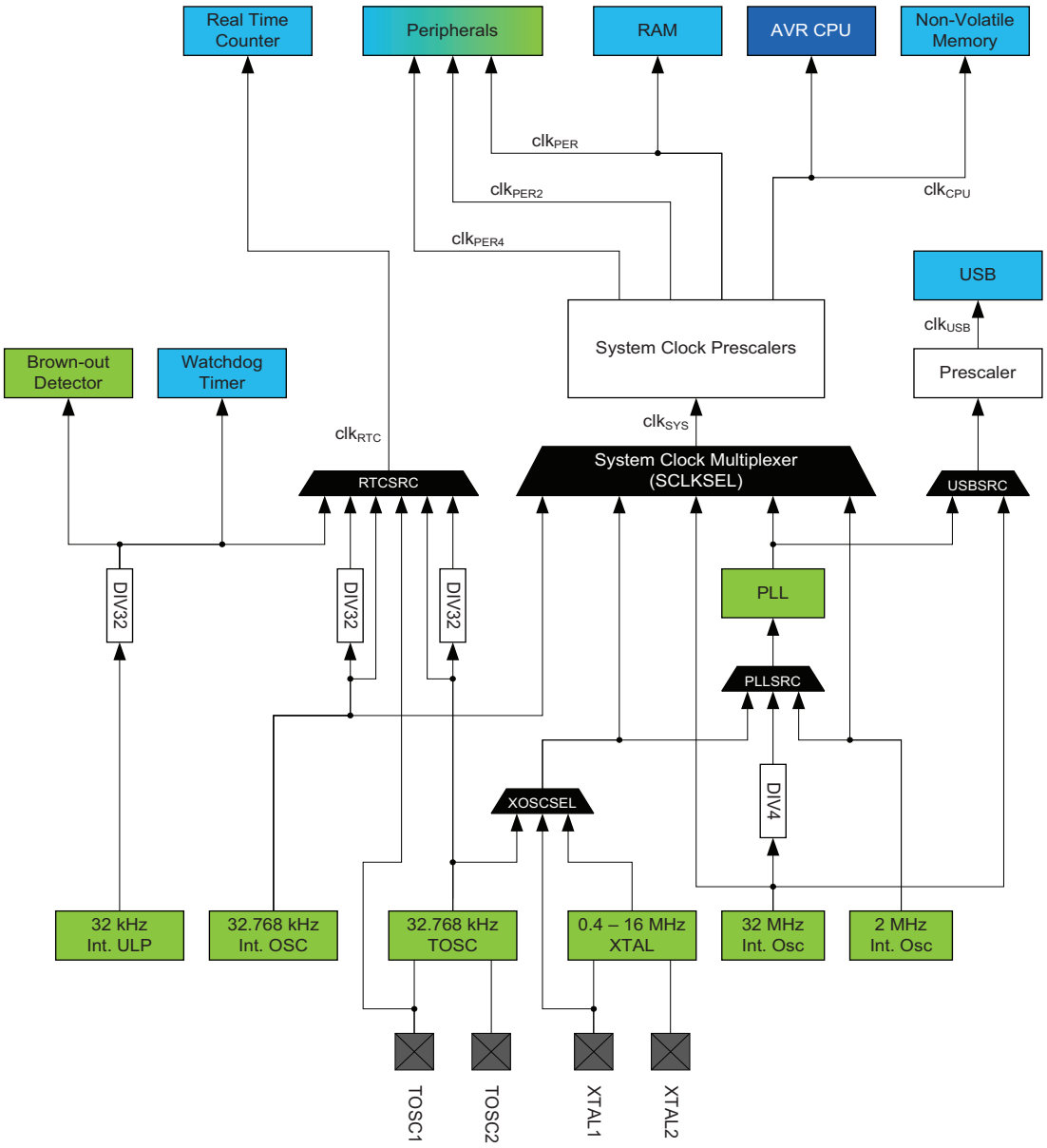
## 10.2 Overview

Atmel AVR XMEGA A4U devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 10-1 on page 22 presents the principal clock system in the XMEGA A4U family of devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 24.

**Figure 10-1. The clock system, clock sources and clock distribution.**




## 10.3 Clock Sources

The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources, DFLLs and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

### 10.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides

a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

### 10.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

### 10.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

### 10.3.4 0.4 - 16MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

### 10.3.5 2MHz Run-time Calibrated Internal Oscillator

The 2MHz run-time calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. A DFLL can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy.

### 10.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency looked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30MHz and 55MHz. The production signature row contains 48MHz calibration values intended used when the oscillator is used a full-speed USB clock source.

### 10.3.7 External Clock Sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 can be used as input for an external clock signal. The TOSC1 and TOSC2 pins is dedicated to driving a 32.768kHz crystal oscillator.

### 10.3.8 PLL with 1x-31x Multiplication Factor

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

# 11. Power Management and Sleep Modes

## 11.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

## 11.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

## 11.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

### 11.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, event system and DMA controller are kept running. Any enabled interrupt will wake the device.

### 11.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

### 11.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

### 11.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

### 11.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

# 12. System Control and Reset

## 12.1 Features

- Reset the microcontroller and set it to initial state when a reset source goes active
- Multiple reset sources that cover different situations
  - Power-on reset
  - External reset
  - Watchdog reset
  - Brownout reset
  - PDI reset
  - Software reset
- Asynchronous operation
  - No running system clock in the device is required for reset
- Reset status register for reading the reset source from the application code

## 12.2 Overview

The reset system issues a microcontroller reset and sets the device to its initial state. This is for situations where operation should not start or continue, such as when the microcontroller operates below its power supply rating. If a reset source goes active, the device enters and is kept in reset until all reset sources have released their reset. The I/O pins are immediately tri-stated. The program counter is set to the reset vector location, and all I/O registers are set to their initial values. The SRAM content is kept. However, if the device accesses the SRAM when a reset occurs, the content of the accessed location can not be guaranteed.

After reset is released from all reset sources, the default oscillator is started and calibrated before the device starts running from the reset vector address. By default, this is the lowest program memory address, 0, but it is possible to move the reset vector to the lowest address in the boot section.

The reset functionality is asynchronous, and so no running system clock is required to reset the device. The software reset feature makes it possible to issue a controlled system reset from the user software.

The reset status register has individual status flags for each reset source. It is cleared at power-on reset, and shows which sources have issued a reset since the last power-on.

## 12.3 Reset Sequence

A reset request from any reset source will immediately reset the device and keep it in reset as long as the request is active. When all reset requests are released, the device will go through three stages before the device starts running again:

- Reset counter delay
- Oscillator startup
- Oscillator calibration

If another reset requests occurs during this process, the reset sequence will start over again.

## 12.4 Reset Sources

### 12.4.1 Power-on Reset

A power-on reset (POR) is generated by an on-chip detection circuit. The POR is activated when the $V_{CC}$ rises and reaches the POR threshold voltage ($V_{POT}$), and this will start the reset sequence.

The POR is also activated to power down the device properly when the $V_{CC}$ falls and drops below the $V_{POT}$ level.

The $V_{POT}$ level is higher for falling $V_{CC}$ than for rising $V_{CC}$. Consult the datasheet for POR characteristics data.

### 12.4.2 Brownout Detection

The on-chip brownout detection (BOD) circuit monitors the $V_{CC}$ level during operation by comparing it to a fixed, programmable level that is selected by the BODLEVEL fuses. If disabled, BOD is forced on at the lowest level during chip erase and when the PDI is enabled.

### 12.4.3 External Reset

The external reset circuit is connected to the external $\overline{\text{RESET}}$ pin. The external reset will trigger when the $\overline{\text{RESET}}$ pin is driven below the $\overline{\text{RESET}}$ pin threshold voltage, $V_{RST}$, for longer than the minimum pulse period, $t_{EXT}$. The reset will be held as long as the pin is kept low. The $\overline{\text{RESET}}$ pin includes an internal pull-up resistor.

### 12.4.4 Watchdog Reset

The watchdog timer (WDT) is a system function for monitoring correct program operation. If the WDT is not reset from the software within a programmable timeout period, a watchdog reset will be given. The watchdog reset is active for one to two clock cycles of the 2MHz internal oscillator. For more details see "WDT – Watchdog Timer" on page 28.

### 12.4.5 Software Reset

The software reset makes it possible to issue a system reset from software by writing to the software reset bit in the reset control register.The reset will be issued within two CPU clock cycles after writing the bit. It is not possible to execute any instruction from when a software reset is requested until it is issued.

### 12.4.6 Program and Debug Interface Reset

The program and debug interface reset contains a separate reset source that is used to reset the device during external programming and debugging. This reset source is accessible only from external debuggers and programmers.

# 13. WDT – Watchdog Timer

## 13.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

## 13.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

# 14. Interrupts and Programmable Multilevel Interrupt Controller

## 14.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

## 14.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

## 14.3 Interrupt vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA A4U devices are shown in Table 14-1 on page 30. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA AU manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 14-1 on page 30. The program address is the word address.

**Table 14-1. Reset and interrupt vectors**

| Program address (base address) | Source | Interrupt description |
|---|---|---|
| 0x000 | RESET | |
| 0x002 | OSCF_INT_vect | Crystal oscillator failure interrupt vector (NMI) |
| 0x004 | PORTC_INT_base | Port C interrupt base |
| 0x008 | PORTR_INT_base | Port R interrupt base |
| 0x00C | DMA_INT_base | DMA controller interrupt base |
| 0x014 | RTC_INT_base | Real time counter interrupt base |
| 0x018 | TWIC_INT_base | Two-Wire Interface on Port C interrupt base |
| 0x01C | TCC0_INT_base | Timer/counter 0 on port C interrupt base |
| 0x028 | TCC1_INT_base | Timer/counter 1 on port C interrupt base |
| 0x030 | SPIC_INT_vect | SPI on port C interrupt vector |
| 0x032 | USARTC0_INT_base | USART 0 on port C interrupt base |
| 0x038 | USARTC1_INT_base | USART 1 on port C interrupt base |
| 0x03E | AES_INT_vect | AES interrupt vector |
| 0x040 | NVM_INT_base | Nonvolatile Memory interrupt base |
| 0x044 | PORTB_INT_base | Port B interrupt base |
| 0x056 | PORTE_INT_base | Port E interrupt base |
| 0x05A | TWIE_INT_base | Two-wire Interface on Port E interrupt base |
| 0x05E | TCE0_INT_base | Timer/counter 0 on port E interrupt base |
| 0x06A | TCE1_INT_base | Timer/counter 1 on port E interrupt base |
| 0x074 | USARTE0_INT_base | USART 0 on port E interrupt base |
| 0x080 | PORTD_INT_base | Port D interrupt base |
| 0x084 | PORTA_INT_base | Port A interrupt base |
| 0x088 | ACA_INT_base | Analog Comparator on Port A interrupt base |
| 0x08E | ADCA_INT_base | Analog to Digital Converter on Port A interrupt base |
| 0x09A | TCD0_INT_base | Timer/counter 0 on port D interrupt base |
| 0x0A6 | TCD1_INT_base | Timer/counter 1 on port D interrupt base |
| 0x0AE | SPID_INT_vector | SPI on port D interrupt vector |
| 0x0B0 | USARTD0_INT_base | USART 0 on port D interrupt base |
| 0x0B6 | USARTD1_INT_base | USART 1 on port D interrupt base |
| 0x0FA | USB_INT_base | USB on port D interrupt base |

# 15. I/O Ports

## 15.1 Features

- 34 general purpose input and output pins with individual configuration
- Output driver with configurable driver and pull settings:
  - Totem-pole
  - Wired-AND
  - Wired-OR
  - Bus-keeper
  - Inverted I/O
- Input with synchronous and/or asynchronous sensing with interrupts and events
  - Sense both edges
  - Sense rising edges
  - Sense falling edges
  - Sense low level
- Optional pull-up and pull-down resistor on input and Wired-OR/AND configurations
- Optional slew rate control
- Asynchronous pin change sensing that can wake the device from all sleep modes
- Two port interrupts with pin masking per I/O port
- Efficient and safe access to port pins
  - Hardware read-modify-write through dedicated toggle/clear/set registers
  - Configuration of multiple pins in a single operation
  - Mapping of port registers into bit-accessible I/O memory space
- Peripheral clocks output on port pin
- Real-time counter clock output to port pin
- Event channels can be output on port pin
- Remapping of digital peripheral pin functions
  - Selectable USART, SPI, and timer/counter input/output pin locations

## 15.2 Overview

One port consists of up to eight port pins: pin 0 to 7. Each port pin can be configured as input or output with configurable driver and pull settings. They also implement synchronous and asynchronous input sensing with interrupts and events for selectable pin change conditions. Asynchronous pin-change sensing means that a pin change can wake the device from all sleep modes, included the modes where no clocks are running.

All functions are individual and configurable per pin, but several pins can be configured in a single operation. The pins have hardware read-modify-write (RMW) functionality for safe and correct change of drive value and/or pull resistor configuration. The direction of one port pin can be changed without unintentionally changing the direction of any other pin.

The port pin configuration also controls input and output selection of other device functions. It is possible to have both the peripheral clock and the real-time clock output to a port pin, and available for external use. The same applies to events from the event system that can be used to synchronize and control external functions. Other digital peripherals, such as USART, SPI, and timer/counters, can be remapped to selectable pin locations in order to optimize pin-out versus application needs.

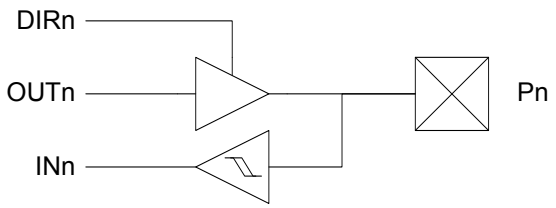
The notation of the ports are PORTA, PORTB, PORTC, PORTD, PORTE, and PORTR.

## 15.3 Output Driver

All port pins (Pn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

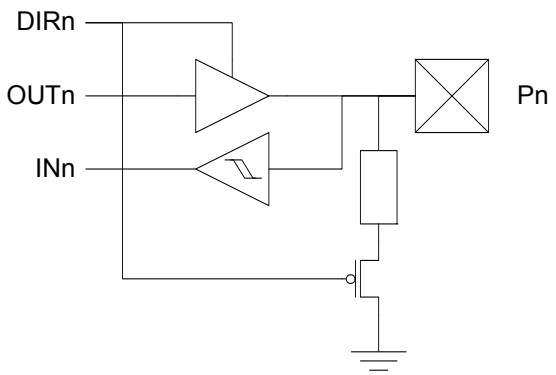
### 15.3.1 Push-pull

**Figure 15-1. I/O configuration - Totem-pole.**



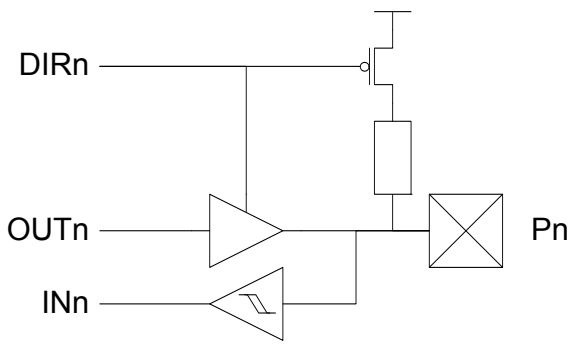

### 15.3.2 Pull-down

**Figure 15-2. I/O configuration - Totem-pole with pull-down (on input).**




### 15.3.3 Pull-up

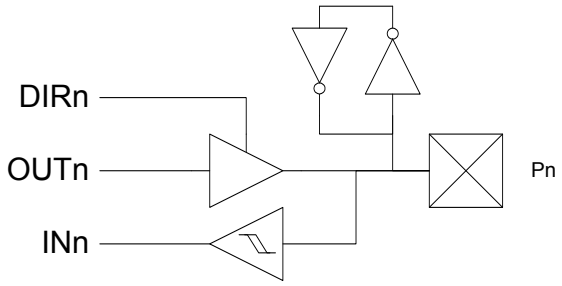
**Figure 15-3. I/O configuration - Totem-pole with pull-up (on input).**




### 15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

**Figure 15-4. I/O configuration - Totem-pole with bus-keeper.**




### 15.3.5 Others

**Figure 15-5. Output configuration - Wired-OR with optional pull-down.**

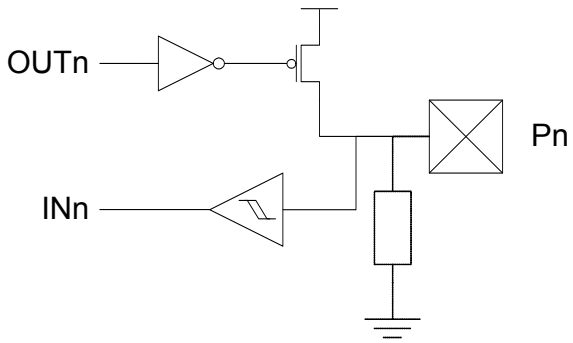
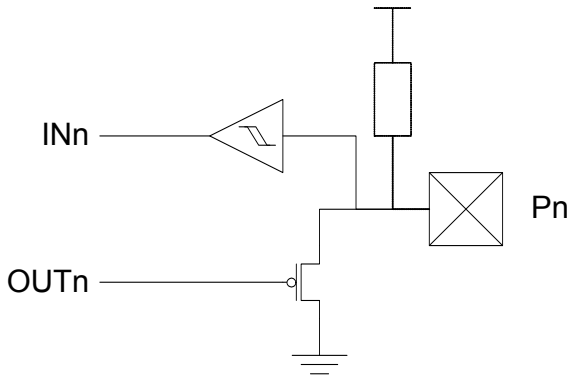


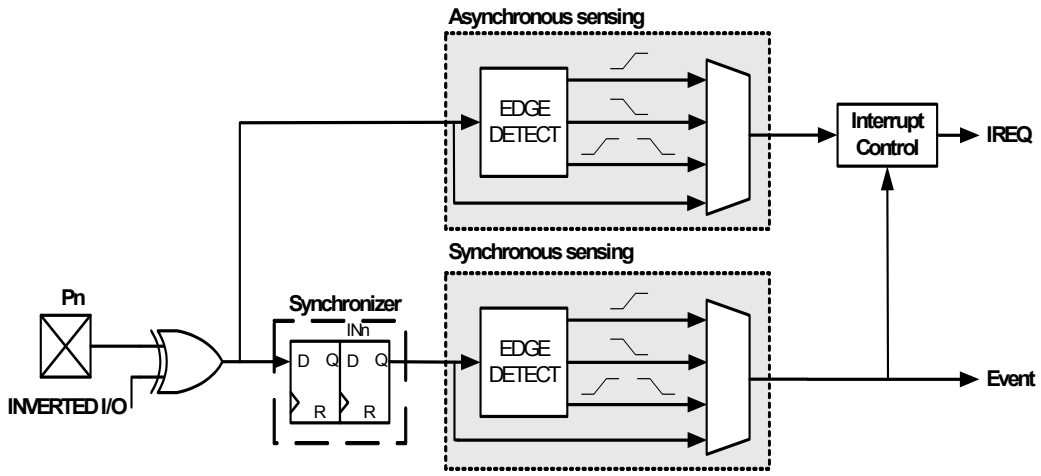

**Figure 15-6. I/O configuration - Wired-AND with optional pull-up.**



## 15.4 Input sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 15-7.

**Figure 15-7. Input sensing system overview.**




When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

## 15.5 Alternate Port Functions

Most port pins have alternate pin functions in addition to being a general purpose I/O pin. When an alternate function is enabled, it might override the normal port pin function or pin value. This happens when other peripherals that require pins are enabled or configured to use pins. If and how a peripheral will override and use pins is described in the section for that peripheral. "Pinout and Pin Functions" on page 55 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

# 16. TC0/1 – 16-bit Timer/Counter Type 0 and 1

## 16.1 Features

- Five 16-bit timer/counters
  - Three timer/counters of type 0
  - Two timer/counters of type 1
  - Split-mode enabling two 8-bit timer/counter from each timer/counter type 0
- 32-bit timer/counter support by cascading two timer/counters
- Up to four compare or capture (CC) channels
  - Four CC channels for timer/counters of type 0
  - Two CC channels for timer/counters of type 1
- Double buffered timer period setting
- Double buffered capture or compare channels
- Waveform generation:
  - Frequency generation
  - Single-slope pulse width modulation
  - Dual-slope pulse width modulation
- Input capture:
  - Input capture with noise cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Timer overflow and error interrupts/events
- One compare match or input capture interrupt/event per CC channel
- Can be used with event system for:
  - Quadrature decoding
  - Count and direction control
  - Capture
- Can be used with DMA and to trigger DMA transactions
- High-resolution extension
  - Increases frequency and waveform resolution by 4x (2-bit) or 8x (3-bit)
- Advanced waveform extension:
  - Low- and high-side output with programmable dead-time insertion (DTI)
- Event controlled fault protection for safe disabling of drivers

## 16.2 Overview

Atmel AVR XMEGA devices have a set of five flexible 16-bit Timer/Counters (TC). Their capabilities include accurate program execution timing, frequency and waveform generation, and input capture with time and frequency measurement of digital signals. Two timer/counters can be cascaded to create a 32-bit timer/counter with optional 32-bit capture.

A timer/counter consists of a base counter and a set of compare or capture (CC) channels. The base counter can be used to count clock cycles or events. It has direction control and period setting that can be used for timing. The CC channels can be used together with the base counter to do compare match control, frequency generation, and pulse width waveform modulation, as well as various input capture operations. A timer/counter can be configured for either capture or compare functions, but cannot perform both at the same time.

A timer/counter can be clocked and timed from the peripheral clock with optional prescaling or from the event system. The event system can also be used for direction control and capture trigger or to synchronize operations.

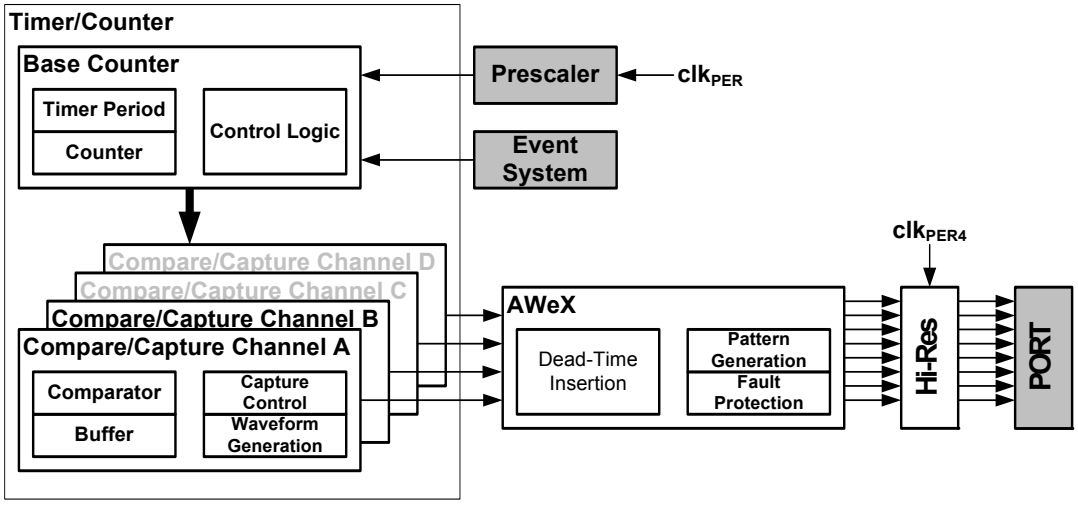
There are two differences between timer/counter type 0 and type 1. Timer/counter 0 has four CC channels, and timer/counter 1 has two CC channels. All information related to CC channels 3 and 4 is valid only for timer/counter 0. Only Timer/Counter 0 has the split mode feature that split it into two 8-bit Timer/Counters with four compare channels each.

Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This are only available for Timer/Counter 0. See "AWeX – Advanced Waveform Extension" on page 38 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See "Hi-Res – High Resolution Extension" on page 39 for more details.

**Figure 16-1. Overview of a Timer/Counter and closely related peripherals.**




PORTC and PORTD each has one Timer/Counter 0 and one Timer/Counter1. PORTE has one Timer/Conter0. Notation of these are TCC0 (Time/Counter C0), TCC1, TCD0, TCD1 and TCE0, respectively.

# 17. TC2 - Timer/Counter Type 2

## 17.1 Features

- Six eight-bit timer/counters
  - Three Low-byte timer/counter
  - Three High-byte timer/counter
- Up to eight compare channels in each Timer/Counter 2
  - Four compare channels for the low-byte timer/counter
  - Four compare channels for the high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control
- Can be used to trigger DMA transactions

## 17.2 Overview

There are four Timer/Counter 2. These are realized when a Timer/Counter 0 is set in split mode. It is then a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts, events and DMA triggers. The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

PORTC, and PORTD each has one Timer/Counter 2.

Notation of these are TCC2 (Time/Counter C2) and TCD2, respectively.

# 18. AWeX – Advanced Waveform Extension

## 18.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
  - 8-bit resolution
  - Separate high and low side dead-time setting
  - Double buffered dead time
  - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
  - Double buffered pattern generation
  - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

## 18.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the timer/counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives flexibility in the selection of fault triggers.

The AWeX is available for TCC0. The notation of this is AWEXC.

# 19. Hi-Res – High Resolution Extension

## 19.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

## 19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock ($Clk_{PER4}$). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There are three hi-res extensions that each can be enabled for each timer/counters pair on PORTC, PORTD and PORTE. The notation of these are HIRESC, HIRESD and HIRESE, respectively.

# 20. RTC – 16-bit Real-Time Counter

## 20.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

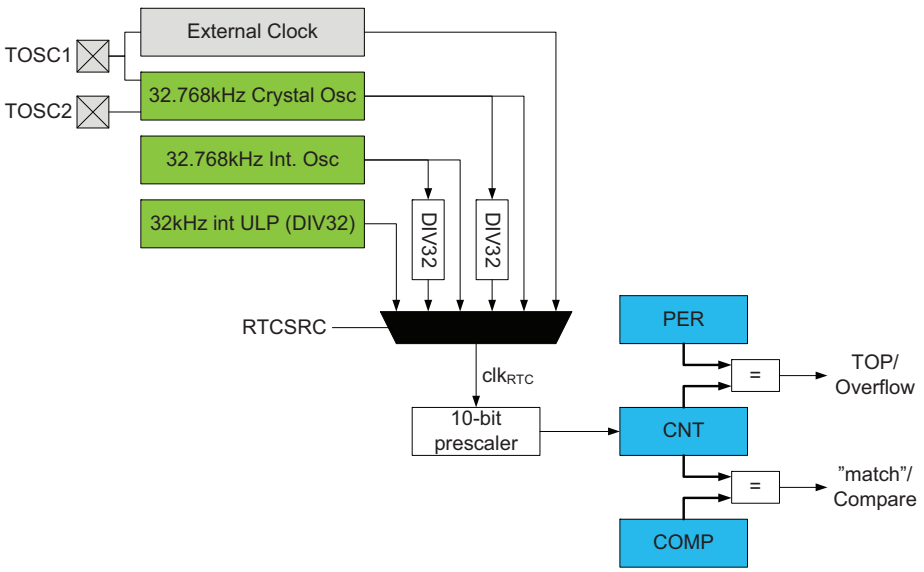
## 20.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

**Figure 20-1. Real-time counter overview.**



# 21. USB – Universal Serial Bus Interface

## 21.1 Features

- One USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface
- Integrated on-chip USB transceiver, no external components needed
- 16 endpoint addresses with full endpoint flexibility for up to 31 endpoints
  - One input endpoint per endpoint address
  - One output endpoint per endpoint address
- Endpoint address transfer type selectable to
  - Control transfers
  - Interrupt transfers
  - Bulk transfers
  - Isochronous transfers
- Configurable data payload size per endpoint, up to 1023 bytes
- Endpoint configuration and data buffers located in internal SRAM
  - Configurable location for endpoint configuration data
  - Configurable location for each endpoint's data buffer
- Built-in direct memory access (DMA) to internal SRAM for:
  - Endpoint configurations
  - Reading and writing endpoint data
- Ping-pong operation for higher throughput and double buffered operation
  - Input and output endpoint data buffers used in a single direction
  - CPU/DMA controller can update data buffer during transfer
- Multipacket transfer for reduced interrupt load and software intervention
  - Data payload exceeding maximum packet size is transferred in one continuous transfer
  - No interrupts or software interaction on packet transaction level
- Transaction complete FIFO for workflow management when using multiple endpoints
  - Tracks all completed transactions in a first-come, first-served work queue
- Clock selection independent of system clock source and selection
- Minimum 1.5MHz CPU clock required for low speed USB operation
- Minimum 12MHz CPU clock required for full speed operation
- Connection to event system
- On chip debug possibilities during USB transactions

## 21.2 Overview

The USB module is a USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface.

The USB supports 16 endpoint addresses. All endpoint addresses have one input and one output endpoint, for a total of 31 configurable endpoints and one control endpoint. Each endpoint address is fully configurable and can be configured for any of the four transfer types; control, interrupt, bulk, or isochronous. The data payload size is also selectable, and it supports data payloads up to 1023 bytes.

No dedicated memory is allocated for or included in the USB module. Internal SRAM is used to keep the configuration for each endpoint address and the data buffer for each endpoint. The memory locations used for endpoint configurations and data buffers are fully configurable. The amount of memory allocated is fully dynamic, according to the number of endpoints in use and the configuration of these. The USB module has built-in direct memory access (DMA), and will read/write data from/to the SRAM when a USB transaction takes place.

To maximize throughput, an endpoint address can be configured for ping-pong operation. When done, the input and output endpoints are both used in the same direction. The CPU or DMA controller can then read/write one data buffer while the USB module writes/reads the others, and vice versa. This gives double buffered communication.

Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USB.

# 22. TWI – Two-Wire Interface

## 22.1 Features

- Two Identical two-wire interface peripherals
- Bidirectional, two-wire communication interface
  - Phillips $I^2C$ compatible
  - System Management Bus (SMBus) compatible
- Bus master and slave operation supported
  - Slave operation
  - Single bus master operation
  - Bus master in multi-master bus environment
  - Multi-master arbitration
- Flexible slave address match functions
  - 7-bit and general call address recognition in hardware
  - 10-bit addressing supported
  - Address mask register for dual address match or address range masking
  - Optional software address recognition for unlimited number of addresses
- Slave can operate in all sleep modes, including power-down
- Slave address match can wake device from all sleep modes
- 100kHz and 400kHz bus frequency support
- Slew-rate limited output drivers
- Input filter for bus noise and spike suppression
- Support arbitration between start/repeated start and data bit (SMBus)
- Slave arbitration allows support for address resolve protocol (ARP) (SMBus)

## 22.2 Overview

The two-wire interface (TWI) is a bidirectional, two-wire communication interface. It is $I^2C$ and System Management Bus (SMBus) compatible. The only external hardware needed to implement the bus is one pull-up resistor on each bus line.

A device connected to the bus must act as a master or a slave. The master initiates a data transaction by addressing a slave on the bus and telling whether it wants to transmit or receive data. One bus can have many slaves and one or several masters that can take control of the bus. An arbitration process handles priority if more than one master tries to transmit data at the same time. Mechanisms for resolving bus contention are inherent in the protocol.

The TWI module supports master and slave functionality. The master and slave functionality are separated from each other, and can be enabled and configured separately. The master module supports multi-master bus operation and arbitration. It contains the baud rate generator. Both 100kHz and 400kHz bus frequency is supported. Quick command and smart mode can be enabled to auto-trigger operations and reduce software complexity.

The slave module implements 7-bit address match and general address call recognition in hardware. 10-bit addressing is also supported. A dedicated address mask register can act as a second address match register or as a register for address range masking. The slave continues to operate in all sleep modes, including power-down mode. This enables the slave to wake up the device from all sleep modes on TWI address match. It is possible to disable the address matching to let this be handled in software instead.

The TWI module will detect START and STOP conditions, bus collisions, and bus errors. Arbitration lost, errors, collision, and clock hold on the bus are also detected and indicated in separate status flags available in both master and slave modes.

It is possible to disable the TWI drivers in the device, and enable a four-wire digital interface for connecting to an external TWI bus driver. This can be used for applications where the device operates from a different $V_{CC}$ voltage than used by the TWI bus.

PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

# 23. SPI – Serial Peripheral Interface

## 23.1 Features

- Two Identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

## 23.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID.

# 24. USART

## 24.1 Features

- Five identical USART peripherals
- Full-duplex operation
- Asynchronous or synchronous operation
  - Synchronous clock rates up to 1/2 of the device clock frequency
  - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits
- Fractional baud rate generator
  - Can generate desired baud rate from any system clock frequency
  - No need for external oscillator with certain frequencies
- Built-in error detection and correction schemes
  - Odd or even parity generation and parity check
  - Data overrun and framing error detection
  - Noise filtering includes false start bit detection and digital low-pass filter
- Separate interrupts for
  - Transmit complete
  - Transmit data register empty
  - Receive complete
- Multiprocessor communication mode
  - Addressing scheme to address a specific devices on a multidevice bus
  - Enable unaddressed devices to automatically ignore all frames
- Master SPI mode
  - Double buffered operation
  - Operation up to 1/2 of the peripheral clock frequency
- IRCOM module for IrDA compliant pulse modulation/demodulation

## 24.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2Kbps.

PORTC and PORTD each has two USARTs. PORTE has one USART. Notation of these peripherals are USARTC0, USARTC1, USARTD0, USARTD1 and USARTE0, respectively.

# 25. IRCOM – IR Communication Module

## 25.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
  - 3/16 of the baud rate period
  - Fixed pulse period, 8-bit programmable
  - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

## 25.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

# 26. AES and DES Crypto Engine

## 26.1 Features

- Data Encryption Standard (DES) CPU instruction
- Advanced Encryption Standard (AES) crypto module
- DES Instruction
  - Encryption and decryption
  - DES supported
  - Encryption/decryption in 16 CPU clock cycles per 8-byte block
- AES crypto module
  - Encryption and decryption
  - Supports 128-bit keys
  - Supports XOR data load mode to the state memory
  - Encryption/decryption in 375 clock cycles per 16-byte block

## 26.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used standards for cryptography. These are supported through an AES peripheral module and a DES CPU instruction, and the communication interfaces and the CPU can use these for fast, encrypted communication and secure data storage.

DES is supported by an instruction in the AVR CPU. The 8-byte key and 8-byte data blocks must be loaded into the register file, and then the DES instruction must be executed 16 times to encrypt/decrypt the data block.

The AES crypto module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done. The encrypted/encrypted data can then be read out, and an optional interrupt can be generated. The AES crypto module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

# 27. CRC – Cyclic Redundancy Check Generator

## 27.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory, DMA controller and CPU
  - Continuous CRC on data going through a DMA channel
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

## 27.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- **CRC-16:**

| | |
|---|---|
| Polynomial: | $x^{16}+x^{12}+x^{5}+1$ |
| Hex value: | 0x1021 |

- **CRC-32:**

| | |
|---|---|
| Polynomial: | $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$ |
| Hex value: | 0x04C11DB7 |

# 28. ADC – 12-bit Analog to Digital Converter

## 28.1 Features

- One Analog to Digital Converter (ADC)
- 12-bit resolution
- Up to two million samples per second
  - Two inputs can be sampled simultaneously using ADC and 1x gain stage
  - Four inputs can be sampled within 1.5µs
  - Down to 2.5µs conversion time with 8-bit resolution
  - Down to 3.5µs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 12 single-ended inputs
  - 12x4 differential inputs without gain
  - 8x4 differential inputs with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Four internal inputs
  - Internal temperature sensor
  - DAC output
  - $AV_{CC}$ voltage divided by 10
  - 1.1V bandgap voltage
- Four conversion channels with individual input control and result registers
  - Enable four parallel configurations and results
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional DMA transfer of conversion results
- Optional interrupt/event on compare result

## 28.2 Overview

The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to two million samples per second (msps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

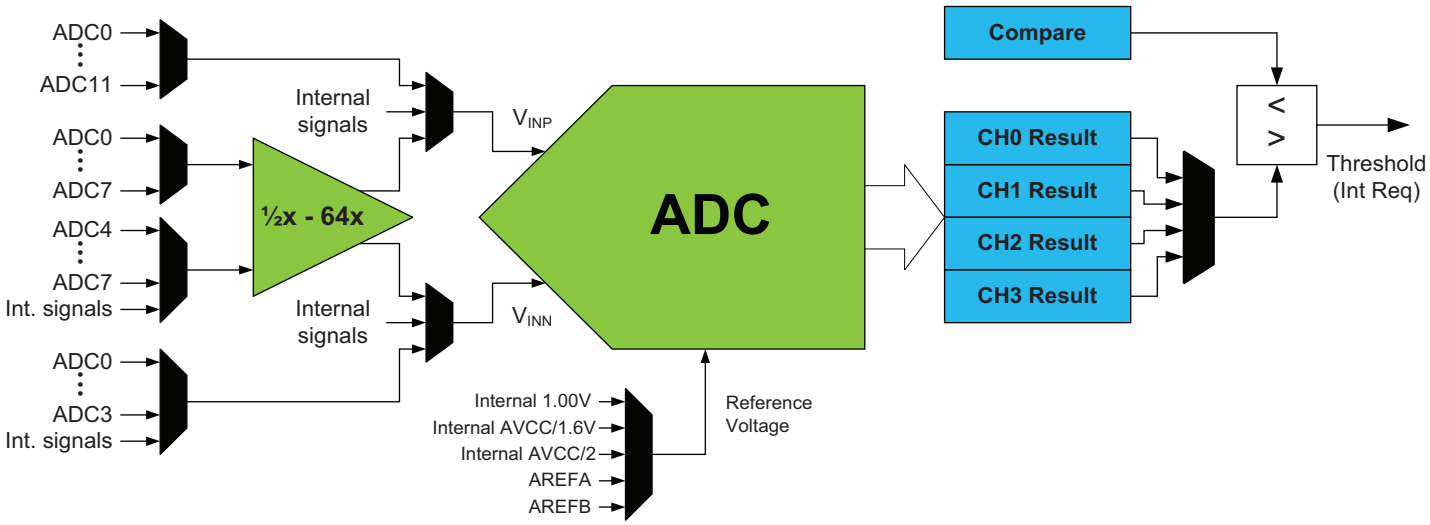
This is a pipelined ADC that consists of several consecutive stages. The pipelined design allows a high sample rate at a low system clock frequency. It also means that a new input can be sampled and a new ADC conversion started while other ADC conversions are still ongoing. This removes dependencies between sample rate and propagation delay.

The ADC has four conversion channels (0-3) with individual input selection, result registers, and conversion start control. The ADC can then keep and use four parallel configurations and results, and this will ease use for applications with high data throughput or for multiple modules using the ADC independently. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The output from the DAC, $AV_{CC}/10$ and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

**Figure 28-1. ADC overview.**




Two inputs can be sampled simultaneously as both the ADC and the gain stage include sample and hold circuits, and the gain stage has 1x gain setting. Four inputs can be sampled within 1.5µs without any intervention by the application.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5µs for 12-bit to 2.5µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA has one ADC. Notation of this peripheral is ADCA.

# 29. DAC – 12-bit Digital to Analog Converter

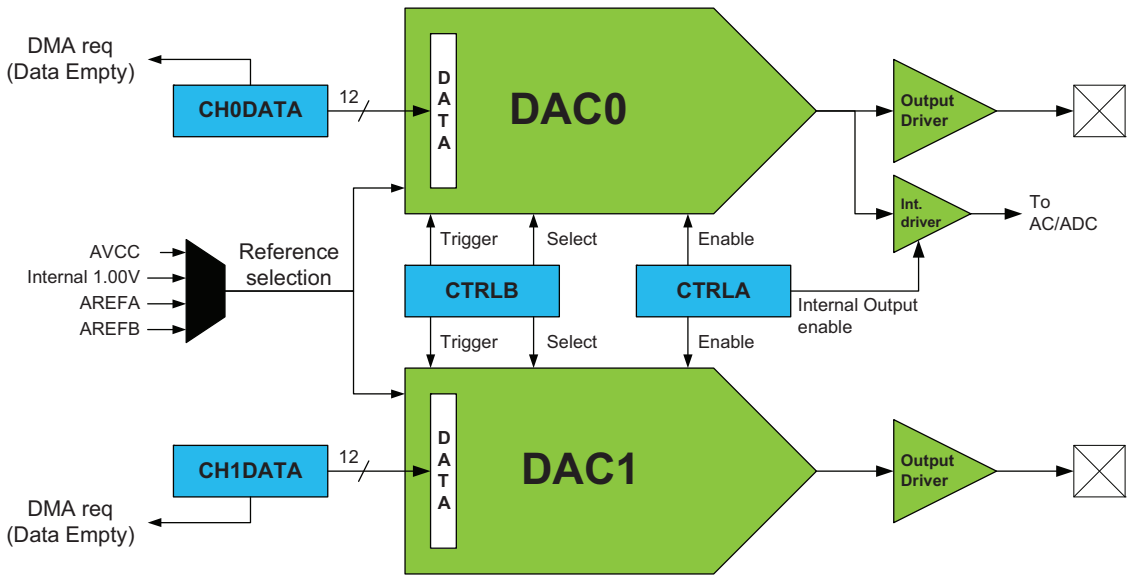
## 29.1 Features

- One Digital to Analog Converter (DAC)
- 12-bit resolution
- Two independent, continuous-drive output channels
- Up to one million samples per second conversion rate per DAC channel
- Built-in calibration that removes:
  - Offset error
  - Gain error
- Multiple conversion trigger sources
  - On new available data
  - Events from the event system
- High drive capabilities and support for
  - Resistive loads
  - Capacitive loads
  - Combined resistive and capacitive loads
- Internal and external reference options
- DAC output available as input to analog comparator and ADC
- Low-power mode, with reduced drive strength
- Optional DMA transfer of data

## 29.2 Overview

The digital-to-analog converter (DAC) converts digital values to voltages. The DAC has two channels, each with 12-bit resolution, and is capable of converting up to one million samples per second (msps) on each channel. The built-in calibration system can remove offset and gain error when loaded with calibration values from software.

**Figure 29-1. DAC overview.**



A DAC conversion is automatically started when new data to be converted are available. Events from the event system can also be used to trigger a conversion, and this enables synchronized and timed conversions between the DAC and other peripherals, such as a timer/counter. The DMA controller can be used to transfer data to the DAC.

The DAC has high drive strength, and is capable of driving both resistive and capacitive loads, aswell as loads which combine both. A low-power mode is available, which will reduce the drive strength of the output. Internal and external voltage references can be used. The DAC output is also internally available for use as input to the analog comparator or ADC.

PORTB has one DAC. Notation of this peripheral is DACB.

# 30. AC – Analog Comparator

## 30.1 Features

- Two Analog Comparators (ACs)
- Selectable propagation delay versus current consumption
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal $AV_{CC}$ voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

## 30.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

Two important properties of the analog comparator's dynamic behavior are: hysteresis and propagation delay. Both of these parameters may be adjusted in order to achieve the optimal operation for each application.

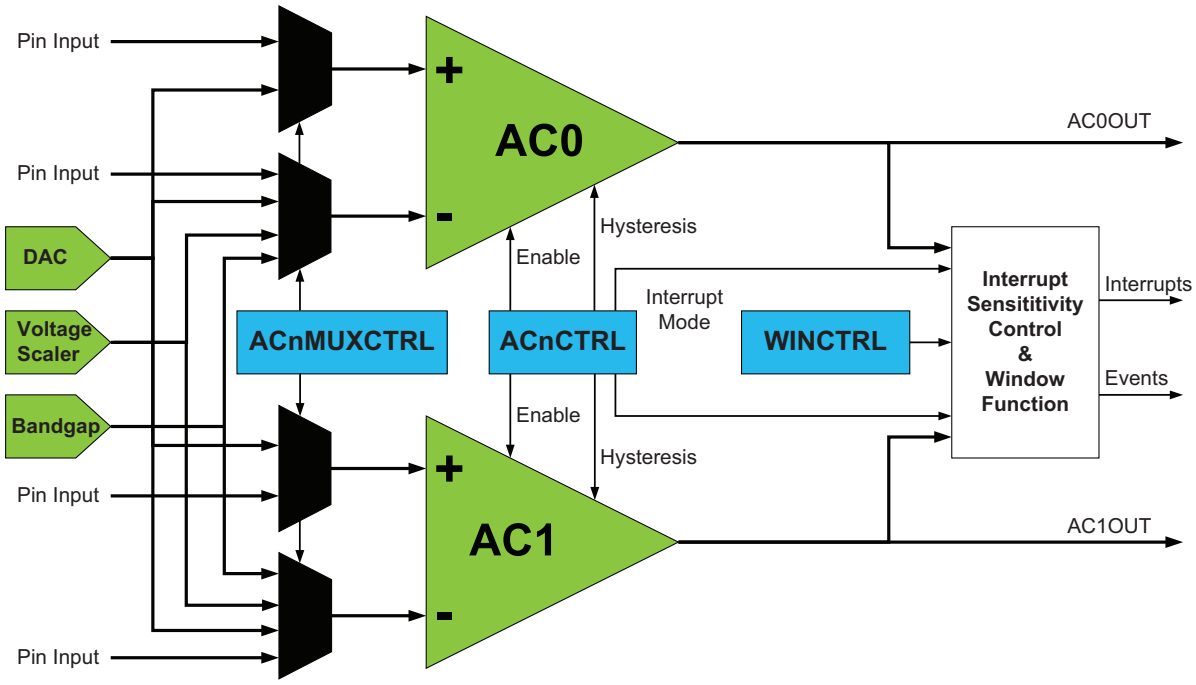
The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

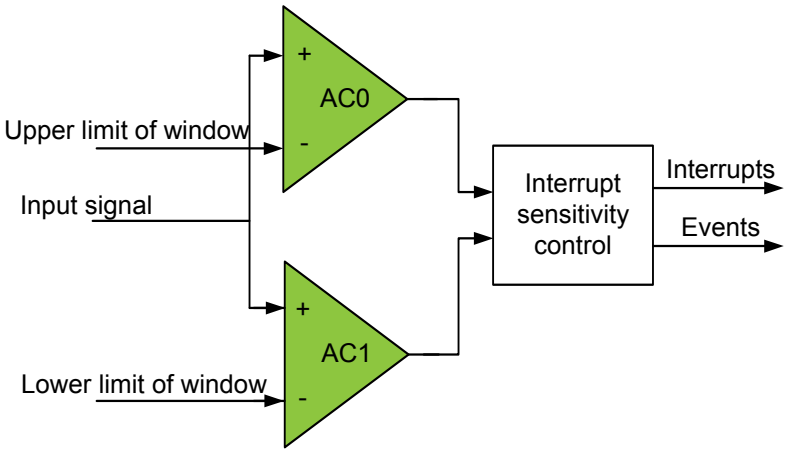
PORTA has one AC pair. Notation is ACA.

**Figure 30-1. Analog comparator overview.**




The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 30-2.

**Figure 30-2. Analog comparator window function.**



# 31. Programming and Debugging

## 31.1 Features

- Programming
  - External programming through PDI interface
    - Minimal protocol overhead for fast operation
    - Built-in error detection and handling for reliable operation
  - Boot loader support for programming through any communication interface
- Debugging
  - Nonintrusive, real-time, on-chip debug system
  - No software or hardware resources required from device except pin connection
  - Program flow control
    - Go, Stop, Reset, Step Into, Step Over, Step Out, Run-to-Cursor
  - Unlimited number of user program breakpoints
  - Unlimited number of user data breakpoints, break on:
    - Data location read, write, or both read and write
    - Data location content equal or not equal to a value
    - Data location content is greater or smaller than a value
    - Data location content is within or outside a range
  - No limitation on device clock frequency
- Program and Debug Interface (PDI)
  - Two-pin interface for external programming and debugging
  - Uses the Reset pin and a dedicated pin
  - No I/O pins required during programming or debugging

## 31.2 Overview

The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of a device.

The PDI supports fast programming of nonvolatile memory (NVM) spaces; flash, EEPOM, fuses, lock bits, and the user signature row.

Debug is supported through an on-chip debug system that offers nonintrusive, real-time debug. It does not require any software or hardware resources except for the device pin connection. Using the Atmel tool chain, it offers complete program flow control and support for an unlimited number of program and complex data breakpoints. Application debug can be done from a C or other high-level language source code level, as well as from an assembler and disassembler level.

Programming and debugging can be done through the PDI physical layer. This is a two-pin interface that uses the Reset pin for the clock input (PDI_CLK) and one other dedicated pin for data input and output (PDI_DATA). Any external programmer or on-chip debugger/emulator can be directly connected to this interface.

# 32. Pinout and Pin Functions

The device pinout is shown in “Pinout/Block Diagram” on page 4. In addition to general purpose I/O functionality, each pin can have several alternate functions. This will depend on which peripheral is enabled and connected to the actual pin. Only one of the pin functions can be used at time.

## 32.1 Alternate Pin Function Description

The tables below show the notation for all pin functions available and describe its function.

### 32.1.1 Operation/Power Supply

| | |
|---|---|
| $V_{CC}$ | Digital supply voltage |
| $AV_{CC}$ | Analog supply voltage |
| GND | Ground |

### 32.1.2 Port Interrupt functions

| | |
|---|---|
| SYNC | Port pin with full synchronous and limited asynchronous interrupt function |
| ASYNC | Port pin with full synchronous and full asynchronous interrupt function |

### 32.1.3 Analog functions

| | |
|---|---|
| ACn | Analog Comparator input pin n |
| ACnOUT | Analog Comparator n Output |
| ADCn | Analog to Digital Converter input pin n |
| DACn | Digital to Analog Converter output pin n |
| $A_{REF}$ | Analog Reference input pin |

### 32.1.4 Timer/Counter and AWEX functions

| | |
|---|---|
| OCnxLS | Output Compare Channel x Low Side for Timer/Counter n |
| OCnxHS | Output Compare Channel x High Side for Timer/Counter n |

### 32.1.5 Communication functions

| | |
|---|---|
| SCL | Serial Clock for TWI |
| SDA | Serial Data for TWI |
| SCLIN | Serial Clock In for TWI when external driver interface is enabled |
| SCLOUT | Serial Clock Out for TWI when external driver interface is enabled |
| SDAIN | Serial Data In for TWI when external driver interface is enabled |
| SDAOUT | Serial Data Out for TWI when external driver interface is enabled |
| XCKn | Transfer Clock for USART n |
| RXDn | Receiver Data for USART n |
| TXDn | Transmitter Data for USART n |
| SS | Slave Select for SPI |
| MOSI | Master Out Slave In for SPI |
| MISO | Master In Slave Out for SPI |
| SCK | Serial Clock for SPI |
| D- | Data- for USB |
| D+ | Data+ for USB |

### 32.1.6 Oscillators, Clock and Event

| | |
|---|---|
| TOSCn | Timer Oscillator pin n |
| XTALn | Input/Output for Oscillator pin n |
| CLKOUT | Peripheral Clock Output |
| EVOUT | Event Channel Output |
| RTCOUT | RTC Clock Source Output |

### 32.1.7 Debug/System functions

| | |
|---|---|
| RESET | Reset pin |
| PDI_CLK | Program and Debug Interface Clock pin |
| PDI_DATA | Program and Debug Interface Data pin |

## 32.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

**Table 32-1. Port A - alternate functions.**

| PORT A | PIN # | INTERRUPT | ADCA POS/ GAINPOS | ADCA NEG | ADCA GAINNEG | ACA POS | ACA NEG | ACAOUT | REFA |
|---|---|---|---|---|---|---|---|---|---|
| **GND** | 38 | | | | | | | | |
| **AVCC** | 39 | | | | | | | | |
| **PA0** | 40 | SYNC | ADC0 | ADC0 | | AC0 | AC0 | | AREF |
| **PA1** | 41 | SYNC | ADC1 | ADC1 | | AC1 | AC1 | | |
| **PA2** | 42 | SYNC/ASYNC | ADC2 | ADC2 | | AC2 | | | |
| **PA3** | 43 | SYNC | ADC3 | ADC3 | | AC3 | AC3 | | |
| **PA4** | 44 | SYNC | ADC4 | | ADC4 | AC4 | | | |
| **PA5** | 1 | SYNC | ADC5 | | ADC5 | AC5 | AC5 | | |
| **PA6** | 2 | SYNC | ADC6 | | ADC6 | AC6 | | AC1OUT | |
| **PA7** | 3 | SYNC | ADC7 | | ADC7 | | AC7 | AC0OUT | |

**Table 32-2. Port B - alternate functions.**

| PORT B | PIN # | INTERRUPT | ADCA POS | DACB | REFB |
|---|---|---|---|---|---|
| **PB0** | 4 | SYNC | ADC8 | | AREF |
| **PB1** | 5 | SYNC | ADC9 | | |
| **PB2** | 6 | SYNC/ASYNC | ADC10 | DAC0 | |
| **PB3** | 7 | SYNC | ADC11 | DAC1 | |

**Table 32-3. Port C - alternate functions.**

| PORT C | PIN # | INTERRUPT | TCC0 (1)(2) | AWEXC | TCC1 | USART C0(3) | USART C1 | SPIC(4) | TWIC | TWIC w/ext driver | CLOCKOUT (5) | EVENTOUT (6) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **GND** | 8 | | | | | | | | | | | |
| **VCC** | 9 | | | | | | | | | | | |
| **PC0** | 10 | SYNC | OC0A | $\overline{\text{OC0ALS}}$ | | | | | SDA | SDAIN | | |
| **PC1** | 11 | SYNC | OC0B | OC0AHS | | XCK0 | | | SCL | SCLIN | | |
| **PC2** | 12 | SYNC/ ASYNC | OC0C | $\overline{\text{OC0BLS}}$ | | RXD0 | | | | SDAOUT | | |
| **PC3** | 13 | SYNC | OC0D | OC0BHS | | TXD0 | | | | SCLOUT | | |
| **PC4** | 14 | SYNC | | $\overline{\text{OC0CLS}}$ | OC1A | | | $\overline{\text{SS}}$ | | | | |
| **PC5** | 15 | SYNC | | OC0CHS | OC1B | | XCK1 | MOSI | | | | |
| **PC6** | 16 | SYNC | | $\overline{\text{OC0DLS}}$ | | | RXD1 | MISO | | | $clk_{RTC}$ | |
| **PC7** | 17 | SYNC | | OC0DHS | | | TXD1 | SCK | | | $clk_{PER}$ | EVOUT |

Notes:
1. Pin mapping of all TC0 can optionally be moved to high nibble of port
2. If TC0 is configured as TC2 all eight pins can be used for PWM output.
3. Pin mapping of all USART0 can optionally be moved to high nibble of port.
4. Pins MOSI and SCK for all SPI can optionally be swapped.
5. CLKOUT can optionally be moved between port C, D and E and between pin 4 and 7.
6. EVOUT can optionally be moved between port C, D and E and between pin 4 and 7.

**Table 32-4. Port D - alternate functions.**

| PORT D | PIN # | INTERRUPT | TCD0 | TCD1 | USB | USARTD0 | USARTD1 | SPID | CLOCKOUT | EVENTOUT |
|---|---|---|---|---|---|---|---|---|---|---|
| **GND** | 18 | | | | | | | | | |
| **VCC** | 19 | | | | | | | | | |
| **PD0** | 20 | SYNC | OC0A | | | | | | | |
| **PD1** | 21 | SYNC | OC0B | | | XCK0 | | | | |
| **PD2** | 22 | SYNC/ASYNC | OC0C | | | RXD0 | | | | |
| **PD3** | 23 | SYNC | OC0D | | | TXD0 | | | | |
| **PD4** | 24 | SYNC | | OC1A | | | | $\overline{\text{SS}}$ | | |
| **PD5** | 25 | SYNC | | OC1B | | | XCK1 | MOSI | | |
| **PD6** | 26 | SYNC | | | D- | | RXD1 | MISO | | |
| **PD7** | 27 | SYNC | | | D+ | | TXD1 | SCK | $clk_{PER}$ | EVOUT |

**Table 32-5. Port E - alternate functions.**

| PORT E | PIN # | INTERRUPT | TCE0 | USARTE0 | TWIE |
|---|---|---|---|---|---|
| **PE0** | 28 | SYNC | OC0A | | SDA |
| **PE1** | 29 | SYNC | OC0B | XCK0 | SCL |
| **GND** | 30 | | | | |
| **VCC** | 31 | | | | |
| **PE2** | 32 | SYNC/ASYNC | OC0C | RXD0 | |
| **PE3** | 33 | SYNC | OC0D | TXD0 | |

**Table 32-6. Port R - alternate functions.**

| PORT R | PIN # | INTERRUPT | PDI | XTAL | TOSC[1] |
|---|---|---|---|---|---|
| **PDI** | 34 | | PDI_DATA | | |
| $\overline{\text{RESET}}$ | 35 | | PDI_CLOCK | | |
| **PR0** | 36 | SYNC | | XTAL2 | TOSC2 |
| **PR1** | 37 | SYNC | | XTAL1 | TOSC1 |

Note: 1. TOSC pins can optionally be moved to PE2/PE3.

# 33. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA A4U. For complete register description and summary for each peripheral module, refer to the XMEGA AU manual.

**Table 33-1. Peripheral module address map.**

| Base address | Name | Description |
|---|---|---|
| 0x0000 | GPIO | General Purpose IO Registers |
| 0x0010 | VPORT0 | Virtual Port 0 |
| 0x0014 | VPORT1 | Virtual Port 1 |
| 0x0018 | VPORT2 | Virtual Port 2 |
| 0x001C | VPORT3 | Virtual Port 2 |
| 0x0030 | CPU | CPU |
| 0x0040 | CLK | Clock Control |
| 0x0048 | SLEEP | Sleep Controller |
| 0x0050 | OSC | Oscillator Control |
| 0x0060 | DFLLRC32M | DFLL for the 32MHz Internal RC Oscillator |
| 0x0068 | DFLLRC2M | DFLL for the 2MHz RC Oscillator |
| 0x0070 | PR | Power Reduction |
| 0x0078 | RST | Reset Controller |
| 0x0080 | WDT | Watch-Dog Timer |
| 0x0090 | MCU | MCU Control |
| 0x00A0 | PMIC | Programmable MUltilevel Interrupt Controller |
| 0x00B0 | PORTCFG | Port Configuration |
| 0x00C0 | AES | AES Module |
| 0x00D0 | CRC | CRC Module |
| 0x0100 | DMA | DMA Module |
| 0x0180 | EVSYS | Event System |
| 0x01C0 | NVM | Non Volatile Memory (NVM) Controller |
| 0x0200 | ADCA | Analog to Digital Converter on port A |
| 0x0380 | ACA | Analog Comparator pair on port A |
| 0x0400 | RTC | Real Time Counter |
| 0x0480 | TWIC | Two Wire Interface on port C |
| 0x04A0 | TWIE | Two Wire Interface on port E |
| 0x04C0 | USB | Universal Serial Bus Interface |
| 0x0600 | PORTA | Port A |

| Base address | Name | Description |
|---|---|---|
| 0x0620 | PORTB | Port B |
| 0x0640 | PORTC | Port C |
| 0x0660 | PORTD | Port D |
| 0x0680 | PORTE | Port E |
| 0x07E0 | PORTR | Port R |
| 0x0800 | TCC0 | Timer/Counter 0 on port C |
| 0x0840 | TCC1 | Timer/Counter 1 on port C |
| 0x0880 | AWEXC | Advanced Waveform Extension on port C |
| 0x0890 | HIRESC | High Resolution Extension on port C |
| 0x08A0 | USARTC0 | USART 0 on port C |
| 0x08B0 | USARTC1 | USART 1 on port C |
| 0x08C0 | SPIC | Serial Peripheral Interface on port C |
| 0x08F8 | IRCOM | Infrared Communication Module |
| 0x0900 | TCD0 | Timer/Counter 0 on port D |
| 0x0940 | TCD1 | Timer/Counter 1 on port D |
| 0x0990 | HIRESD | High Resolution Extension on port D |
| 0x09A0 | USARTD0 | USART 0 on port D |
| 0x09B0 | USARTD1 | USART 1 on port D |
| 0x09C0 | SPID | Serial Peripheral Interface on port D |
| 0x0A00 | TCE0 | Timer/Counter 0 on port E |
| 0x0A80 | AWEXE | Advanced Waveform Extensionon port E |
| 0x0A90 | HIRESE | High Resolution Extension on port E |
| 0x0AA0 | USARTE0 | USART 0 on port E |

# 34. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| Arithmetic and Logic Instructions | | | | | |
| ADD | Rd, Rr | Add without Carry | Rd ← Rd + Rr | Z,C,N,V,S,H | 1 |
| ADC | Rd, Rr | Add with Carry | Rd ← Rd + Rr + C | Z,C,N,V,S,H | 1 |
| ADIW | Rd, K | Add Immediate to Word | Rd ← Rd + 1:Rd + K | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract without Carry | Rd ← Rd - Rr | Z,C,N,V,S,H | 1 |
| SUBI | Rd, K | Subtract Immediate | Rd ← Rd - K | Z,C,N,V,S,H | 1 |
| SBC | Rd, Rr | Subtract with Carry | Rd ← Rd - Rr - C | Z,C,N,V,S,H | 1 |
| SBCI | Rd, K | Subtract Immediate with Carry | Rd ← Rd - K - C | Z,C,N,V,S,H | 1 |
| SBIW | Rd, K | Subtract Immediate from Word | Rd + 1:Rd ← Rd + 1:Rd - K | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND | Rd ← Rd • Rr | Z,N,V,S | 1 |
| ANDI | Rd, K | Logical AND with Immediate | Rd ← Rd • K | Z,N,V,S | 1 |
| OR | Rd, Rr | Logical OR | Rd ← Rd v Rr | Z,N,V,S | 1 |
| ORI | Rd, K | Logical OR with Immediate | Rd ← Rd v K | Z,N,V,S | 1 |
| EOR | Rd, Rr | Exclusive OR | Rd ← Rd ⊕ Rr | Z,N,V,S | 1 |
| COM | Rd | One's Complement | Rd ← $FF - Rd | Z,C,N,V,S | 1 |
| NEG | Rd | Two's Complement | Rd ← $00 - Rd | Z,C,N,V,S,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V,S | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | Rd ← Rd • ($FFh - K) | Z,N,V,S | 1 |
| INC | Rd | Increment | Rd ← Rd + 1 | Z,N,V,S | 1 |
| DEC | Rd | Decrement | Rd ← Rd - 1 | Z,N,V,S | 1 |
| TST | Rd | Test for Zero or Minus | Rd ← Rd • Rd | Z,N,V,S | 1 |
| CLR | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V,S | 1 |
| SER | Rd | Set Register | Rd ← $FF | None | 1 |
| MUL | Rd,Rr | Multiply Unsigned | R1:R0 ← Rd x Rr (UU) | Z,C | 2 |
| MULS | Rd,Rr | Multiply Signed | R1:R0 ← Rd x Rr (SS) | Z,C | 2 |
| MULSU | Rd,Rr | Multiply Signed with Unsigned | R1:R0 ← Rd x Rr (SU) | Z,C | 2 |
| FMUL | Rd,Rr | Fractional Multiply Unsigned | R1:R0 ← Rd x Rr<<1 (UU) | Z,C | 2 |
| FMULS | Rd,Rr | Fractional Multiply Signed | R1:R0 ← Rd x Rr<<1 (SS) | Z,C | 2 |
| FMULSU | Rd,Rr | Fractional Multiply Signed with Unsigned | R1:R0 ← Rd x Rr<<1 (SU) | Z,C | 2 |
| DES | K | Data Encryption | if (H = 0) then R15:R0 ← Encrypt(R15:R0, K)<br>else if (H = 1) then R15:R0 ← Decrypt(R15:R0, K) | | 1/2 |
| Branch instructions | | | | | |
| RJMP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IJMP | | Indirect Jump to (Z) | PC(15:0) ← Z,<br>PC(21:16) ← 0 | None | 2 |
| EIJMP | | Extended Indirect Jump to (Z) | PC(15:0) ← Z,<br>PC(21:16) ← EIND | None | 2 |
| JMP | k | Jump | PC ← k | None | 3 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| RCALL | k | Relative Call Subroutine | PC ← PC + k + 1 | None | 2 / 3 (1) |
| ICALL | | Indirect Call to (Z) | PC(15:0) ← Z,<br>PC(21:16) ← 0 | None | 2 / 3 (1) |
| EICALL | | Extended Indirect Call to (Z) | PC(15:0) ← Z,<br>PC(21:16) ← EIND | None | 3 (1) |
| CALL | k | call Subroutine | PC ← k | None | 3 / 4 (1) |
| RET | | Subroutine Return | PC ← STACK | None | 4 / 5 (1) |
| RETI | | Interrupt Return | PC ← STACK | I | 4 / 5 (1) |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) PC ← PC + 2 or 3 | None | 1 / 2 / 3 |
| CP | Rd,Rr | Compare | Rd - Rr | Z,C,N,V,S,H | 1 |
| CPC | Rd,Rr | Compare with Carry | Rd - Rr - C | Z,C,N,V,S,H | 1 |
| CPI | Rd,K | Compare with Immediate | Rd - K | Z,C,N,V,S,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b) = 0) PC ← PC + 2 or 3 | None | 1 / 2 / 3 |
| SBRS | Rr, b | Skip if Bit in Register Set | if (Rr(b) = 1) PC ← PC + 2 or 3 | None | 1 / 2 / 3 |
| SBIC | A, b | Skip if Bit in I/O Register Cleared | if (I/O(A,b) = 0) PC ← PC + 2 or 3 | None | 2 / 3 / 4 |
| SBIS | A, b | Skip if Bit in I/O Register Set | If (I/O(A,b) =1) PC ← PC + 2 or 3 | None | 2 / 3 / 4 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BREQ | k | Branch if Equal | if (Z = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BRLO | k | Branch if Lower | if (C = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRMI | k | Branch if Minus | if (N = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRPL | k | Branch if Plus | if (N = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V= 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BRLT | k | Branch if Less Than, Signed | if (N ⊕ V= 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| BRIE | k | Branch if Interrupt Enabled | if (I = 1) then PC ← PC + k + 1 | None | 1 / 2 |
| BRID | k | Branch if Interrupt Disabled | if (I = 0) then PC ← PC + k + 1 | None | 1 / 2 |
| Data transfer instructions | | | | | |
| MOV | Rd, Rr | Copy Register | Rd ← Rr | None | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| MOVW | Rd, Rr | Copy Register Pair | Rd+1:Rd ← Rr+1:Rr | None | 1 |
| LDI | Rd, K | Load Immediate | Rd ← K | None | 1 |
| LDS | Rd, k | Load Direct from data space | Rd ← (k) | None | 2 (1)(2) |
| LD | Rd, X | Load Indirect | Rd ← (X) | None | 1 (1)(2) |
| LD | Rd, X+ | Load Indirect and Post-Increment | Rd ← (X)<br>X ← X + 1 | None | 1 (1)(2) |
| LD | Rd, -X | Load Indirect and Pre-Decrement | X ← X - 1, ← X - 1<br>Rd ← (X) ← (X) | None | 2 (1)(2) |
| LD | Rd, Y | Load Indirect | Rd ← (Y) ← (Y) | None | 1 (1)(2) |
| LD | Rd, Y+ | Load Indirect and Post-Increment | Rd ← (Y)<br>Y ← Y + 1 | None | 1 (1)(2) |
| LD | Rd, -Y | Load Indirect and Pre-Decrement | Y ← Y - 1<br>Rd ← (Y) | None | 2 (1)(2) |
| LDD | Rd, Y+q | Load Indirect with Displacement | Rd ← (Y + q) | None | 2 (1)(2) |
| LD | Rd, Z | Load Indirect | Rd ← (Z) | None | 1 (1)(2) |
| LD | Rd, Z+ | Load Indirect and Post-Increment | Rd ← (Z),<br>Z ← Z+1 | None | 1 (1)(2) |
| LD | Rd, -Z | Load Indirect and Pre-Decrement | Z ← Z - 1,<br>Rd ← (Z) | None | 2 (1)(2) |
| LDD | Rd, Z+q | Load Indirect with Displacement | Rd ← (Z + q) | None | 2 (1)(2) |
| STS | k, Rr | Store Direct to Data Space | (k) ← Rd | None | 2 (1) |
| ST | X, Rr | Store Indirect | (X) ← Rr | None | 1 (1) |
| ST | X+, Rr | Store Indirect and Post-Increment | (X) ← Rr,<br>X ← X + 1 | None | 1 (1) |
| ST | -X, Rr | Store Indirect and Pre-Decrement | X ← X - 1,<br>(X) ← Rr | None | 2 (1) |
| ST | Y, Rr | Store Indirect | (Y) ← Rr | None | 1 (1) |
| ST | Y+, Rr | Store Indirect and Post-Increment | (Y) ← Rr,<br>Y ← Y + 1 | None | 1 (1) |
| ST | -Y, Rr | Store Indirect and Pre-Decrement | Y ← Y - 1,<br>(Y) ← Rr | None | 2 (1) |
| STD | Y+q, Rr | Store Indirect with Displacement | (Y + q) ← Rr | None | 2 (1) |
| ST | Z, Rr | Store Indirect | (Z) ← Rr | None | 1 (1) |
| ST | Z+, Rr | Store Indirect and Post-Increment | (Z) ← Rr<br>Z ← Z + 1 | None | 1 (1) |
| ST | -Z, Rr | Store Indirect and Pre-Decrement | Z ← Z - 1 | None | 2 (1) |
| STD | Z+q,Rr | Store Indirect with Displacement | (Z + q) ← Rr | None | 2 (1) |
| LPM | | Load Program Memory | R0 ← (Z) | None | 3 |
| LPM | Rd, Z | Load Program Memory | Rd ← (Z) | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Increment | Rd ← (Z),<br>Z ← Z + 1 | None | 3 |
| ELPM | | Extended Load Program Memory | R0 ← (RAMPZ:Z) | None | 3 |
| ELPM | Rd, Z | Extended Load Program Memory | Rd ← (RAMPZ:Z) | None | 3 |

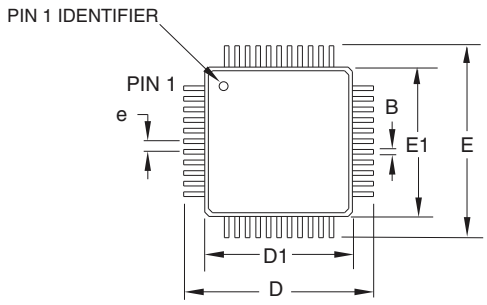
| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| ELPM | Rd, Z+ | Extended Load Program Memory and Post-Increment | Rd ← (RAMPZ:Z),<br>Z ← Z + 1 | None | 3 |
| SPM | | Store Program Memory | (RAMPZ:Z) ← R1:R0 | None | - |
| SPM | Z+ | Store Program Memory and Post-Increment by 2 | (RAMPZ:Z) ← R1:R0,<br>Z ← Z + 2 | None | - |
| IN | Rd, A | In From I/O Location | Rd ← I/O(A) | None | 1 |
| OUT | A, Rr | Out To I/O Location | I/O(A) ← Rr | None | 1 |
| PUSH | Rr | Push Register on Stack | STACK ← Rr | None | 1 (1) |
| POP | Rd | Pop Register from Stack | Rd ← STACK | None | 2 (1) |
| XCH | Z, Rd | Exchange RAM location | Temp ← Rd,<br>Rd ← (Z),<br>(Z) ← Temp | None | 2 |
| LAS | Z, Rd | Load and Set RAM location | Temp ← Rd,<br>Rd ← (Z),<br>(Z) ← Temp v (Z) | None | 2 |
| LAC | Z, Rd | Load and Clear RAM location | Temp ← Rd,<br>Rd ← (Z),<br>(Z) ← ($FFh – Rd) ● (Z) | None | 2 |
| LAT | Z, Rd | Load and Toggle RAM location | Temp ← Rd,<br>Rd ← (Z),<br>(Z) ← Temp ⊕ (Z) | None | 2 |
| Bit and bit-test instructions | | | | | |
| LSL | Rd | Logical Shift Left | Rd(n+1) ← Rd(n),<br>Rd(0) ← 0,<br>C ← Rd(7) | Z,C,N,V,H | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) ← Rd(n+1),<br>Rd(7) ← 0,<br>C ← Rd(0) | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0) ← C,<br>Rd(n+1) ← Rd(n),<br>C ← Rd(7) | Z,C,N,V,H | 1 |
| ROR | Rd | Rotate Right Through Carry | Rd(7) ← C,<br>Rd(n) ← Rd(n+1),<br>C ← Rd(0) | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | Rd(n) ← Rd(n+1), n=0..6 | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | Rd(3..0) ↔ Rd(7..4) | None | 1 |
| BSET | s | Flag Set | SREG(s) ← 1 | SREG(s) | 1 |
| BCLR | s | Flag Clear | SREG(s) ← 0 | SREG(s) | 1 |
| SBI | A, b | Set Bit in I/O Register | I/O(A, b) ← 1 | None | 1 |
| CBI | A, b | Clear Bit in I/O Register | I/O(A, b) ← 0 | None | 1 |
| BST | Rr, b | Bit Store from Register to T | T ← Rr(b) | T | 1 |
| BLD | Rd, b | Bit load from T to Register | Rd(b) ← T | None | 1 |
| SEC | | Set Carry | C ← 1 | C | 1 |
| CLC | | Clear Carry | C ← 0 | C | 1 |
| SEN | | Set Negative Flag | N ← 1 | N | 1 |
| CLN | | Clear Negative Flag | N ← 0 | N | 1 |
| SEZ | | Set Zero Flag | Z ← 1 | Z | 1 |

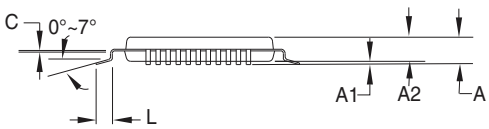
| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| CLZ | | Clear Zero Flag | Z ← 0 | Z | 1 |
| SEI | | Global Interrupt Enable | I ← 1 | I | 1 |
| CLI | | Global Interrupt Disable | I ← 0 | I | 1 |
| SES | | Set Signed Test Flag | S ← 1 | S | 1 |
| CLS | | Clear Signed Test Flag | S ← 0 | S | 1 |
| SEV | | Set Two's Complement Overflow | V ← 1 | V | 1 |
| CLV | | Clear Two's Complement Overflow | V ← 0 | V | 1 |
| SET | | Set T in SREG | T ← 1 | T | 1 |
| CLT | | Clear T in SREG | T ← 0 | T | 1 |
| SEH | | Set Half Carry Flag in SREG | H ← 1 | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | H ← 0 | H | 1 |
| MCU control instructions | | | | | |
| BREAK | | Break | (See specific descr. for BREAK) | None | 1 |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR) | None | 1 |

Notes:
1. Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing Internal SRAM.

# 35. Packaging information

## 35.1 44A




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 11.75 | 12.00 | 12.25 | |
| D1 | 9.90 | 10.00 | 10.10 | Note 2 |
| E | 11.75 | 12.00 | 12.25 | |
| E1 | 9.90 | 10.00 | 10.10 | Note 2 |
| B | 0.30 | 0.37 | 0.45 | |
| C | 0.09 | (0.17) | 0.20 | |
| L | 0.45 | 0.60 | 0.75 | |
| e | 0.80 TYP | | | |

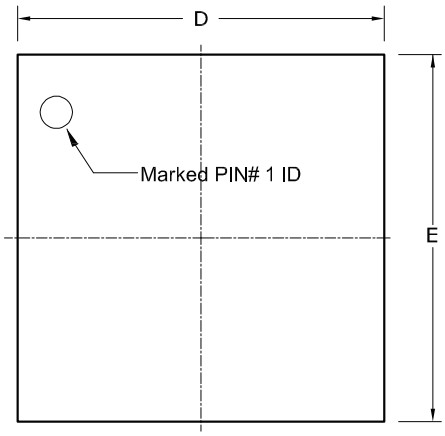
Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

06/02/2014

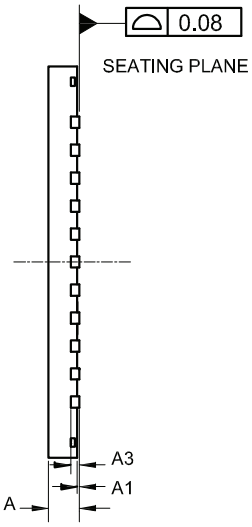
| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| Atmel Package Drawing Contact: packagedrawings@atmel.com | **44A,** 44-lead, 10 x 10mm body size, 1.0mm body thickness, 0.8 mm lead pitch, thin profile plastic quad flat package (TQFP) | 44A | C |

## 35.2 PW

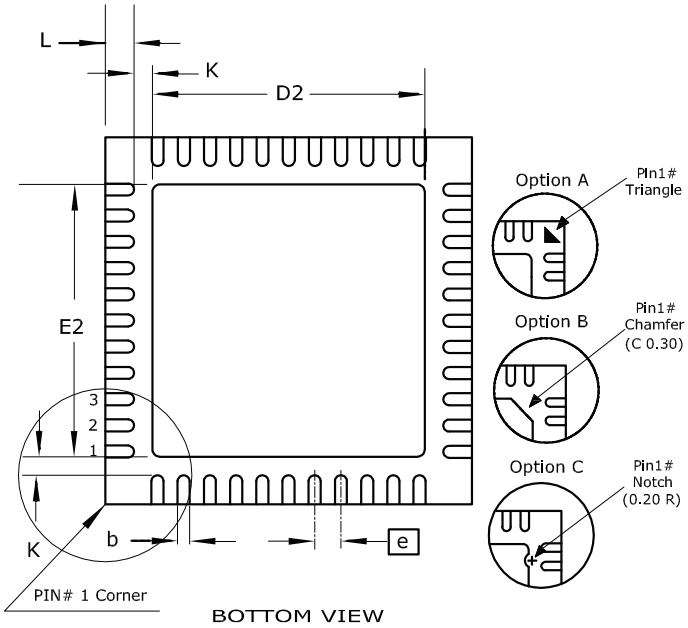
DRAWINGS NOT SCALED




TOP VIEW




SIDE VIEW




BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

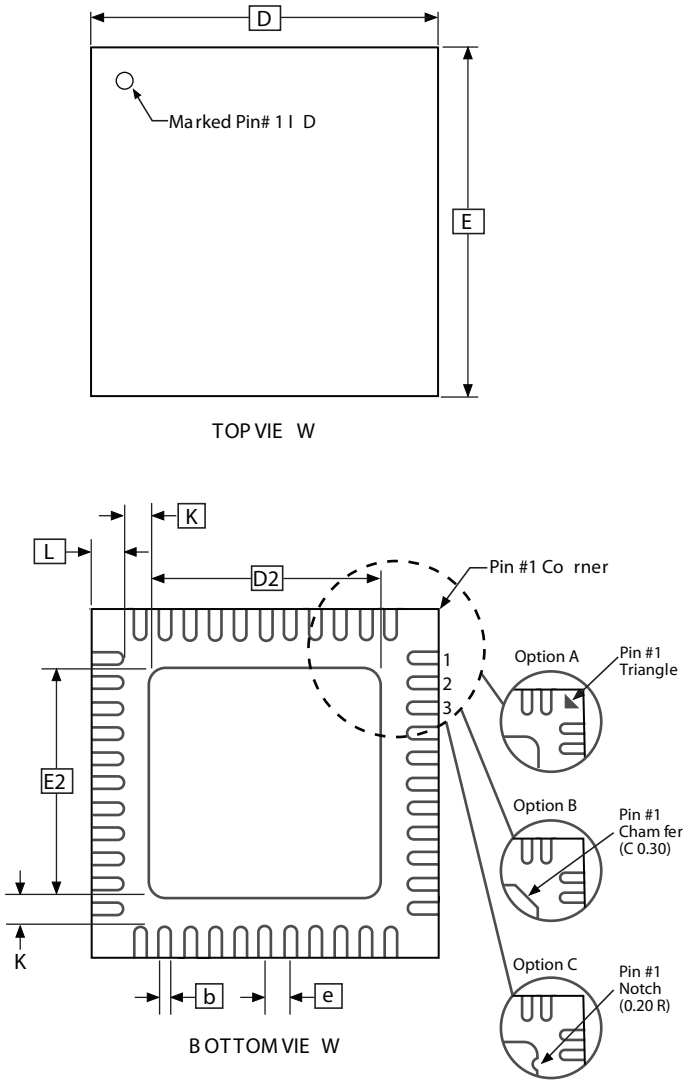
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | ----- | 1.00 | |
| A1 | ---- | 0.02 | 0.05 | |
| A3 | 0.20 REF | | | |
| D/E | 6.90 | 7.00 | 7.10 | |
| D2/E2 | 5.00 | 5.20 | 5.40 | |
| L | 0.45 | 0.55 | 0.65 | |
| K | ---- | 0.35 | ---- | |
| b | 0.18 | 0.23 | 0.30 | 2 |
| e | 0.50 BSC | | | |
| n | 44 | | | |

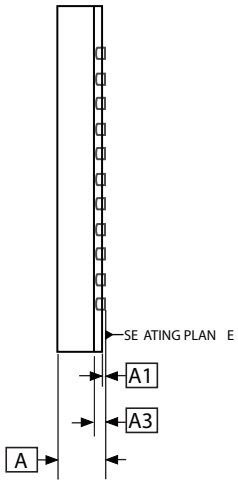
Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-1 for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

02/17/2012

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| Atmel **Package Drawing Contact: packagedrawings@atmel.com** | PW, 44 Lds - 0.50mm Pitch, 7x7x1mm Body size<br>Very Thin Quad Flat Package (Punched) (VQFN) Sawn | ZCP | PW | H |

## 35.3 44M1




Note: JEDEC Standard MO-220, Fig . 1 (S AW Singulation) VKKD-3 .

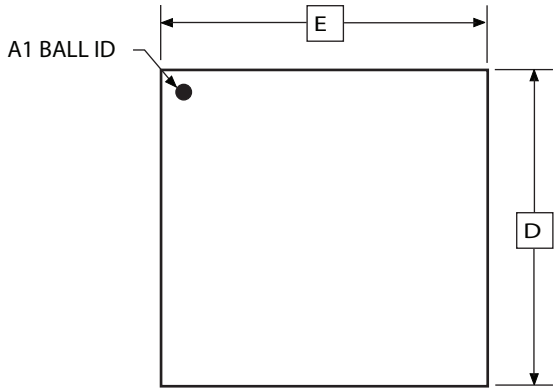
COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | 0.90 | 1.00 | |
| A1 | – | 0.02 | 0.05 | |
| A3 | | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | 6.90 | 7.00 | 7.10 | |
| D2 | 5.00 | 5.20 | 5.40 | |
| E | 6.90 | 7.00 | 7.10 | |
| E2 | 5.00 | 5.20 | 5.40 | |
| e | | 0.50 BSC | | |
| L | 0.59 | 0.64 | 0.69 | |
| K | 0.20 | 0.26 | 0.41 | |

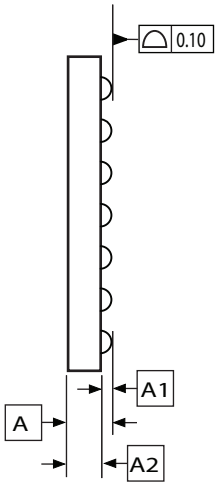
02/13/2014

| | | | | |
|---|---|---|---|---|
| Atmel Package Drawing Contact: packagedrawings@atmel.com | TITLE<br>44M1, 44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN) | GPC<br>ZWS | DRAWING NO.<br>44M1 | REV.<br>H |

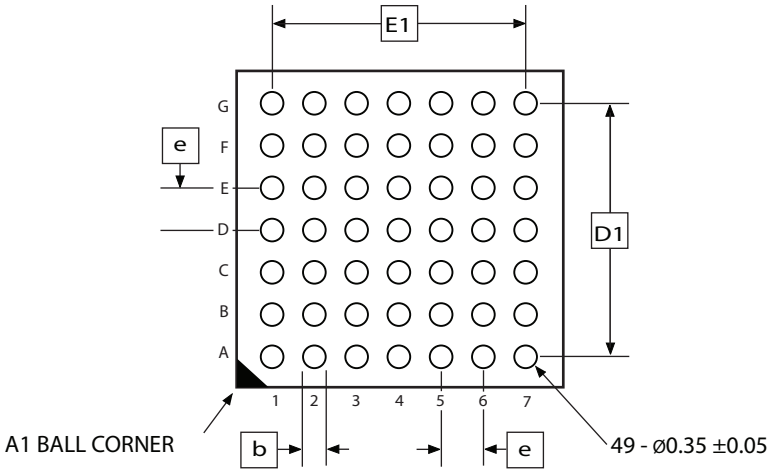
## 35.4 49C2




TOP VIEW




SIDE VIEW




BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.00 | |
| A1 | 0.20 | – | – | |
| A2 | 0.65 | – | – | |
| D | 4.90 | 5.00 | 5.10 | |
| D1 | | 3.90 BSC | | |
| E4.90 | 5.00 | 5.10 | | |
| E1 | | 3.90 BSC | | |
| b | 0.30 | 0.35 | 0.40 | |
| e | | 0.65 BSC | | |

3/14/08

| | | | | |
|---|---|---|---|---|
| Atmel Package Drawing Contact: packagedrawings@atmel.com | TITLE<br>49C2, 49-ball (7 x 7 array), 0.65mm pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA) | GPC<br>CBD | DRAWING NO.<br>49C2 | REV.<br>A |

# 36. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

## 36.1 ATxmega16A4U

### 36.1.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-1 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 36-1. Absolute maximum ratings.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | -0.3 | | 4 | V |
| $I_{VCC}$ | Current into a $V_{CC}$ pin | | | | 200 | mA |
| $I_{GND}$ | Current out of a Gnd pin | | | | 200 | mA |
| $V_{PIN}$ | Pin voltage with respect to Gnd and $V_{CC}$ | | -0.5 | | $V_{CC}$+0.5 | V |
| $I_{PIN}$ | I/O pin sink/source current | | -25 | | 25 | mA |
| $T_A$ | Storage temperature | | -65 | | 150 | °C |
| $T_j$ | Junction temperature | | | | 150 | °C |

### 36.1.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

**Table 36-2. General operating conditions.**

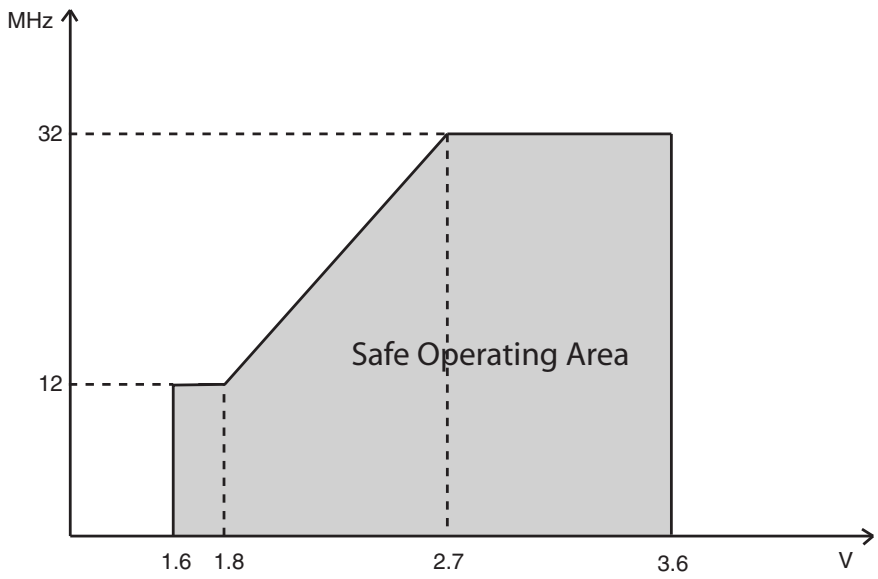
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | 1.60 | | 3.6 | V |
| $AV_{CC}$ | Analog supply voltage | | 1.60 | | 3.6 | V |
| $T_A$ | Temperature range | | -40 | | 85 | °C |
| $T_j$ | Junction temperature | | -40 | | 105 | °C |

**Table 36-3. Operating voltage and frequency.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{CPU}$ | CPU clock frequency | $V_{CC}$ = 1.6V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 1.8V | 0 | | 12 | |
| | | $V_{CC}$ = 2.7V | 0 | | 32 | |
| | | $V_{CC}$ = 3.6V | 0 | | 32 | |

The maximum CPU clock frequency depends on $V_{CC}$. As shown in Figure 36-1 the Frequency vs. $V_{CC}$ curve is linear between 1.8V < $V_{CC}$ < 2.7V.

**Figure 36-1. Maximum Frequency vs. $V_{CC}$.**



### 36.1.3 Current consumption

**Table 36-4. Current consumption for Active mode and sleep modes.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Active power consumption [1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 40 | | µA |
| | | | $V_{CC}$ = 3.0V | | 80 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 230 | | |
| | | | $V_{CC}$ = 3.0V | | 480 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 430 | 600 | |
| | | | $V_{CC}$ = 3.0V | | 0.9 | 1.4 | mA |
| | | 32MHz, Ext. Clk | | | 9.6 | 12 | |
| | Idle power consumption [1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 2.4 | | µA |
| | | | $V_{CC}$ = 3.0V | | 3.9 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 62 | | |
| | | | $V_{CC}$ = 3.0V | | 118 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 125 | 225 | |
| | | | $V_{CC}$ = 3.0V | | 240 | 350 | |
| | | 32MHz, Ext. Clk | | | 3.8 | 5.5 | mA |
| | Power-down power consumption | T = 25°C | $V_{CC}$ = 3.0V | | 0.1 | 1.0 | µA |
| | | T = 85°C | | | 1.2 | 4.5 | |
| | | T = 105°C | | | 3.5 | 6.0 | |
| | | WDT and Sampled BOD enabled, T = 25°C | $V_{CC}$ = 3.0V | | 1.3 | 3.0 | |
| | | WDT and Sampled BOD enabled, T = 85°C | | | 2.4 | 6.0 | |
| | | WDT and Sampled BOD enabled, T = 105°C | | | 4.5 | 8.0 | |
| | Power-save power consumption [2] | RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C | $V_{CC}$ = 1.8V | | 1.2 | | µA |
| | | | $V_{CC}$ = 3.0V | | 1.3 | | |
| | | RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.6 | 2.0 | |
| | | | $V_{CC}$ = 3.0V | | 0.7 | 2.0 | |
| | | RTC from low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.8 | 3.0 | |
| | | | $V_{CC}$ = 3.0V | | 1.0 | 3.0 | |
| | Reset power consumption | Current through $\overline{\text{RESET}}$ pin substracted | $V_{CC}$ = 3.0V | | 320 | | µA |

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

**Table 36-5. Current consumption for modules and peripherals.**

| Symbol | Parameter | Condition [1] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | ULP oscillator | | | | 1.0 | | µA |
| | 32.768kHz int. oscillator | | | | 27 | | µA |
| | 2MHz int. oscillator | | | | 85 | | µA |
| | | DFLL enabled with 32.768kHz int. osc. as reference | | | 115 | | |
| | 32MHz int. oscillator | | | | 270 | | µA |
| | | DFLL enabled with 32.768kHz int. osc. as reference | | | 460 | | |
| | PLL | 20x multiplication factor,<br>32MHz int. osc. DIV4 as reference | | | 220 | | µA |
| | Watchdog timer | | | | 1.0 | | µA |
| | BOD | Continuous mode | | | 138 | | µA |
| | | Sampled mode, includes ULP oscillator | | | 1.2 | | |
| | Internal 1.0V reference | | | | 100 | | µA |
| | Temperature sensor | | | | 95 | | µA |
| | ADC | 250ksps<br>$V_{REF}$ = Ext ref | | | 3.0 | | mA |
| | | | CURRLIMIT = LOW | | 2.6 | | |
| | | | CURRLIMIT = MEDIUM | | 2.1 | | |
| | | | CURRLIMIT = HIGH | | 1.6 | | |
| | DAC | 250ksps<br>$V_{REF}$ = Ext ref<br>No load | Normal mode | | 1.9 | | mA |
| | | | Low Power mode | | 1.1 | | |
| | AC | High speed mode | | | 330 | | µA |
| | | Low power mode | | | 130 | | |
| | DMA | 615kbps between I/O registers and SRAM | | | 108 | | µA |
| | Timer/counter | | | | 16 | | µA |
| | USART | Rx and Tx enabled, 9600 BAUD | | | 2.5 | | µA |
| | Flash memory and EEPROM programming | | | | 4.0 | 8.0 | mA |

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at $V_{CC}$ = 3.0V, $Clk_{SYS}$ = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

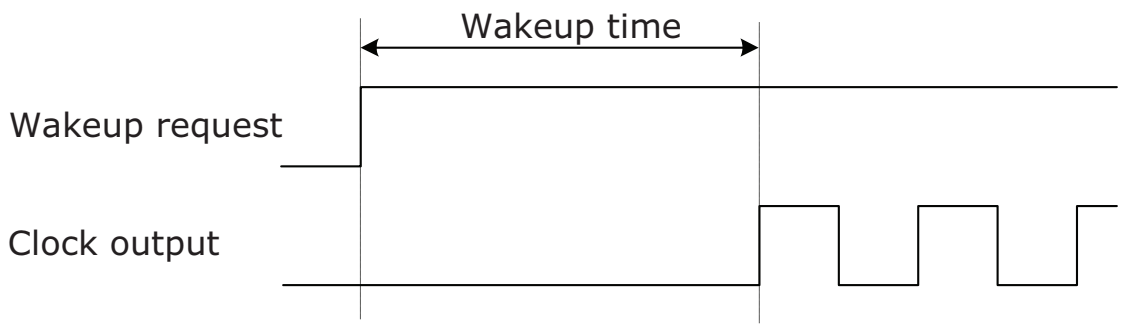
### 36.1.4 Wake-up time from sleep modes

**Table 36-6. Device wake-up time from sleep modes with various system clock sources.**

| Symbol | Parameter | Condition | Min. | Typ. [1] | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{wakeup}$ | Wake-up time from idle, standby, and extended standby mode | External 2MHz clock | | 2.0 | | µs |
| | | 32.768kHz internal oscillator | | 120 | | |
| | | 2MHz internal oscillator | | 2.0 | | |
| | | 32MHz internal oscillator | | 0.2 | | |
| | Wake-up time from power-save and power-down mode | External 2MHz clock | | 4.5 | | |
| | | 32.768kHz internal oscillator | | 320 | | |
| | | 2MHz internal oscillator | | 9.0 | | |
| | | 32MHz internal oscillator | | 5.0 | | |

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

**Figure 36-2. Wake-up time definition.**



### 36.1.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

**Table 36-7. I/O pin characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ (1)/ $I_{OL}$ (2) | I/O pin source/sink current | | | -20 | | 20 | mA |
| $V_{IH}$ | High level input voltage | $V_{CC}$ = 2.7 - 3.6V | | 2.0 | | $V_{CC}$+0.3 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | 0.7*$V_{CC}$ | | $V_{CC}$+0.3 | |
| | | $V_{CC}$ = 1.6 - 2.0V | | 0.8*$V_{CC}$ | | $V_{CC}$+0.3 | |
| $V_{IL}$ | Low level input voltage | $V_{CC}$ = 2.7- 3.6V | | -0.3 | | 0.8 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | -0.3 | | 0.3*$V_{CC}$ | |
| | | $V_{CC}$ = 1.6 - 2.0V | | -0.3 | | 0.2*$V_{CC}$ | |
| $V_{OH}$ | High level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OH}$ = -2mA | 2.4 | 0.94*$V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OH}$ = -1mA | 2.0 | 0.96*$V_{CC}$ | | |
| | | | $I_{OH}$ = -2mA | 1.7 | 0.92*$V_{CC}$ | | |
| | | $V_{CC}$ = 3.3V | $I_{OH}$ = -8mA | 2.6 | 2.9 | | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = -6mA | 2.1 | 2.6 | | |
| | | $V_{CC}$ = 1.8V | $I_{OH}$ = -2mA | 1.4 | 1.6 | | |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OL}$ = 2mA | | 0.05*$V_{CC}$ | 0.4 | V |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OL}$ = 1mA | | 0.03*$V_{CC}$ | 0.4 | |
| | | | $I_{OL}$ = 2mA | | 0.06*$V_{CC}$ | 0.7 | |
| | | $V_{CC}$ = 3.3V | $I_{OL}$ = 15mA | | 0.4 | 0.76 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 10mA | | 0.3 | 0.64 | |
| | | $V_{CC}$ = 1.8V | $I_{OL}$ = 5mA | | 0.2 | 0.46 | |
| $I_{IN}$ | Input leakage current | T = 25°C | | | <0.01 | 0.1 | µA |
| $R_P$ | Pull/buss keeper resistor | | | | 24 | | kΩ |
| $t_r$ | Rise time | No load | | | 4.0 | | ns |
| | | | slew rate limitation | | 7.0 | | |

Notes:
1. The sum of all $I_{OH}$ for PORTA and PORTB must not exceed 100mA.
   The sum of all $I_{OH}$ for PORTC must not exceed 200mA.
   The sum of all $I_{OH}$ for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
   The sum of all $I_{OH}$ for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.
2. The sum of all $I_{OL}$ for PORTA and PORTB must not exceed 100mA.
   The sum of all $I_{OL}$ for PORTC must not exceed 200mA.
   The sum of all $I_{OL}$ for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
   The sum of all $I_{OL}$ for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.

### 36.1.6 ADC characteristics

**Table 36-8. Power supply, reference and input range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $V_{REF}$ | Reference voltage | | 1.0 | | $AV_{CC}$- 0.6 | V |
| $R_{in}$ | Input resistance | Switched | | 4.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched | | 4.4 | | pF |
| $R_{AREF}$ | Reference input resistance | (leakage only) | | >10 | | MΩ |
| $C_{AREF}$ | Reference input capacitance | Static load | | 7.0 | | pF |
| $V_{IN}$ | Input range | | -0.1 | | $AV_{CC}$+0.1 | V |
| | Conversion range | Differential mode, Vinp - Vinn | $-V_{REF}$ | | $V_{REF}$ | V |
| | Conversion range | Single ended unsigned mode, Vinp | -ΔV | | $V_{REF}$-ΔV | V |
| ΔV | Fixed offset voltage | | | 190 | | LSB |

**Table 36-9. Clock and timing.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{ADC}$ | ADC Clock frequency | Maximum is 1/4 of peripheral clock frequency | 100 | | 2000 | kHz |
| | | Measuring internal signals | 100 | | 125 | |
| $f_{ADC}$ | Sample rate | Current limitation (CURRLIMIT) off | 100 | | 2000 | ksps |
| | | CURRLIMIT = LOW | 100 | | 1500 | |
| | | CURRLIMIT = MEDIUM | 100 | | 1000 | |
| | | CURRLIMIT = HIGH | 100 | | 500 | |
| | Sampling time | 1/2 $Clk_{ADC}$ cycle | 0.25 | | 5 | µs |
| | Conversion time (latency) | (RES+2)/2+(GAIN !=0)<br>RES (Resolution) = 8 or 12 | 5 | | 8 | $Clk_{ADC}$ cycles |
| | Start-up time | ADC clock cycles | | 12 | 24 | $Clk_{ADC}$ cycles |
| | ADC settling time | After changing reference or input mode | | 7 | 7 | $Clk_{ADC}$ cycles |
| | | After ADC flush | | 1 | 1 | |

**Table 36-10. Accuracy characteristics.**

| Symbol | Parameter | Condition [2] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Resolution | Programmable to 8 or 12 bit | | 8 | 12 | 12 | Bits |
| INL [1] | Integral non-linearity | 500ksps | $V_{CC}$-1.0V < $V_{REF}$< $V_{CC}$-0.6V | | ±1.2 | ±2.0 | lsb |
| | | | All $V_{REF}$ | | ±1.5 | ±3.0 | |
| | | 2000ksps | $V_{CC}$-1.0V < $V_{REF}$< $V_{CC}$-0.6V | | ±1.0 | ±2.0 | |
| | | | All $V_{REF}$ | | ±1.5 | ±3.0 | |
| DNL [1] | Differential non-linearity | guaranteed monotonic | | | <±0.8 | <±1.0 | lsb |
| | Offset error | | | | -1.0 | | mV |
| | | Temperature drift | | | <0.01 | | mV/K |
| | | Operating voltage drift | | | <0.6 | | mV/V |
| | Gain error | Differential mode | External reference | | -1.0 | | mV |
| | | | $AV_{CC}$/1.6 | | 10 | | |
| | | | $AV_{CC}$/2.0 | | 8.0 | | |
| | | | Bandgap | | ±5.0 | | |
| | | Temperature drift | | | <0.02 | | mV/K |
| | | Operating voltage drift | | | <0.5 | | mV/V |
| | Noise | Differential mode, shorted input 2msps, $V_{CC}$ = 3.6V, $Clk_{PER}$ = 16MHz | | | 0.4 | | mV rms |

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external $V_{REF}$ is used.

**Table 36-11. Gain stage characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $R_{in}$ | Input resistance | Switched in normal mode | | | 4.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched in normal mode | | | 4.4 | | pF |
| | Signal range | Gain stage output | | 0 | | $V_{CC}$- 0.6 | V |
| | Propagation delay | ADC conversion rate | | | 1.0 | | $Clk_{ADC}$ cycles |
| | Sample rate | Same as ADC | | 100 | | 1000 | kHz |
| INL [1] | Integral non-linearity | 500ksps | All gain settings | | ±1.5 | ±4 | lsb |
| | Gain error | 1x gain, normal mode | | | -0.8 | | % |
| | | 8x gain, normal mode | | | -2.5 | | |
| | | 64x gain, normal mode | | | -3.5 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Offset error, input referred | 1x gain, normal mode | | | -2 | | mV |
| | | 8x gain, normal mode | | | -5 | | |
| | | 64x gain, normal mode | | | -4 | | |
| | Noise | 1x gain, normal mode | $V_{CC}$ = 3.6V Ext. $V_{REF}$ | | 0.5 | | mV rms |
| | | 8x gain, normal mode | | | 1.5 | | |
| | | 64x gain, normal mode | | | 11 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

### 36.1.7 DAC Characteristics

**Table 36-12. Power supply, reference and output range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $AV_{REF}$ | External reference voltage | | 1.0 | | $V_{CC}$- 0.6 | V |
| $R_{channel}$ | DC output impedance | | | | 50 | Ω |
| | Linear output voltage range | | 0.15 | | $AV_{CC}$-0.15 | V |
| $R_{AREF}$ | Reference input resistance | | | >10 | | MΩ |
| CAREF | Reference input capacitance | Static load | | 7 | | pF |
| | Minimum resistance load | | 1.0 | | | kΩ |
| | Maximum capacitance load | | | | 100 | pF |
| | | 1000Ω serial resistance | | | 1.0 | nF |
| | Output sink/source | Operating within accuracy specification | | | $AV_{CC}$/1000 | mA |
| | | Safe operation | | | 10 | |

**Table 36-13. Clock and timing.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{DAC}$ | Conversion rate | $C_{load}$=100pF, maximum step size | Normal mode | 0 | | 1000 | ksps |
| | | | Low power mode | | | 500 | |

**Table 36-14. Accuracy characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Input resolution | | | | | 12 | Bits |
| INL [(1)] | Integral non-linearity | $V_{REF}$= Ext 1.0V | $V_{CC}$ = 1.6V | | ±2.0 | ±3 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±2.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±2.0 | ±4 | |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±4 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±5.0 | | |
| | | | $V_{CC}$ = 3.6V | | ±5.0 | | |
| DNL [(1)] | Differential non-linearity | $V_{REF}$=Ext 1.0V | $V_{CC}$ = 1.6V | | ±1.5 | 3.0 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±1.0 | 3.5 | |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±4.5 | | |
| | | | $V_{CC}$ = 3.6V | | ±4.5 | | |
| | Gain error | After calibration | | | <4.0 | | lsb |
| | Gain calibration step size | | | | 4.0 | | lsb |
| | Gain calibration drift | $V_{REF}$= Ext 1.0V | | | <0.2 | | mV/K |
| | Offset error | After calibration | | | <1.0 | | lsb |
| | Offset calibration step size | | | | 1.0 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

### 36.1.8 Analog Comparator Characteristics

**Table 36-15. Analog Comparator characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{off}$ | Input offset voltage | | | | <±10 | | mV |
| $I_{lk}$ | Input leakage current | | | | <1.0 | | nA |
| | Input voltage range | | | -0.1 | | $AV_{CC}$ | V |
| | AC startup time | | | | 100 | | µs |
| $V_{hys1}$ | Hysteresis, none | | | | 0 | | mV |
| $V_{hys2}$ | Hysteresis, small | mode = High Speed (HS) | | | 13 | | mV |
| | | mode = Low Power (LP) | | | 30 | | |
| $V_{hys3}$ | Hysteresis, large | mode = HS | | | 30 | | mV |
| | | mode = LP | | | 60 | | |
| $t_{delay}$ | Propagation delay | $V_{CC}$ = 3.0V, T= 85°C | mode = HS | | 30 | 90 | ns |
| | | mode = HS | | | 30 | | |
| | | $V_{CC}$ = 3.0V, T= 85°C | mode = LP | | 130 | 500 | |
| | | mode = LP | | | 130 | | |
| | 64-level voltage scaler | Integral non-linearity (INL) | | | 0.3 | 0.5 | lsb |

### 36.1.9 Bandgap and Internal 1.0V Reference Characteristics

**Table 36-16. Bandgap and Internal 1.0V reference characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Startup time | As reference for ADC or DAC | 1 $Clk_{PER}$ + 2.5µs | | | µs |
| | | As input voltage to ADC and AC | | 1.5 | | |
| | Bandgap voltage | | | 1.1 | | V |
| INT1V | Internal 1.00V reference | T= 85°C, after calibration | 0.99 | 1.0 | 1.01 | V |
| | Variation over voltage and temperature | Relative to T= 85°C, $V_{CC}$ = 3.0V | | ±1.5 | | % |

### 36.1.10 Brownout Detection Characteristics

**Table 36-17. Brownout detection characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{BOT}$ | BOD level 0 falling $V_{CC}$ | | 1.60 | 1.62 | 1.72 | V |
| | BOD level 1 falling $V_{CC}$ | | | 1.8 | | |
| | BOD level 2 falling $V_{CC}$ | | | 2.0 | | |
| | BOD level 3 falling $V_{CC}$ | | | 2.2 | | |
| | BOD level 4 falling $V_{CC}$ | | | 2.4 | | |
| | BOD level 5 falling $V_{CC}$ | | | 2.6 | | |
| | BOD level 6 falling $V_{CC}$ | | | 2.8 | | |
| | BOD level 7 falling $V_{CC}$ | | | 3.0 | | |
| $t_{BOD}$ | Detection time | Continuous mode | | 0.4 | | µs |
| | | Sampled mode | | 1000 | | |
| $V_{HYST}$ | Hysteresis | | | 1.2 | | % |

### 36.1.11 External Reset Characteristics

**Table 36-18. External reset characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{EXT}$ | Minimum reset pulse width | | | 95 | 1000 | ns |
| $V_{RST}$ | Reset threshold voltage ($V_{IH}$) | $V_{CC}$ = 2.7 - 3.6V | | 0.60×$V_{CC}$ | | V |
| | | $V_{CC}$ = 1.6 - 2.7V | | 0.60×$V_{CC}$ | | |
| | Reset threshold voltage ($V_{IL}$) | $V_{CC}$ = 2.7 - 3.6V | | 0.50×$V_{CC}$ | | |
| | | $V_{CC}$ = 1.6 - 2.7V | | 0.40×$V_{CC}$ | | |
| $R_{RST}$ | Reset pin Pull-up Resistor | | | 25 | | kΩ |

### 36.1.12 Power-on Reset Characteristics

**Table 36-19. Power-on reset characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{POT-}$ [(1)] | POR threshold voltage falling $V_{CC}$ | $V_{CC}$ falls faster than 1V/ms | 0.4 | 1.0 | | V |
| | | $V_{CC}$ falls at 1V/ms or slower | 0.8 | 1.0 | | |
| $V_{POT+}$ | POR threshold voltage rising $V_{CC}$ | | | 1.3 | 1.59 | V |

Note: 1. $V_{POT-}$ values are only valid when BOD is disabled. When BOD is enabled $V_{POT-}$ = $V_{POT+}$.

### 36.1.13 Flash and EEPROM Memory Characteristics

**Table 36-20. Endurance and data retention.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Flash | Write/Erase cycles | 25°C | 10K | | | Cycle |
| | | | 85°C | 10K | | | |
| | | | 105°C | 2K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 85°C | 25 | | | |
| | | | 105°C | 10 | | | |
| | EEPROM | Write/Erase cycles | 25°C | 100K | | | Cycle |
| | | | 85°C | 100K | | | |
| | | | 105°C | 30K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 85°C | 25 | | | |
| | | | 105°C | 10 | | | |

**Table 36-21. Programming time.**

| Symbol | Parameter | Condition | | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Chip Erase | 16KB Flash, EEPROM[2] and SRAM Erase | | | 45 | | ms |
| | Application Erase | Section erase | | | 6 | | ms |
| | Flash | Page erase | | | 4 | | ms |
| | | Page write | | | 4 | | |
| | | Atomic page erase and write | | | 8 | | |
| | EEPROM | Page erase | | | 4 | | ms |
| | | Page write | | | 4 | | |
| | | Atomic page erase and write | | | 8 | | |

Notes:
1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

### 36.1.14 Clock and Oscillator Characteristics

#### 36.1.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

**Table 36-22. 32.768kHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency | | | 32.768 | | kHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$ = 3.0V | -0.5 | | 0.5 | % |
| | User calibration accuracy | | -0.5 | | 0.5 | % |

#### 36.1.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

**Table 36-23. 2MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 1.8 | | 2.2 | MHz |
| | Factory calibrated frequency | | | 2.0 | | MHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | % |
| | DFLL calibration stepsize | | | 0.21 | | % |

#### 36.1.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

**Table 36-24. 32MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 30 | | 55 | MHz |
| | Factory calibrated frequency | | | 32 | | MHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | % |
| | DFLL calibration step size | | | 0.22 | | % |

#### 36.1.14.4 32kHz Internal ULP Oscillator characteristics

**Table 36-25. 32kHz internal ULP oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Output frequency | | | 32 | | kHz |
| | Accuracy | | -30 | | 30 | % |

### 36.1.14.5 Internal Phase Locked Loop (PLL) characteristics

**Table 36-26. Internal PLL characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input frequency | Output frequency must be within $f_{OUT}$ | 0.4 | | 64 | MHz |
| $f_{OUT}$ | Output frequency [1] | $V_{CC}$= 1.6 - 1.8V | 20 | | 48 | MHz |
| | | $V_{CC}$= 2.7 - 3.6V | 20 | | 128 | |
| | Start-up time | | | 25 | | µs |
| | Re-lock time | | | 25 | | µs |

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

### 36.1.14.6 External clock characteristics

**Figure 36-3. External clock drive waveform**

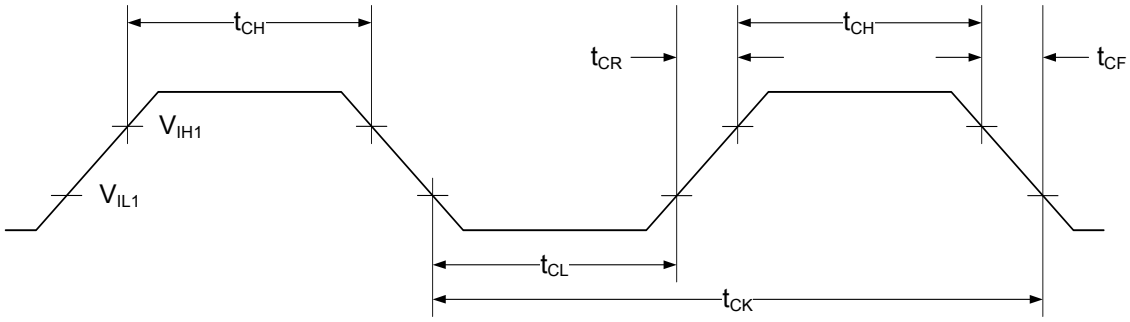



**Table 36-27. External clock used as system clock without prescaling.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock Frequency [1] | $V_{CC}$ = 1.6 - 1.8V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 32 | |
| $t_{CK}$ | Clock Period | $V_{CC}$ = 1.6 - 1.8V | 83.3 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 31.5 | | | |
| $t_{CH}$ | Clock High Time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

**Table 36-28. External clock with prescaler [1] for system clock.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock Frequency [2] | $V_{CC}$ = 1.6 - 1.8V | 0 | | 90 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 142 | |
| $t_{CK}$ | Clock Period | $V_{CC}$ = 1.6 - 1.8V | 11 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 7 | | | |
| $t_{CH}$ | Clock High Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

### 36.1.14.7 External 16MHz crystal oscillator and XOSC characteristic

**Table 36-29. External 16MHz crystal oscillator and XOSC characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Cycle to cycle jitter | XOSCPWR=0 | FRQRANGE=0 | | <10 | | ns |
| | | | FRQRANGE=1, 2, or 3 | | <1.0 | | |
| | | XOSCPWR=1 | | | <1.0 | | |
| | Long term jitter | XOSCPWR=0 | FRQRANGE=0 | | <6.0 | | ns |
| | | | FRQRANGE=1, 2, or 3 | | <0.5 | | |
| | | XOSCPWR=1 | | | <0.5 | | |
| | Frequency error | XOSCPWR=0 | FRQRANGE=0 | | <0.1 | | % |
| | | | FRQRANGE=1 | | <0.05 | | |
| | | | FRQRANGE=2 or 3 | | <0.005 | | |
| | | XOSCPWR=1 | | | <0.005 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Duty cycle | XOSCPWR=0 | FRQRANGE=0 | | 40 | | % |
| | | | FRQRANGE=1 | | 42 | | |
| | | | FRQRANGE=2 or 3 | | 45 | | |
| | | XOSCPWR=1 | | | 48 | | |
| $R_Q$ | Negative impedance [1] | XOSCPWR=0, FRQRANGE=0 | 0.4MHz resonator, CL=100pF | 2.4k | | | Ω |
| | | | 1MHz crystal, CL=20pF | 8.7k | | | |
| | | | 2MHz crystal, CL=20pF | 2.1k | | | |
| | | XOSCPWR=0, FRQRANGE=1, CL=20pF | 2MHz crystal | 4.2k | | | |
| | | | 8MHz crystal | 250 | | | |
| | | | 9MHz crystal | 195 | | | |
| | | XOSCPWR=0, FRQRANGE=2, CL=20pF | 8MHz crystal | 360 | | | |
| | | | 9MHz crystal | 285 | | | |
| | | | 12MHz crystal | 155 | | | |
| | | XOSCPWR=0, FRQRANGE=3, CL=20pF | 9MHz crystal | 365 | | | |
| | | | 12MHz crystal | 200 | | | |
| | | | 16MHz crystal | 105 | | | |
| | | XOSCPWR=1, FRQRANGE=0, CL=20pF | 9MHz crystal | 435 | | | |
| | | | 12MHz crystal | 235 | | | |
| | | | 16MHz crystal | 125 | | | |
| | | XOSCPWR=1, FRQRANGE=1, CL=20pF | 9MHz crystal | 495 | | | |
| | | | 12MHz crystal | 270 | | | |
| | | | 16MHz crystal | 145 | | | |
| | | XOSCPWR=1, FRQRANGE=2, CL=20pF | 12MHz crystal | 305 | | | |
| | | | 16MHz crystal | 160 | | | |
| | | XOSCPWR=1, FRQRANGE=3, CL=20pF | 12MHz crystal | 380 | | | |
| | | | 16MHz crystal | 205 | | | |
| | ESR | SF = Safety factor | | | | min($R_Q$)/SF | kΩ |
| $C_{XTAL1}$ | Parasitic capacitance XTAL1 pin | | | | 5.4 | | pF |
| $C_{XTAL2}$ | Parasitic capacitance XTAL2 pin | | | | 7.1 | | pF |
| $C_{LOAD}$ | Parasitic capacitance load | | | | 3.07 | | pF |

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

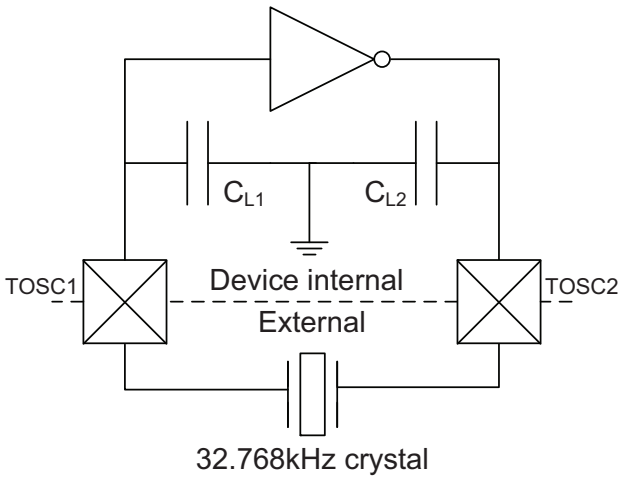
### 36.1.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

**Table 36-30. External 32.768kHz crystal oscillator and TOSC characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ESR/R1 | Recommended crystal equivalent series resistance (ESR) | Crystal load capacitance 6.5pF | | | 60 | kΩ |
| | | Crystal load capacitance 9.0pF | | | 35 | |
| $C_{TOSC1}$ | Parasitic capacitance TOSC1 pin | | | 5.4 | | pF |
| | | Alternate TOSC location | | 4.0 | | |
| $C_{TOSC2}$ | Parasitic capacitance TOSC2 pin | | | 7.1 | | pF |
| | | Alternate TOSC location | | 4.0 | | |
| | Recommended safety factor | capacitance load matched to crystal specification | 3 | | | |

Note: 1. See Figure 36-4 for definition.

**Figure 36-4. TOSC input capacitance.**




The parasitic capacitance between the TOSC pins is $C_{L1}$ + $C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

### 36.1.15 SPI Characteristics

**Figure 36-5. SPI timing requirements in master mode.**

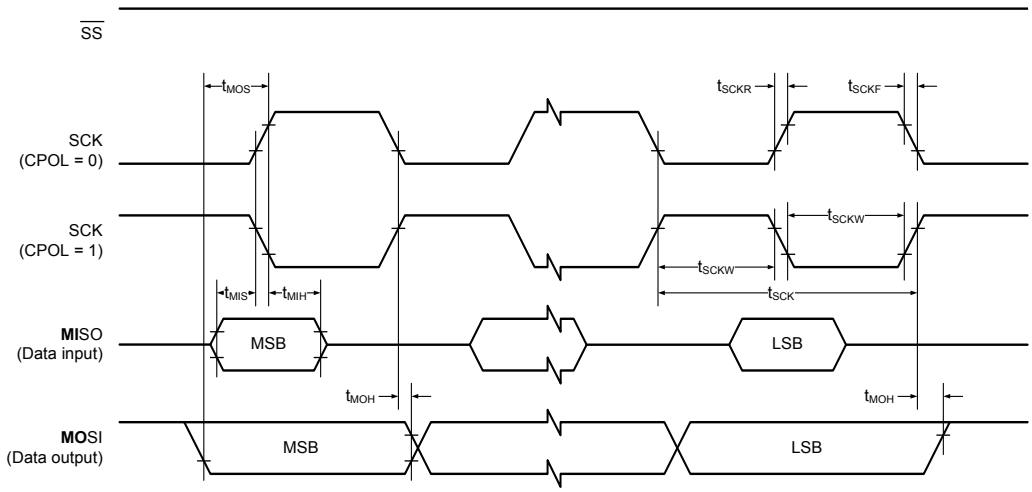



**Figure 36-6. SPI timing requirements in slave mode.**

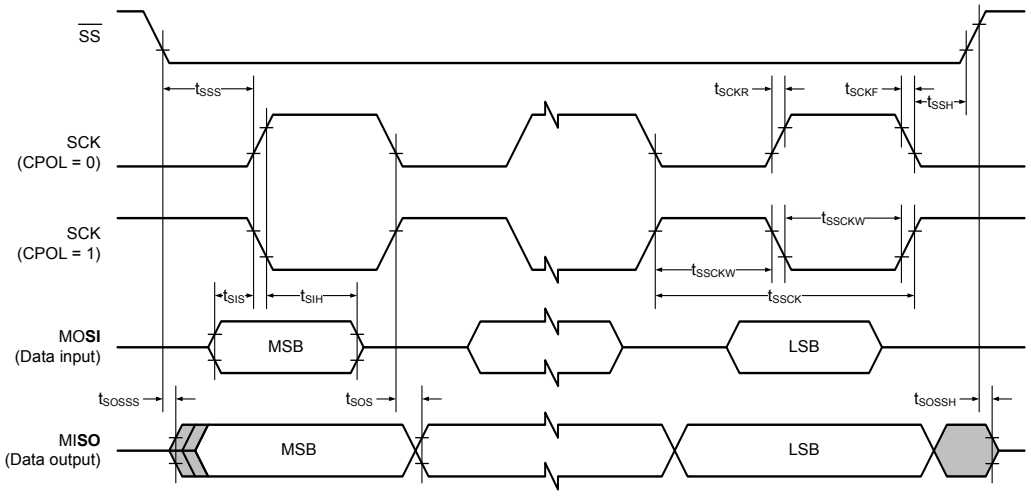


**Table 36-31. SPI timing characteristics and requirements.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{SCK}$ | SCK period | Master | | (See Table 21-4 in XMEGA AU Manual) | | ns |
| $t_{SCKW}$ | SCK high/low width | Master | | 0.5*SCK | | |
| $t_{SCKR}$ | SCK rise time | Master | | 2.7 | | |
| $t_{SCKF}$ | SCK fall time | Master | | 2.7 | | |
| $t_{MIS}$ | MISO setup to SCK | Master | | 10 | | |
| $t_{MIH}$ | MISO hold after SCK | Master | | 10 | | |
| $t_{MOS}$ | MOSI setup SCK | Master | | 0.5*SCK | | |
| $t_{MOH}$ | MOSI hold after SCK | Master | | 1 | | |
| $t_{SSCK}$ | Slave SCK Period | Slave | 4*t $Clk_{PER}$ | | | |
| $t_{SSCKW}$ | SCK high/low width | Slave | 2*t $Clk_{PER}$ | | | |
| $t_{SSCKR}$ | SCK rise time | Slave | | | 1600 | |
| $t_{SSCKF}$ | SCK fall time | Slave | | | 1600 | |
| $t_{SIS}$ | MOSI setup to SCK | Slave | 3 | | | |
| $t_{SIH}$ | MOSI hold after SCK | Slave | t $Clk_{PER}$ | | | |
| $t_{SSS}$ | $\overline{SS}$ setup to SCK | Slave | 21 | | | |
| $t_{SSH}$ | $\overline{SS}$ hold after SCK | Slave | 20 | | | |
| $t_{SOS}$ | MISO setup SCK | Slave | | 8 | | |
| $t_{SOH}$ | MISO hold after SCK | Slave | | 13 | | |
| $t_{SOSS}$ | MISO setup after $\overline{SS}$ low | Slave | | 11 | | |
| $t_{SOSH}$ | MISO hold after $\overline{SS}$ high | Slave | | 8 | | |

### 36.1.16 Two-Wire Interface Characteristics

Table 36-32 on page 92 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-7 on page 91.

**Figure 36-7. Two-wire interface bus timing.**

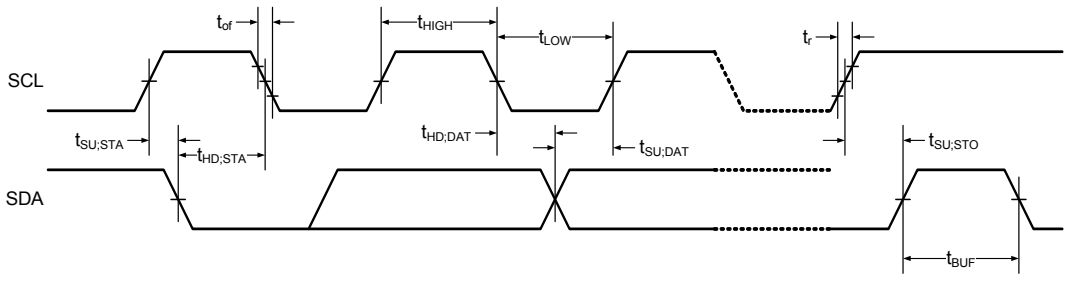


**Table 36-32. Two-wire interface characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | $0.7*V_{CC}$ | | $V_{CC}+0.5$ | V |
| $V_{IL}$ | Input low voltage | | 0.5 | | $0.3*V_{CC}$ | V |
| $V_{hys}$ | Hysteresis of Schmitt trigger inputs | | $0.05*V_{CC}$ (1) | | | V |
| $V_{OL}$ | Output low voltage | 3mA, sink current | 0 | | 0.4 | V |
| $t_r$ | Rise time for both SDA and SCL | | $20+0.1C_b$ (1)(2) | | 300 | ns |
| $t_{of}$ | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ | $10pF < C_b < 400pF$ (2) | $20+0.1C_b$ (1)(2) | | 250 | ns |
| $t_{SP}$ | Spikes suppressed by input filter | | 0 | | 50 | ns |
| $I_I$ | Input current for each I/O Pin | $0.1V_{CC} < V_I < 0.9V_{CC}$ | -10 | | 10 | µA |
| $C_I$ | Capacitance for each I/O Pin | | | | 10 | pF |
| $f_{SCL}$ | SCL clock frequency | $f_{PER}$ (3)>max($10f_{SCL}$, 250kHz) | 0 | | 400 | kHz |
| $R_P$ | Value of pull-up resistor | $f_{SCL} \leq 100kHz$ | $\frac{V_{CC}-0.4V}{3mA}$ | | $\frac{100ns}{C_b}$ | Ω |
| | | $f_{SCL} > 100kHz$ | | | $\frac{300ns}{C_b}$ | |
| $t_{HD;STA}$ | Hold time (repeated) START condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{LOW}$ | Low period of SCL clock | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |
| $t_{HIGH}$ | High period of SCL clock | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{HD;DAT}$ | Data hold time | $f_{SCL} \leq 100kHz$ | 0 | | 3.45 | µs |
| | | $f_{SCL} > 100kHz$ | 0 | | 0.9 | |
| $t_{SU;DAT}$ | Data setup time | $f_{SCL} \leq 100kHz$ | 250 | | | ns |
| | | $f_{SCL} > 100kHz$ | 100 | | | |
| $t_{SU;STO}$ | Setup time for STOP condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{BUF}$ | Bus free time between a STOP and START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. $C_b$ = Capacitance of one bus line in pF.
3. $f_{PER}$ = Peripheral clock frequency.

## 36.2 ATxmega32A4U

### 36.2.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-33 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 36-33. Absolute maximum ratings.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | -0.3 | | 4 | V |
| $I_{VCC}$ | Current into a $V_{CC}$ pin | | | | 200 | mA |
| $I_{GND}$ | Current out of a Gnd pin | | | | 200 | mA |
| $V_{PIN}$ | Pin voltage with respect to Gnd and $V_{CC}$ | | -0.5 | | $V_{CC}$+0.5 | V |
| $I_{PIN}$ | I/O pin sink/source current | | -25 | | 25 | mA |
| $T_A$ | Storage temperature | | -65 | | 150 | °C |
| $T_j$ | Junction temperature | | | | 150 | °C |

### 36.2.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-34 in order for all other electrical characteristics and typical characteristics of the device to be valid.

**Table 36-34. General operating conditions.**

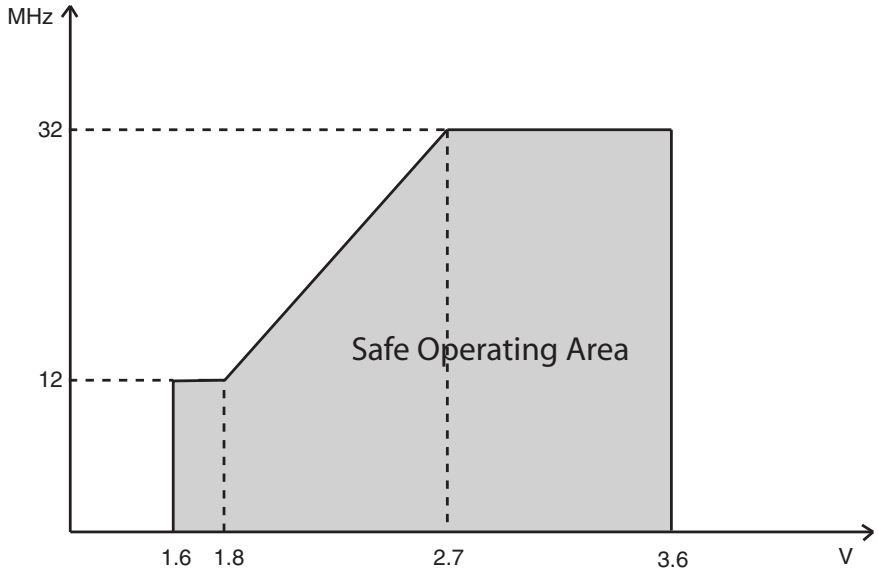
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | 1.60 | | 3.6 | V |
| $AV_{CC}$ | Analog supply voltage | | 1.60 | | 3.6 | V |
| $T_A$ | Temperature range | | -40 | | 85 | °C |
| $T_j$ | Junction temperature | | -40 | | 105 | °C |

**Table 36-35. Operating voltage and frequency.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{CPU}$ | CPU clock frequency | $V_{CC}$ = 1.6V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 1.8V | 0 | | 12 | |
| | | $V_{CC}$ = 2.7V | 0 | | 32 | |
| | | $V_{CC}$ = 3.6V | 0 | | 32 | |

The maximum CPU clock frequency depends on $V_{CC}$. As shown in Figure 36-8 the Frequency vs. $V_{CC}$ curve is linear between 1.8V < $V_{CC}$ < 2.7V.

**Figure 36-8. Maximum Frequency vs. $V_{CC}$.**



### 36.2.3 Current consumption

**Table 36-36. Current consumption for Active mode and sleep modes.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Active power consumption[1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 40 | | µA |
| | | | $V_{CC}$ = 3.0V | | 80 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 230 | | |
| | | | $V_{CC}$ = 3.0V | | 480 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 430 | 600 | |
| | | | $V_{CC}$ = 3.0V | | 0.9 | 1.4 | mA |
| | | 32MHz, Ext. Clk | | | 9.6 | 12 | |
| | Idle power consumption[1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 2.4 | | µA |
| | | | $V_{CC}$ = 3.0V | | 3.9 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 62 | | |
| | | | $V_{CC}$ = 3.0V | | 118 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 125 | 225 | |
| | | | $V_{CC}$ = 3.0V | | 240 | 350 | |
| | | 32MHz, Ext. Clk | | | 3.8 | 5.5 | mA |
| | Power-down power consumption | T = 25°C | $V_{CC}$ = 3.0V | | 0.1 | 1.0 | µA |
| | | T = 85°C | | | 1.2 | 4.5 | |
| | | T = 105°C | | | 3.5 | 6.0 | |
| | | WDT and sampled BOD enabled, T = 25°C | $V_{CC}$ = 3.0V | | 1.3 | 3.0 | |
| | | WDT and sampled BOD enabled, T = 85°C | | | 2.4 | 6.0 | |
| | | WDT and sampled BOD enabled, T = 105°C | | | 4.5 | 8.0 | |
| | Power-save power consumption[2] | RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C | $V_{CC}$ = 1.8V | | 1.2 | | µA |
| | | | $V_{CC}$ = 3.0V | | 1.3 | | |
| | | RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.6 | 2.0 | |
| | | | $V_{CC}$ = 3.0V | | 0.7 | 2.0 | |
| | | RTC from low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.8 | 3.0 | |
| | | | $V_{CC}$ = 3.0V | | 1.0 | 3.0 | |
| | Reset power consumption | Current through $\overline{\text{RESET}}$ pin substracted | $V_{CC}$ = 3.0V | | 320 | | |

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

**Table 36-37. Current consumption for modules and peripherals.**

| Symbol | Parameter | Condition [1] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | ULP oscillator | | | | 1.0 | | µA |
| | 32.768kHz int. oscillator | | | | 27 | | µA |
| | 2MHz int. oscillator | | | | 85 | | µA |
| | | DFLL enabled with 32.768kHz int. osc. as reference | | | 115 | | |
| | 32MHz int. oscillator | | | | 270 | | µA |
| | | DFLL enabled with 32.768kHz int. osc. as reference | | | 460 | | |
| | PLL | 20x multiplication factor,<br>32MHz int. osc. DIV4 as reference | | | 220 | | µA |
| | Watchdog timer | | | | 1.0 | | µA |
| | BOD | Continuous mode | | | 138 | | µA |
| | | Sampled mode, includes ULP oscillator | | | 1.2 | | |
| | Internal 1.0V reference | | | | 100 | | µA |
| | Temperature sensor | | | | 95 | | µA |
| | ADC | 250ksps<br>$V_{REF}$ = Ext ref | | | 3.0 | | mA |
| | | | CURRLIMIT = LOW | | 2.6 | | |
| | | | CURRLIMIT = MEDIUM | | 2.1 | | |
| | | | CURRLIMIT = HIGH | | 1.6 | | |
| | DAC | 250ksps<br>$V_{REF}$ = Ext ref<br>No load | Normal mode | | 1.9 | | mA |
| | | | Low power mode | | 1.1 | | |
| | AC | High speed mode | | | 330 | | µA |
| | | Low power mode | | | 130 | | |
| | DMA | 615kbps between I/O registers and SRAM | | | 108 | | µA |
| | Timer/counter | | | | 16 | | µA |
| | USART | Rx and Tx enabled, 9600 BAUD | | | 2.5 | | µA |
| | Flash memory and EEPROM programming | | | | 4.0 | 8.0 | mA |

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at $V_{CC}$ = 3.0V, $Clk_{SYS}$ = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

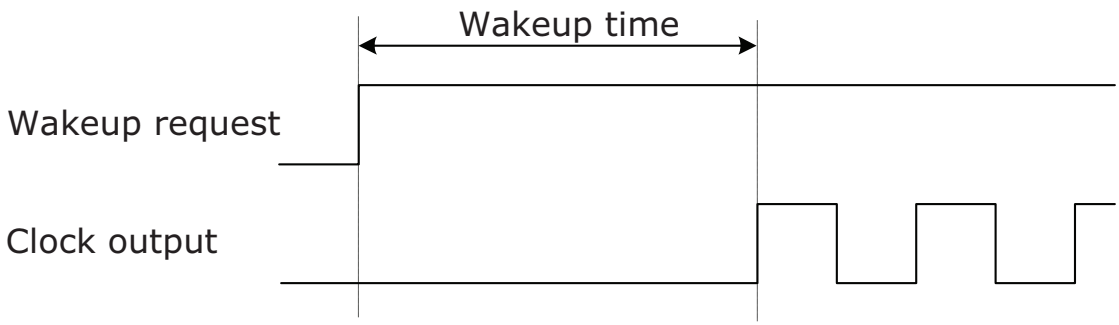
### 36.2.4 Wake-up time from sleep modes

**Table 36-38. Device wake-up time from sleep modes with various system clock sources.**

| Symbol | Parameter | Condition | Min. | Typ. [1] | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{wakeup}$ | Wake-up time from idle, standby, and extended standby mode | External 2MHz clock | | 2.0 | | µs |
| | | 32.768kHz internal oscillator | | 120 | | |
| | | 2MHz internal oscillator | | 2.0 | | |
| | | 32MHz internal oscillator | | 0.2 | | |
| | Wake-up time from power-save and power-down mode | External 2MHz clock | | 4.5 | | µs |
| | | 32.768kHz internal oscillator | | 320 | | |
| | | 2MHz internal oscillator | | 9.0 | | |
| | | 32MHz internal oscillator | | 5.0 | | |

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-9. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

**Figure 36-9. Wake-up time definition.**



### 36.2.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

**Table 36-39. I/O pin characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ (1)/ $I_{OL}$ (2) | I/O pin source/sink current | | | -20 | | 20 | mA |
| $V_{IH}$ | High level input voltage | $V_{CC}$ = 2.7 - 3.6V | | 2.0 | | $V_{CC}$+0.3 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | 0.7*$V_{CC}$ | | $V_{CC}$+0.3 | |
| | | $V_{CC}$ = 1.6 - 2.0V | | 0.8*$V_{CC}$ | | $V_{CC}$+0.3 | |
| $V_{IL}$ | Low level input voltage | $V_{CC}$ = 2.7- 3.6V | | -0.3 | | 0.8 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | -0.3 | | 0.3*$V_{CC}$ | |
| | | $V_{CC}$ = 1.6 - 2.0V | | -0.3 | | 0.2*$V_{CC}$ | |
| $V_{OH}$ | High level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OH}$ = -2mA | 2.4 | 0.94*$V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OH}$ = -1mA | 2.0 | 0.96*$V_{CC}$ | | |
| | | | $I_{OH}$ = -2mA | 1.7 | 0.92*$V_{CC}$ | | |
| | | $V_{CC}$ = 3.3V | $I_{OH}$ = -8mA | 2.6 | 2.9 | | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = -6mA | 2.1 | 2.6 | | |
| | | $V_{CC}$ = 1.8V | $I_{OH}$ = -2mA | 1.4 | 1.6 | | |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OL}$ = 2mA | | 0.05*$V_{CC}$ | 0.4 | V |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OL}$ = 1mA | | 0.03*$V_{CC}$ | 0.4 | |
| | | | $I_{OL}$ = 2mA | | 0.06*$V_{CC}$ | 0.7 | |
| | | $V_{CC}$ = 3.3V | $I_{OL}$ = 15mA | | 0.4 | 0.76 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 10mA | | 0.3 | 0.64 | |
| | | $V_{CC}$ = 1.8V | $I_{OL}$ = 5mA | | 0.2 | 0.46 | |
| $I_{IN}$ | Input leakage current | T = 25°C | | | <0.01 | 0.1 | µA |
| $R_P$ | Pull/buss keeper resistor | | | | 24 | | kΩ |
| $t_r$ | Rise time | No load | | | 4.0 | | ns |
| | | | slew rate limitation | | 7.0 | | |

Notes:
1. The sum of all $I_{OH}$ for PORTA and PORTB must not exceed 100mA.
The sum of all $I_{OH}$ for PORTC must not exceed 200mA.
The sum of all $I_{OH}$ for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
The sum of all $I_{OH}$ for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.
2. The sum of all $I_{OL}$ for PORTA and PORTB must not exceed 100mA.
The sum of all $I_{OL}$ for PORTC must not exceed 200mA.
The sum of all $I_{OL}$ for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
The sum of all $I_{OL}$ for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.

### 36.2.6 ADC characteristics

**Table 36-40. Power supply, reference and input range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $V_{REF}$ | Reference voltage | | 1 | | $AV_{CC}$- 0.6 | V |
| $R_{in}$ | Input resistance | Switched | | 4.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched | | 4.4 | | pF |
| $R_{AREF}$ | Reference input resistance | (leakage only) | | >10 | | MΩ |
| $C_{AREF}$ | Reference input capacitance | Static load | | 7 | | pF |
| $V_{IN}$ | Input range | | -0.1 | | $AV_{CC}$+0.1 | V |
| | Conversion range | Differential mode, Vinp - Vinn | $-V_{REF}$ | | $V_{REF}$ | V |
| | Conversion range | Single ended unsigned mode, Vinp | -ΔV | | $V_{REF}$-ΔV | V |
| ΔV | Fixed offset voltage | | | 190 | | LSB |

**Table 36-41. Clock and timing.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{ADC}$ | ADC clock frequency | Maximum is 1/4 of peripheral clock frequency | 100 | | 2000 | kHz |
| | | Measuring internal signals | 100 | | 125 | |
| $f_{ADC}$ | Sample rate | Current limitation (CURRLIMIT) off | 100 | | 2000 | ksps |
| | | CURRLIMIT = LOW | 100 | | 1500 | |
| | | CURRLIMIT = MEDIUM | 100 | | 1000 | |
| | | CURRLIMIT = HIGH | 100 | | 500 | |
| | Sampling time | 1/2 $Clk_{ADC}$ cycle | 0.25 | | 5 | µs |
| | Conversion time (latency) | (RES+2)/2+(GAIN !=0)<br>RES (Resolution) = 8 or 12 | 5 | | 8 | $Clk_{ADC}$ cycles |
| | Start-up time | ADC clock cycles | | 12 | 24 | $Clk_{ADC}$ cycles |
| | ADC settling time | After changing reference or input mode | | 7 | 7 | $Clk_{ADC}$ cycles |
| | | After ADC flush | | 1 | 1 | |

**Table 36-42. Accuracy characteristics.**

| Symbol | Parameter | Condition [2] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Resolution | Programmable to 8 or 12 bit | | 8 | 12 | 12 | Bits |
| INL[1] | Integral non-linearity | 500ksps | $V_{CC}$-1.0V < $V_{REF}$< $V_{CC}$-0.6V | | ±1.2 | ±2.0 | lsb |
| | | | All $V_{REF}$ | | ±1.5 | ±3.0 | |
| | | 2000ksps | $V_{CC}$-1.0V < $V_{REF}$< $V_{CC}$-0.6V | | ±1.0 | ±2.0 | |
| | | | All $V_{REF}$ | | ±1.5 | ±3.0 | |
| DNL[1] | Differential non-linearity | guaranteed monotonic | | | <±0.8 | <±1.0 | lsb |
| | Offset error | | | | -1.0 | | mV |
| | | Temperature drift | | | <0.01 | | mV/K |
| | | Operating voltage drift | | | <0.6 | | mV/V |
| | Gain error | Differential mode | External reference | | -1.0 | | mV |
| | | | $AV_{CC}$/1.6 | | 10 | | |
| | | | $AV_{CC}$/2.0 | | 8.0 | | |
| | | | Bandgap | | ±5.0 | | |
| | | Temperature drift | | | <0.02 | | mV/K |
| | | Operating voltage drift | | | <0.5 | | mV/V |
| | Noise | Differential mode, shorted input 2msps, $V_{CC}$ = 3.6V, $Clk_{PER}$ = 16MHz | | | 0.4 | | mV rms |

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external $V_{REF}$ is used.

**Table 36-43. Gain stage characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $R_{in}$ | Input resistance | Switched in normal mode | | | 4.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched in normal mode | | | 4.4 | | pF |
| | Signal range | Gain stage output | | 0 | | $V_{CC}$- 0.6 | V |
| | Propagation delay | ADC conversion rate | | | 1.0 | | $Clk_{ADC}$ cycles |
| | Sample rate | Same as ADC | | 100 | | 1000 | kHz |
| INL [1] | Integral non-linearity | 500ksps | All gain settings | | ±1.5 | ±4.0 | lsb |
| | Gain error | 1x gain, normal mode | | | -0.8 | | % |
| | | 8x gain, normal mode | | | -2.5 | | |
| | | 64x gain, normal mode | | | -3.5 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Offset error, input referred | 1x gain, normal mode | | | -2.0 | | mV |
| | | 8x gain, normal mode | | | -5.0 | | |
| | | 64x gain, normal mode | | | -4.0 | | |
| | Noise | 1x gain, normal mode | $V_{CC}$ = 3.6V Ext. $V_{REF}$ | | 0.5 | | mV rms |
| | | 8x gain, normal mode | | | 1.5 | | |
| | | 64x gain, normal mode | | | 11 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

### 36.2.7 DAC Characteristics

**Table 36-44. Power supply, reference and output range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $AV_{REF}$ | External reference voltage | | 1.0 | | $V_{CC}$- 0.6 | V |
| $R_{channel}$ | DC output impedance | | | | 50 | Ω |
| | Linear output voltage range | | 0.15 | | $AV_{CC}$-0.15 | V |
| $R_{AREF}$ | Reference input resistance | | | >10 | | MΩ |
| CAREF | Reference input capacitance | Static load | | 7.0 | | pF |
| | Minimum Resistance load | | 1.0 | | | kΩ |
| | Maximum capacitance load | | | | 100 | pF |
| | | 1000Ω serial resistance | | | 1.0 | nF |
| | Output sink/source | Operating within accuracy specification | | | $AV_{CC}$/1000 | mA |
| | | Safe operation | | | 10 | |

**Table 36-45. Clock and timing.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{DAC}$ | Conversion rate | $C_{load}$=100pF, maximum step size | Normal mode | 0 | | 1000 | ksps |
| | | | Low power mode | | | 500 | |

**Table 36-46. Accuracy characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Input resolution | | | | | 12 | Bits |
| INL [(1)] | Integral non-linearity | $V_{REF}$= Ext 1.0V | $V_{CC}$ = 1.6V | | ±2.0 | ±3.0 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±2.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±2.0 | ±4.0 | |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±4.0 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±5.0 | | |
| | | | $V_{CC}$ = 3.6V | | ±5.0 | | |
| DNL [(1)] | Differential non-linearity | $V_{REF}$=Ext 1.0V | $V_{CC}$ = 1.6V | | ±1.5 | 3.0 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±1.0 | 3.5 | |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±4.5 | | |
| | | | $V_{CC}$ = 3.6V | | ±4.5 | | |
| | Gain error | After calibration | | | <4.0 | | lsb |
| | Gain calibration step size | | | | 4.0 | | lsb |
| | Gain calibration drift | $V_{REF}$= Ext 1.0V | | | <0.2 | | mV/K |
| | Offset error | After calibration | | | <1.0 | | lsb |
| | Offset calibration step size | | | | 1.0 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

### 36.2.8 Analog Comparator Characteristics

**Table 36-47. Analog Comparator characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{off}$ | Input offset voltage | | | | <±10 | | mV |
| $I_{lk}$ | Input leakage current | | | | <1 | | nA |
| | Input voltage range | | | -0.1 | | $AV_{CC}$ | V |
| | AC startup time | | | | 100 | | µs |
| $V_{hys1}$ | Hysteresis, none | | | | 0 | | mV |
| $V_{hys2}$ | Hysteresis, small | mode = High Speed (HS) | | | 13 | | mV |
| | | mode = Low Power (LP) | | | 30 | | |
| $V_{hys3}$ | Hysteresis, large | mode = HS | | | 30 | | mV |
| | | mode = LP | | | 60 | | |
| $t_{delay}$ | Propagation delay | $V_{CC}$ = 3.0V, T= 85°C | mode = HS | | 30 | 90 | ns |
| | | mode = HS | | | 30 | | |
| | | $V_{CC}$ = 3.0V, T= 85°C | mode = LP | | 130 | 500 | |
| | | mode = LP | | | 130 | | |
| | 64-level voltage scaler | Integral non-linearity (INL) | | | 0.3 | 0.5 | lsb |

### 36.2.9 Bandgap and Internal 1.0V Reference Characteristics

**Table 36-48. Bandgap and Internal 1.0V reference characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Startup time | As reference for ADC or DAC | 1 $Clk_{PER}$ + 2.5µs | | | µs |
| | | As input voltage to ADC and AC | | 1.5 | | |
| | Bandgap voltage | | | 1.1 | | V |
| INT1V | Internal 1.00V reference | T= 85°C, after calibration | 0.99 | 1.0 | 1.01 | V |
| | Variation over voltage and temperature | Relative to T= 85°C, $V_{CC}$ = 3.0V | | ±1.5 | | % |

### 36.2.10 Brownout Detection Characteristics

**Table 36-49. Brownout detection characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{BOT}$ | BOD level 0 falling $V_{CC}$ | | 1.60 | 1.62 | 1.72 | V |
| | BOD level 1 falling $V_{CC}$ | | | 1.8 | | |
| | BOD level 2 falling $V_{CC}$ | | | 2.0 | | |
| | BOD level 3 falling $V_{CC}$ | | | 2.2 | | |
| | BOD level 4 falling $V_{CC}$ | | | 2.4 | | |
| | BOD level 5 falling $V_{CC}$ | | | 2.6 | | |
| | BOD level 6 falling $V_{CC}$ | | | 2.8 | | |
| | BOD level 7 falling $V_{CC}$ | | | 3.0 | | |
| $t_{BOD}$ | Detection time | Continuous mode | | 0.4 | | µs |
| | | Sampled mode | | 1000 | | |
| $V_{HYST}$ | Hysteresis | | | 1.2 | | % |

### 36.2.11 External Reset Characteristics

**Table 36-50. External reset characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{EXT}$ | Minimum reset pulse width | | | 95 | 1000 | ns |
| $V_{RST}$ | Reset threshold voltage ($V_{IH}$) | $V_{CC}$ = 2.7 - 3.6V | | 0.60*$V_{CC}$ | | V |
| | | $V_{CC}$ = 1.6 - 2.7V | | 0.60*$V_{CC}$ | | |
| | Reset threshold voltage ($V_{IL}$) | $V_{CC}$ = 2.7 - 3.6V | | 0.50*$V_{CC}$ | | |
| | | $V_{CC}$ = 1.6 - 2.7V | | 0.40*$V_{CC}$ | | |
| $R_{RST}$ | Reset pin Pull-up Resistor | | | 25 | | kΩ |

### 36.2.12 Power-on Reset Characteristics

**Table 36-51. Power-on reset characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{POT-}$ [(1)] | POR threshold voltage falling $V_{CC}$ | $V_{CC}$ falls faster than 1V/ms | 0.4 | 1.0 | | V |
| | | $V_{CC}$ falls at 1V/ms or slower | 0.8 | 1.0 | | |
| $V_{POT+}$ | POR threshold voltage rising $V_{CC}$ | | | 1.3 | 1.59 | V |

Note: 1. $V_{POT-}$ values are only valid when BOD is disabled. When BOD is enabled $V_{POT-}$ = $V_{POT+}$.

### 36.2.13 Flash and EEPROM Memory Characteristics

**Table 36-52. Endurance and data retention.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Flash | Write/Erase cycles | 25°C | 10K | | | Cycle |
| | | | 85°C | 10K | | | |
| | | | 105°C | 2K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 85°C | 25 | | | |
| | | | 105°C | 10 | | | |
| | EEPROM | Write/Erase cycles | 25°C | 100K | | | Cycle |
| | | | 85°C | 100K | | | |
| | | | 105°C | 30K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 85°C | 25 | | | |
| | | | 105°C | 10 | | | |

**Table 36-53. Programming time.**

| Symbol | Parameter | Condition | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| | Chip Erase | 32KB Flash, EEPROM[2] and SRAM erase | | 50 | | ms |
| | Application Erase | Section erase | | 6 | | ms |
| | Flash | Page erase | | 4 | | ms |
| | | Page write | | 4 | | |
| | | Atomic page erase and write | | 8 | | |
| | EEPROM | Page erase | | 4 | | ms |
| | | Page write | | 4 | | |
| | | Atomic page erase and write | | 8 | | |

Notes:
1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

### 36.2.14 Clock and Oscillator Characteristics

#### 36.2.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

**Table 36-54. 32.768kHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency | | | 32.768 | | kHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$ = 3.0V | -0.5 | | 0.5 | % |
| | User calibration accuracy | | -0.5 | | 0.5 | % |

#### 36.2.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

**Table 36-55. 2MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 1.8 | | 2.2 | MHz |
| | Factory calibrated frequency | | | 2.0 | | MHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | % |
| | DFLL calibration stepsize | | | 0.21 | | % |

#### 36.2.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

**Table 36-56. 32MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 30 | | 55 | MHz |
| | Factory calibrated frequency | | | 32 | | MHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | % |
| | DFLL calibration step size | | | 0.22 | | % |

#### 36.2.14.4 32kHz Internal ULP Oscillator characteristics

**Table 36-57. 32kHz internal ULP oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Output frequency | | | 32 | | kHz |
| | Accuracy | | -30 | | 30 | % |

### 36.2.14.5 Internal Phase Locked Loop (PLL) characteristics

**Table 36-58. Internal PLL characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input frequency | Output frequency must be within $f_{OUT}$ | 0.4 | | 64 | MHz |
| $f_{OUT}$ | Output frequency (1) | $V_{CC}$= 1.6 - 1.8V | 20 | | 48 | MHz |
| | | $V_{CC}$= 2.7 - 3.6V | 20 | | 128 | |
| | Start-up time | | | 25 | | µs |
| | Re-lock time | | | 25 | | µs |

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

### 36.2.14.6 External clock characteristics

**Figure 36-10. External clock drive waveform**

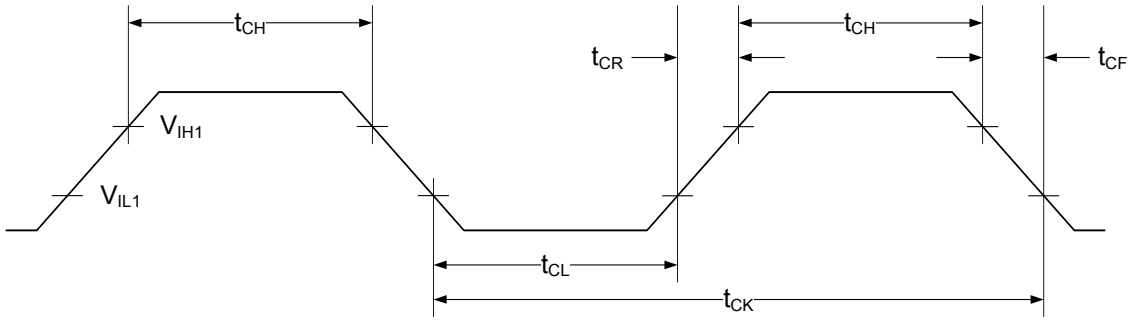



**Table 36-59. External clock used as system clock without prescaling.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock Frequency (1) | $V_{CC}$ = 1.6 - 1.8V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 32 | |
| $t_{CK}$ | Clock Period | $V_{CC}$ = 1.6 - 1.8V | 83.3 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 31.5 | | | |
| $t_{CH}$ | Clock High Time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

**Table 36-60. External clock with prescaler [1] for system clock.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock Frequency [2] | $V_{CC}$ = 1.6 - 1.8V | 0 | | 90 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 142 | |
| $t_{CK}$ | Clock Period | $V_{CC}$ = 1.6 - 1.8V | 11 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 7 | | | |
| $t_{CH}$ | Clock High Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

### 36.2.14.7 External 16MHz crystal oscillator and XOSC characteristic

**Table 36-61. External 16MHz crystal oscillator and XOSC characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Cycle to cycle jitter | XOSCPWR=0 | FRQRANGE=0 | | <10 | | ns |
| | | | FRQRANGE=1, 2, or 3 | | <1 | | |
| | | XOSCPWR=1 | | | <1 | | |
| | Long term jitter | XOSCPWR=0 | FRQRANGE=0 | | <6 | | ns |
| | | | FRQRANGE=1, 2, or 3 | | <0.5 | | |
| | | XOSCPWR=1 | | | <0.5 | | |
| | Frequency error | XOSCPWR=0 | FRQRANGE=0 | | <0.1 | | % |
| | | | FRQRANGE=1 | | <0.05 | | |
| | | | FRQRANGE=2 or 3 | | <0.005 | | |
| | | XOSCPWR=1 | | | <0.005 | | |
| | Duty cycle | XOSCPWR=0 | FRQRANGE=0 | | 40 | | % |
| | | | FRQRANGE=1 | | 42 | | |
| | | | FRQRANGE=2 or 3 | | 45 | | |
| | | XOSCPWR=1 | | | 48 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $R_Q$ | Negative impedance [1] | XOSCPWR=0, FRQRANGE=0 | 0.4MHz resonator, CL=100pF | 2.4k | | | Ω |
| | | | 1MHz crystal, CL=20pF | 8.7k | | | |
| | | | 2MHz crystal, CL=20pF | 2.1k | | | |
| | | XOSCPWR=0, FRQRANGE=1, CL=20pF | 2MHz crystal | 4.2k | | | |
| | | | 8MHz crystal | 250 | | | |
| | | | 9MHz crystal | 195 | | | |
| | | XOSCPWR=0, FRQRANGE=2, CL=20pF | 8MHz crystal | 360 | | | |
| | | | 9MHz crystal | 285 | | | |
| | | | 12MHz crystal | 155 | | | |
| | | XOSCPWR=0, FRQRANGE=3, CL=20pF | 9MHz crystal | 365 | | | |
| | | | 12MHz crystal | 200 | | | |
| | | | 16MHz crystal | 105 | | | |
| | | XOSCPWR=1, FRQRANGE=0, CL=20pF | 9MHz crystal | 435 | | | |
| | | | 12MHz crystal | 235 | | | |
| | | | 16MHz crystal | 125 | | | |
| | | XOSCPWR=1, FRQRANGE=1, CL=20pF | 9MHz crystal | 495 | | | |
| | | | 12MHz crystal | 270 | | | |
| | | | 16MHz crystal | 145 | | | |
| | | XOSCPWR=1, FRQRANGE=2, CL=20pF | 12MHz crystal | 305 | | | |
| | | | 16MHz crystal | 160 | | | |
| | | XOSCPWR=1, FRQRANGE=3, CL=20pF | 12MHz crystal | 380 | | | |
| | | | 16MHz crystal | 205 | | | |
| | ESR | SF = Safety factor | | | | min($R_Q$)/SF | kΩ |
| $C_{XTAL1}$ | Parasitic capacitance XTAL1 pin | | | | 5.4 | | pF |
| $C_{XTAL2}$ | Parasitic capacitance XTAL2 pin | | | | 7.1 | | pF |
| $C_{LOAD}$ | Parasitic capacitance load | | | | 3.07 | | pF |

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

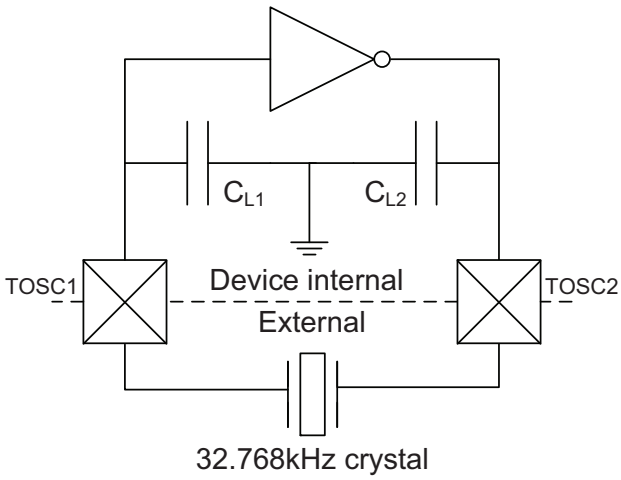
### 36.2.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

**Table 36-62. External 32.768kHz crystal oscillator and TOSC characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ESR/R1 | Recommended crystal equivalent series resistance (ESR) | Crystal load capacitance 6.5pF | | | 60 | kΩ |
| | | Crystal load capacitance 9.0pF | | | 35 | |
| $C_{TOSC1}$ | Parasitic capacitance TOSC1 pin | | | 5.4 | | pF |
| | | Alternate TOSC location | | 4.0 | | |
| $C_{TOSC2}$ | Parasitic capacitance TOSC2 pin | | | 7.1 | | pF |
| | | Alternate TOSC location | | 4.0 | | |
| | Recommended safety factor | capacitance load matched to crystal specification | 3.0 | | | |

Note: 1. See Figure 36-11 for definition.

**Figure 36-11.TOSC input capacitance.**




The parasitic capacitance between the TOSC pins is $C_{L1}$ + $C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

### 36.2.15 SPI Characteristics

**Figure 36-12. SPI timing requirements in master mode.**

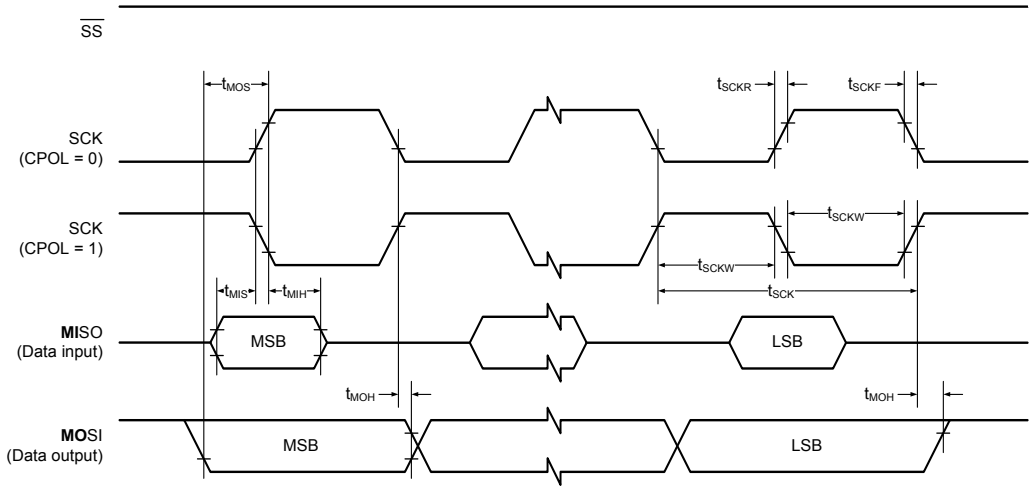



**Figure 36-13. SPI timing requirements in slave mode.**

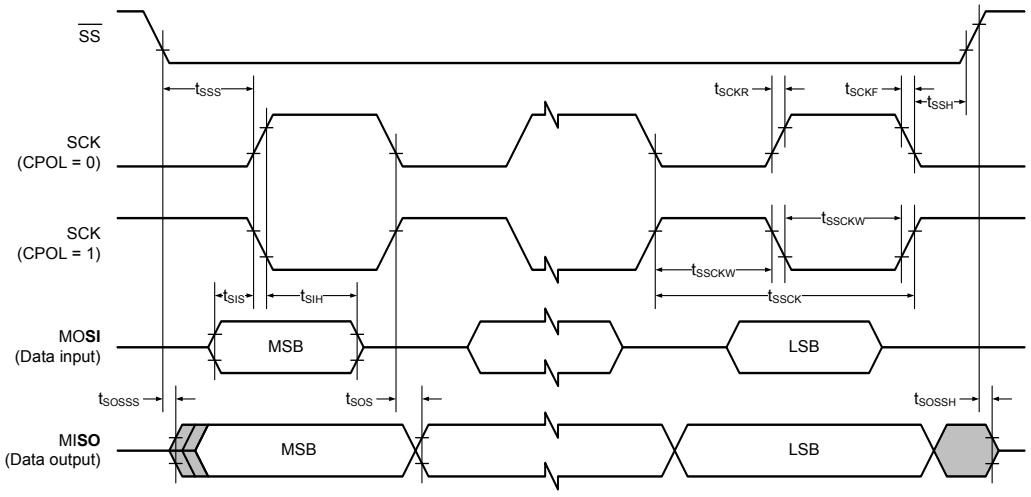


**Table 36-63. SPI timing characteristics and requirements.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{SCK}$ | SCK period | Master | | (See Table 21-4 in XMEGA AU Manual) | | ns |
| $t_{SCKW}$ | SCK high/low width | Master | | 0.5×SCK | | |
| $t_{SCKR}$ | SCK rise time | Master | | 2.7 | | |
| $t_{SCKF}$ | SCK fall time | Master | | 2.7 | | |
| $t_{MIS}$ | MISO setup to SCK | Master | | 10 | | |
| $t_{MIH}$ | MISO hold after SCK | Master | | 10 | | |
| $t_{MOS}$ | MOSI setup SCK | Master | | 0.5×SCK | | |
| $t_{MOH}$ | MOSI hold after SCK | Master | | 1.0 | | |
| $t_{SSCK}$ | Slave SCK Period | Slave | 4×t $Clk_{PER}$ | | | |
| $t_{SSCKW}$ | SCK high/low width | Slave | 2×t $Clk_{PER}$ | | | |
| $t_{SSCKR}$ | SCK rise time | Slave | | | 1600 | |
| $t_{SSCKF}$ | SCK fall time | Slave | | | 1600 | |
| $t_{SIS}$ | MOSI setup to SCK | Slave | 3.0 | | | |
| $t_{SIH}$ | MOSI hold after SCK | Slave | t $Clk_{PER}$ | | | |
| $t_{SSS}$ | $\overline{SS}$ setup to SCK | Slave | 21 | | | |
| $t_{SSH}$ | $\overline{SS}$ hold after SCK | Slave | 20 | | | |
| $t_{SOS}$ | MISO setup SCK | Slave | | 8.0 | | |
| $t_{SOH}$ | MISO hold after SCK | Slave | | 13 | | |
| $t_{SOSS}$ | MISO setup after $\overline{SS}$ low | Slave | | 11 | | |
| $t_{SOSH}$ | MISO hold after $\overline{SS}$ high | Slave | | 8.0 | | |

### 36.2.16 Two-Wire Interface Characteristics

Table 36-64 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-14.

**Figure 36-14. Two-wire interface bus timing.**

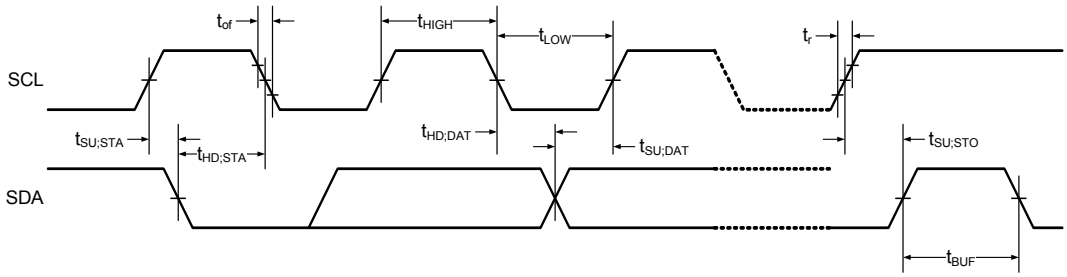



**Table 36-64. Two-wire interface characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | $0.7V_{CC}$ | | $V_{CC}$+0.5 | V |
| $V_{IL}$ | Input low voltage | | 0.5 | | $0.3 \times V_{CC}$ | V |
| $V_{hys}$ | Hysteresis of Schmitt trigger inputs | | $0.05V_{CC}$ (1) | | | V |
| $V_{OL}$ | Output low voltage | 3mA, sink current | 0 | | 0.4 | V |
| $t_r$ | Rise time for both SDA and SCL | | $20+0.1C_b$ (1)(2) | | 300 | ns |
| $t_{of}$ | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ | $10pF < C_b < 400pF$ (2) | $20+0.1C_b$ (1)(2) | | 250 | ns |
| $t_{SP}$ | Spikes suppressed by Input filter | | 0 | | 50 | ns |
| $I_I$ | Input current for each I/O Pin | $0.1V_{CC} < V_I < 0.9V_{CC}$ | -10 | | 10 | µA |
| $C_I$ | Capacitance for each I/O Pin | | | | 10 | pF |
| $f_{SCL}$ | SCL clock frequency | $f_{PER}$ (3)>max($10f_{SCL}$, 250kHz) | 0 | | 400 | kHz |
| $R_P$ | Value of pull-up resistor | $f_{SCL} \leq 100kHz$ | $\frac{V_{CC}-0.4V}{3mA}$ | | $\frac{100ns}{C_b}$ | Ω |
| | | $f_{SCL} > 100kHz$ | | | $\frac{300ns}{C_b}$ | |
| $t_{HD;STA}$ | Hold time (repeated) START condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{LOW}$ | Low period of SCL Clock | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |
| $t_{HIGH}$ | High period of SCL Clock | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{HD;DAT}$ | Data hold time | $f_{SCL} \leq 100kHz$ | 0 | | 3.45 | µs |
| | | $f_{SCL} > 100kHz$ | 0 | | 0.9 | |
| $t_{SU;DAT}$ | Data setup time | $f_{SCL} \leq 100kHz$ | 250 | | | ns |
| | | $f_{SCL} > 100kHz$ | 100 | | | |
| $t_{SU;STO}$ | Setup time for STOP condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{BUF}$ | Bus free time between a STOP and START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. $C_b$ = Capacitance of one bus line in pF.
3. $f_{PER}$ = Peripheral clock frequency.

## 36.3 ATxmega64A4U

### 36.3.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-65 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 36-65. Absolute maximum ratings.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | -0.3 | | 4.0 | V |
| $I_{VCC}$ | Current into a $V_{CC}$ pin | | | | 200 | mA |
| $I_{GND}$ | Current out of a Gnd pin | | | | 200 | mA |
| $V_{PIN}$ | Pin voltage with respect to Gnd and $V_{CC}$ | | -0.5 | | $V_{CC}$+0.5 | V |
| $I_{PIN}$ | I/O pin sink/source current | | -25 | | 25 | mA |
| $T_A$ | Storage temperature | | -65 | | 150 | °C |
| $T_j$ | Junction temperature | | | | 150 | °C |

### 36.3.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-66 in order for all other electrical characteristics and typical characteristics of the device to be valid.

**Table 36-66. General operating conditions.**

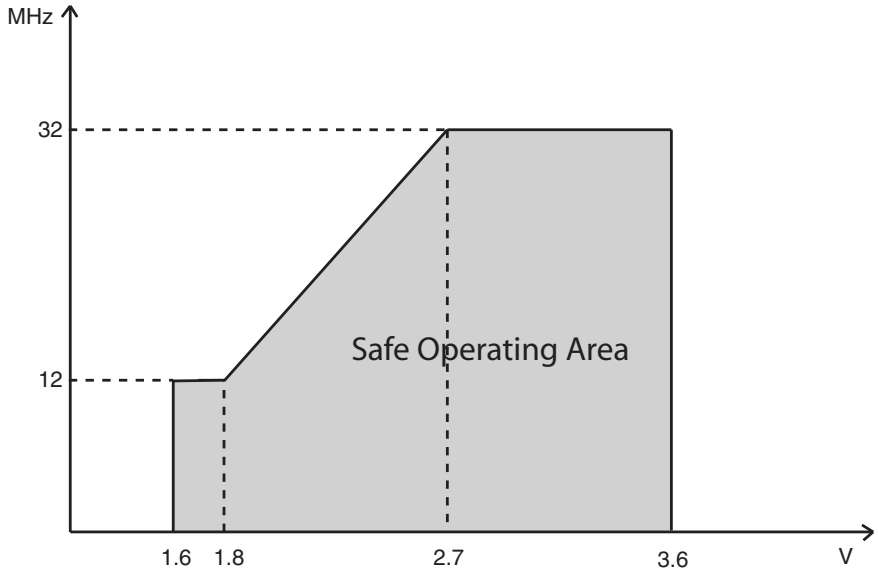
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | 1.60 | | 3.6 | V |
| $AV_{CC}$ | Analog supply voltage | | 1.60 | | 3.6 | V |
| $T_A$ | Temperature range | | -40 | | 85 | °C |
| $T_j$ | Junction temperature | | -40 | | 105 | °C |

**Table 36-67. Operating voltage and frequency.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{CPU}$ | CPU clock frequency | $V_{CC}$ = 1.6V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 1.8V | 0 | | 12 | |
| | | $V_{CC}$ = 2.7V | 0 | | 32 | |
| | | $V_{CC}$ = 3.6V | 0 | | 32 | |

The maximum CPU clock frequency depends on $V_{CC}$. As shown in Figure 36-15 the Frequency vs. $V_{CC}$ curve is linear between 1.8V < $V_{CC}$ < 2.7V.

**Figure 36-15.Maximum Frequency vs. $V_{CC}$.**



### 36.3.3 Current consumption

**Table 36-68. Current consumption for Active mode and sleep modes.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Active power consumption [1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 52 | | µA |
| | | | $V_{CC}$ = 3.0V | | 132 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 223 | | |
| | | | $V_{CC}$ = 3.0V | | 476 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 400 | 600 | |
| | | | $V_{CC}$ = 3.0V | | 0.8 | 1.4 | mA |
| | | 32MHz, Ext. Clk | | | 8.2 | 12 | |
| | Idle power consumption [1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 2.4 | | µA |
| | | | $V_{CC}$ = 3.0V | | 3.5 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 57 | | |
| | | | $V_{CC}$ = 3.0V | | 110 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 115 | 225 | |
| | | | $V_{CC}$ = 3.0V | | 216 | 350 | |
| | | 32MHz, Ext. Clk | | | 3.5 | 5.5 | mA |
| | Power-down power consumption | T = 25°C | $V_{CC}$ = 3.0V | | 0.1 | 1.0 | µA |
| | | T = 85°C | | | 1.2 | 4.5 | |
| | | T = 105°C | | | 2.4 | 6.0 | |
| | | WDT and Sampled BOD enabled, T = 25°C | $V_{CC}$ = 3.0V | | 1.4 | 3.0 | |
| | | WDT and Sampled BOD enabled, T = 85°C | | | 2.4 | 6.0 | |
| | | WDT and Sampled BOD enabled, T = 105°C | | | 3.5 | 8.0 | |
| | Power-save power consumption [2] | RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C | $V_{CC}$ = 1.8V | | 1.2 | | µA |
| | | | $V_{CC}$ = 3.0V | | 1.5 | | |
| | | RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.6 | 2.0 | |
| | | | $V_{CC}$ = 3.0V | | 0.7 | 2.0 | |
| | | RTC from low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.8 | 3.0 | |
| | | | $V_{CC}$ = 3.0V | | 1.0 | 3.0 | |
| | Reset power consumption | Current through $\overline{\text{RESET}}$ pin substracted | $V_{CC}$ = 3.0V | | 140 | | |

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

**Table 36-69. Current consumption for modules and peripherals.**

| Symbol | Parameter | Condition [1] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | ULP oscillator | | | | 1.0 | | µA |
| | 32.768kHz int. oscillator | | | | 29 | | µA |
| | 2MHz int. oscillator | | | | 85 | | µA |
| | | DFLL enabled with 32.768kHz int. osc. as reference | | | 120 | | |
| | 32MHz int. oscillator | | | | 300 | | µA |
| | | DFLL enabled with 32.768kHz int. osc. as reference | | | 465 | | |
| | PLL | 20x multiplication factor,<br>32MHz int. osc. DIV4 as reference | | | 320 | | µA |
| | Watchdog timer | | | | 1.0 | | µA |
| | BOD | Continuous mode | | | 138 | | µA |
| | | Sampled mode, includes ULP oscillator | | | 1.0 | | |
| | Internal 1.0V reference | | | | 103 | | µA |
| | Temperature sensor | | | | 100 | | µA |
| | ADC | 250ksps<br>$V_{REF}$ = Ext ref | | | 3.0 | | mA |
| | | | CURRLIMIT = LOW | | 2.6 | | |
| | | | CURRLIMIT = MEDIUM | | 2.1 | | |
| | | | CURRLIMIT = HIGH | | 1.6 | | |
| | DAC | 250ksps<br>$V_{REF}$ = Ext ref<br>No load | Normal mode | | 1.9 | | mA |
| | | | Low power mode | | 1.1 | | |
| | AC | High speed mode | | | 330 | | µA |
| | | Low pPower mode | | | 130 | | |
| | DMA | 615KBps between I/O registers and SRAM | | | 108 | | µA |
| | Timer/counter | | | | 16 | | µA |
| | USART | Rx and Tx enabled, 9600 BAUD | | | 2.5 | | µA |
| | Flash memory and EEPROM programming | | | | 8.0 | | mA |

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at $V_{CC}$ = 3.0V, $Clk_{SYS}$ = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

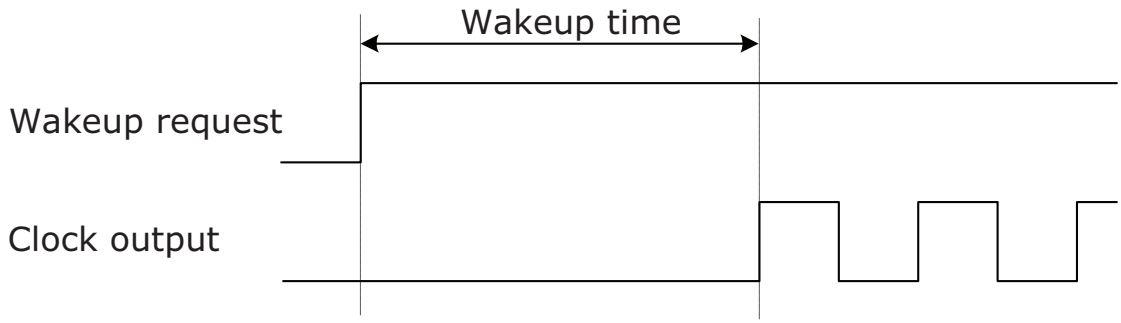
### 36.3.4 Wake-up time from sleep modes

**Table 36-70. Device wake-up time from sleep modes with various system clock sources.**

| Symbol | Parameter | Condition | Min. | Typ. [1] | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{wakeup}$ | Wake-up time from idle, standby, and extended standby mode | External 2MHz clock | | 2.0 | | µs |
| | | 32.768kHz internal oscillator | | 120 | | |
| | | 2MHz internal oscillator | | 2.0 | | |
| | | 32MHz internal oscillator | | 0.2 | | |
| | Wake-up time from power-save and power-down mode | External 2MHz clock | | 4.5 | | µs |
| | | 32.768kHz internal oscillator | | 320 | | |
| | | 2MHz internal oscillator | | 9.0 | | |
| | | 32MHz internal oscillator | | 4.0 | | |

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-16. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

**Figure 36-16.Wake-up time definition.**



### 36.3.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

**Table 36-71. I/O pin characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ (1)/ $I_{OL}$ (2) | I/O pin source/sink current | | | -20 | | 20 | mA |
| $V_{IH}$ | High level input voltage | $V_{CC}$ = 2.7- 3.6V | | 2.0 | | $V_{CC}$+0.3 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | 0.7*$V_{CC}$ | | $V_{CC}$+0.3 | |
| | | $V_{CC}$ = 1.6 - 2.0V | | 0.8*$V_{CC}$ | | $V_{CC}$+0.3 | |
| $V_{IL}$ | Low level input voltage | $V_{CC}$ = 2.7- 3.6V | | -0.3 | | 0.8 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | -0.3 | | 0.3*$V_{CC}$ | |
| | | $V_{CC}$ = 1.6 - 2.0V | | -0.3 | | 0.2*$V_{CC}$ | |
| $V_{OH}$ | High level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OH}$ = -2mA | 2.4 | 0.94*$V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OH}$ = -1mA | 2.0 | 0.96*$V_{CC}$ | | |
| | | | $I_{OH}$ = -2mA | 1.7 | 0.92*$V_{CC}$ | | |
| | | $V_{CC}$ = 3.3V | $I_{OH}$ = -8mA | 2.6 | 2.9 | | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = -6mA | 2.1 | 2.6 | | |
| | | $V_{CC}$ = 1.8V | $I_{OH}$ = -2mA | 1.4 | 1.6 | | |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OL}$ = 2mA | | 0.02*$V_{CC}$ | 0.4 | V |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OL}$ = 1mA | | 0.01*$V_{CC}$ | 0.4 | |
| | | | $I_{OL}$ = 2mA | | 0.02*$V_{CC}$ | 0.7 | |
| | | $V_{CC}$ = 3.3V | $I_{OL}$ = 15mA | | 0.4 | 0.76 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 10mA | | 0.3 | 0.64 | |
| | | $V_{CC}$ = 1.8V | $I_{OL}$ = 5mA | | 0.2 | 0.46 | |
| $I_{IN}$ | Input leakage current | T = 25°C | | | <0.01 | 0.1 | µA |
| | | XOSC and TOSC pins | | | <0.02 | 1.1 | |
| $R_P$ | Pull/buss keeper resistor | | | | 24 | | kΩ |
| $t_r$ | Rise time | No load | | | 4.0 | | ns |
| | | | slew rate limitation | | 7.0 | | |

Notes:
1. The sum of all $I_{OH}$ for PORTA and PORTB must not exceed 100mA.
The sum of all $I_{OH}$ for PORTC must not exceed 200mA.
The sum of all $I_{OH}$ for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
The sum of all $I_{OH}$ for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.
2. The sum of all $I_{OL}$ for PORTA and PORTB must not exceed 100mA.
The sum of all $I_{OL}$ for PORTC must not exceed 200mA.
The sum of all $I_{OL}$ for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
The sum of all $I_{OL}$ for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.

### 36.3.6 ADC characteristics

**Table 36-72. Power supply, reference and input range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $V_{REF}$ | Reference voltage | | 1.0 | | $AV_{CC}$- 0.6 | V |
| $R_{in}$ | Input resistance | Switched | | 4.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched | | 4.4 | | pF |
| $R_{AREF}$ | Reference input resistance | (leakage only) | | >10 | | MΩ |
| $C_{AREF}$ | Reference input capacitance | Static load | | 7.0 | | pF |
| $V_{IN}$ | Input range | | -0.1 | | $AV_{CC}$+0.1 | V |
| | Conversion range | Differential mode, Vinp - Vinn | $-V_{REF}$ | | $V_{REF}$ | V |
| | Conversion range | Single ended unsigned mode, Vinp | -ΔV | | $V_{REF}$-ΔV | V |
| ΔV | Fixed offset voltage | | | 190 | | lsb |

**Table 36-73. Clock and timing.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{ADC}$ | ADC clock frequency | Maximum is 1/4 of peripheral clock frequency | 100 | | 2000 | kHz |
| | | Measuring internal signals | 100 | | 125 | |
| $f_{ADC}$ | Sample rate | Current limitation (CURRLIMIT) off | 100 | | 2000 | ksps |
| | | CURRLIMIT = LOW | 100 | | 1500 | |
| | | CURRLIMIT = MEDIUM | 100 | | 1000 | |
| | | CURRLIMIT = HIGH | 100 | | 500 | |
| | Sampling time | 1/2 $Clk_{ADC}$ cycle | 0.25 | | 5 | µs |
| | Conversion time (latency) | (RES+2)/2+(GAIN !=0)<br>RES (Resolution) = 8 or 12 | 5 | | 8 | $Clk_{ADC}$ cycles |
| | Start-up time | ADC clock cycles | | 12 | 24 | $Clk_{ADC}$ cycles |
| | ADC settling time | After changing reference or input mode | | 7 | 7 | $Clk_{ADC}$ cycles |
| | | After ADC flush | | 1 | 1 | |

**Table 36-74. Accuracy characteristics.**

| Symbol | Parameter | Condition [2] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Resolution | Programmable to 8 or 12 bit | | 8 | 12 | 12 | Bits |
| INL [1] | Integral non-linearity | 500ksps | $V_{CC}$-1.0V < $V_{REF}$< $V_{CC}$-0.6V | | ±1.2 | ±2 | lsb |
| | | | All $V_{REF}$ | | ±1.5 | ±3 | |
| | | 2000ksps | $V_{CC}$-1.0V < $V_{REF}$< $V_{CC}$-0.6V | | ±1.0 | ±2 | |
| | | | All $V_{REF}$ | | ±1.5 | ±3 | |
| DNL [1] | Differential non-linearity | guaranteed monotonic | | | <±0.8 | <±1 | lsb |
| | Offset error | | | | -1 | | mV |
| | | Temperature drift | | | <0.01 | | mV/K |
| | | Operating voltage drift | | | <0.6 | | mV/V |
| | Gain error | Differential mode | External reference | | -1 | | mV |
| | | | $AV_{CC}$/1.6 | | 10 | | |
| | | | $AV_{CC}$/2.0 | | 8 | | |
| | | | Bandgap | | ±5 | | |
| | | Temperature drift | | | <0.02 | | mV/K |
| | | Operating voltage drift | | | <0.5 | | mV/V |
| | Noise | Differential mode, shorted input 2msps, $V_{CC}$ = 3.6V, $Clk_{PER}$ = 16MHz | | | 0.4 | | mV rms |

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external $V_{REF}$ is used.

**Table 36-75. Gain stage characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $R_{in}$ | Input resistance | Switched in normal mode | | | 4.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched in normal mode | | | 4.4 | | pF |
| | Signal range | Gain stage output | | 0 | | $V_{CC}$- 0.6 | V |
| | Propagation delay | ADC conversion rate | | | 1.0 | | $Clk_{ADC}$ cycles |
| | Sample rate | Same as ADC | | 100 | | 1000 | kHz |
| INL [1] | Integral non-linearity | 500ksps | All gain settings | | ±1.5 | ±4.0 | lsb |
| | Gain error | 1x gain, normal mode | | | -0.8 | | % |
| | | 8x gain, normal mode | | | -2.5 | | |
| | | 64x gain, normal mode | | | -3.5 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Offset error, input referred | 1x gain, normal mode | | | -2 | | mV |
| | | 8x gain, normal mode | | | -5 | | |
| | | 64x gain, normal mode | | | -4 | | |
| | Noise | 1x gain, normal mode | $V_{CC}$ = 3.6V Ext. $V_{REF}$ | | 0.5 | | mV rms |
| | | 8x gain, normal mode | | | 1.5 | | |
| | | 64x gain, normal mode | | | 11 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

### 36.3.7 DAC Characteristics

**Table 36-76. Power supply, reference and output range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $AV_{REF}$ | External reference voltage | | 1.0 | | $V_{CC}$- 0.6 | V |
| $R_{channel}$ | DC output impedance | | | | 50 | Ω |
| | Linear output voltage range | | 0.15 | | $AV_{CC}$-0.15 | V |
| $R_{AREF}$ | Reference input resistance | | | >10 | | MΩ |
| CAREF | Reference input capacitance | Static load | | 7 | | pF |
| | Minimum resistance load | | 1.0 | | | kΩ |
| | Maximum capacitance load | | | | 100 | pF |
| | | 1000Ω serial resistance | | | 1.0 | nF |
| | Output sink/source | Operating within accuracy specification | | | $AV_{CC}$/1000 | mA |
| | | Safe operation | | | 10 | |

**Table 36-77. Clock and timing.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{DAC}$ | Conversion rate | $C_{load}$=100pF, maximum step size | Normal mode | 0 | | 1000 | ksps |
| | | | Low power mode | | | 500 | |

**Table 36-78. Accuracy characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Input resolution | | | | | 12 | Bits |
| INL [(1)] | Integral non-linearity | $V_{REF}$= Ext 1.0V | $V_{CC}$ = 1.6V | | ±2.0 | ±3.0 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±2.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±2.0 | ±4.0 | |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±4.0 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±5.0 | | |
| | | | $V_{CC}$ = 3.6V | | ±5.0 | | |
| DNL [(1)] | Differential non-linearity | $V_{REF}$=Ext 1.0V | $V_{CC}$ = 1.6V | | ±1.5 | 3.0 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±1.0 | 3.5 | |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±4.5 | | |
| | | | $V_{CC}$ = 3.6V | | ±4.5 | | |
| | Gain error | After calibration | | | <4.0 | | lsb |
| | Gain calibration step size | | | | 4.0 | | lsb |
| | Gain calibration drift | $V_{REF}$= Ext 1.0V | | | <0.2 | | mV/K |
| | Offset error | After calibration | | | <1.0 | | lsb |
| | Offset calibration step size | | | | 1.0 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

### 36.3.8 Analog Comparator Characteristics

**Table 36-79. Analog Comparator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{off}$ | Input offset voltage | | | <±10 | | mV |
| $I_{lk}$ | Input leakage current | | | <1 | | nA |
| | Input voltage range | | -0.1 | | $AV_{CC}$ | V |
| | AC startup time | | | 100 | | µs |
| $V_{hys1}$ | Hysteresis, none | | | 0 | | mV |
| $V_{hys2}$ | Hysteresis, small | mode = High Speed (HS) | | 20 | | mV |
| | | mode = Low Power (LP) | | 30 | | |
| $V_{hys3}$ | Hysteresis, large | mode = HS | | 35 | | mV |
| | | mode = LP | | 60 | | |
| $t_{delay}$ | Propagation delay | $V_{CC}$ = 3.0V, T= 85°C, mode = HS | | 30 | 90 | ns |
| | | mode = HS | | 30 | | |
| | | $V_{CC}$ = 3.0V, T= 85°C, mode = LP | | 130 | 500 | |
| | | mode = LP | | 130 | | |
| | 64-level voltage scaler | Integral non-linearity (INL) | | 0.3 | 0.5 | lsb |

### 36.3.9 Bandgap and Internal 1.0V Reference Characteristics

**Table 36-80. Bandgap and Internal 1.0V reference characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Startup time | As reference for ADC or DAC | 1 $Clk_{PER}$ + 2.5µs | | | µs |
| | | As input voltage to ADC and AC | | 1.5 | | |
| | Bandgap voltage | | | 1.1 | | V |
| INT1V | Internal 1.00V reference | T= 85°C, after calibration | 0.99 | 1 | 1.01 | V |
| | Variation over voltage and temperature | Relative to T= 85°C, $V_{CC}$ = 3.0V | | ±1.5 | | % |

### 36.3.10 Brownout Detection Characteristics

**Table 36-81. Brownout detection characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{BOT}$ | BOD level 0 falling $V_{CC}$ | | 1.50 | 1.62 | 1.72 | V |
| | BOD level 1 falling $V_{CC}$ | | | 1.8 | | |
| | BOD level 2 falling $V_{CC}$ | | | 2.0 | | |
| | BOD level 3 falling $V_{CC}$ | | | 2.2 | | |
| | BOD level 4 falling $V_{CC}$ | | | 2.4 | | |
| | BOD level 5 falling $V_{CC}$ | | | 2.6 | | |
| | BOD level 6 falling $V_{CC}$ | | | 2.8 | | |
| | BOD level 7 falling $V_{CC}$ | | | 3.0 | | |
| $t_{BOD}$ | Detection time | Continuous mode | | 0.4 | | µs |
| | | Sampled mode | | 1000 | | |
| $V_{HYST}$ | Hysteresis | | | 1.2 | | % |

### 36.3.11 External Reset Characteristics

**Table 36-82. External reset characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{EXT}$ | Minimum reset pulse width | | 1000 | 95 | | ns |
| $V_{RST}$ | Reset threshold voltage ($V_{IH}$) | $V_{CC}$ = 2.7 - 3.6V | | 0.60×$V_{CC}$ | | V |
| | | $V_{CC}$ = 1.6 - 2.7V | | 0.60×$V_{CC}$ | | |
| | Reset threshold voltage ($V_{IL}$) | $V_{CC}$ = 2.7 - 3.6V | | 0.50×$V_{CC}$ | | |
| | | $V_{CC}$ = 1.6 - 2.7V | | 0.40×$V_{CC}$ | | |
| $R_{RST}$ | Reset pin Pull-up Resistor | | | 25 | | kΩ |

### 36.3.12 Power-on Reset Characteristics

**Table 36-83. Power-on reset characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{POT-}$ [1] | POR threshold voltage falling $V_{CC}$ | $V_{CC}$ falls faster than 1V/ms | 0.4 | 1.0 | | V |
| | | $V_{CC}$ falls at 1V/ms or slower | 0.8 | 1.0 | | |
| $V_{POT+}$ | POR threshold voltage rising $V_{CC}$ | | | 1.3 | 1.59 | |

Note: 1. $V_{POT-}$ values are only valid when BOD is disabled. When BOD is enabled $V_{POT-}$ = $V_{POT+}$.

### 36.3.13 Flash and EEPROM Memory Characteristics

**Table 36-84. Endurance and data retention.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Flash | Write/Erase cycles | 25°C | 10K | | | Cycle |
| | | | 85°C | 10K | | | |
| | | | 105°C | 2K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 85°C | 25 | | | |
| | | | 105°C | 10 | | | |
| | EEPROM | Write/Erase cycles | 25°C | 100K | | | Cycle |
| | | | 85°C | 100K | | | |
| | | | 105°C | 30K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 85°C | 25 | | | |
| | | | 105°C | 10 | | | |

**Table 36-85. Programming time.**

| Symbol | Parameter | Condition | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| | Chip Erase | 64KB Flash, EEPROM[2] and SRAM Erase | | 55 | | ms |
| | Application Erase | Section erase | | 6 | | ms |
| | Flash | Page erase | | 4 | | ms |
| | | Page write | | 4 | | |
| | | Atomic page erase and write | | 8 | | |
| | EEPROM | Page erase | | 4 | | ms |
| | | Page write | | 4 | | |
| | | Atomic page erase and write | | 8 | | |

Notes:
1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

### 36.3.14 Clock and Oscillator Characteristics

#### 36.3.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

**Table 36-86. 32.768kHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency | | | 32.768 | | kHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$ = 3.0V | -0.5 | | 0.5 | % |
| | User calibration accuracy | | -0.5 | | 0.5 | % |

#### 36.3.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

**Table 36-87. 2MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 1.8 | | 2.2 | MHz |
| | Factory calibrated frequency | | | 2.0 | | MHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | % |
| | DFLL calibration stepsize | | | 0.21 | | % |

#### 36.3.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

**Table 36-88. 32MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 30 | | 55 | MHz |
| | Factory calibrated frequency | | | 32 | | MHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | % |
| | DFLL calibration step size | | | 0.22 | | % |

### 36.3.14.4 32kHz Internal ULP Oscillator characteristics

**Table 36-89. 32kHz internal ULP oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Factory calibrated frequency | | | 32 | | kHz |
| | Factory calibrated accuracy | T = 85°C, $V_{CC}$ = 3.0V | -12 | | 12 | % |
| | Accuracy | | -30 | | 30 | % |

### 36.3.14.5 Internal Phase Locked Loop (PLL) characteristics

**Table 36-90. Internal PLL characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input frequency | Output frequency must be within $f_{OUT}$ | 0.4 | | 64 | MHz |
| $f_{OUT}$ | Output frequency (1) | $V_{CC}$= 1.6 - 1.8V | 20 | | 48 | MHz |
| | | $V_{CC}$= 2.7 - 3.6V | 20 | | 128 | |
| | Start-up time | | | 25 | | µs |
| | Re-lock time | | | 25 | | µs |

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

### 36.3.14.6 External clock characteristics

**Figure 36-17. External clock drive waveform**

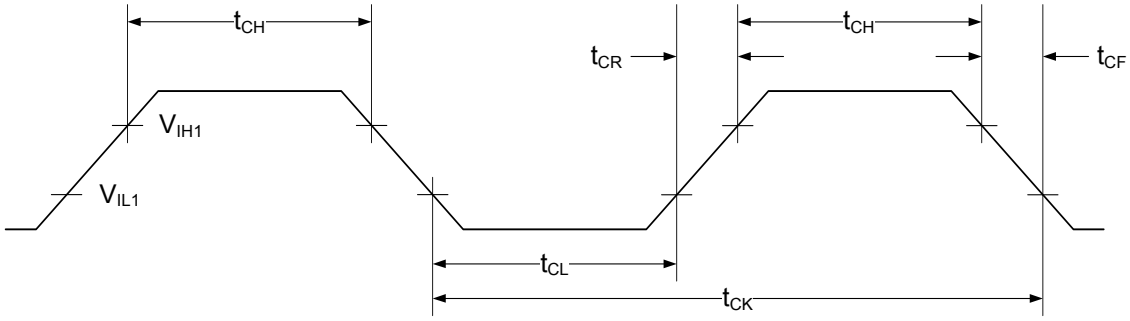



**Table 36-91. External clock used as system clock without prescaling.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock Frequency (1) | $V_{CC}$ = 1.6 - 1.8V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 32 | |
| $t_{CK}$ | Clock Period | $V_{CC}$ = 1.6 - 1.8V | 83.3 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 31.5 | | | |
| $t_{CH}$ | Clock High Time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

**Table 36-92. External clock with prescaler [(1)] for system clock.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock Frequency [(2)] | $V_{CC}$ = 1.6 - 1.8V | 0 | | 90 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 142 | |
| $t_{CK}$ | Clock Period | $V_{CC}$ = 1.6 - 1.8V | 11 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 7 | | | |
| $t_{CH}$ | Clock High Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

### 36.3.14.7 External 16MHz crystal oscillator and XOSC characteristic

**Table 36-93. External 16MHz crystal oscillator and XOSC characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Cycle to cycle jitter | XOSCPWR=0 | FRQRANGE=0 | | <10 | | ns |
| | | | FRQRANGE=1, 2, or 3 | | <1 | | |
| | | XOSCPWR=1 | | | <1 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Long term jitter | XOSCPWR=0 | FRQRANGE=0 | | <6 | | ns |
| | | | FRQRANGE=1, 2, or 3 | | <0.5 | | |
| | | XOSCPWR=1 | | | <0.5 | | |
| | Frequency error | XOSCPWR=0 | FRQRANGE=0 | | <0.1 | | % |
| | | | FRQRANGE=1 | | <0.05 | | |
| | | | FRQRANGE=2 or 3 | | <0.005 | | |
| | | XOSCPWR=1 | | | <0.005 | | |
| | Duty cycle | XOSCPWR=0 | FRQRANGE=0 | | 40 | | % |
| | | | FRQRANGE=1 | | 42 | | |
| | | | FRQRANGE=2 or 3 | | 45 | | |
| | | XOSCPWR=1 | | | 48 | | |
| $R_Q$ | Negative impedance [1] | XOSCPWR=0, FRQRANGE=0 | 0.4MHz resonator, CL=100pF | 2.4k | | | Ω |
| | | | 1MHz crystal, CL=20pF | 8.7k | | | |
| | | | 2MHz crystal, CL=20pF | 2.1k | | | |
| | | XOSCPWR=0, FRQRANGE=1, CL=20pF | 2MHz crystal | 4.2k | | | |
| | | | 8MHz crystal | 250 | | | |
| | | | 9MHz crystal | 195 | | | |
| | | XOSCPWR=0, FRQRANGE=2, CL=20pF | 8MHz crystal | 360 | | | |
| | | | 9MHz crystal | 285 | | | |
| | | | 12MHz crystal | 155 | | | |
| | | XOSCPWR=0, FRQRANGE=3, CL=20pF | 9MHz crystal | 365 | | | |
| | | | 12MHz crystal | 200 | | | |
| | | | 16MHz crystal | 105 | | | |
| | | XOSCPWR=1, FRQRANGE=0, CL=20pF | 9MHz crystal | 435 | | | |
| | | | 12MHz crystal | 235 | | | |
| | | | 16MHz crystal | 125 | | | |
| | | XOSCPWR=1, FRQRANGE=1, CL=20pF | 9MHz crystal | 495 | | | |
| | | | 12MHz crystal | 270 | | | |
| | | | 16MHz crystal | 145 | | | |
| | | XOSCPWR=1, FRQRANGE=2, CL=20pF | 12MHz crystal | 305 | | | |
| | | | 16MHz crystal | 160 | | | |
| | | XOSCPWR=1, FRQRANGE=3, CL=20pF | 12MHz crystal | 380 | | | |
| | | | 16MHz crystal | 205 | | | |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | ESR | SF = Safety factor | | | min($R_Q$)/SF | kΩ |
| $C_{XTAL1}$ | Parasitic capacitance XTAL1 pin | | | 5.60 | | pF |
| $C_{XTAL2}$ | Parasitic capacitance XTAL2 pin | | | 7.62 | | pF |
| $C_{LOAD}$ | Parasitic capacitance load | | | 3.23 | | pF |

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization

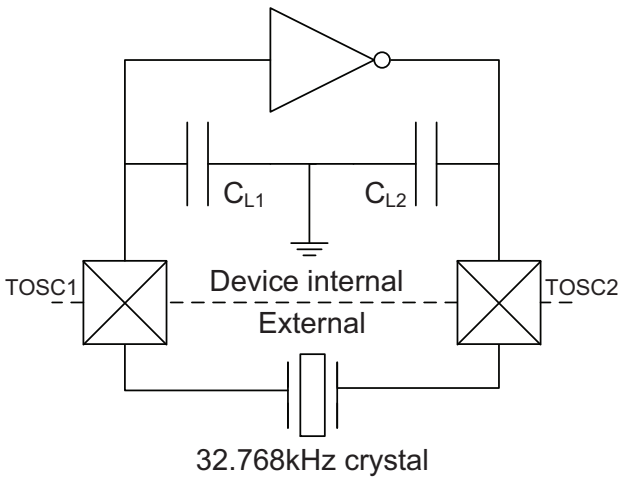
### 36.3.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

**Table 36-94. External 32.768kHz crystal oscillator and TOSC characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ESR/R1 | Recommended crystal equivalent series resistance (ESR) | Crystal load capacitance 6.5pF | | | 60 | kΩ |
| | | Crystal load capacitance 9.0pF | | | 35 | |
| $C_{TOSC1}$ | Parasitic capacitance TOSC1 pin | | | 5.4 | | pF |
| | | Alternate TOSC location | | 4.0 | | |
| $C_{TOSC2}$ | Parasitic capacitance TOSC2 pin | | | 7.1 | | pF |
| | | Alternate TOSC location | | 4.0 | | |
| | Recommended safety factor | capacitance load matched to crystal specification | 3 | | | |

Note: 1. See Figure 36-18 for definition.

**Figure 36-18. TOSC input capacitance.**




The parasitic capacitance between the TOSC pins is $C_{L1}$ + $C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

### 36.3.15 SPI Characteristics

**Figure 36-19.SPI timing requirements in master mode.**

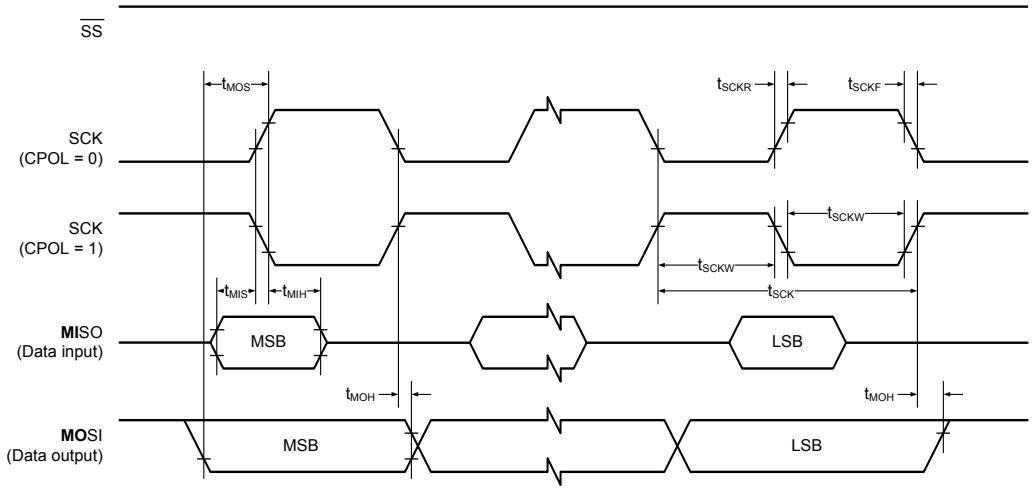



**Figure 36-20.SPI timing requirements in slave mode.**

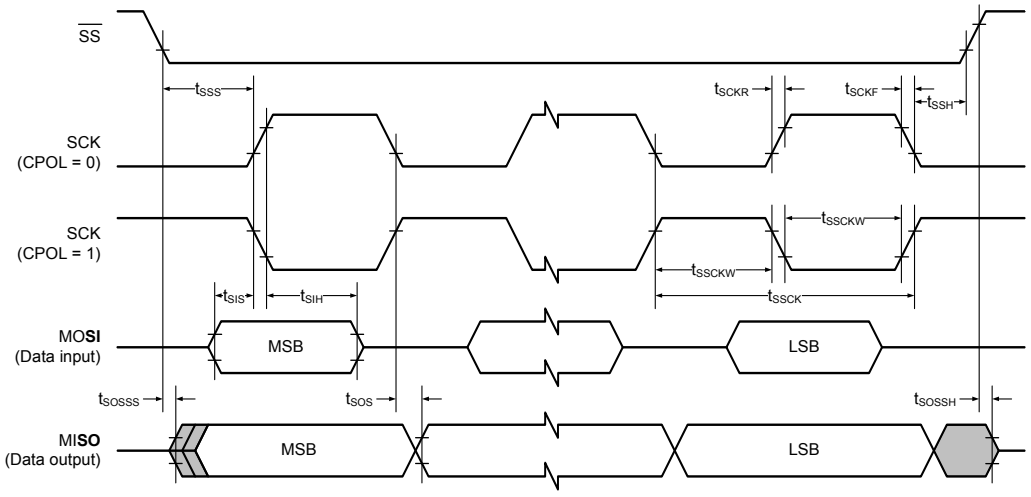


**Table 36-95. SPI timing characteristics and requirements.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{SCK}$ | SCK period | Master | | (See Table 21-4 in XMEGA AU Manual) | | ns |
| $t_{SCKW}$ | SCK high/low width | Master | | 0.5*SCK | | |
| $t_{SCKR}$ | SCK rise time | Master | | 2.7 | | |
| $t_{SCKF}$ | SCK fall time | Master | | 2.7 | | |
| $t_{MIS}$ | MISO setup to SCK | Master | | 11 | | |
| $t_{MIH}$ | MISO hold after SCK | Master | | 0 | | |
| $t_{MOS}$ | MOSI setup SCK | Master | | 0.5*SCK | | |
| $t_{MOH}$ | MOSI hold after SCK | Master | | 1.0 | | |
| $t_{SSCK}$ | Slave SCK Period | Slave | 4*t $Clk_{PER}$ | | | |
| $t_{SSCKW}$ | SCK high/low width | Slave | 2*t $Clk_{PER}$ | | | |
| $t_{SSCKR}$ | SCK rise time | Slave | | | 1600 | |
| $t_{SSCKF}$ | SCK fall time | Slave | | | 1600 | |
| $t_{SIS}$ | MOSI setup to SCK | Slave | 3.0 | | | |
| $t_{SIH}$ | MOSI hold after SCK | Slave | $t_{PER}$ | | | |
| $t_{SSS}$ | $\overline{SS}$ setup to SCK | Slave | 20 | | | |
| $t_{SSH}$ | $\overline{SS}$ hold after SCK | Slave | 20 | | | |
| $t_{SOS}$ | MISO setup SCK | Slave | | 8.0 | | |
| $t_{SOH}$ | MISO hold after SCK | Slave | | 13.0 | | |
| $t_{SOSS}$ | MISO setup after $\overline{SS}$ low | Slave | | 11.0 | | |
| $t_{SOSH}$ | MISO hold after $\overline{SS}$ high | Slave | | 8.0 | | |

### 36.3.16 Two-Wire Interface Characteristics

Table 36-96 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-21.

**Figure 36-21.Two-wire interface bus timing.**

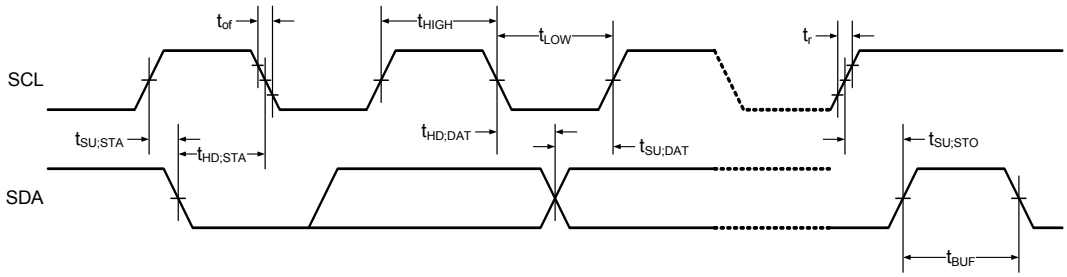



**Table 36-96. Two-wire interface characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | | $0.7*V_{CC}$ | | $V_{CC}+0.5$ | V |
| $V_{IL}$ | Input low voltage | | -0.5 | | $0.3*V_{CC}$ | V |
| $V_{hys}$ | Hysteresis of Schmitt trigger inputs | | $0.05*V_{CC}$ (1) | | 0 | V |
| $V_{OL}$ | Output low voltage | 3mA, sink current | 0 | | 0.4 | V |
| $t_r$ | Rise time for both SDA and SCL | | $20+0.1C_b$ (1)(2) | | 0 | ns |
| $t_{of}$ | Output fall time from $V_{IHmin}$ to $V_{ILmax}$ | $10pF < C_b < 400pF$ (2) | $20+0.1C_b$ (1)(2) | | 300 | ns |
| $t_{SP}$ | Spikes suppressed by input filter | | 0 | | 50 | ns |
| $I_I$ | Input current for each I/O pin | $0.1V_{CC} < V_I < 0.9V_{CC}$ | -10 | | 10 | µA |
| $C_I$ | Capacitance for each I/O pin | | 0 | | 10 | pF |
| $f_{SCL}$ | SCL clock frequency | $f_{PER}$ (3)>max($10f_{SCL}$, 250kHz) | 0 | | 400 | kHz |
| $R_P$ | Value of pull-up resistor | $f_{SCL} \leq 100kHz$ | $\frac{V_{CC}-0.4V}{3mA}$ | | $\frac{100ns}{C_b}$ | Ω |
| | | $f_{SCL} > 100kHz$ | | | $\frac{300ns}{C_b}$ | |
| $t_{HD;STA}$ | Hold time (repeated) START condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{LOW}$ | Low period of SCL clock | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |
| $t_{HIGH}$ | High period of SCL clock | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{HD;DAT}$ | Data hold time | $f_{SCL} \leq 100kHz$ | 0 | | 3.45 | µs |
| | | $f_{SCL} > 100kHz$ | 0 | | 0.9 | |
| $t_{SU;DAT}$ | Data setup time | $f_{SCL} \leq 100kHz$ | 250 | | | ns |
| | | $f_{SCL} > 100kHz$ | 100 | | | |
| $t_{SU;STO}$ | Setup time for STOP condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{BUF}$ | Bus free time between a STOP and START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. $C_b$ = Capacitance of one bus line in pF.
3. $f_{PER}$ = Peripheral clock frequency.

## 36.4 ATxmega128A4U

### 36.4.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-97 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 36-97. Absolute maximum ratings.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | -0.3 | | 4 | V |
| $I_{VCC}$ | Current into a $V_{CC}$ pin | | | | 200 | mA |
| $I_{GND}$ | Current out of a Gnd pin | | | | 200 | mA |
| $V_{PIN}$ | Pin voltage with respect to Gnd and $V_{CC}$ | | -0.5 | | $V_{CC}$+0.5 | V |
| $I_{PIN}$ | I/O pin sink/source current | | -25 | | 25 | mA |
| $T_A$ | Storage temperature | | -65 | | 150 | °C |
| $T_j$ | Junction temperature | | | | 150 | °C |

### 36.4.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-98 in order for all other electrical characteristics and typical characteristics of the device to be valid.

**Table 36-98. General operating conditions.**

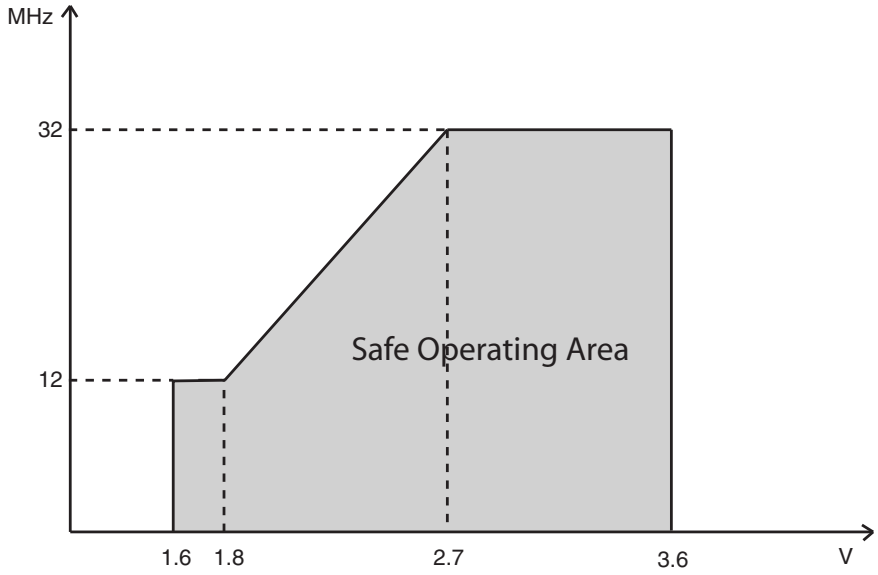
| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power supply voltage | | 1.60 | | 3.6 | V |
| $AV_{CC}$ | Analog supply voltage | | 1.60 | | 3.6 | V |
| $T_A$ | Temperature range | | -40 | | 85 | °C |
| $T_j$ | Junction temperature | | -40 | | 105 | °C |

**Table 36-99. Operating voltage and frequency.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{CPU}$ | CPU clock frequency | $V_{CC}$ = 1.6V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 1.8V | 0 | | 12 | |
| | | $V_{CC}$ = 2.7V | 0 | | 32 | |
| | | $V_{CC}$ = 3.6V | 0 | | 32 | |

The maximum CPU clock frequency depends on $V_{CC}$. As shown in Figure 36-22 the Frequency vs. $V_{CC}$ curve is linear between 1.8V < $V_{CC}$ < 2.7V.

**Figure 36-22.Maximum Frequency vs. $V_{CC}$.**



### 36.4.3 Current consumption

**Table 36-100.Current consumption for Active mode and sleep modes.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Active power consumption [1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 55 | | µA |
| | | | $V_{CC}$ = 3.0V | | 135 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 255 | | |
| | | | $V_{CC}$ = 3.0V | | 535 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 460 | 600 | |
| | | | $V_{CC}$ = 3.0V | | 1.0 | 1.4 | mA |
| | | 32MHz, Ext. Clk | | | 9.5 | 12 | |
| | Idle power consumption [1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 2.9 | | µA |
| | | | $V_{CC}$ = 3.0V | | 3.9 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 62 | | |
| | | | $V_{CC}$ = 3.0V | | 118 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 125 | 225 | |
| | | | $V_{CC}$ = 3.0V | | 240 | 350 | |
| | | 32MHz, Ext. Clk | | | 3.8 | 5.5 | mA |
| | Power-down power consumption | T = 25°C | $V_{CC}$ = 3.0V | | 0.1 | 1.0 | µA |
| | | T = 85°C | | | 1.5 | 4.5 | |
| | | T = 105°C | | | 0.1 | 8.6 | |
| | | WDT and Sampled BOD enabled, T = 25°C | $V_{CC}$ = 3.0V | | 1.4 | 3.0 | |
| | | WDT and Sampled BOD enabled, T = 85°C | | | 2.8 | 6.0 | |
| | | WDT and Sampled BOD enabled, T = 105°C | | | 1.4 | 8.8 | |
| | Power-save power consumption [2] | RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C | $V_{CC}$ = 1.8V | | 1.2 | | µA |
| | | | $V_{CC}$ = 3.0V | | 1.5 | | |
| | | RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.6 | 2.0 | |
| | | | $V_{CC}$ = 3.0V | | 0.7 | 2.0 | |
| | | RTC from low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.8 | 3.0 | |
| | | | $V_{CC}$ = 3.0V | | 1.0 | 3.0 | |
| | Reset power consumption | Current through $\overline{\text{RESET}}$ pin substracted | $V_{CC}$ = 3.0V | | 300 | | µA |

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

**Table 36-101.Current consumption for modules and peripherals.**

| Symbol | Parameter | Condition [1] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | ULP oscillator | | | | 1.0 | | µA |
| | 32.768kHz int. oscillator | | | | 29 | | µA |
| | 2MHz int. oscillator | | | | 85 | | µA |
| | | DFLL enabled with 32.768kHz int. osc. as reference | | | 115 | | |
| | 32MHz int. oscillator | | | | 270 | | µA |
| | | DFLL enabled with 32.768kHz int. osc. as reference | | | 440 | | |
| | PLL | 20x multiplication factor,<br>32MHz int. osc. DIV4 as reference | | | 320 | | µA |
| | Watchdog timer | | | | 1.0 | | µA |
| | BOD | Continuous mode | | | 138 | | µA |
| | | Sampled mode, includes ULP oscillator | | | 1.2 | | |
| | Internal 1.0V reference | | | | 260 | | µA |
| | Temperature sensor | | | | 250 | | µA |
| | ADC | 250ksps<br>$V_{REF}$ = Ext ref | | | 3.0 | | mA |
| | | | CURRLIMIT = LOW | | 2.6 | | |
| | | | CURRLIMIT = MEDIUM | | 2.1 | | |
| | | | CURRLIMIT = HIGH | | 1.6 | | |
| | DAC | 250ksps<br>$V_{REF}$ = Ext ref<br>No load | Normal mode | | 1.9 | | mA |
| | | | Low power mode | | 1.1 | | |
| | AC | High speed mode | | | 330 | | µA |
| | | Low power mode | | | 130 | | |
| | DMA | 615kbps between I/O registers and SRAM | | | 108 | | µA |
| | Timer/counter | | | | 16 | | µA |
| | USART | Rx and Tx enabled, 9600 BAUD | | | 2.5 | | µA |
| | Flash memory and EEPROM programming | | | | 4.0 | 8.0 | mA |

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at $V_{CC}$ = 3.0V, $Clk_{SYS}$ = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

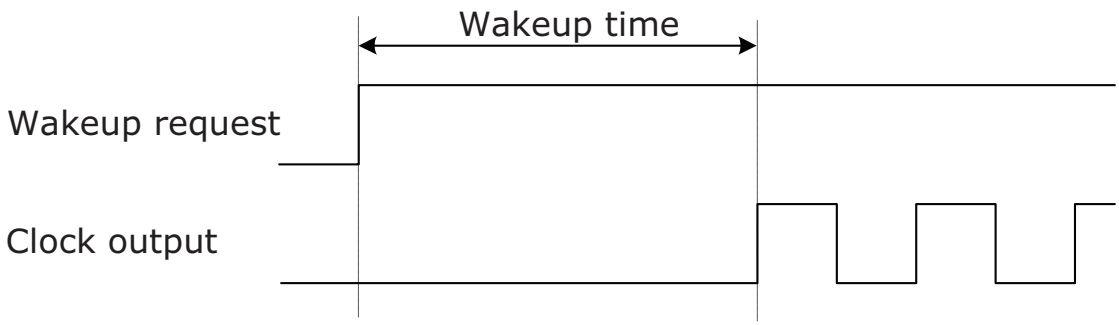
### 36.4.4 Wake-up time from sleep modes

**Table 36-102. Device wake-up time from sleep modes with various system clock sources.**

| Symbol | Parameter | Condition | Min. | Typ. [1] | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{wakeup}$ | Wake-up time from idle, standby, and extended standby mode | External 2MHz clock | | 2.0 | | µs |
| | | 32.768kHz internal oscillator | | 120 | | |
| | | 2MHz internal oscillator | | 2.0 | | |
| | | 32MHz internal oscillator | | 0.2 | | |
| | Wake-up time from power-save and power-down mode | External 2MHz clock | | 4.5 | | µs |
| | | 32.768kHz internal oscillator | | 320 | | |
| | | 2MHz internal oscillator | | 9.0 | | |
| | | 32MHz internal oscillator | | 5.0 | | |

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-23. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

**Figure 36-23.Wake-up time definition.**



### 36.4.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

**Table 36-103.I/O pin characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{OH}$ (1)/ $I_{OL}$ (2) | I/O pin source/sink current | | | -20 | | 20 | mA |
| $V_{IH}$ | High level input voltage | $V_{CC}$ = 2.7 - 3.6V | | 2.0 | | $V_{CC}$+0.3 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | 0.7*$V_{CC}$ | | $V_{CC}$+0.3 | |
| | | $V_{CC}$ = 1.6 - 2.0V | | 0.8*$V_{CC}$ | | $V_{CC}$+0.3 | |
| $V_{IL}$ | Low level input voltage | $V_{CC}$ = 2.7- 3.6V | | -0.3 | | 0.8 | V |
| | | $V_{CC}$ = 2.0 - 2.7V | | -0.3 | | 0.3*$V_{CC}$ | |
| | | $V_{CC}$ = 1.6 - 2.0V | | -0.3 | | 0.2*$V_{CC}$ | |
| $V_{OH}$ | High level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OH}$ = -2mA | 2.4 | 0.94*$V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OH}$ = -1mA | 2.0 | 0.96*$V_{CC}$ | | |
| | | | $I_{OH}$ = -2mA | 1.7 | 0.92*$V_{CC}$ | | |
| | | $V_{CC}$ = 3.3V | $I_{OH}$ = -8mA | 2.6 | 2.9 | | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = -6mA | 2.1 | 2.6 | | |
| | | $V_{CC}$ = 1.8V | $I_{OH}$ = -2mA | 1.4 | 1.6 | | |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = 3.0 - 3.6V | $I_{OL}$ = 2mA | | 0.05 | 0.4 | V |
| | | $V_{CC}$ = 2.3 - 2.7V | $I_{OL}$ = 1mA | | 0.03 | 0.4 | |
| | | | $I_{OL}$ = 2mA | | 0.06 | 0.7 | |
| | | $V_{CC}$ = 3.3V | $I_{OL}$ = 15mA | | 0.4 | 0.76 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 10mA | | 0.3 | 0.64 | |
| | | $V_{CC}$ = 1.8V | $I_{OL}$ = 5mA | | 0.2 | 0.46 | |
| $I_{IN}$ | Input leakage current | T = 25°C | | | <0.01 | 0.1 | µA |
| $R_P$ | Pull/buss keeper resistor | | | | 24 | | kΩ |
| $t_r$ | Rise time | No load | | | 4.0 | | ns |
| | | | slew rate limitation | | 7.0 | | |

Notes:
1. The sum of all $I_{OH}$ for PORTA and PORTB must not exceed 100mA.
   The sum of all $I_{OH}$ for PORTC must not exceed 200mA.
   The sum of all $I_{OH}$ for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
   The sum of all $I_{OH}$ for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.
2. The sum of all $I_{OL}$ for PORTA and PORTB must not exceed 100mA.
   The sum of all $I_{OL}$ for PORTC must not exceed 200mA.
   The sum of all $I_{OL}$ for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
   The sum of all $I_{OL}$ for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.

### 36.4.6 ADC characteristics

**Table 36-104.Power supply, reference and input range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | V |
| $V_{REF}$ | Reference voltage | | 1 | | $AV_{CC}$- 0.6 | V |
| $R_{in}$ | Input resistance | Switched | | 4.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched | | 4.4 | | pF |
| $R_{AREF}$ | Reference input resistance | (leakage only) | | >10 | | MΩ |
| $C_{AREF}$ | Reference input capacitance | Static load | | 7 | | pF |
| $V_{IN}$ | Input range | | -0.1 | | $AV_{CC}$+0.1 | V |
| | Conversion range | Differential mode, Vinp - Vinn | $-V_{REF}$ | | $V_{REF}$ | V |
| | Conversion range | Single ended unsigned mode, Vinp | -ΔV | | $V_{REF}$-ΔV | V |
| ΔV | Fixed offset voltage | | | 190 | | lsb |

**Table 36-105.Clock and timing.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $Clk_{ADC}$ | ADC Clock frequency | Maximum is 1/4 of Peripheral clock frequency | 100 | | 2000 | kHz |
| | | Measuring internal signals | 100 | | 125 | |
| $f_{ADC}$ | Sample rate | Current limitation (CURRLIMIT) off | 100 | | 2000 | ksps |
| | | CURRLIMIT = LOW | 100 | | 1500 | |
| | | CURRLIMIT = MEDIUM | 100 | | 1000 | |
| | | CURRLIMIT = HIGH | 100 | | 500 | |
| | Sampling time | 1/2 $Clk_{ADC}$ cycle | 0.25 | | 5 | µs |
| | Conversion time (latency) | (RES+2)/2+(GAIN !=0)<br>RES (Resolution) = 8 or 12 | 5 | | 8 | $Clk_{ADC}$ cycles |
| | Start-up time | ADC clock cycles | | 12 | 24 | $Clk_{ADC}$ cycles |
| | ADC settling time | After changing reference or input mode | | 7 | 7 | $Clk_{ADC}$ cycles |
| | | After ADC flush | | 1 | 1 | |

**Table 36-106. Accuracy characteristics.**

| Symbol | Parameter | Condition [2] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Resolution | Programmable to 8 or 12 bit | | 8 | 12 | 12 | Bits |
| INL [1] | Integral non-linearity | 500ksps | $V_{CC}$-1.0V < $V_{REF}$< $V_{CC}$-0.6V | | ±1.2 | ±2 | lsb |
| | | | All $V_{REF}$ | | ±1.5 | ±3 | |
| | | 2000ksps | $V_{CC}$-1.0V < $V_{REF}$< $V_{CC}$-0.6V | | ±1.0 | ±2 | |
| | | | All $V_{REF}$ | | ±1.5 | ±3 | |
| DNL [1] | Differential non-linearity | guaranteed monotonic | | | <±0.8 | <±1 | lsb |
| | Offset error | | | | -1.0 | | mV |
| | | Temperature drift | | | <0.01 | | mV/K |
| | | Operating voltage drift | | | <0.6 | | mV/V |
| | Gain error | Differential mode | External reference | | -1 | | mV |
| | | | $AV_{CC}$/1.6 | | 10 | | |
| | | | $AV_{CC}$/2.0 | | 8.0 | | |
| | | | Bandgap | | ±5 | | |
| | | Temperature drift | | | <0.02 | | mV/K |
| | | Operating voltage drift | | | <0.5 | | mV/V |
| | Noise | Differential mode, shorted input 2msps, $V_{CC}$ = 3.6V, $Clk_{PER}$ = 16MHz | | | 0.4 | | mV rms |

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external $V_{REF}$ is used.

**Table 36-107. Gain stage characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $R_{in}$ | Input resistance | Switched in normal mode | | | 4.0 | | kΩ |
| $C_{sample}$ | Input capacitance | Switched in normal mode | | | 4.4 | | pF |
| | Signal range | Gain stage output | | 0 | | $V_{CC}$- 0.6 | V |
| | Propagation delay | ADC conversion rate | | | 1.0 | | $Clk_{ADC}$ cycles |
| | Sample rate | Same as ADC | | 100 | | 1000 | kHz |
| INL [1] | Integral Non-Linearity | 500ksps | All gain settings | | ±1.5 | ±4.0 | lsb |
| | Gain error | 1x gain, normal mode | | | -0.8 | | % |
| | | 8x gain, normal mode | | | -2.5 | | |
| | | 64x gain, normal mode | | | -3.5 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Offset error, input referred | 1x gain, normal mode | | | -2.0 | | mV |
| | | 8x gain, normal mode | | | -5.0 | | |
| | | 64x gain, normal mode | | | -4.0 | | |
| | Noise | 1x gain, normal mode | $V_{CC}$ = 3.6V Ext. $V_{REF}$ | | 0.5 | | mV rms |
| | | 8x gain, normal mode | | | 1.5 | | |
| | | 64x gain, normal mode | | | 11 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

### 36.4.7 DAC Characteristics

**Table 36-108. Power supply, reference and output range.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | | $V_{CC}$- 0.3 | | $V_{CC}$+ 0.3 | |
| $AV_{REF}$ | External reference voltage | | 1.0 | | $V_{CC}$- 0.6 | V |
| $R_{channel}$ | DC output impedance | | | | 50 | Ω |
| | Linear output voltage range | | 0.15 | | $AV_{CC}$-0.15 | V |
| $R_{AREF}$ | Reference input resistance | | | >10 | | MΩ |
| CAREF | Reference input capacitance | Static load | | 7.0 | | pF |
| | Minimum Resistance load | | 1 | | | kΩ |
| | Maximum capacitance load | | | | 100 | pF |
| | | 1000Ω serial resistance | | | 1 | nF |
| | Output sink/source | Operating within accuracy specification | | | $AV_{CC}$/1000 | mA |
| | | Safe operation | | | 10 | |

**Table 36-109. Clock and timing.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{DAC}$ | Conversion rate | $C_{load}$=100pF, maximum step size | Normal mode | 0 | | 1000 | ksps |
| | | | Low power mode | | | 500 | |

**Table 36-110.Accuracy characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| RES | Input resolution | | | | | 12 | Bits |
| INL [(1)] | Integral non-linearity | $V_{REF}$= Ext 1.0V | $V_{CC}$ = 1.6V | | ±2.0 | ±3.0 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±2.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±2.0 | ±4.0 | |
| | | | $V_{CC}$ = 3.6V | | ±1.5 | ±4.0 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±5.0 | | |
| | | | $V_{CC}$ = 3.6V | | ±5.0 | | |
| DNL [(1)] | Differential non-linearity | $V_{REF}$=Ext 1.0V | $V_{CC}$ = 1.6V | | ±1.5 | 3.0 | lsb |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=$AV_{CC}$ | $V_{CC}$ = 1.6V | | ±1.0 | 3.5 | |
| | | | $V_{CC}$ = 3.6V | | ±0.6 | 1.5 | |
| | | $V_{REF}$=INT1V | $V_{CC}$ = 1.6V | | ±4.5 | | |
| | | | $V_{CC}$ = 3.6V | | ±4.5 | | |
| | Gain error | After calibration | | | <4.0 | | lsb |
| | Gain calibration step size | | | | 4.0 | | lsb |
| | Gain calibration drift | $V_{REF}$= Ext 1.0V | | | <0.2 | | mV/K |
| | Offset error | After calibration | | | <1.0 | | lsb |
| | Offset calibration step size | | | | 1.0 | | |

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

### 36.4.8 Analog Comparator Characteristics

**Table 36-111. Analog Comparator characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{off}$ | Input offset voltage | | | | <±10 | | mV |
| $I_{lk}$ | Input leakage current | | | | <1 | | nA |
| | Input voltage range | | | -0.1 | | $AV_{CC}$ | V |
| | AC startup time | | | | 100 | | µs |
| $V_{hys1}$ | Hysteresis, none | | | | 0 | | mV |
| $V_{hys2}$ | Hysteresis, small | mode = High Speed (HS) | | | 13 | | mV |
| | | mode = Low Power (LP) | | | 30 | | |
| $V_{hys3}$ | Hysteresis, large | mode = HS | | | 30 | | mV |
| | | mode = LP | | | 60 | | |
| $t_{delay}$ | Propagation delay | $V_{CC}$ = 3.0V, T= 85°C | mode = HS | | 30 | 90 | ns |
| | | mode = HS | | | 30 | | |
| | | $V_{CC}$ = 3.0V, T= 85°C | mode = LP | | 130 | 500 | |
| | | mode = LP | | | 130 | | |
| | 64-level voltage scaler | Integral non-linearity (INL) | | | 0.3 | 0.5 | lsb |

### 36.4.9 Bandgap and Internal 1.0V Reference Characteristics

**Table 36-112. Bandgap and Internal 1.0V reference characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Startup time | As reference for ADC or DAC | 1 $Clk_{PER}$ + 2.5µs | | | µs |
| | | As input voltage to ADC and AC | | 1.5 | | |
| | Bandgap voltage | | | 1.1 | | V |
| INT1V | Internal 1.00V reference | T= 85°C, after calibration | 0.99 | 1.0 | 1.01 | V |
| | Variation over voltage and temperature | Relative to T= 85°C, $V_{CC}$ = 3.0V | | ±1.5 | | % |

### 36.4.10 Brownout Detection Characteristics

**Table 36-113. Brownout detection characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{BOT}$ | BOD level 0 falling $V_{CC}$ | | 1.50 | 1.62 | 1.72 | V |
| | BOD level 1 falling $V_{CC}$ | | | 1.8 | | |
| | BOD level 2 falling $V_{CC}$ | | | 2.0 | | |
| | BOD level 3 falling $V_{CC}$ | | | 2.2 | | |
| | BOD level 4 falling $V_{CC}$ | | | 2.4 | | |
| | BOD level 5 falling $V_{CC}$ | | | 2.6 | | |
| | BOD level 6 falling $V_{CC}$ | | | 2.8 | | |
| | BOD level 7 falling $V_{CC}$ | | | 3.0 | | |
| $t_{BOD}$ | Detection time | Continuous mode | | 0.4 | | µs |
| | | Sampled mode | | 1000 | | |
| $V_{HYST}$ | Hysteresis | | | 1.2 | | % |

### 36.4.11 External Reset Characteristics

**Table 36-114. External reset characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{EXT}$ | Minimum reset pulse width | | 1000 | 95 | | ns |
| $V_{RST}$ | Reset threshold voltage ($V_{IH}$) | $V_{CC}$ = 2.7 - 3.6V | 0.60×$V_{CC}$ | | | V |
| | | $V_{CC}$ = 1.6 - 2.7V | 0.60×$V_{CC}$ | | | |
| | Reset threshold voltage ($V_{IL}$) | $V_{CC}$ = 2.7 - 3.6V | | | 0.50×$V_{CC}$ | |
| | | $V_{CC}$ = 1.6 - 2.7V | | | 0.40×$V_{CC}$ | |
| $R_{RST}$ | Reset pin Pull-up Resistor | | | 25 | | kΩ |

### 36.4.12 Power-on Reset Characteristics

**Table 36-115. Power-on reset characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{POT-}$ [(1)] | POR threshold voltage falling $V_{CC}$ | $V_{CC}$ falls faster than 1V/ms | 0.4 | 1.0 | | V |
| | | $V_{CC}$ falls at 1V/ms or slower | 0.8 | 1.0 | | |
| $V_{POT+}$ | POR threshold voltage rising $V_{CC}$ | | | 1.3 | 1.59 | mV |

Note: 1. $V_{POT-}$ values are only valid when BOD is disabled. When BOD is enabled $V_{POT-}$ = $V_{POT+}$.

### 36.4.13 Flash and EEPROM Memory Characteristics

**Table 36-116. Endurance and data retention.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Flash | Write/Erase cycles | 25°C | 10K | | | Cycle |
| | | | 85°C | 10K | | | |
| | | | 105°C | 2K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 85°C | 25 | | | |
| | | | 105°C | 10 | | | |
| | EEPROM | Write/Erase cycles | 25°C | 100K | | | Cycle |
| | | | 85°C | 100K | | | |
| | | | 105°C | 30K | | | |
| | | Data retention | 25°C | 100 | | | Year |
| | | | 85°C | 25 | | | |
| | | | 105°C | 10 | | | |

**Table 36-117. Programming time.**

| Symbol | Parameter | Condition | Min. | Typ.[1] | Max. | Units |
|---|---|---|---|---|---|---|
| | Chip Erase | 128KB Flash, EEPROM[2] and SRAM Erase | | 75 | | ms |
| | Application Erase | Section erase | | 6 | | ms |
| | Flash | Page erase | | 4 | | ms |
| | | Page write | | 4 | | |
| | | Atomic page erase and write | | 8 | | |
| | EEPROM | Page erase | | 4 | | ms |
| | | Page write | | 4 | | |
| | | Atomic page erase and write | | 8 | | |

Notes:
1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

### 36.4.14 Clock and Oscillator Characteristics

#### 36.4.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

**Table 36-118. 32.768kHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency | | | 32.768 | | kHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$ = 3.0V | -0.5 | | 0.5 | % |
| | User calibration accuracy | | -0.5 | | 0.5 | % |

#### 36.4.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

**Table 36-119. 2MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 1.8 | | 2.2 | MHz |
| | Factory calibrated frequency | | | 2.0 | | MHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | % |
| | DFLL calibration stepsize | | | 0.21 | | % |

#### 36.4.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

**Table 36-120. 32MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency range | DFLL can tune to this frequency over voltage and temperature | 30 | | 55 | MHz |
| | Factory calibrated frequency | | | 32 | | MHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | User calibration accuracy | | -0.2 | | 0.2 | % |
| | DFLL calibration step size | | | 0.22 | | % |

#### 36.4.14.4 32kHz Internal ULP Oscillator characteristics

**Table 36-121. 32kHz internal ULP oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Output frequency | | | 32 | | kHz |
| | Accuracy | | -30 | | 30 | % |

### 36.4.14.5 Internal Phase Locked Loop (PLL) characteristics

**Table 36-122. Internal PLL characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input frequency | Output frequency must be within $f_{OUT}$ | 0.4 | | 64 | MHz |
| $f_{OUT}$ | Output frequency (1) | $V_{CC}$= 1.6 - 1.8V | 20 | | 48 | MHz |
| | | $V_{CC}$= 2.7 - 3.6V | 20 | | 128 | |
| | Start-up time | | | 25 | | µs |
| | Re-lock time | | | 25 | | µs |

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

### 36.4.14.6 External clock characteristics

**Figure 36-24. External clock drive waveform**

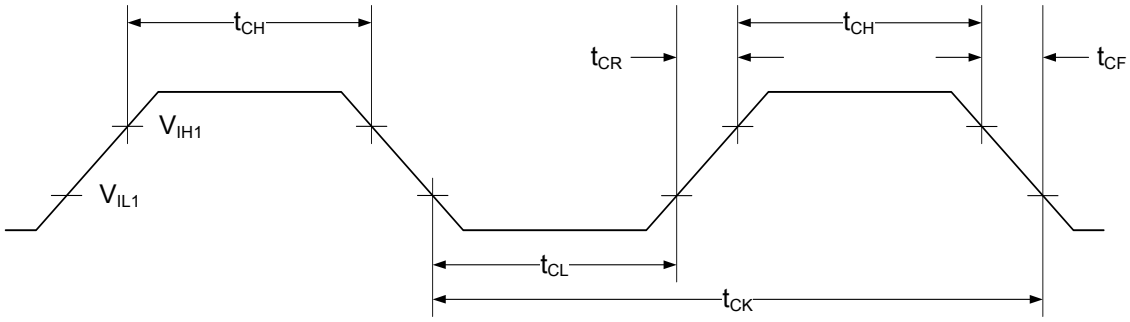



**Table 36-123.External clock used as system clock without prescaling.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock Frequency (1) | $V_{CC}$ = 1.6 - 1.8V | 0 | | 12 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 32 | |
| $t_{CK}$ | Clock Period | $V_{CC}$ = 1.6 - 1.8V | 83.3 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 31.5 | | | |
| $t_{CH}$ | Clock High Time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 30.0 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 12.5 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 10 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 3 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

**Table 36-124. External clock with prescaler [1] for system clock.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $1/t_{CK}$ | Clock Frequency [2] | $V_{CC}$ = 1.6 - 1.8V | 0 | | 90 | MHz |
| | | $V_{CC}$ = 2.7 - 3.6V | 0 | | 142 | |
| $t_{CK}$ | Clock Period | $V_{CC}$ = 1.6 - 1.8V | 11 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 7 | | | |
| $t_{CH}$ | Clock High Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

### 36.4.14.7 External 16MHz crystal oscillator and XOSC characteristic

**Table 36-125. External 16MHz crystal oscillator and XOSC characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Cycle to cycle jitter | XOSCPWR=0 | FRQRANGE=0 | | <10 | | ns |
| | | | FRQRANGE=1, 2, or 3 | | <1 | | |
| | | XOSCPWR=1 | | | <1 | | |
| | Long term jitter | XOSCPWR=0 | FRQRANGE=0 | | <6 | | ns |
| | | | FRQRANGE=1, 2, or 3 | | <0.5 | | |
| | | XOSCPWR=1 | | | <0.5 | | |
| | Frequency error | XOSCPWR=0 | FRQRANGE=0 | | <0.1 | | % |
| | | | FRQRANGE=1 | | <0.05 | | |
| | | | FRQRANGE=2 or 3 | | <0.005 | | |
| | | XOSCPWR=1 | | | <0.005 | | |

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Duty cycle | XOSCPWR=0 | FRQRANGE=0 | | 40 | | % |
| | | | FRQRANGE=1 | | 42 | | |
| | | | FRQRANGE=2 or 3 | | 45 | | |
| | | XOSCPWR=1 | | | 48 | | |
| $R_Q$ | Negative impedance [1] | XOSCPWR=0, FRQRANGE=0 | 0.4MHz resonator, CL=100pF | 2.4k | | | Ω |
| | | | 1MHz crystal, CL=20pF | 8.7k | | | |
| | | | 2MHz crystal, CL=20pF | 2.1k | | | |
| | | XOSCPWR=0, FRQRANGE=1, CL=20pF | 2MHz crystal | 4.2k | | | |
| | | | 8MHz crystal | 250 | | | |
| | | | 9MHz crystal | 195 | | | |
| | | XOSCPWR=0, FRQRANGE=2, CL=20pF | 8MHz crystal | 360 | | | |
| | | | 9MHz crystal | 285 | | | |
| | | | 12MHz crystal | 155 | | | |
| | | XOSCPWR=0, FRQRANGE=3, CL=20pF | 9MHz crystal | 365 | | | |
| | | | 12MHz crystal | 200 | | | |
| | | | 16MHz crystal | 105 | | | |
| | | XOSCPWR=1, FRQRANGE=0, CL=20pF | 9MHz crystal | 435 | | | |
| | | | 12MHz crystal | 235 | | | |
| | | | 16MHz crystal | 125 | | | |
| | | XOSCPWR=1, FRQRANGE=1, CL=20pF | 9MHz crystal | 495 | | | |
| | | | 12MHz crystal | 270 | | | |
| | | | 16MHz crystal | 145 | | | |
| | | XOSCPWR=1, FRQRANGE=2, CL=20pF | 12MHz crystal | 305 | | | |
| | | | 16MHz crystal | 160 | | | |
| | | XOSCPWR=1, FRQRANGE=3, CL=20pF | 12MHz crystal | 380 | | | |
| | | | 16MHz crystal | 205 | | | |
| | ESR | SF = Safety factor | | | | min(RQ)/SF | kΩ |
| $C_{XTAL1}$ | Parasitic capacitance XTAL1 pin | | | | 5.45 | | pF |
| $C_{XTAL2}$ | Parasitic capacitance XTAL2 pin | | | | 7.51 | | pF |
| $C_{LOAD}$ | Parasitic capacitance load | | | | 3.16 | | pF |

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

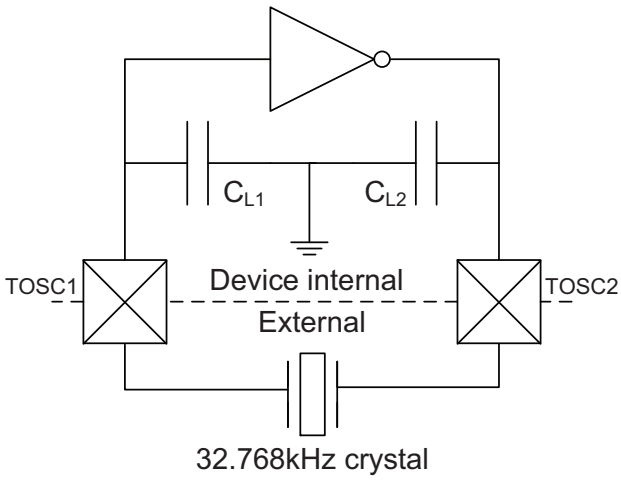
### 36.4.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

**Table 36-126. External 32.768kHz crystal oscillator and TOSC characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ESR/R1 | Recommended crystal equivalent series resistance (ESR) | Crystal load capacitance 6.5pF | | | 60 | kΩ |
| | | Crystal load capacitance 9.0pF | | | 35 | |
| $C_{TOSC1}$ | Parasitic capacitance TOSC1 pin | | | 5.4 | | pF |
| | | Alternate TOSC location | | 4.0 | | |
| $C_{TOSC2}$ | Parasitic capacitance TOSC2 pin | | | 7.1 | | pF |
| | | Alternate TOSC location | | 4.0 | | |
| | Recommended safety factor | capacitance load matched to crystal specification | 3 | | | |

Note: 1. See Figure 36-25 for definition.

**Figure 36-25. TOSC input capacitance.**




The parasitic capacitance between the TOSC pins is $C_{L1} + C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

### 36.4.15 SPI Characteristics

**Figure 36-26. SPI timing requirements in master mode.**

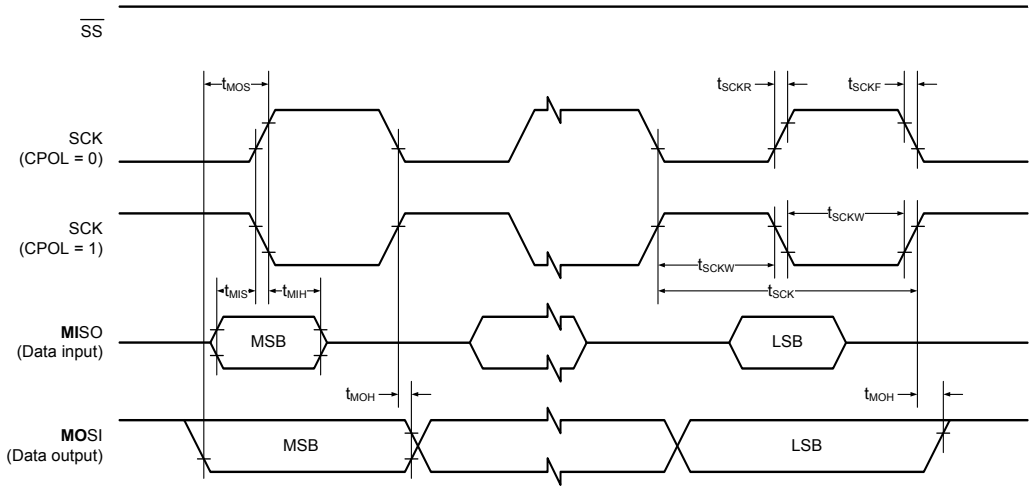



**Figure 36-27. SPI timing requirements in slave mode.**

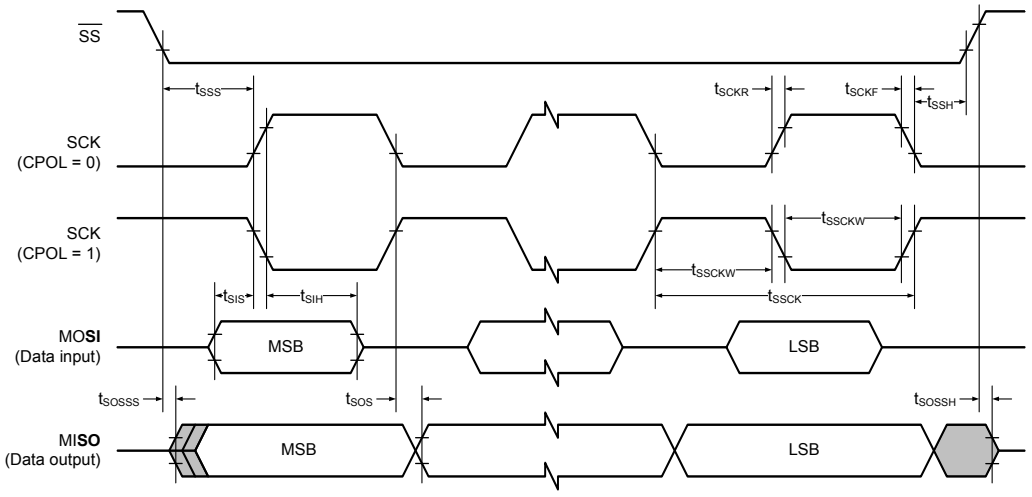


**Table 36-127. SPI timing characteristics and requirements.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{SCK}$ | SCK Period | Master | | (See Table 21-4 in XMEGA AU Manual) | | ns |
| $t_{SCKW}$ | SCK high/low width | Master | | 0.5×SCK | | |
| $t_{SCKR}$ | SCK Rise time | Master | | 2.7 | | |
| $t_{SCKF}$ | SCK Fall time | Master | | 2.7 | | |
| $t_{MIS}$ | MISO setup to SCK | Master | | 10 | | |
| $t_{MIH}$ | MISO hold after SCK | Master | | 10 | | |
| $t_{MOS}$ | MOSI setup SCK | Master | | 0.5×SCK | | |
| $t_{MOH}$ | MOSI hold after SCK | Master | | 1 | | |
| $t_{SSCK}$ | Slave SCK Period | Slave | 4×t $Clk_{PER}$ | | | |
| $t_{SSCKW}$ | SCK high/low width | Slave | 2×t $Clk_{PER}$ | | | |
| $t_{SSCKR}$ | SCK Rise time | Slave | | | 1600 | |
| $t_{SSCKF}$ | SCK Fall time | Slave | | | 1600 | |
| $t_{SIS}$ | MOSI setup to SCK | Slave | 3 | | | |
| $t_{SIH}$ | MOSI hold after SCK | Slave | t $Clk_{PER}$ | | | |
| $t_{SSS}$ | $\overline{SS}$ setup to SCK | Slave | 21 | | | |
| $t_{SSH}$ | $\overline{SS}$ hold after SCK | Slave | 20 | | | |
| $t_{SOS}$ | MISO setup SCK | Slave | | 8 | | |
| $t_{SOH}$ | MISO hold after SCK | Slave | | 13 | | |
| $t_{SOSS}$ | MISO setup after $\overline{SS}$ low | Slave | | 11 | | |
| $t_{SOSH}$ | MISO hold after $\overline{SS}$ high | Slave | | 8 | | |

### 36.4.16 Two-Wire Interface Characteristics

Table 36-128 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-28.

**Figure 36-28. Two-wire interface bus timing.**

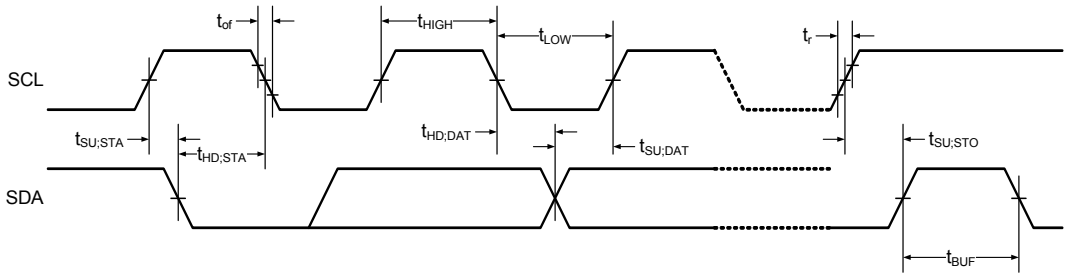



**Table 36-128. Two-wire interface characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | $0.7V_{CC}$ | | $V_{CC}+0.5$ | V |
| $V_{IL}$ | Input Low Voltage | | 0.5 | | $0.3\times V_{CC}$ | V |
| $V_{hys}$ | Hysteresis of Schmitt Trigger Inputs | | $0.05V_{CC}$ (1) | | | V |
| $V_{OL}$ | Output Low Voltage | 3mA, sink current | 0 | | 0.4 | V |
| $t_r$ | Rise Time for both SDA and SCL | | $20+0.1C_b$ (1)(2) | | 300 | ns |
| $t_{of}$ | Output Fall Time from $V_{IHmin}$ to $V_{ILmax}$ | $10pF < C_b < 400pF$ (2) | $20+0.1C_b$ (1)(2) | | 250 | ns |
| $t_{SP}$ | Spikes Suppressed by Input Filter | | 0 | | 50 | ns |
| $I_I$ | Input Current for each I/O Pin | $0.1V_{CC} < V_I < 0.9V_{CC}$ | -10 | | 10 | µA |
| $C_I$ | Capacitance for each I/O Pin | | | | 10 | pF |
| $f_{SCL}$ | SCL Clock Frequency | $f_{PER}$ (3)>max($10f_{SCL}$, 250kHz) | 0 | | 400 | kHz |
| $R_P$ | Value of Pull-up resistor | $f_{SCL} \leq 100kHz$ | $\frac{V_{CC}-0.4V}{3mA}$ | | $\frac{100ns}{C_b}$ | Ω |
| | | $f_{SCL} > 100kHz$ | | | $\frac{300ns}{C_b}$ | |
| $t_{HD;STA}$ | Hold Time (repeated) START condition | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{LOW}$ | Low Period of SCL Clock | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 1.3 | | | |
| $t_{HIGH}$ | High Period of SCL Clock | $f_{SCL} \leq 100kHz$ | 4.0 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | $f_{SCL} \leq 100kHz$ | 4.7 | | | µs |
| | | $f_{SCL} > 100kHz$ | 0.6 | | | |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{HD;DAT}$ | Data hold time | $f_{SCL} \leq$ 100kHz | 0 | | 3.45 | µs |
| | | $f_{SCL}$ > 100kHz | 0 | | 0.9 | |
| $t_{SU;DAT}$ | Data setup time | $f_{SCL} \leq$ 100kHz | 250 | | | ns |
| | | $f_{SCL}$ > 100kHz | 100 | | | |
| $t_{SU;STO}$ | Setup time for STOP condition | $f_{SCL} \leq$ 100kHz | 4.0 | | | µs |
| | | $f_{SCL}$ > 100kHz | 0.6 | | | |
| $t_{BUF}$ | Bus free time between a STOP and START condition | $f_{SCL} \leq$ 100kHz | 4.7 | | | µs |
| | | $f_{SCL}$ > 100kHz | 1.3 | | | |

Notes:
1. Required only for $f_{SCL}$ > 100kHz.
2. $C_b$ = Capacitance of one bus line in pF.
3. $f_{PER}$ = Peripheral clock frequency.

# 37. Typical Characteristics

## 37.1 ATxmega16A4U

### 37.1.1 Current consumption

#### 37.1.1.1 Active mode supply current

**Figure 37-1. Active supply current vs. frequency.**
***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

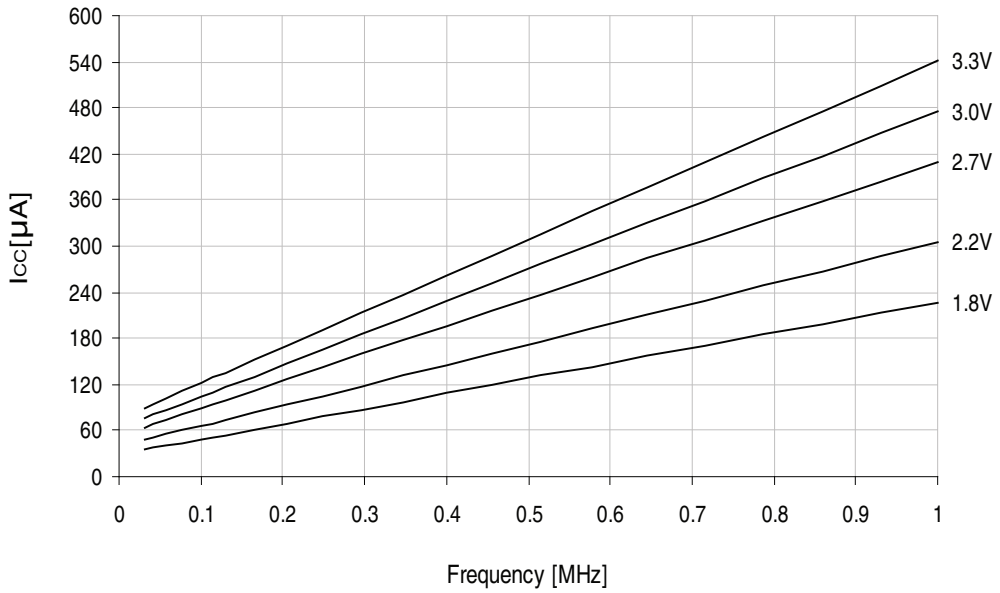



**Figure 37-2. Active supply current vs. frequency.**
***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C.***

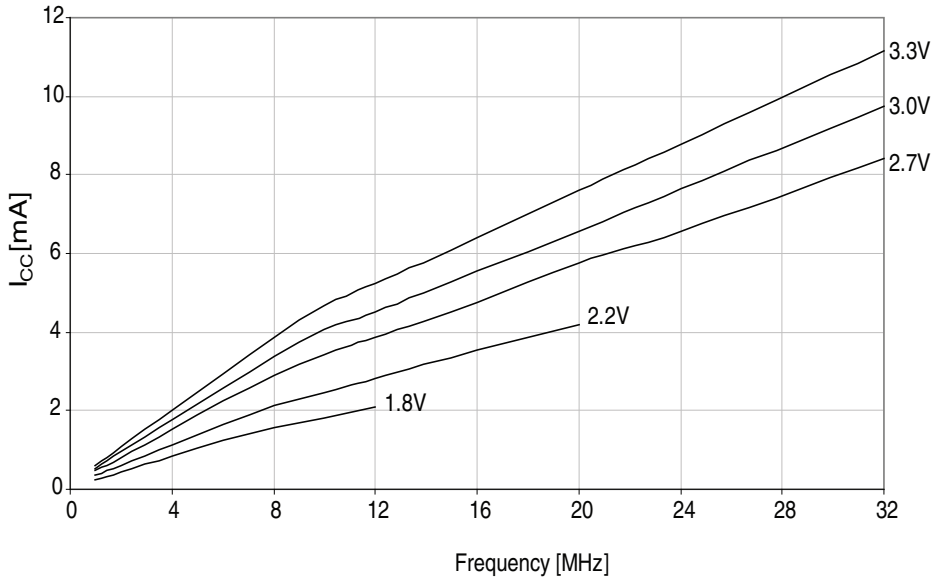


**Figure 37-3. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32.768kHz internal oscillator.***

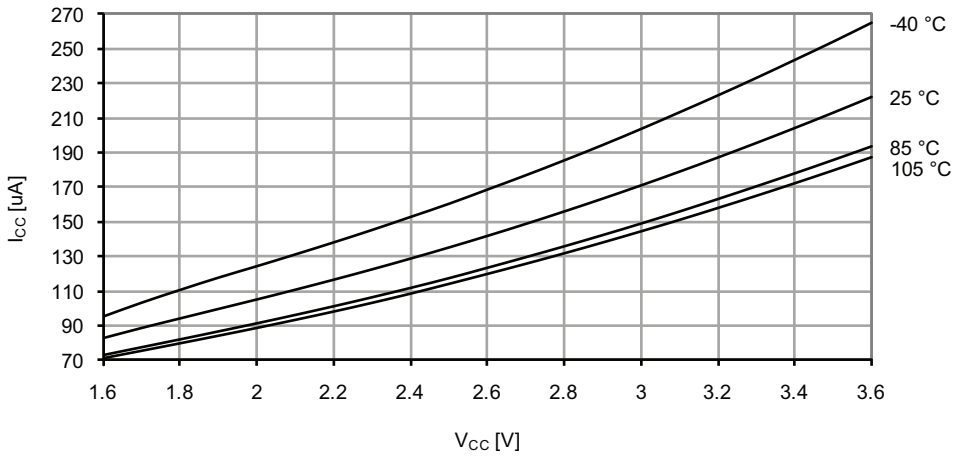



**Figure 37-4. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock.***

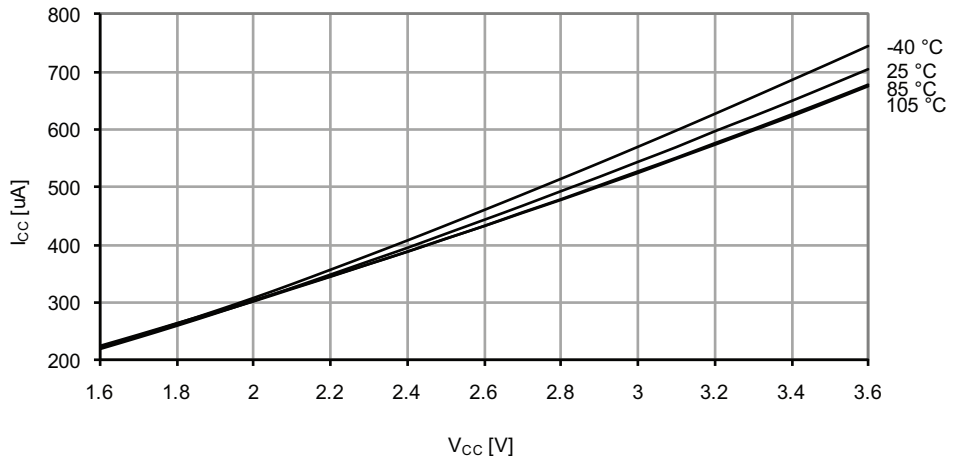


**Figure 37-5. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator.***

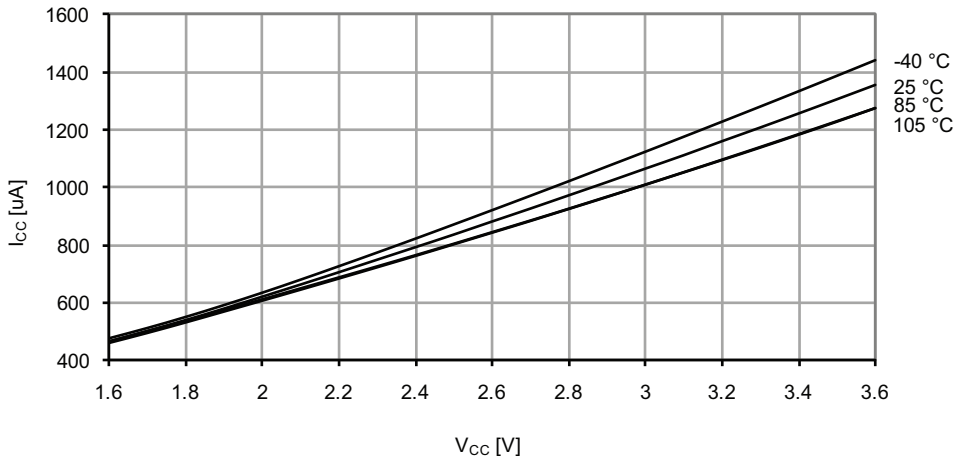



**Figure 37-6. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz.***

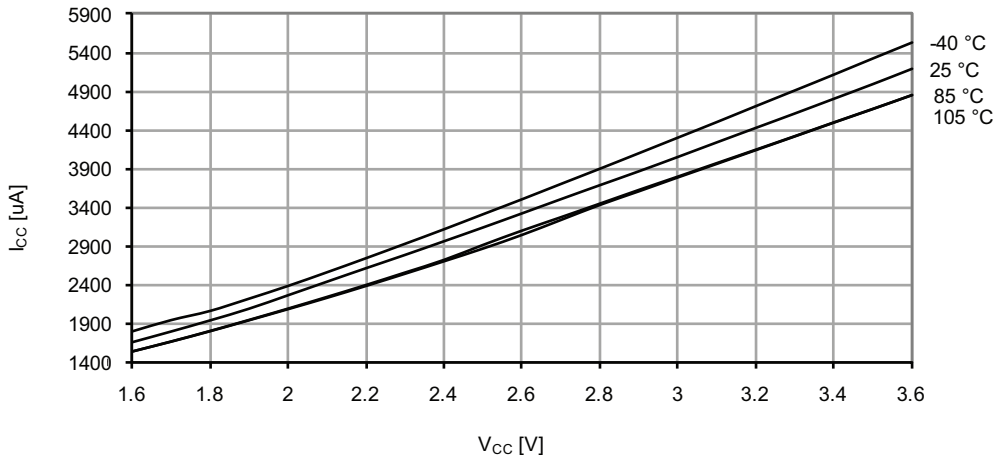
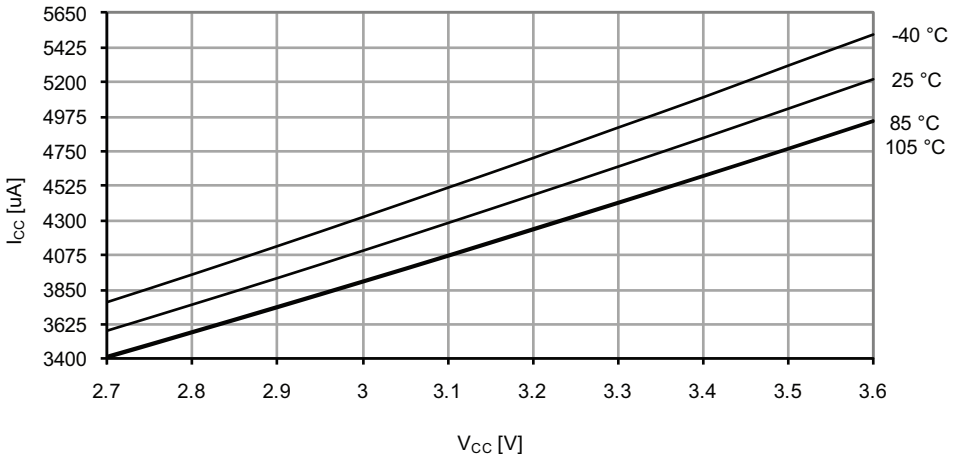


**Figure 37-7. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator.***




### 37.1.1.2 Idle mode supply current

**Figure 37-8. Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

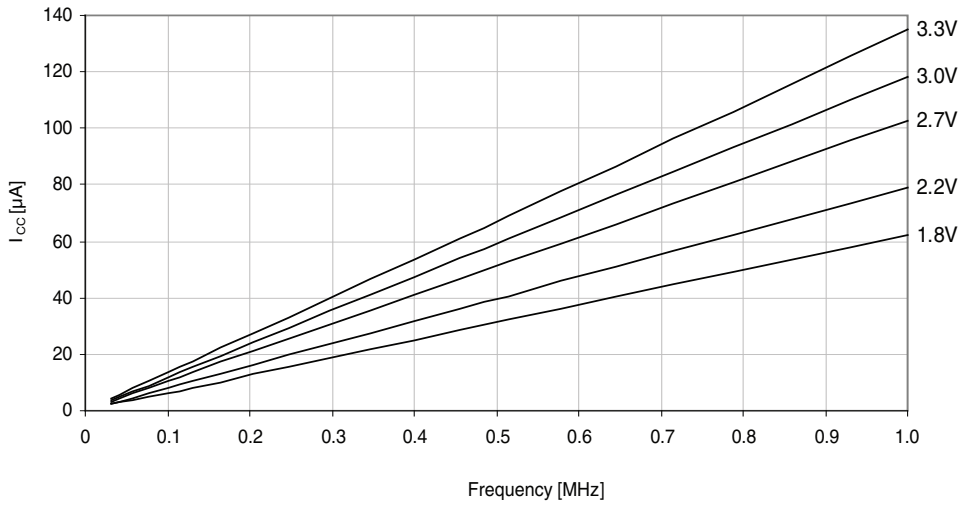


**Figure 37-9. Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C.***

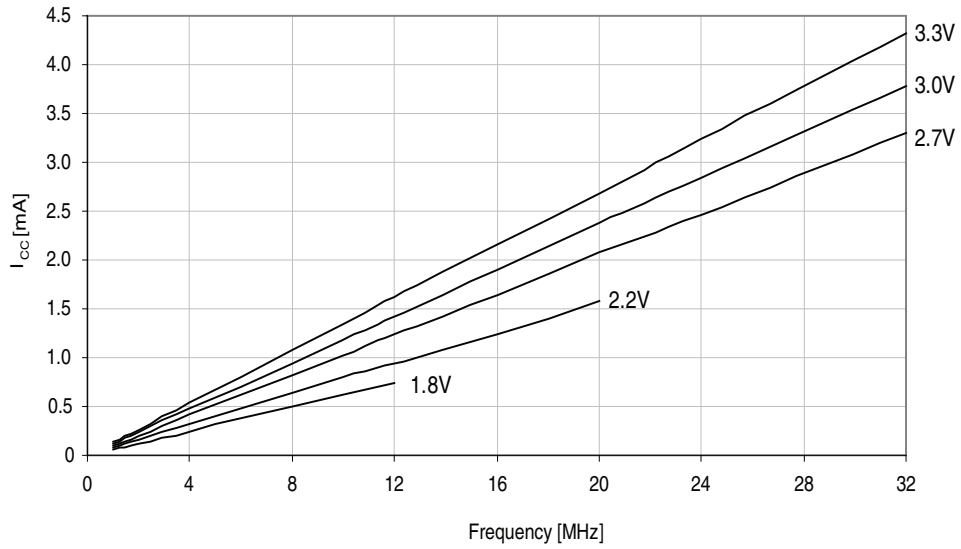



**Figure 37-10. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32.768kHz internal oscillator.***

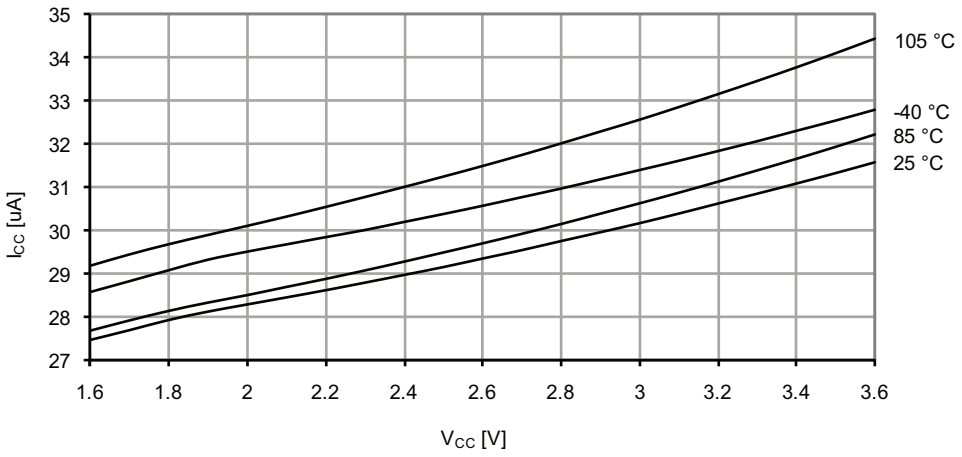


**Figure 37-11. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock.***

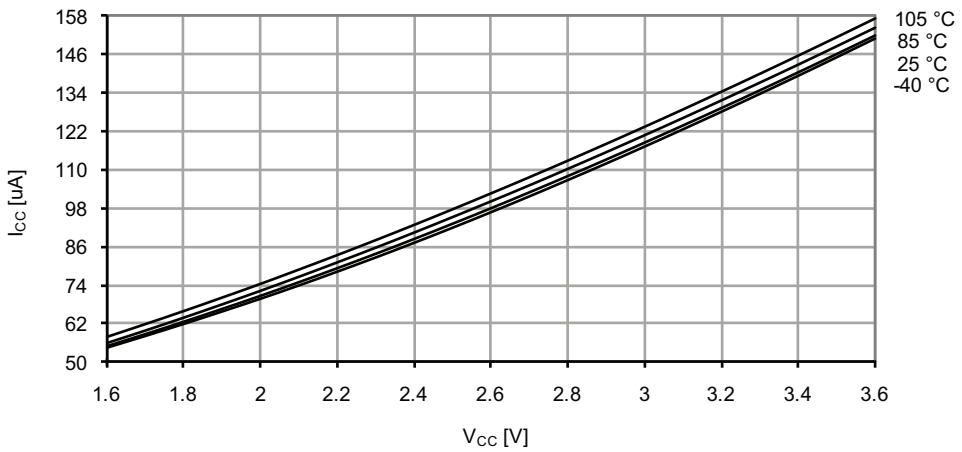



**Figure 37-12. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator.***

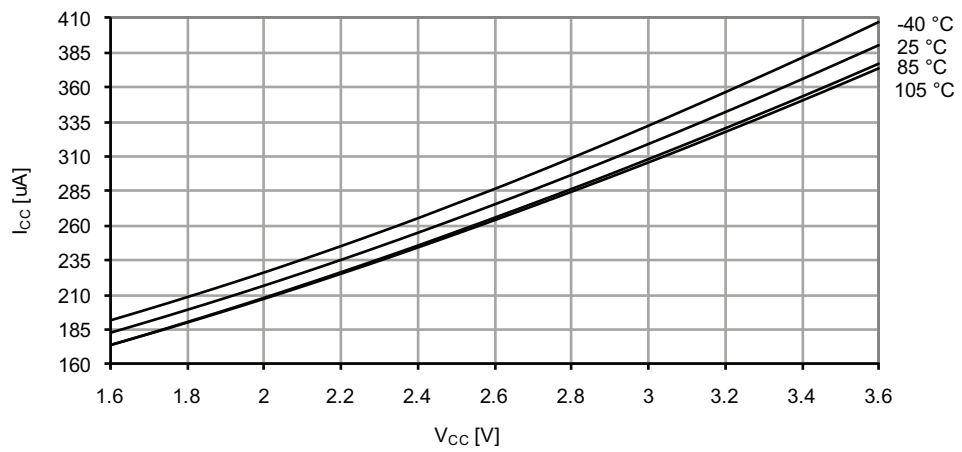


**Figure 37-13. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz.***

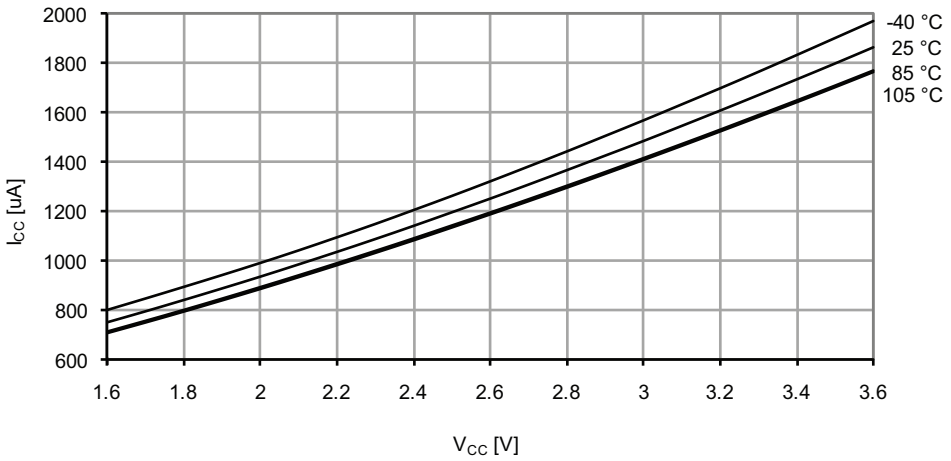
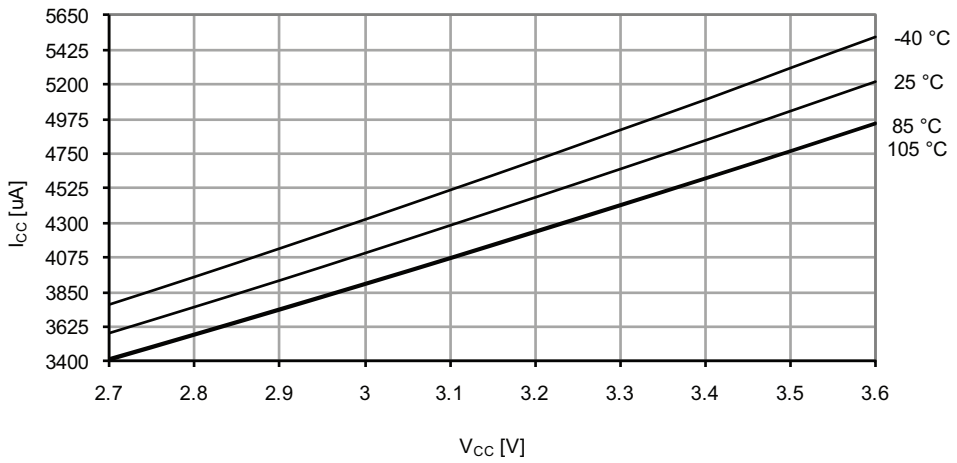



**Figure 37-14. Idle mode current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator.***



#### 37.1.1.3 Power-down mode supply current

**Figure 37-15. Power-down mode supply current vs. temperature.**
***All functions disabled.***

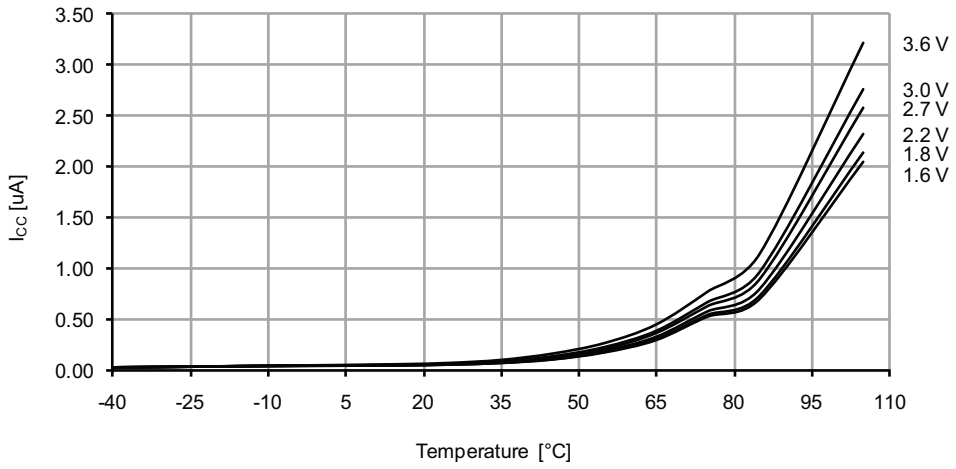



**Figure 37-16. Power-down mode supply current vs. $V_{CC}$.**
***All functions disabled.***

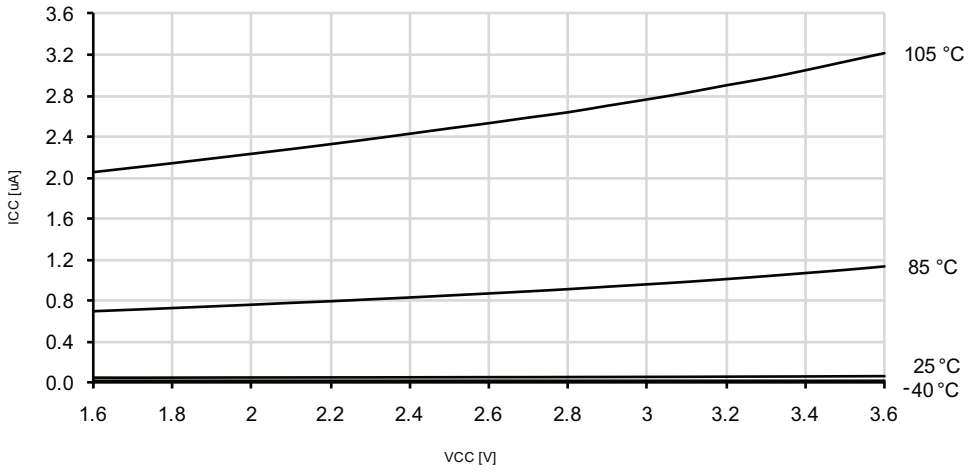
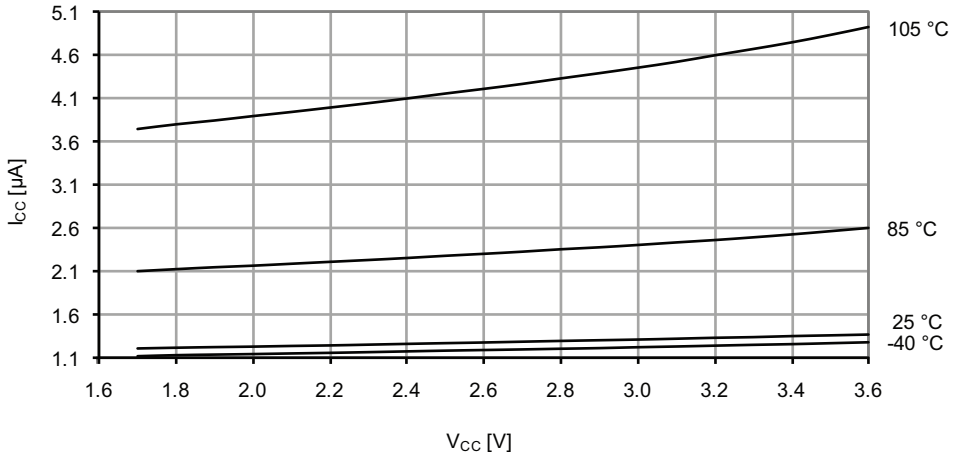


**Figure 37-17. Power-down mode supply current vs. $V_{CC}$.**

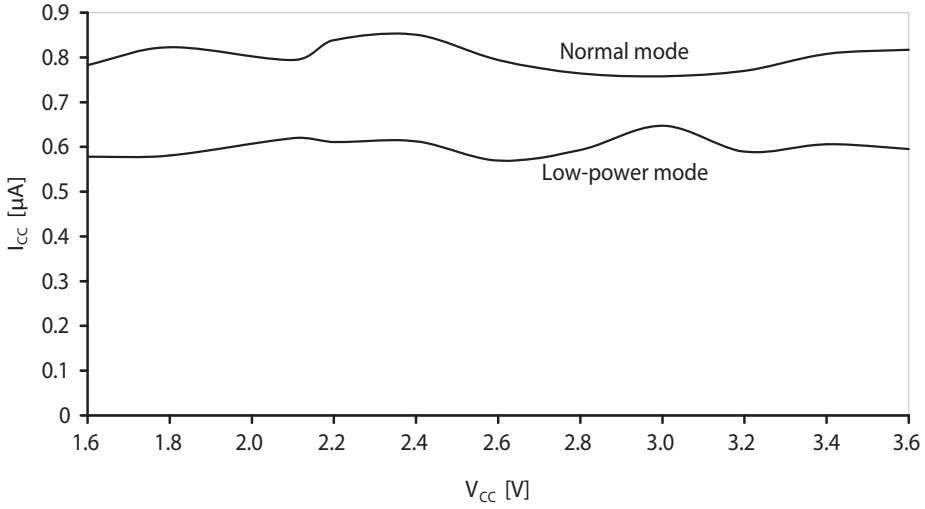
***Watchdog and sampled BOD enabled.***




### 37.1.1.4 Power-save mode supply current

**Figure 37-18. Power-save mode supply current vs.$V_{CC}$.**

***Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.***



#### 37.1.1.5 Standby mode supply current

**Figure 37-19. Standby supply current vs. $V_{CC}$.**
***Standby, $f_{SYS}$ = 1MHz.***

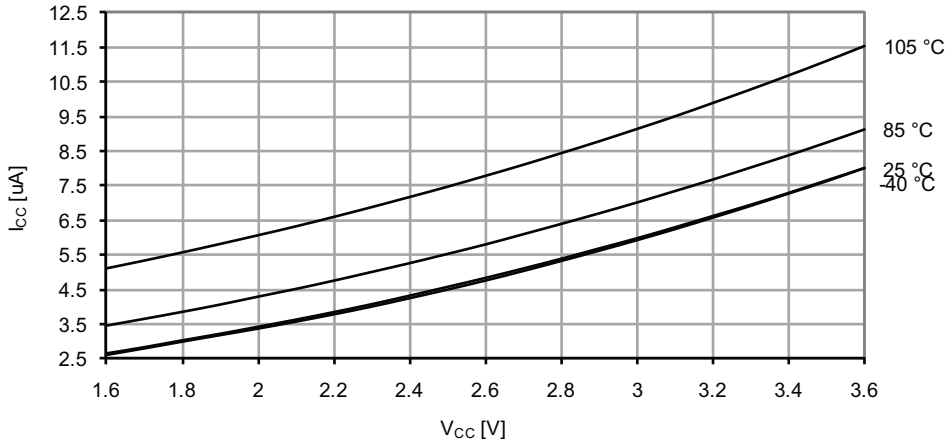
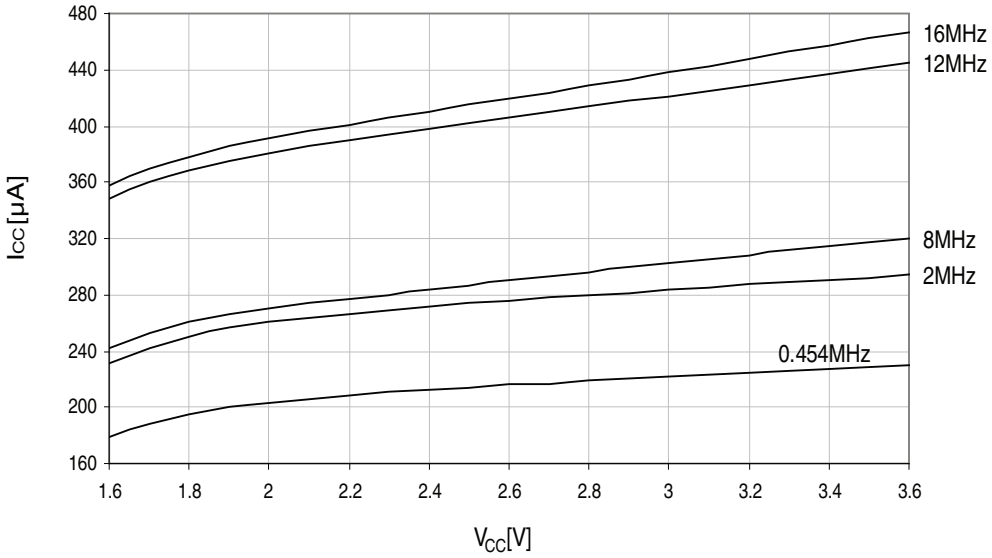



**Figure 37-20. Standby supply current vs. $V_{CC}$.**
***25°C, running from different crystal oscillators.***



### 37.1.2 I/O Pin Characteristics

#### 37.1.2.1 Pull-up

**Figure 37-21. I/O pin pull-up resistor current vs. input voltage.**
***$V_{CC}$ = 1.8V.***

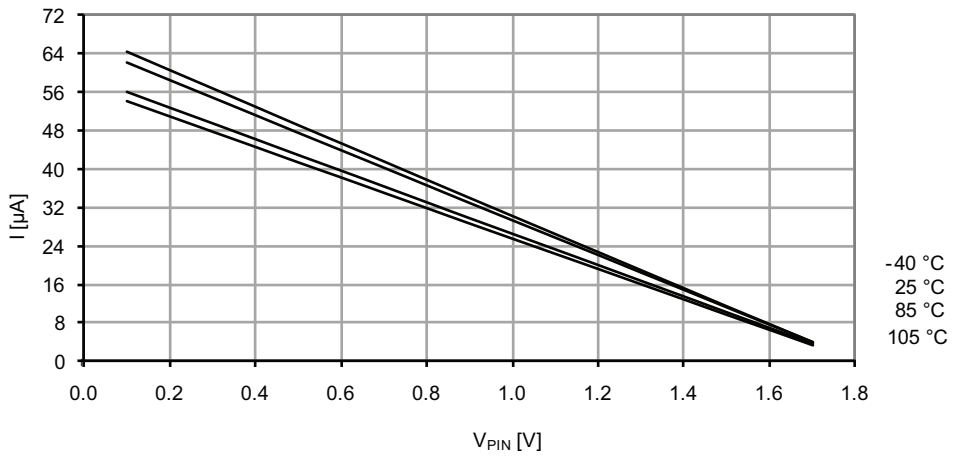



**Figure 37-22. I/O pin pull-up resistor current vs. input voltage.**
***$V_{CC}$ = 3.0V.***

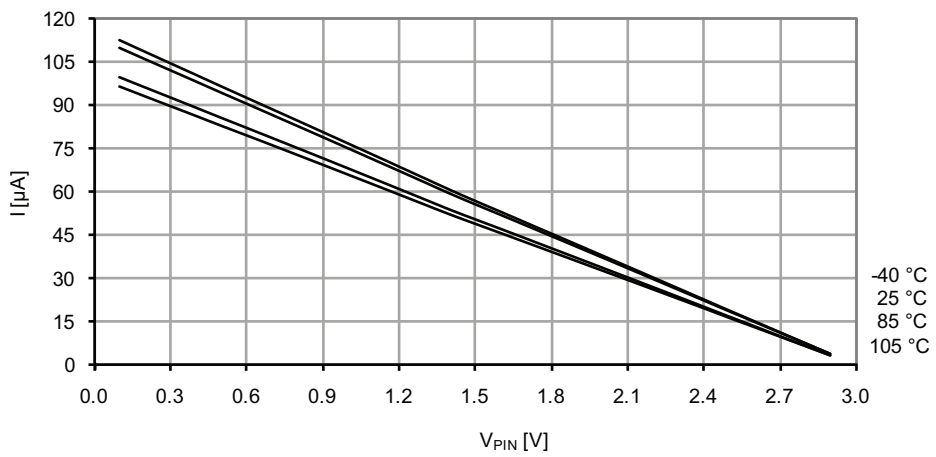
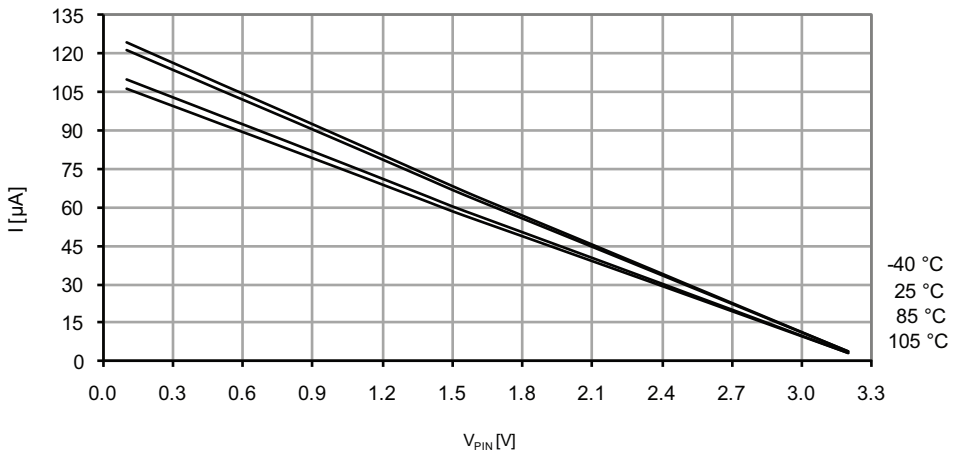


**Figure 37-23. I/O pin pull-up resistor current vs. input voltage.**

***$V_{CC}$ = 3.3V.***




### 37.1.2.2 Output Voltage vs. Sink/Source Current

**Figure 37-24. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 1.8V.***

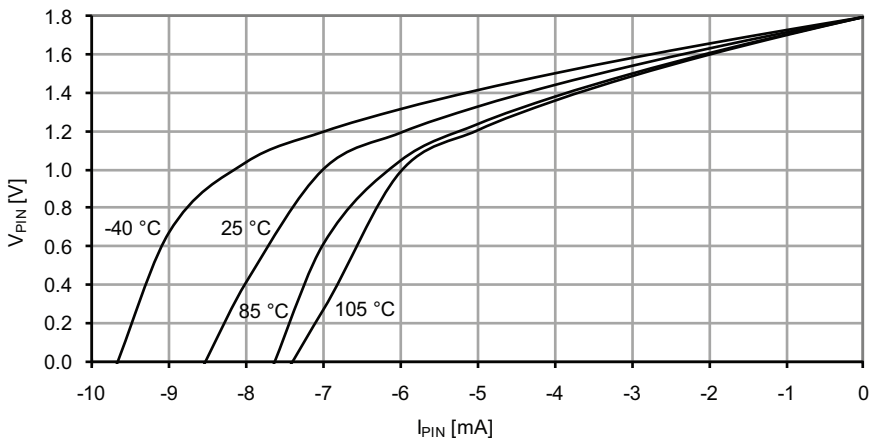


**Figure 37-25. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 3.0V.***

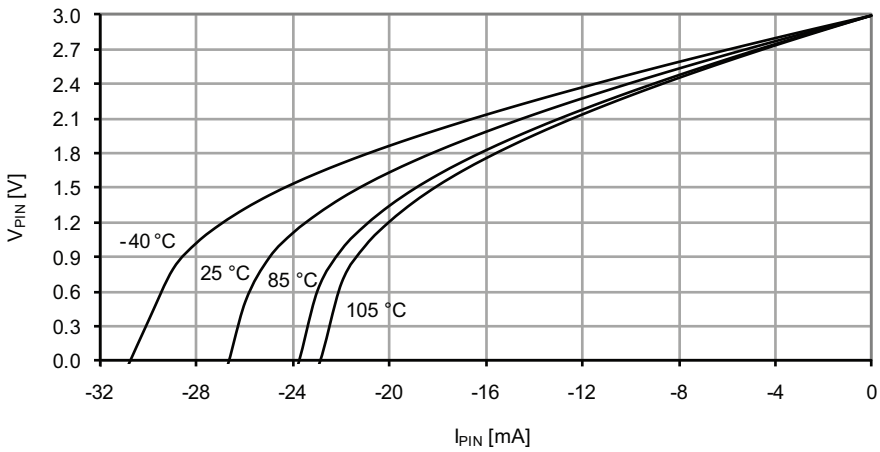



**Figure 37-26. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 3.3V.***

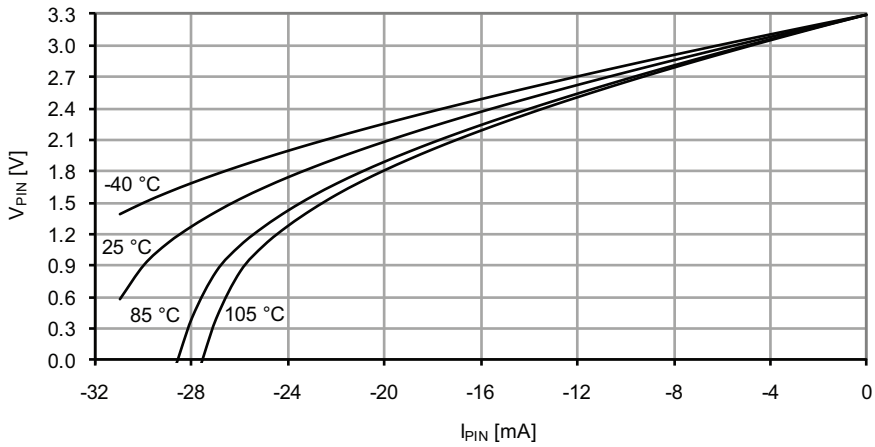


**Figure 37-27. I/O pin output voltage vs. source current.**

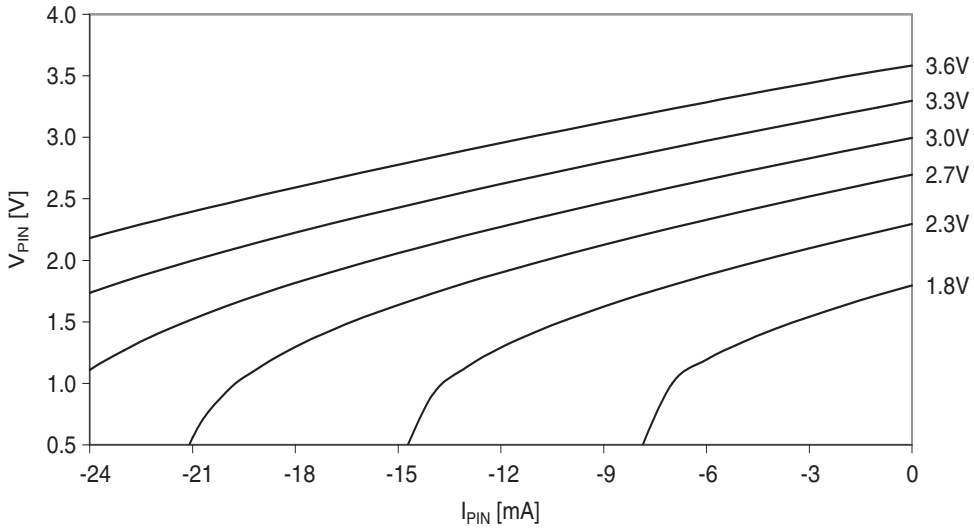



**Figure 37-28. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 1.8V.***

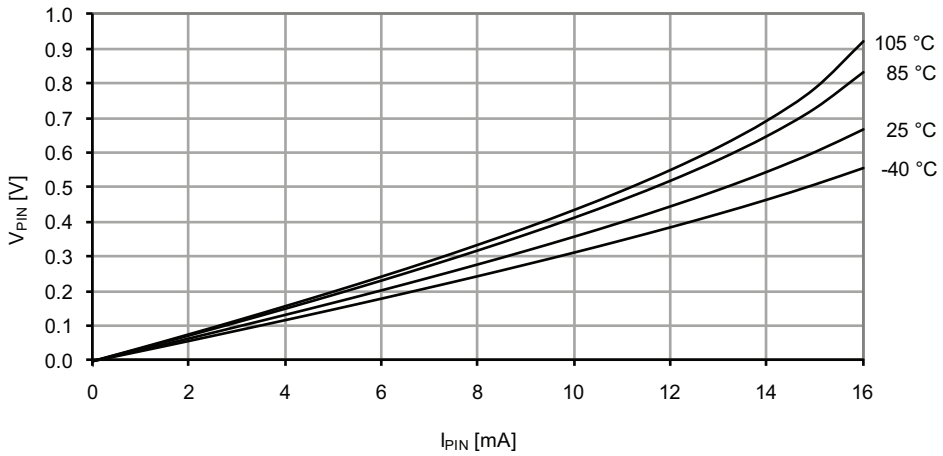


**Figure 37-29. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 3.0V.***

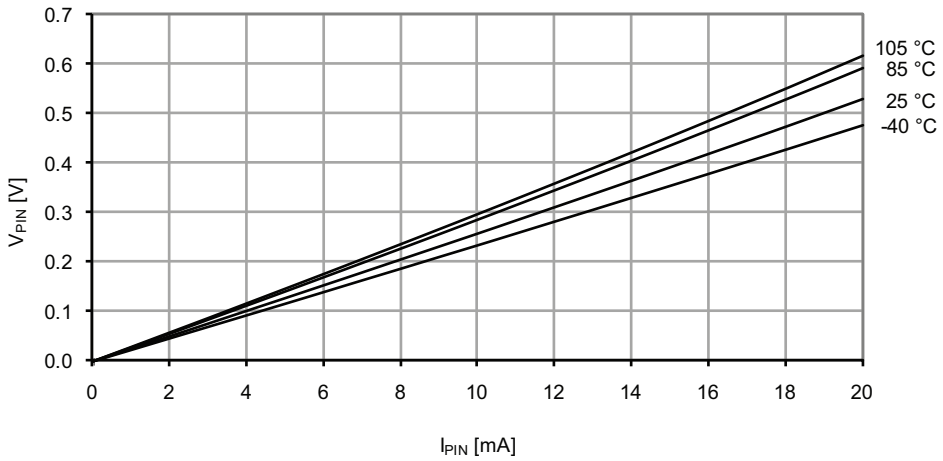



**Figure 37-30. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 3.3V.***

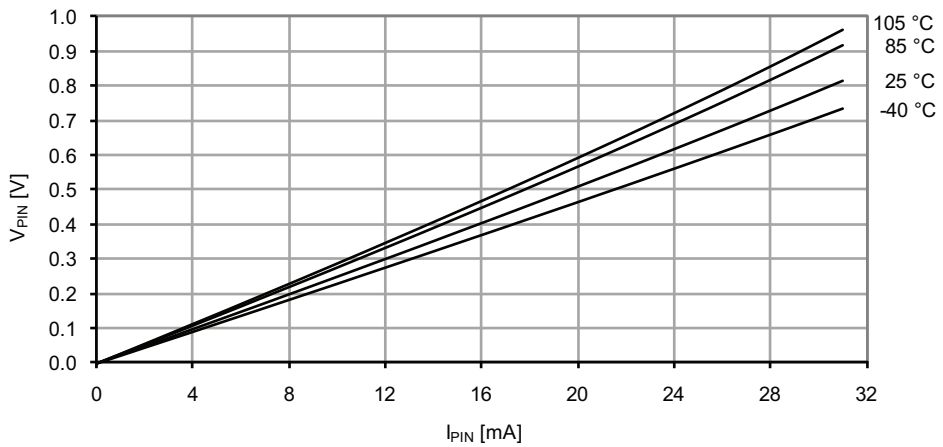
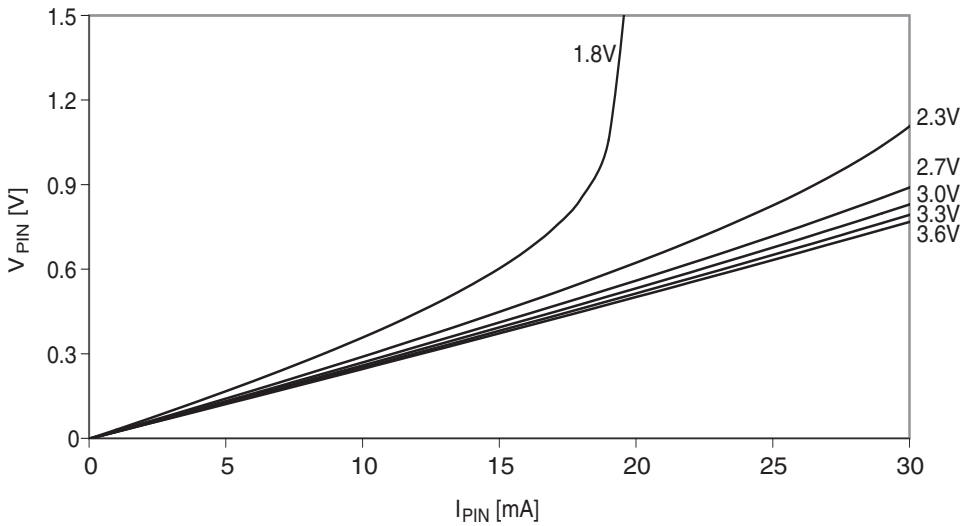



**Figure 37-31. I/O pin output voltage vs. sink current.**



### 37.1.2.3 Thresholds and Hysteresis

**Figure 37-32. I/O pin input threshold voltage vs. $V_{CC}$.**
***T = 25°C.***

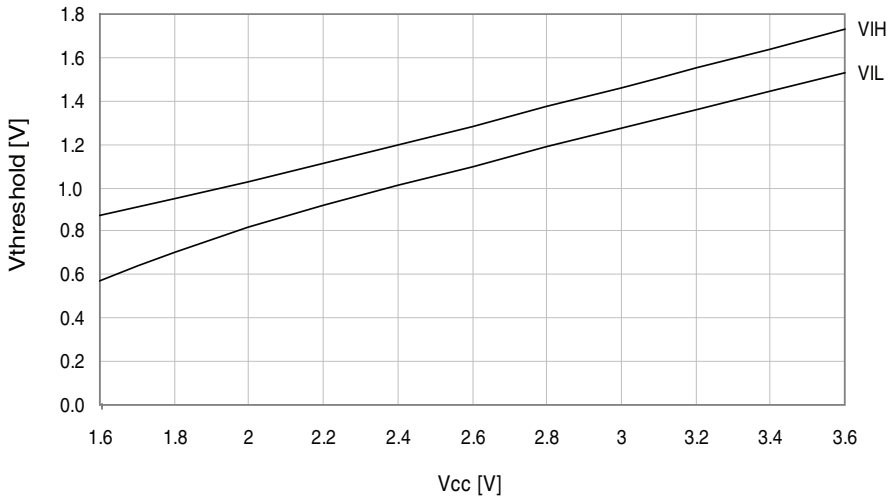



**Figure 37-33. I/O pin input threshold voltage vs. $V_{CC}$.**
***$V_{IH}$ I/O pin read as "1".***

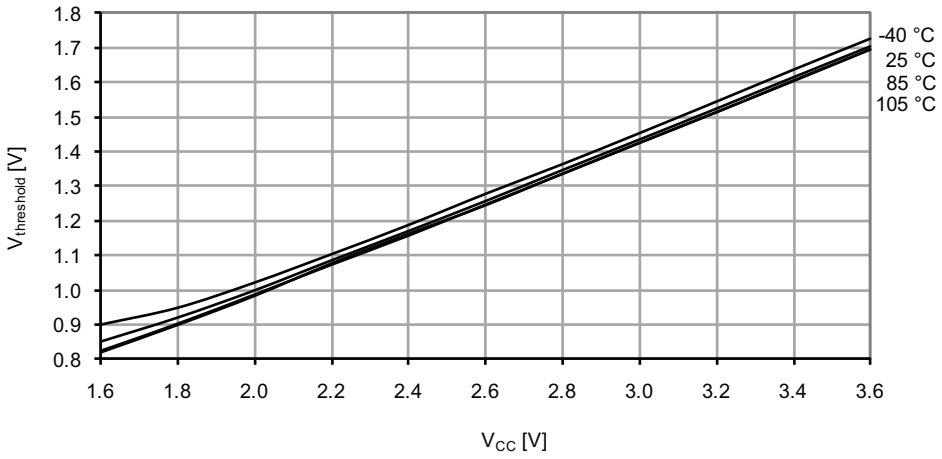


**Figure 37-34. I/O pin input threshold voltage vs. $V_{CC}$.**

***$V_{IL}$ I/O pin read as "0".***

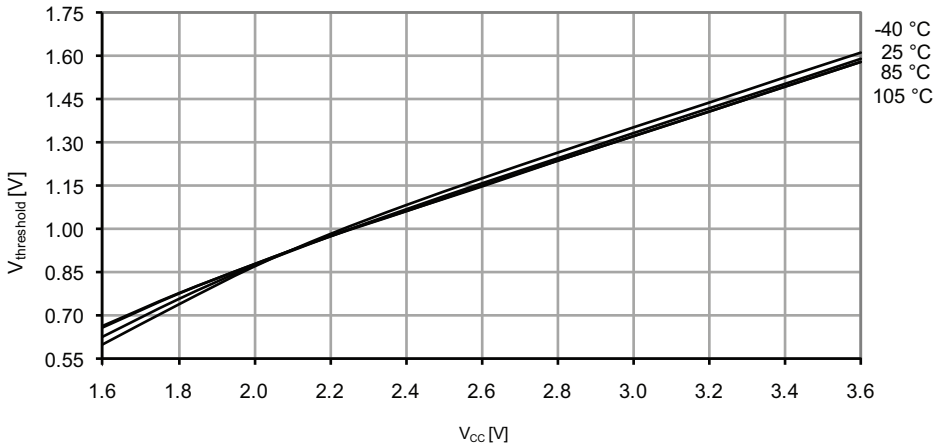
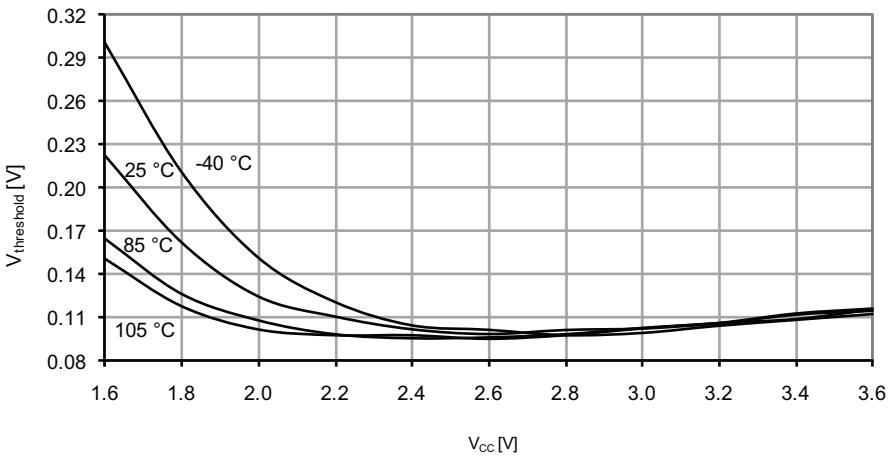



**Figure 37-35. I/O pin input hysteresis vs. $V_{CC}$.**



### 37.1.3 ADC Characteristics

**Figure 37-36. INL error vs. external $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, external reference.***

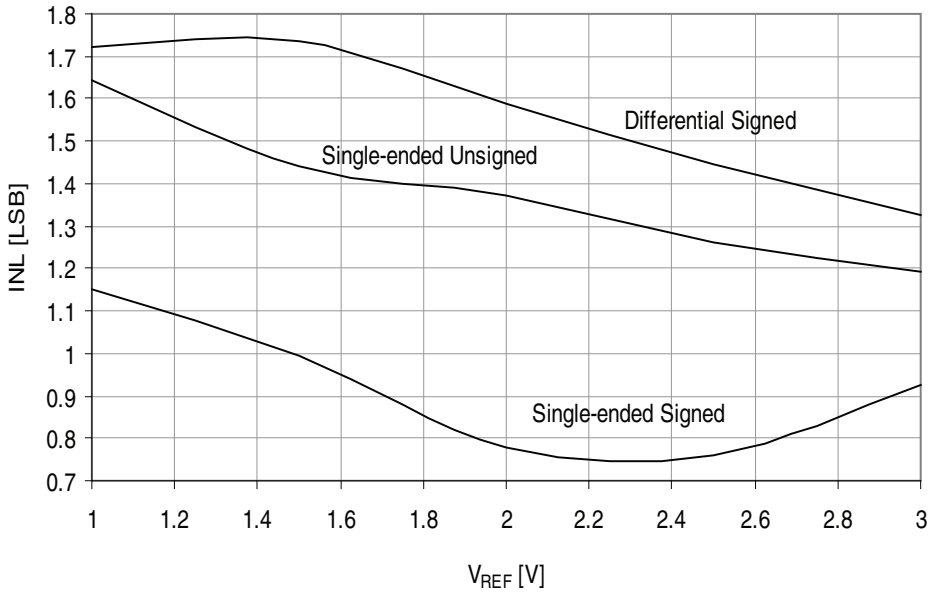



**Figure 37-37. INL error vs. sample rate.**

***T = 25°C, $V_{CC}$ = 3.6V, $V_{REF}$ = 3.0V external.***

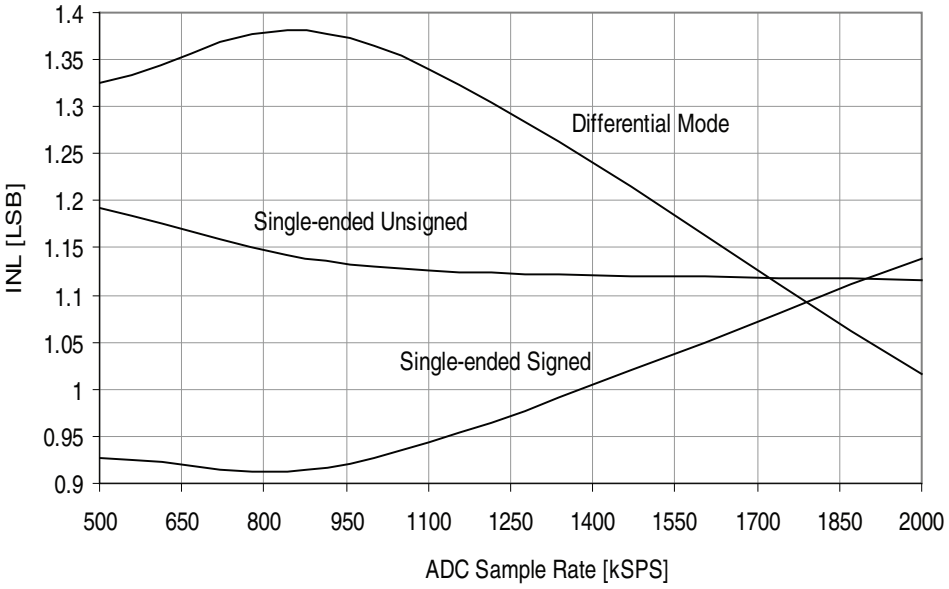


**Figure 37-38. INL error vs. input code**

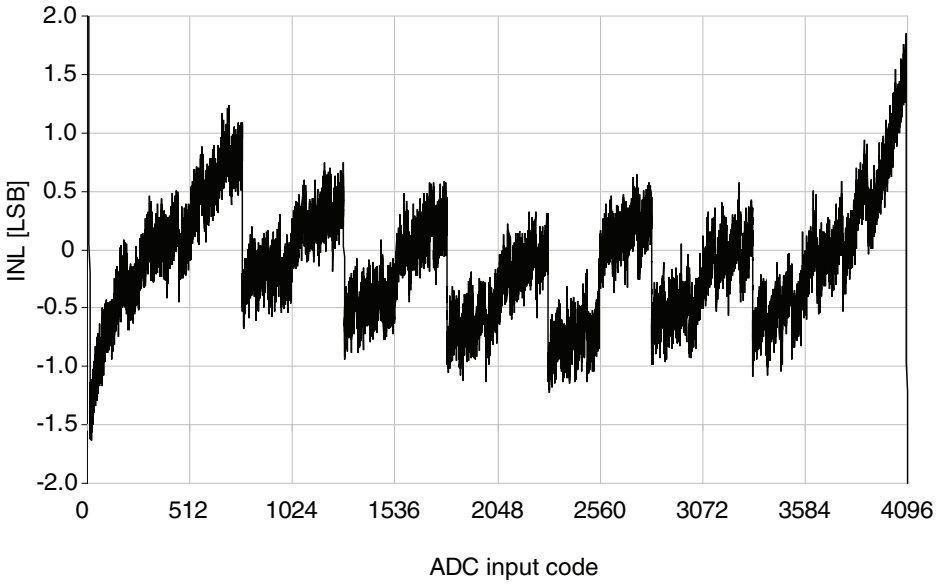



**Figure 37-39. DNL error vs. external $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, external reference.***

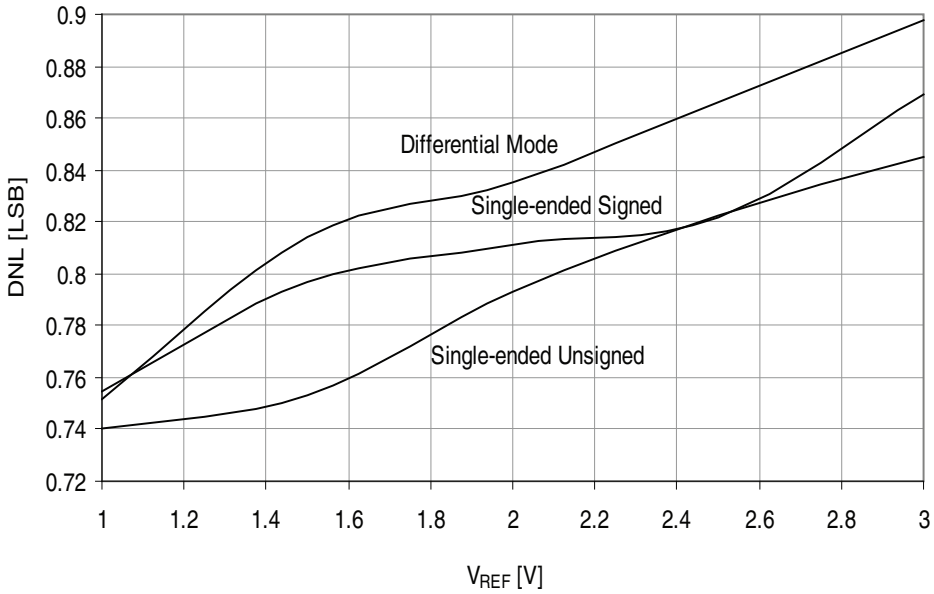


**Figure 37-40. DNL error vs. sample rate.**

***T = 25°C, $V_{CC}$ = 3.6V, $V_{REF}$ = 3.0V external.***

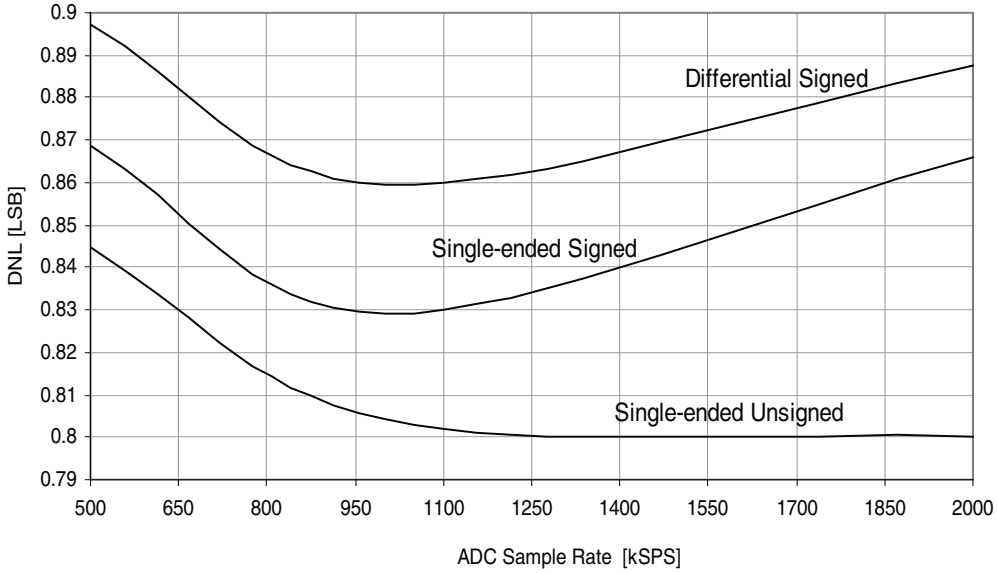



**Figure 37-41. DNL error vs. input code.**

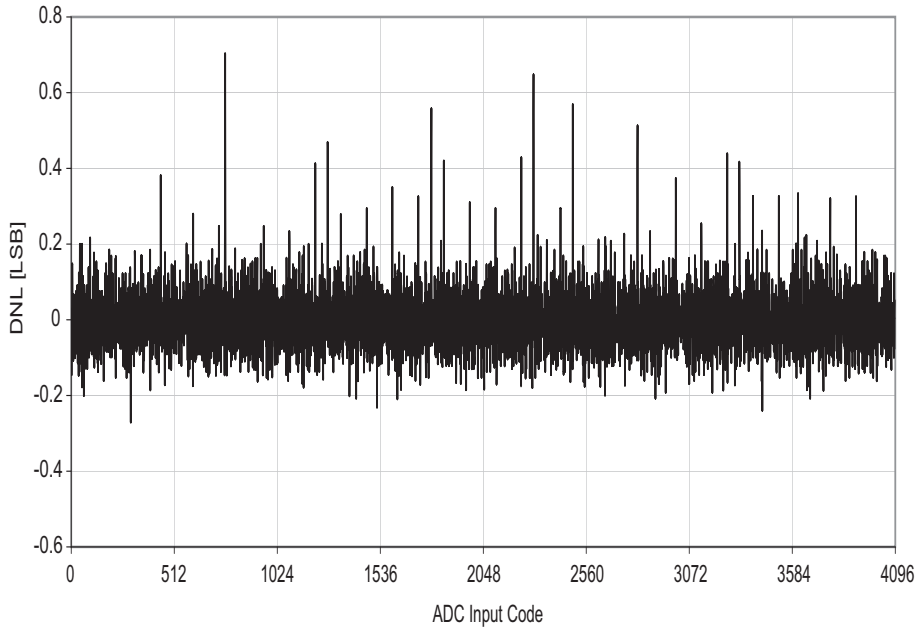


**Figure 37-42. Gain error vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

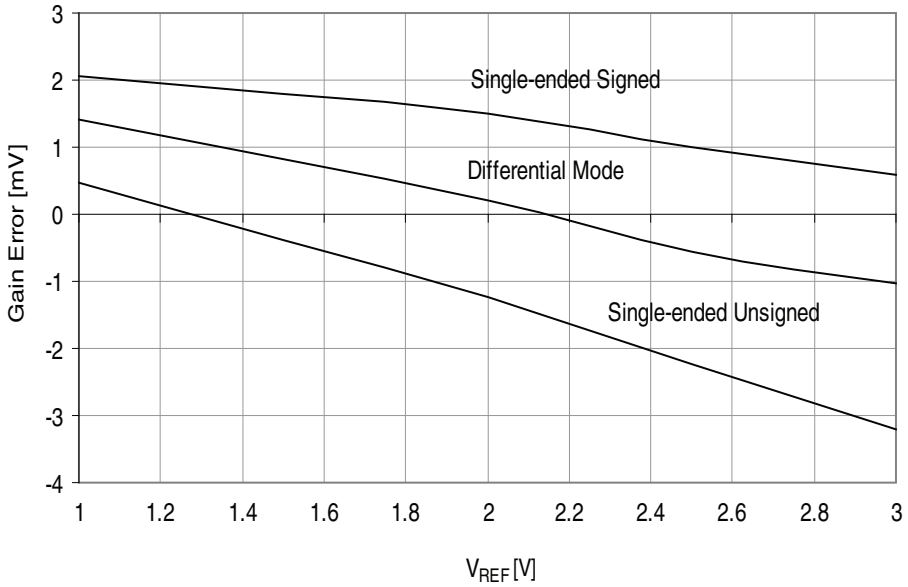



**Figure 37-43. Gain error vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***

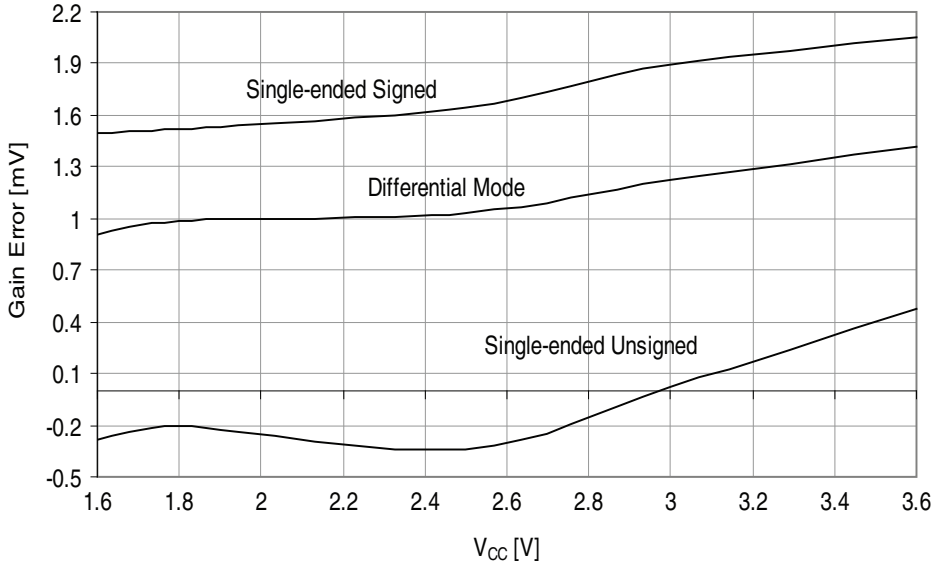


**Figure 37-44. Offset error vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

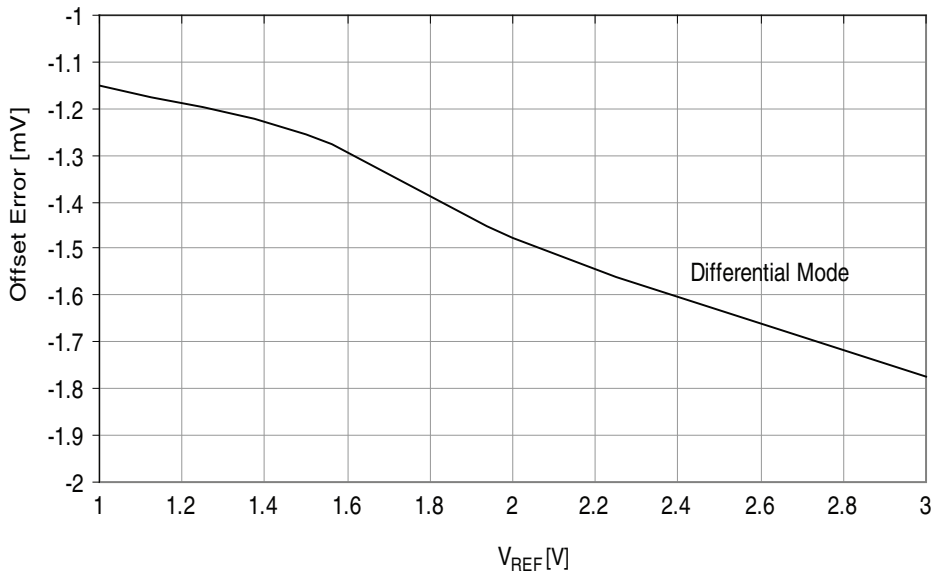



**Figure 37-45. Gain error vs. temperature.**

***$V_{CC}$ = 3.0V, $V_{REF}$ = external 2.0V.***

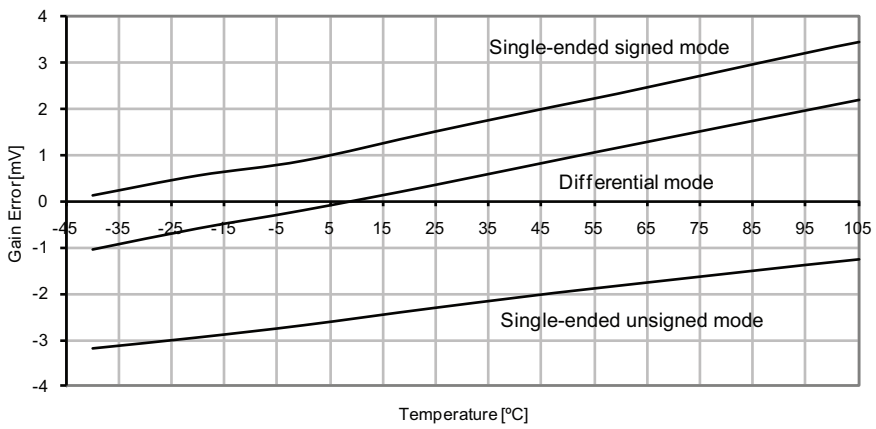


**Figure 37-46. Offset error vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***

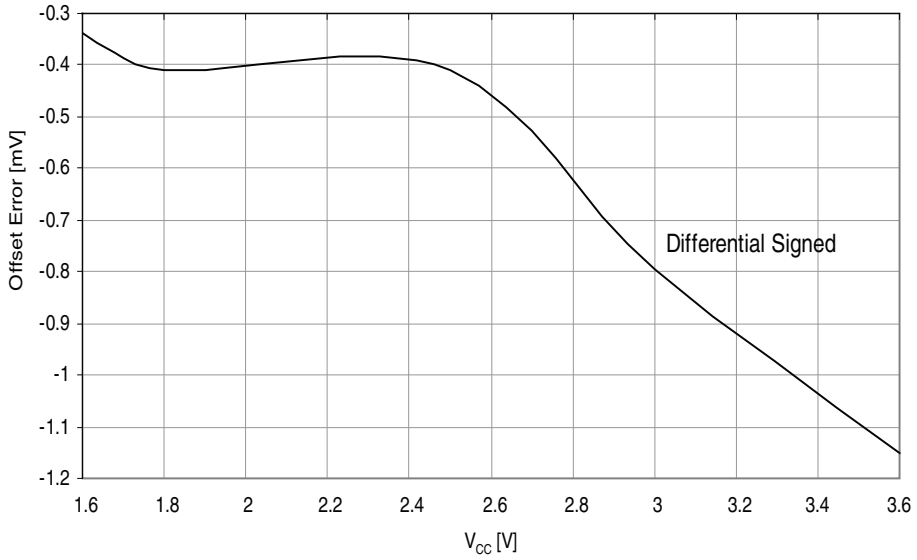



**Figure 37-47. Noise vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

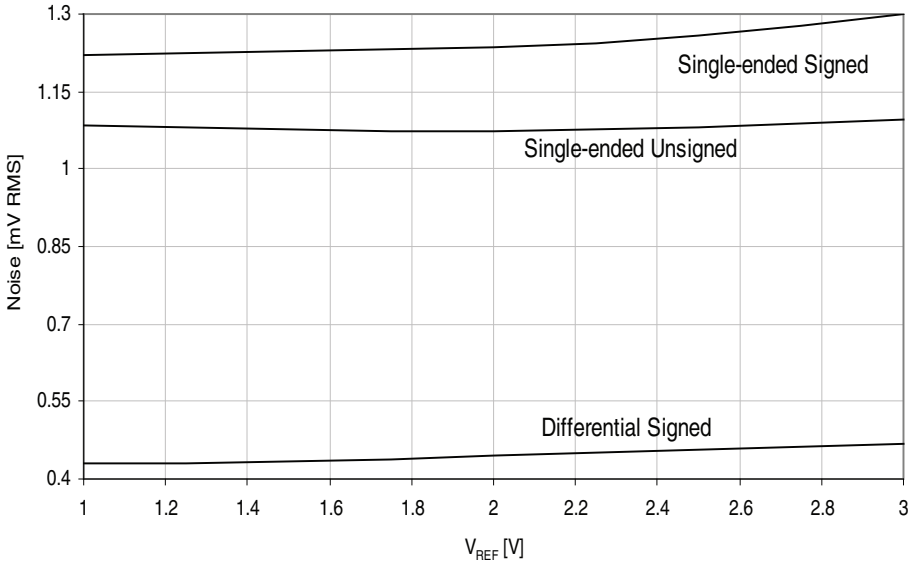
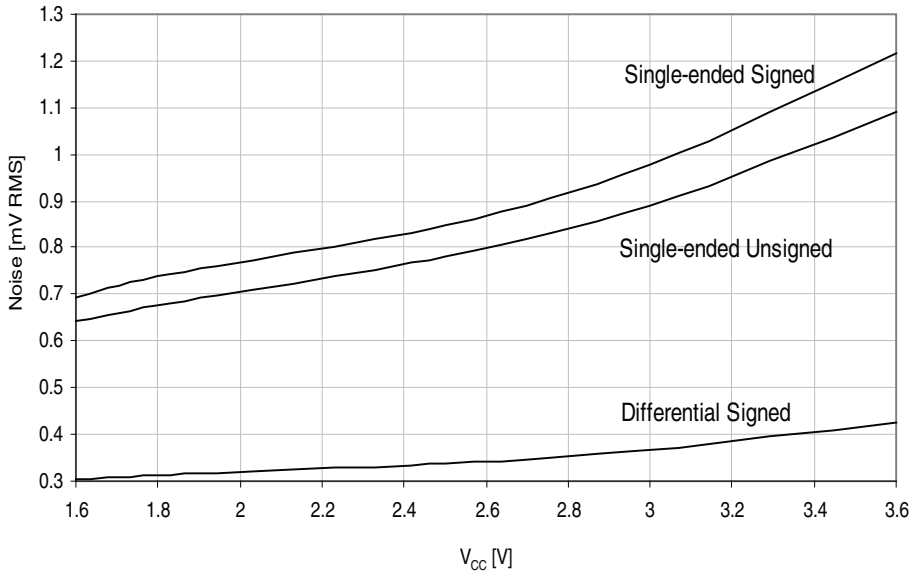


**Figure 37-48. Noise vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***




## 37.1.4 DAC Characteristics

**Figure 37-49. DAC INL error vs. $V_{REF}$.**

***$V_{CC}$ = 3.6V.***

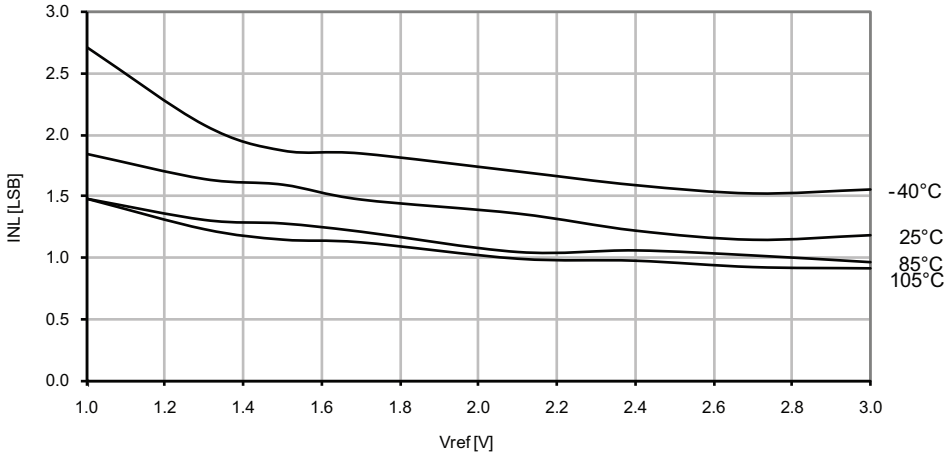


**Figure 37-50. DNL error vs. $V_{REF}$.**

***$V_{CC}$ = 3.6V.***

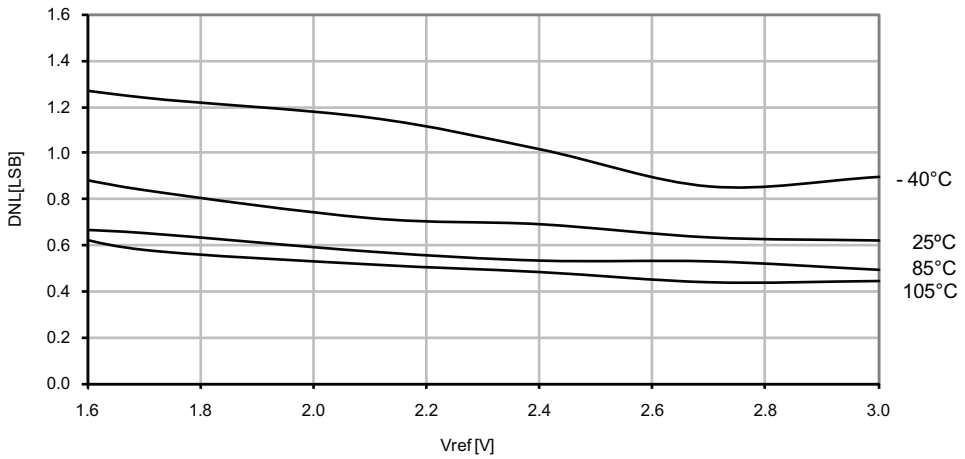
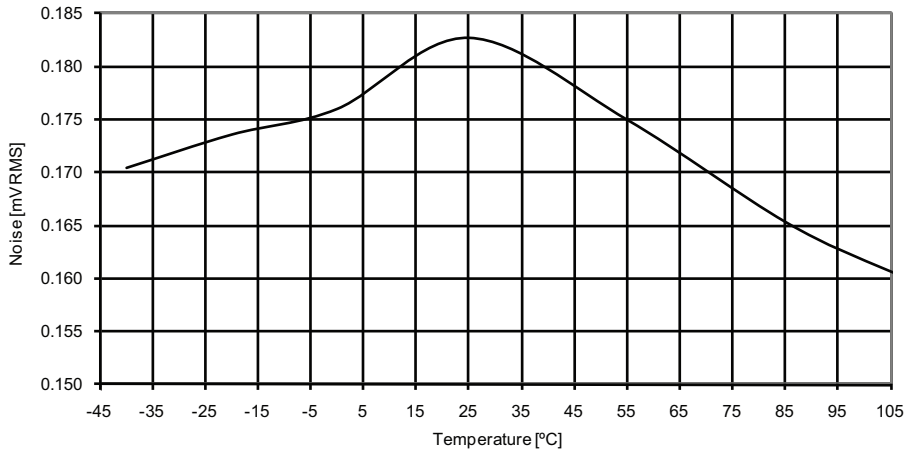



**Figure 37-51. DAC noise vs. temperature.**

***$V_{CC}$ = 3.0V, $V_{REF}$ = 2.4V .***



### 37.1.5 Analog Comparator Characteristics

**Figure 37-52. Analog comparator hysteresis vs. $V_{CC}$.**

***High-speed, small hysteresis.***

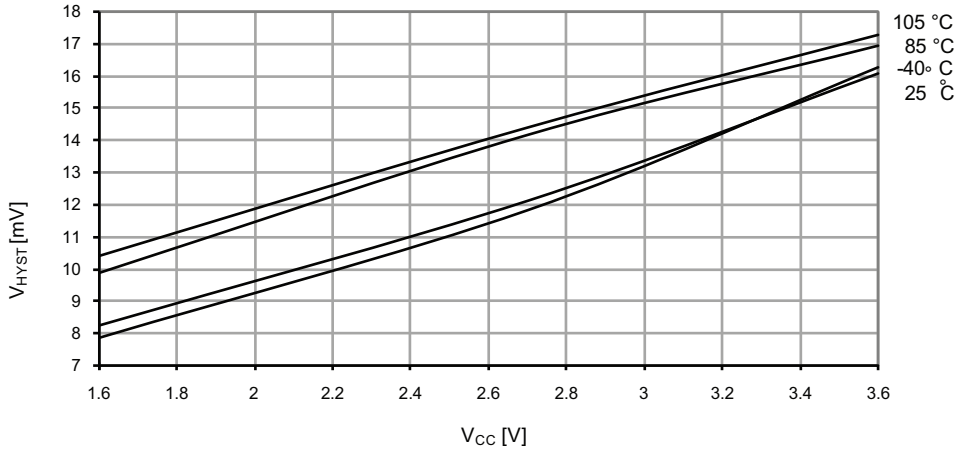



**Figure 37-53. Analog comparator hysteresis vs. $V_{CC}$.**

***Low power, small hysteresis.***

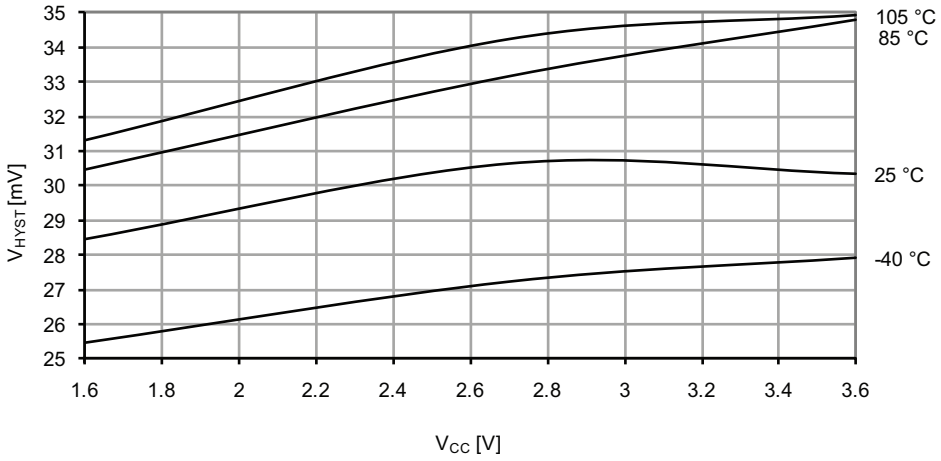


**Figure 37-54. Analog comparator hysteresis vs. $V_{CC}$.**

***High-speed mode, large hysteresis.***

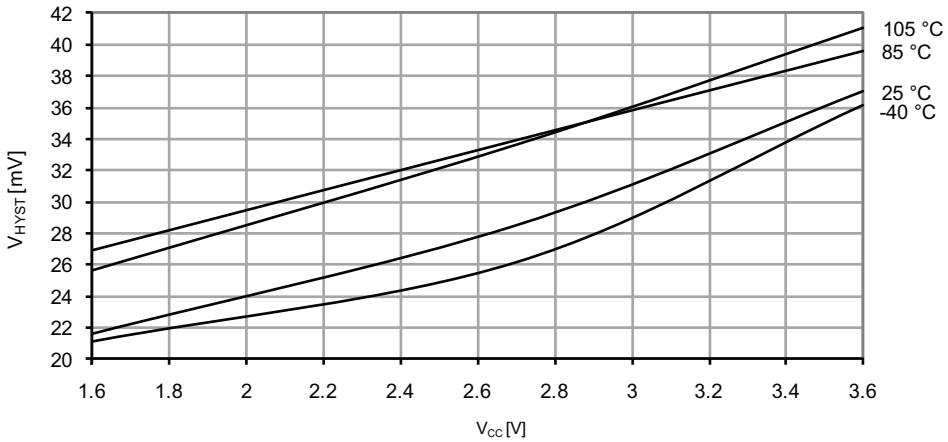



**Figure 37-55. Analog comparator hysteresis vs. $V_{CC}$.**

***Low power, large hysteresis.***

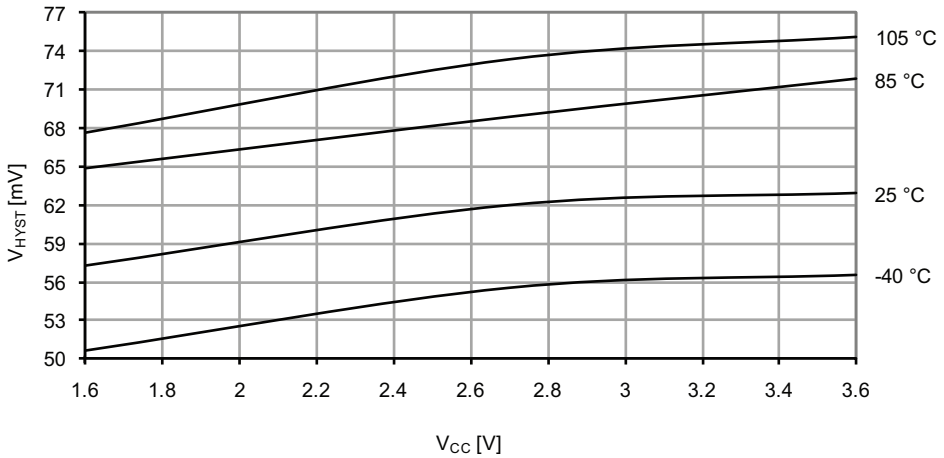


**Figure 37-56. Analog comparator current source vs. calibration value.**

***Temperature = 25°C.***

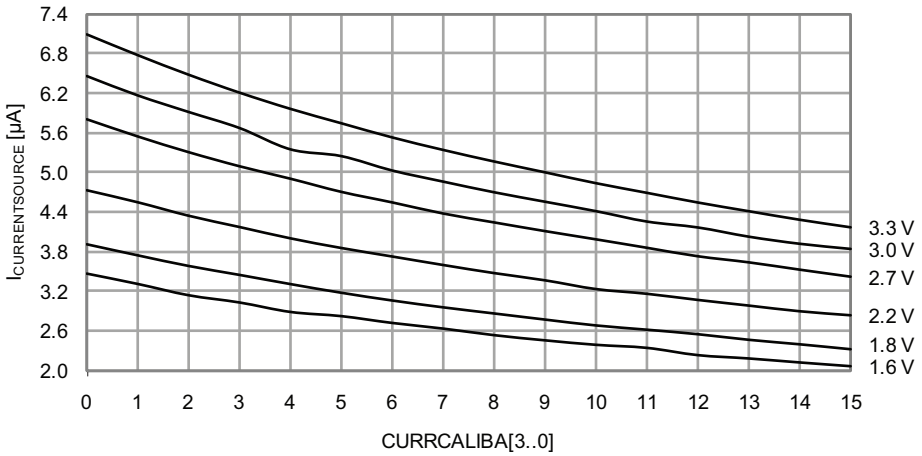



**Figure 37-57. Analog comparator current source vs. calibration value.**

***$V_{CC}$ = 3.0V.***

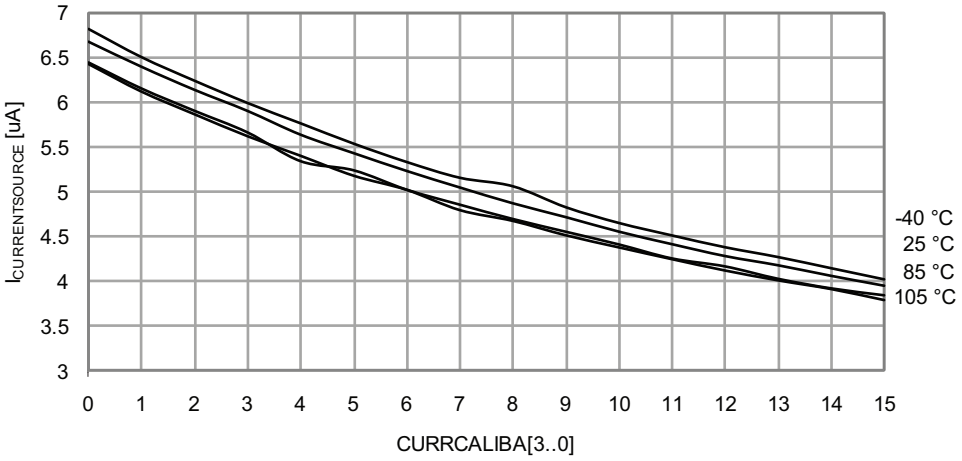
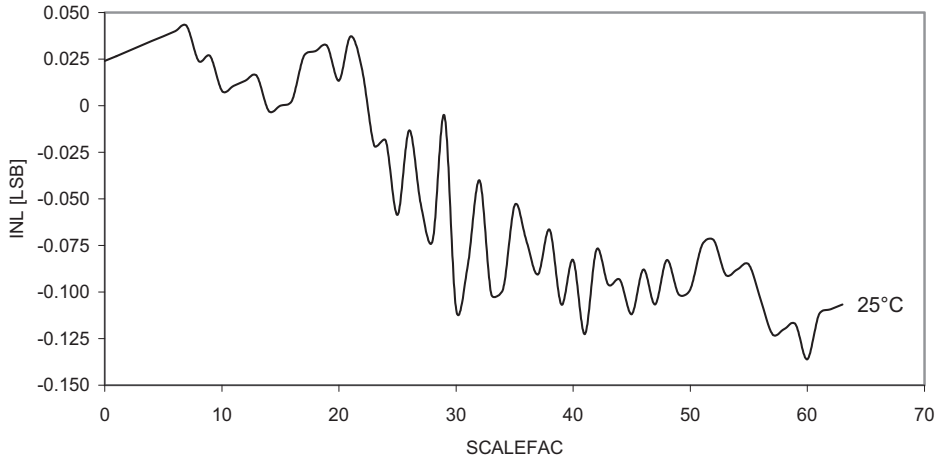


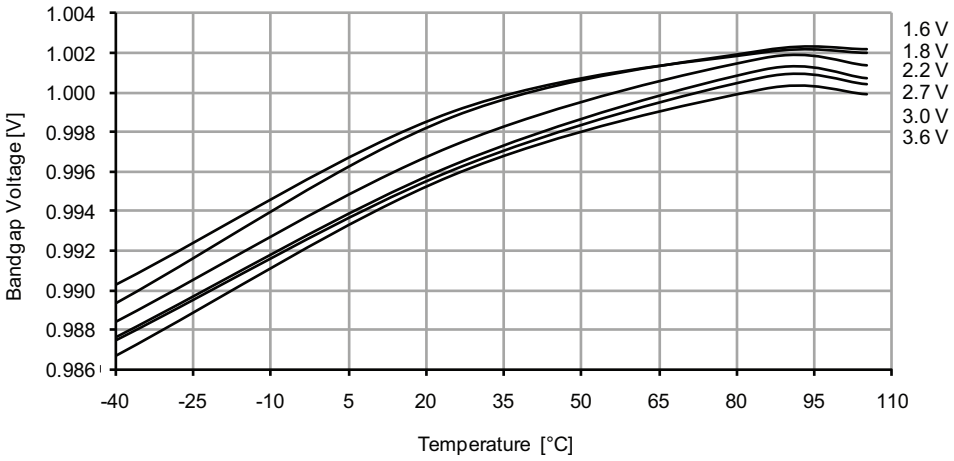
**Figure 37-58. Voltage scaler INL vs. SCALEFAC.**

***T = 25°C, $V_{CC}$ = 3.0V.***




## 37.1.6 Internal 1.0V reference Characteristics

**Figure 37-59. ADC/DAC Internal 1.0V reference vs. temperature.**



### 37.1.7 BOD Characteristics

**Figure 37-60. BOD thresholds vs. temperature.**

***BOD level = 1.6V.***

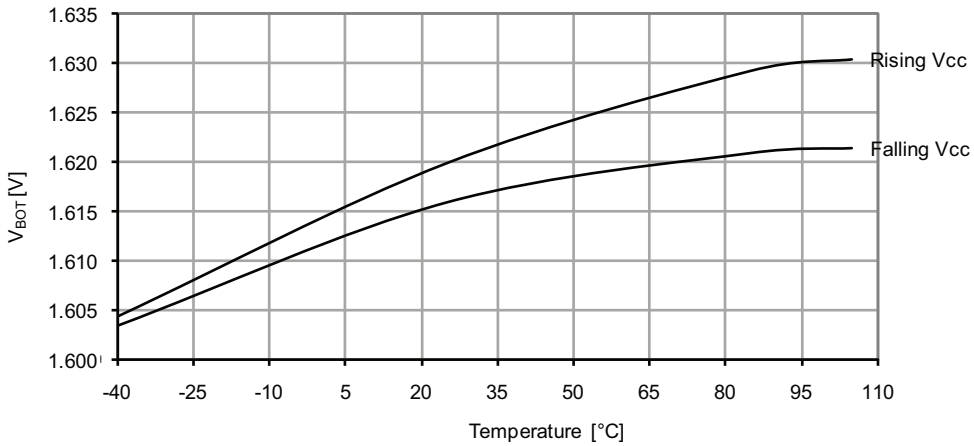
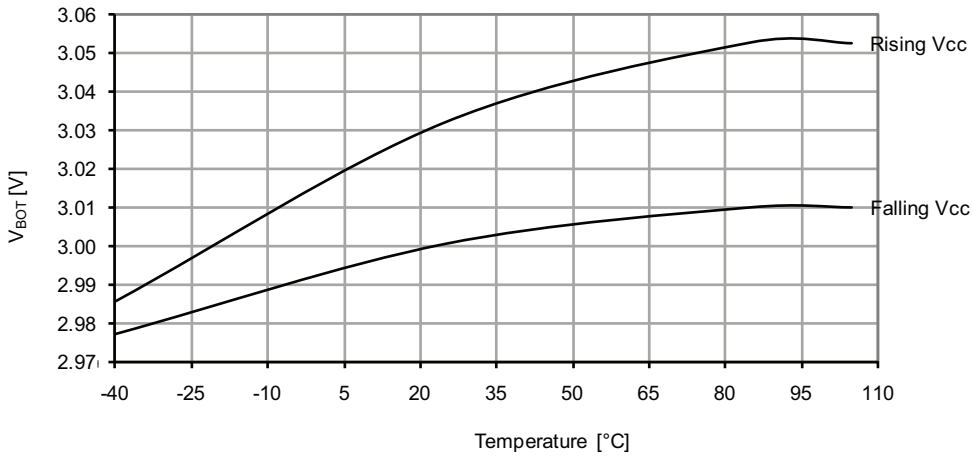



**Figure 37-61. BOD thresholds vs. temperature.**

***BOD level = 3.0V.***



### 37.1.8 External Reset Characteristics

**Figure 37-62. Minimum Reset pin pulse width vs. $V_{CC}$.**

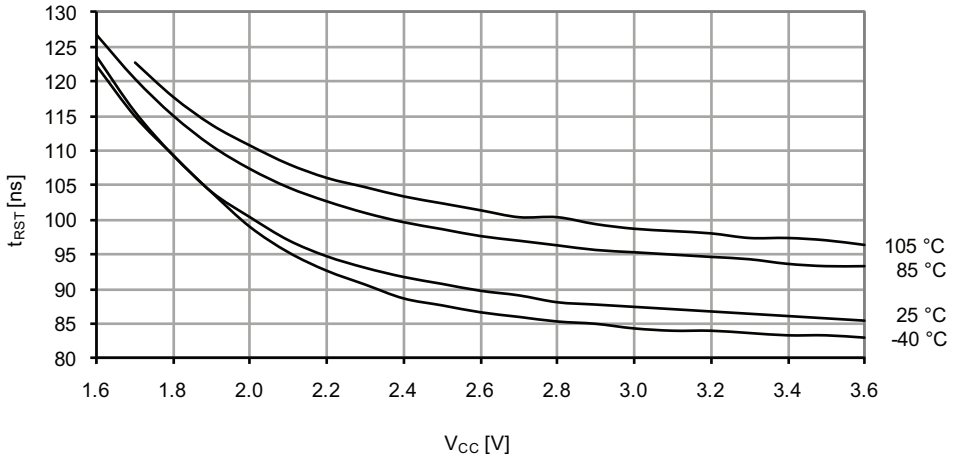



**Figure 37-63. Reset pin pull-up resistor current vs. reset pin voltage.**
***$V_{CC}$ = 1.8V.***

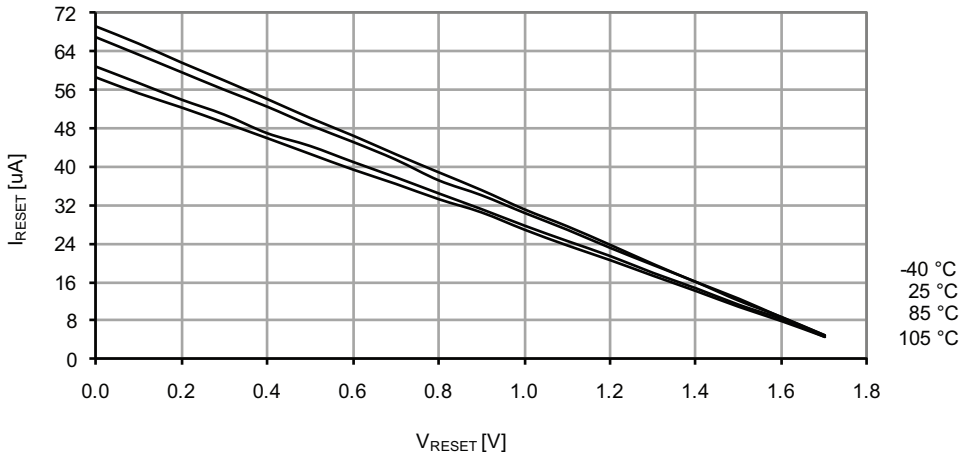


**Figure 37-64. Reset pin pull-up resistor current vs. reset pin voltage.**

***$V_{CC}$ = 3.0V.***

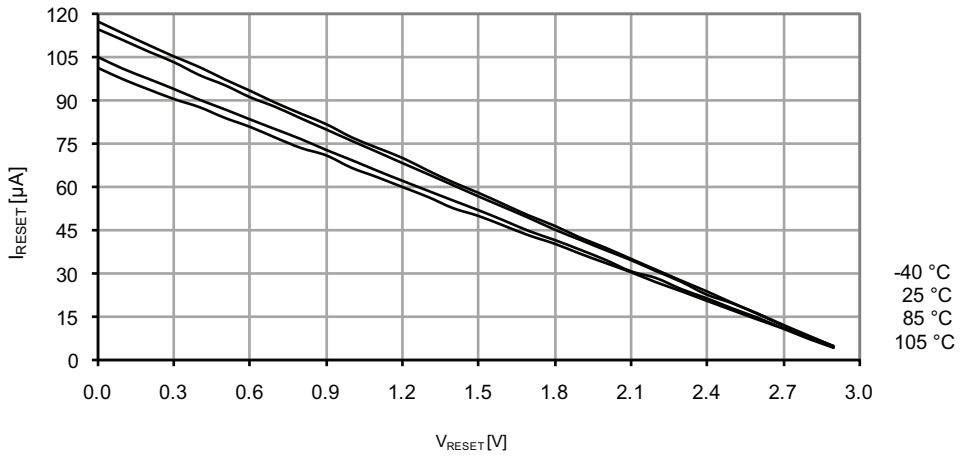



**Figure 37-65. Reset pin pull-up resistor current vs. reset pin voltage.**

***$V_{CC}$ = 3.3V.***

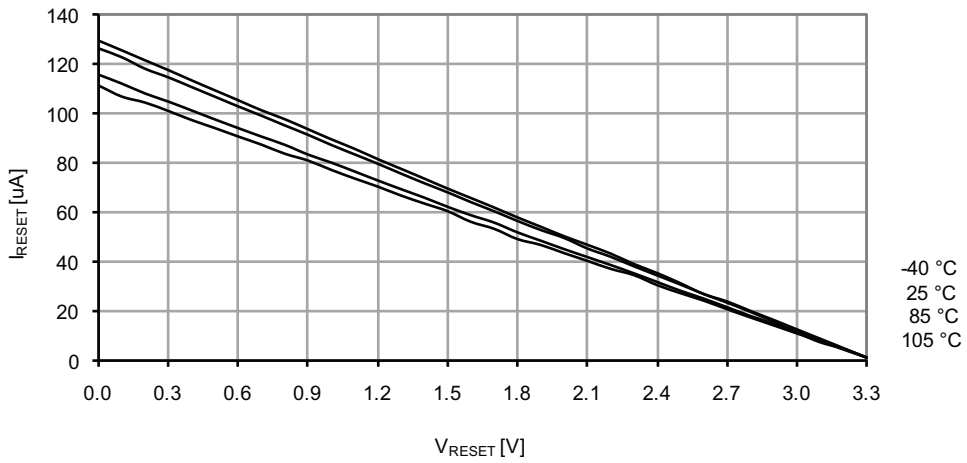


**Figure 37-66. Reset pin input threshold voltage vs. $V_{CC}$.**

***$V_{IH}$ - Reset pin read as "1".***

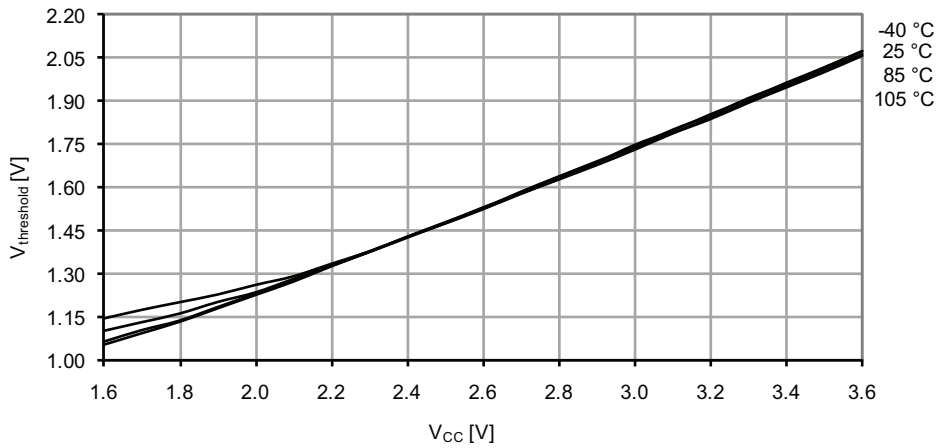
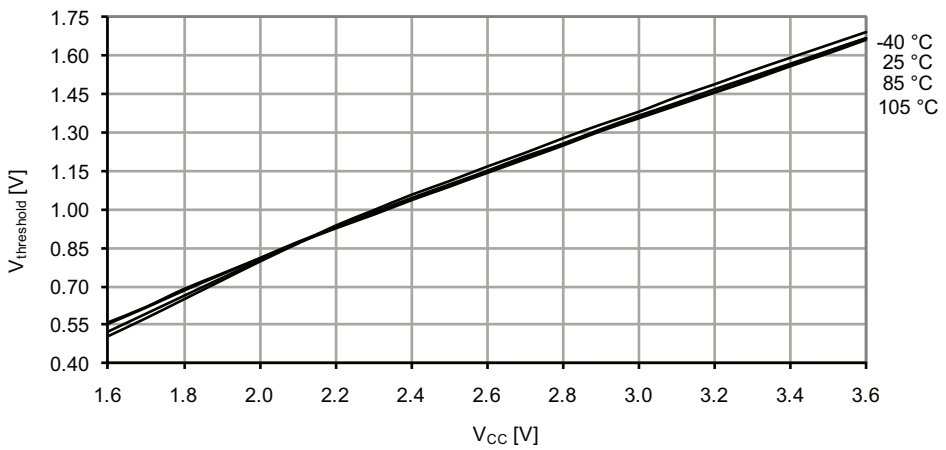



**Figure 37-67. Reset pin input threshold voltage vs. $V_{CC}$.**

***$V_{IL}$ - Reset pin read as "0".***



### 37.1.9 Power-on Reset Characteristics

**Figure 37-68. Power-on reset current consumption vs. $V_{CC}$.**

***BOD level = 3.0V, enabled in continuous mode.***

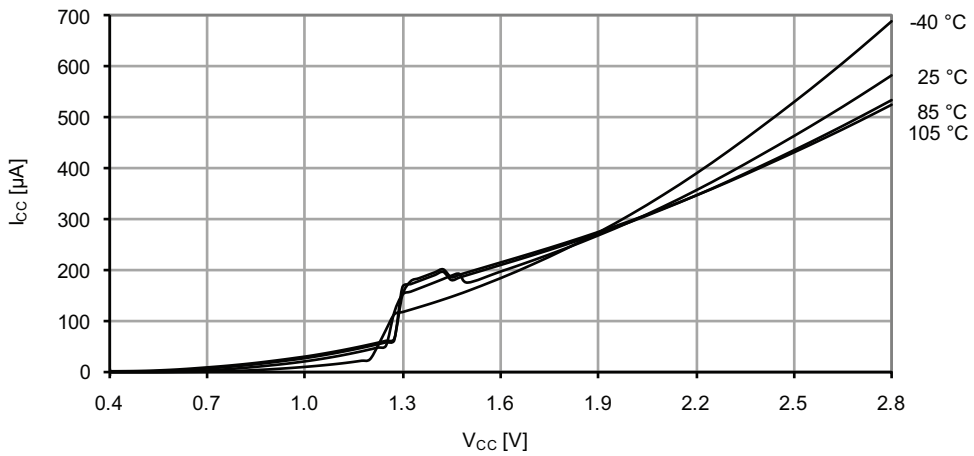
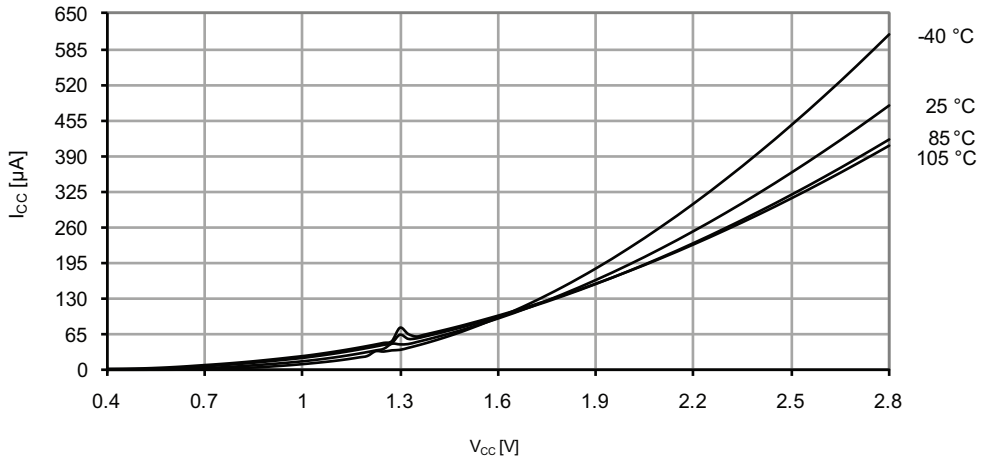



**Figure 37-69. Power-on reset current consumption vs. $V_{CC}$.**

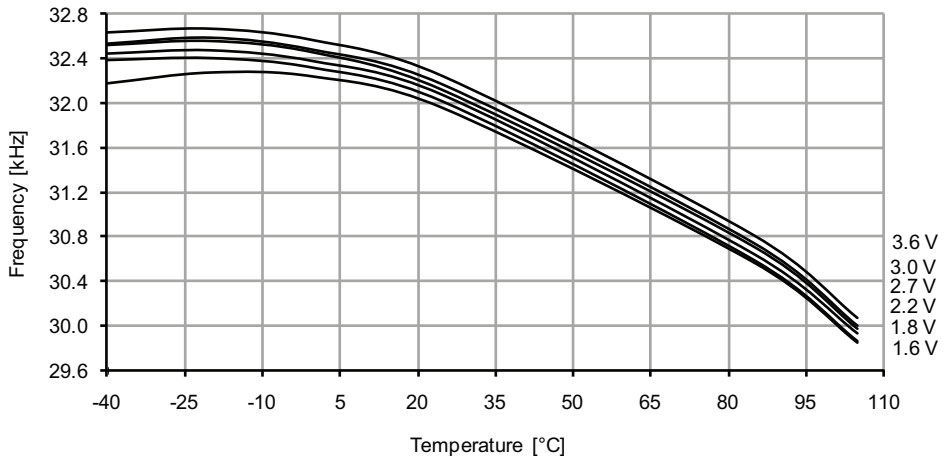
***BOD level = 3.0V, enabled in sampled mode.***



## 37.1.10 Oscillator Characteristics

### 37.1.10.1 Ultra Low-Power internal oscillator

**Figure 37-70. Ultra Low-Power internal oscillator frequency vs. temperature.**




### 37.1.10.2 32.768kHz Internal Oscillator

**Figure 37-71. 32.768kHz internal oscillator frequency vs. temperature.**

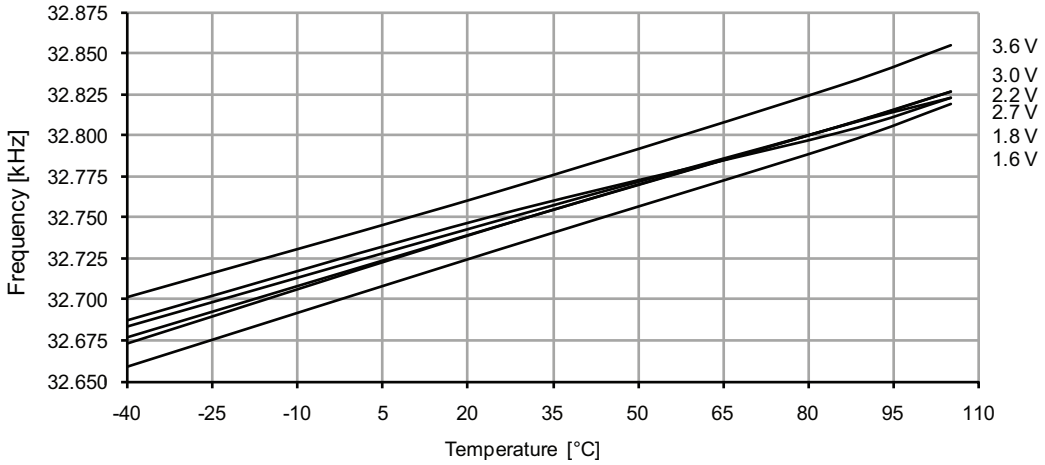
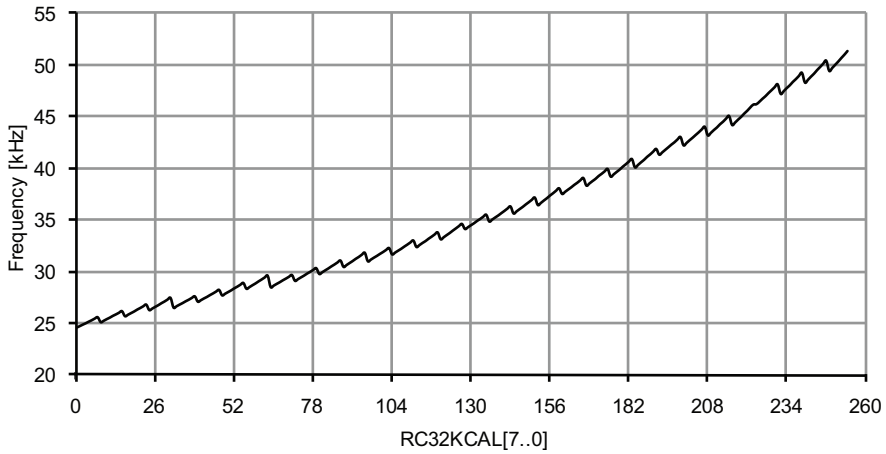


**Figure 37-72. 32.768kHz internal oscillator frequency vs. calibration value.**

***$V_{CC}$ = 3.0V, T = 25°C.***




### 37.1.10.3 2MHz Internal Oscillator

**Figure 37-73. 2MHz internal oscillator frequency vs. temperature.**

***DFLL disabled.***

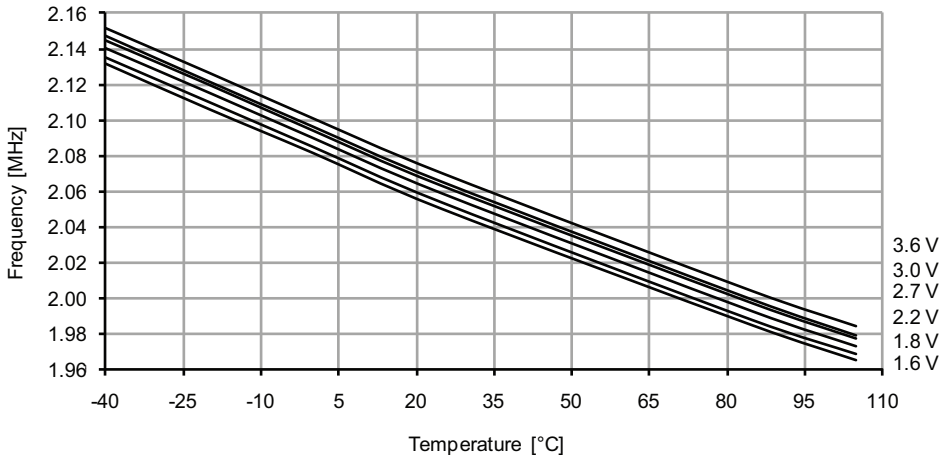


**Figure 37-74. 2MHz internal oscillator frequency vs. temperature.**

***DFLL enabled, from the 32.768kHz internal oscillator .***

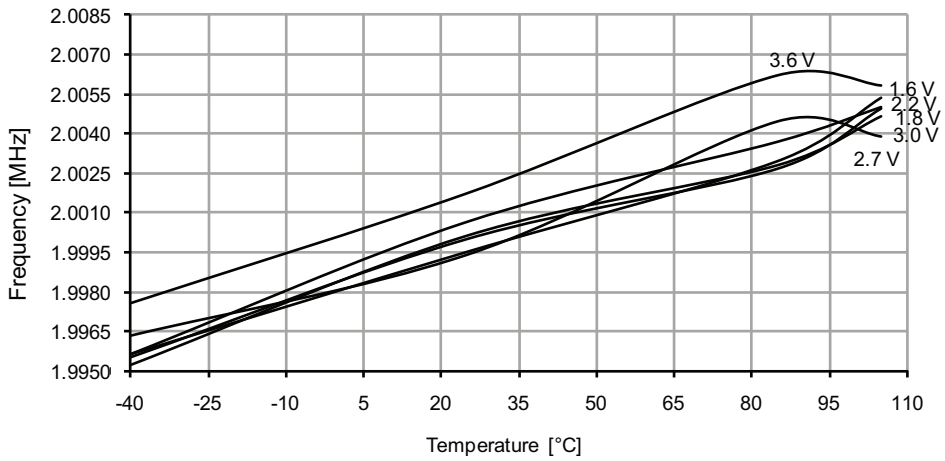
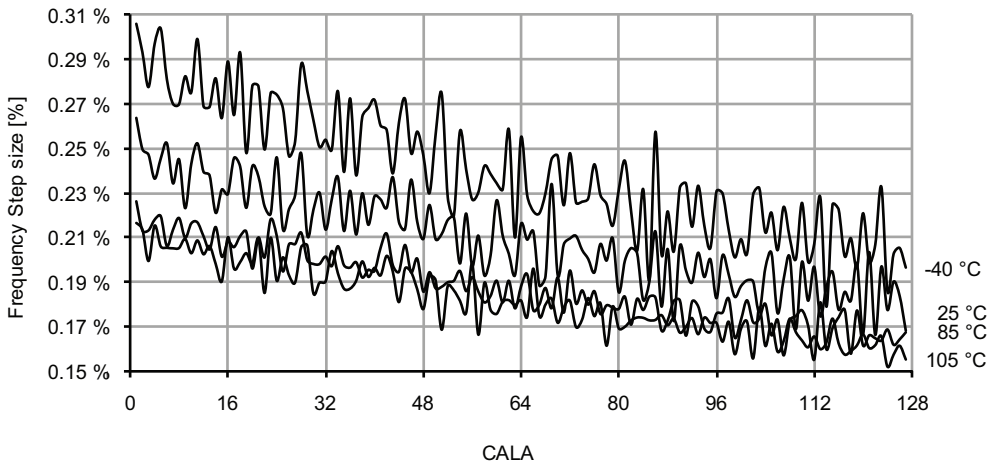



**Figure 37-75. 2MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3V.***



### 37.1.10.4 32MHz Internal Oscillator

**Figure 37-76. 32MHz internal oscillator frequency vs. temperature.**

***DFLL disabled.***

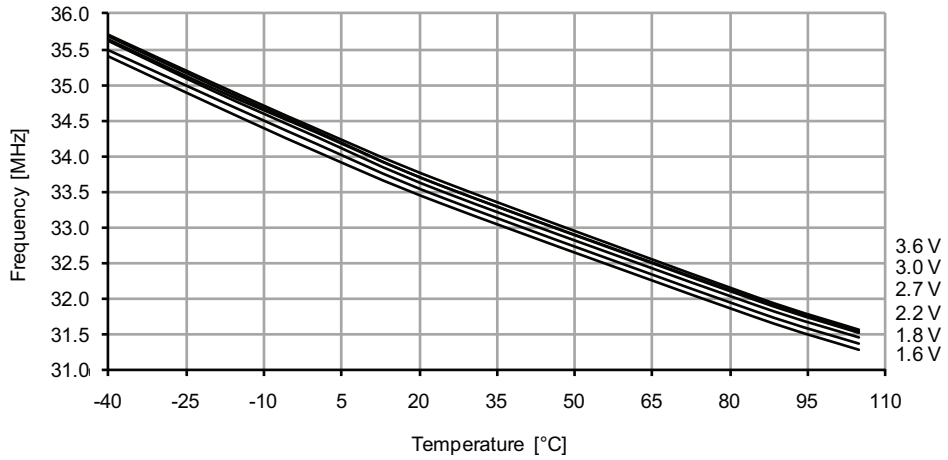



**Figure 37-77. 32MHz internal oscillator frequency vs. temperature.**

***DFLL enabled, from the 32.768kHz internal oscillator.***

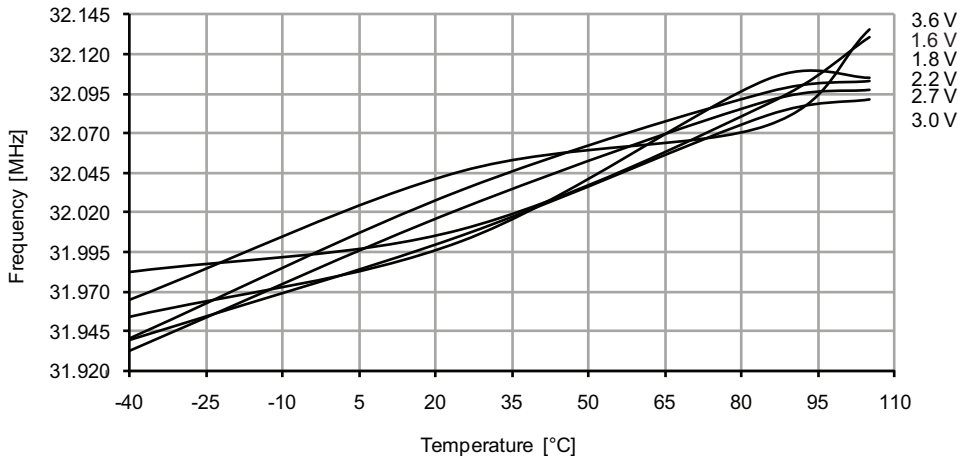


**Figure 37-78. 32MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3.0V.***

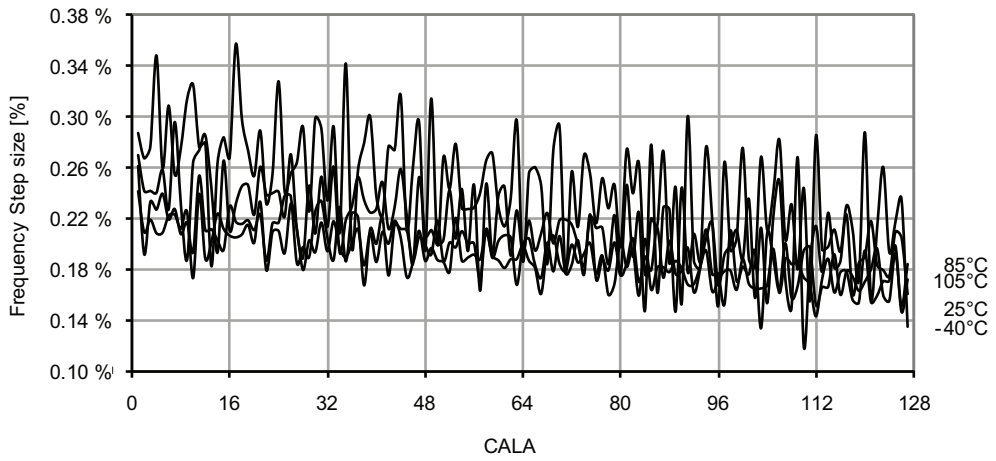
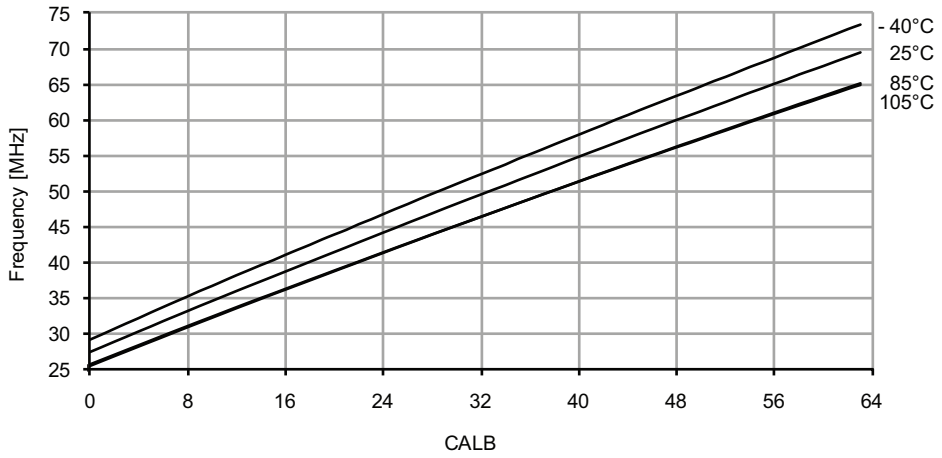



**Figure 37-79. 32MHz internal oscillator frequency vs. CALB calibration value.**

***$V_{CC}$ = 3.0V.***



### 37.1.10.5 32MHz internal oscillator calibrated to 48MHz

**Figure 37-80. 48MHz internal oscillator frequency vs. temperature.**

***DFLL disabled.***

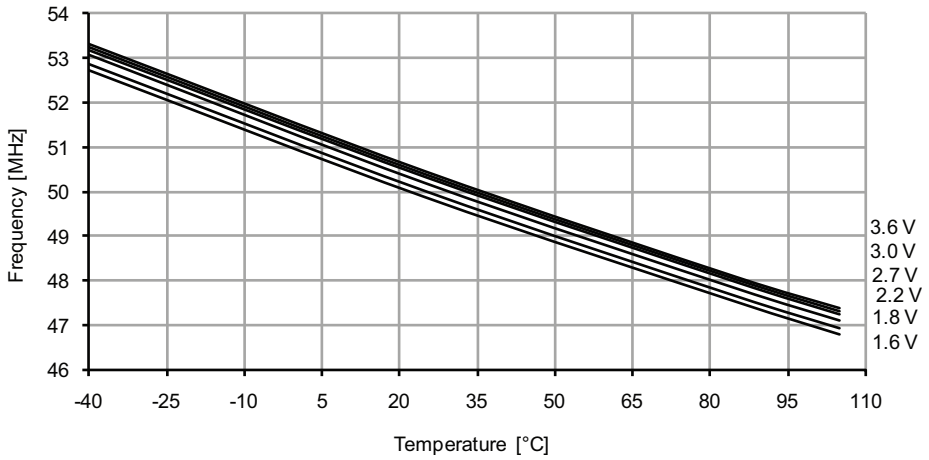



**Figure 37-81. 48MHz internal oscillator frequency vs. temperature.**

***DFLL enabled, from the 32.768kHz internal oscillator.***

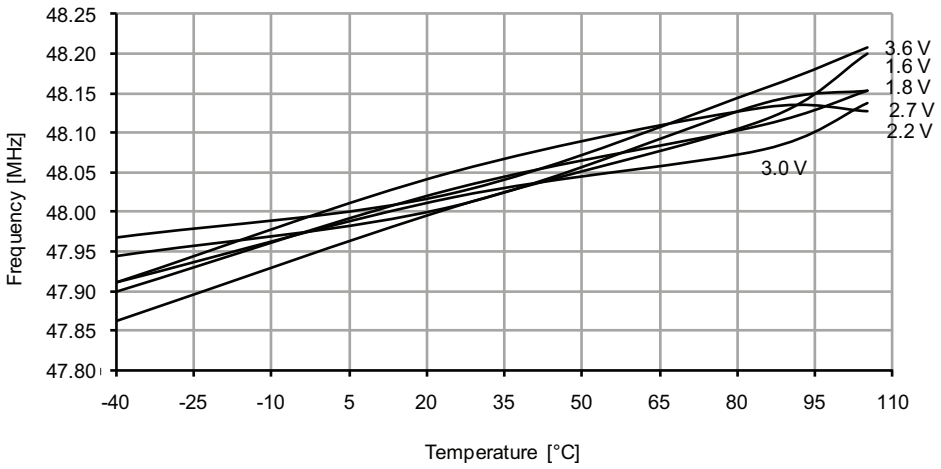
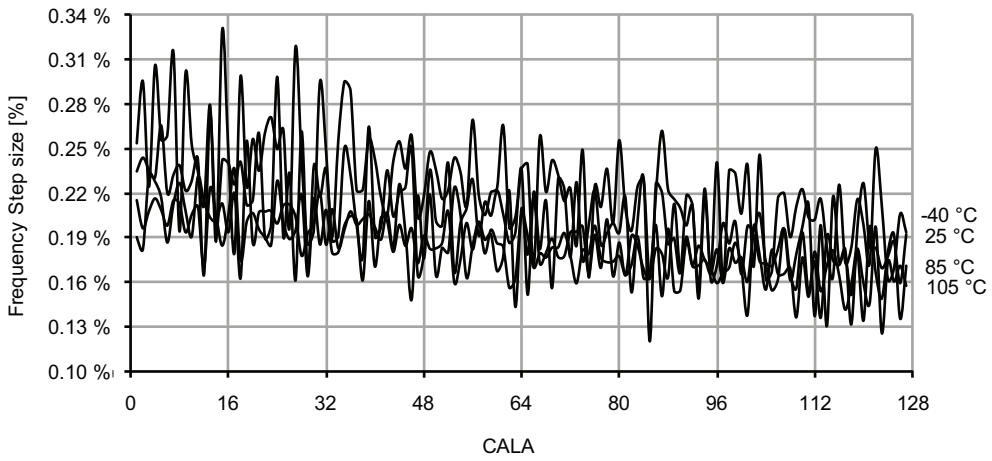


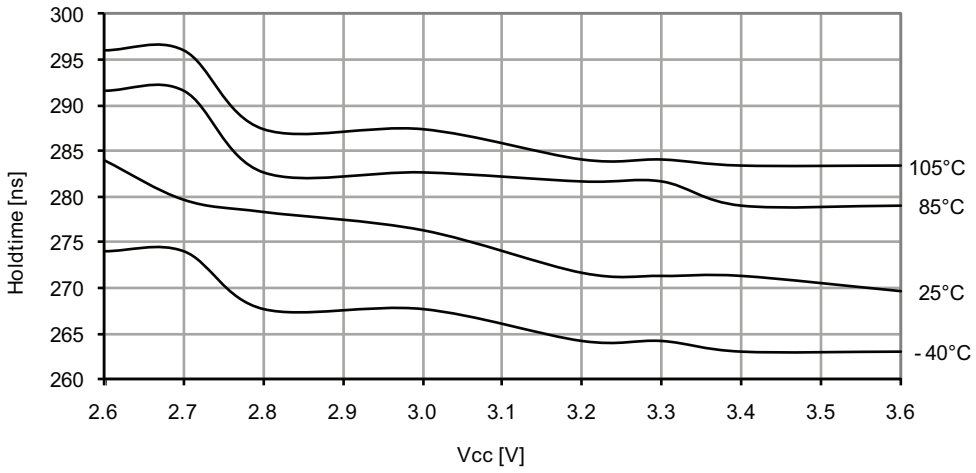
**Figure 37-82. 48MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3.0V.***



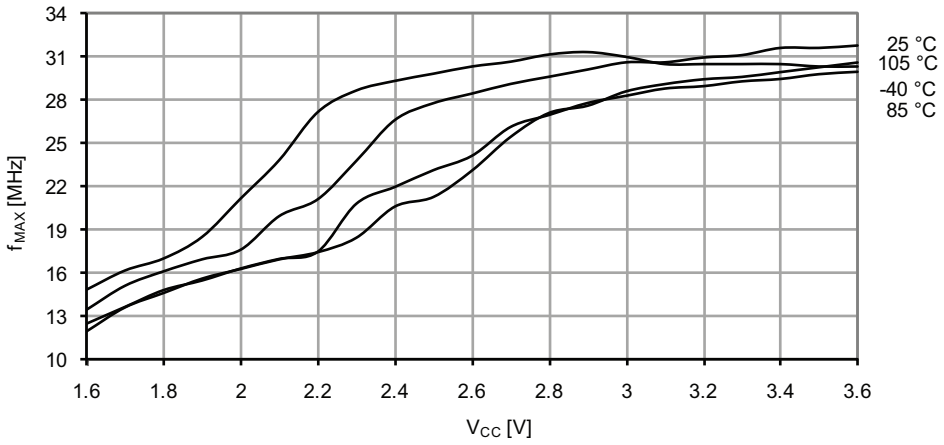

## 37.1.11 Two-Wire Interface characteristics

**Figure 37-83. SDA hold time vs. supply voltage.**



### 37.1.12 PDI characteristics

**Figure 37-84. Maximum PDI frequency vs. $V_{CC}$.**



## 37.2 ATxmega32A4U

### 37.2.1 Current consumption

#### 37.2.1.1 Active mode supply current

**Figure 37-85.Active supply current vs. frequency.**
***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

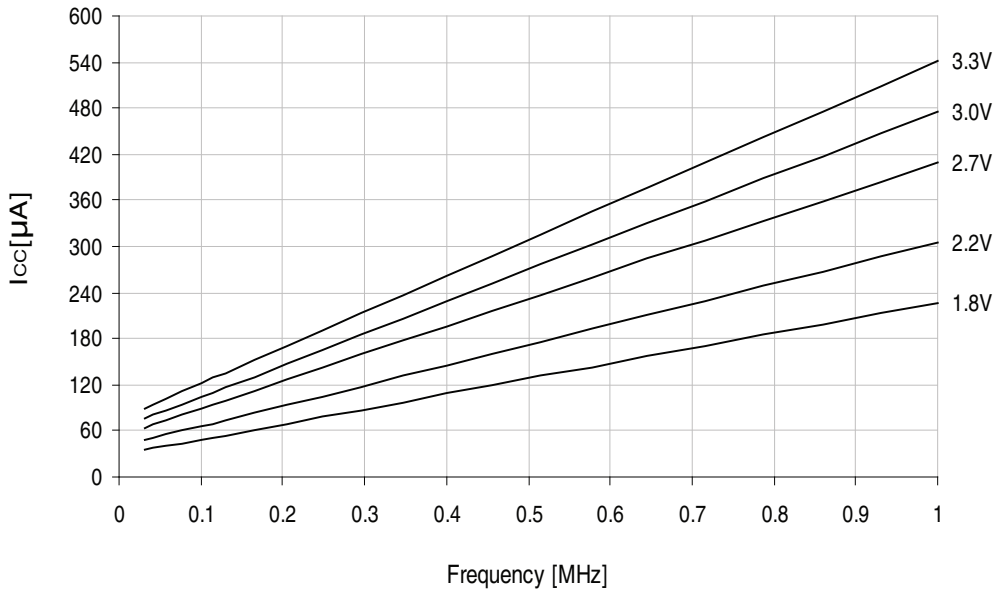



**Figure 37-86.Active supply current vs. frequency.**
***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C.***

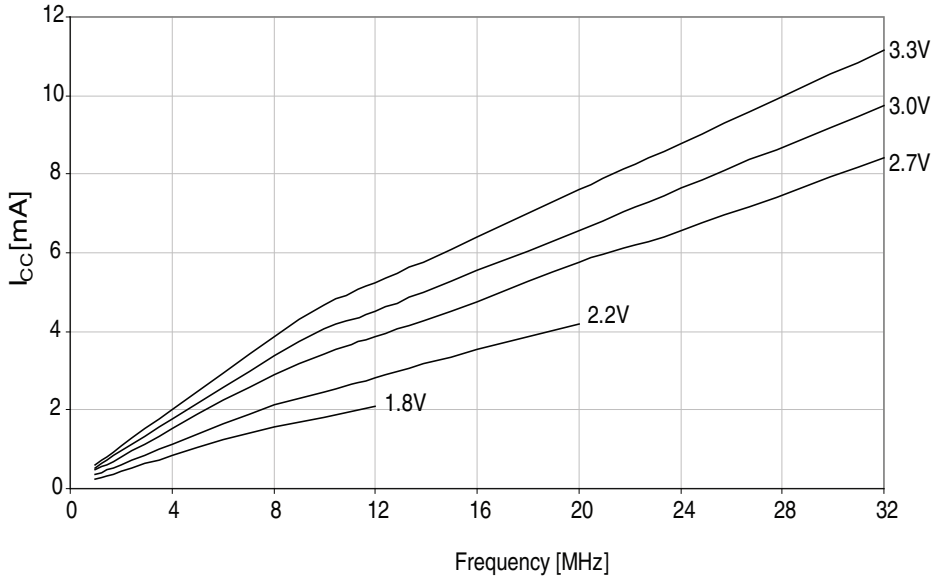


**Figure 37-87.Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32.768kHz internal oscillator.***

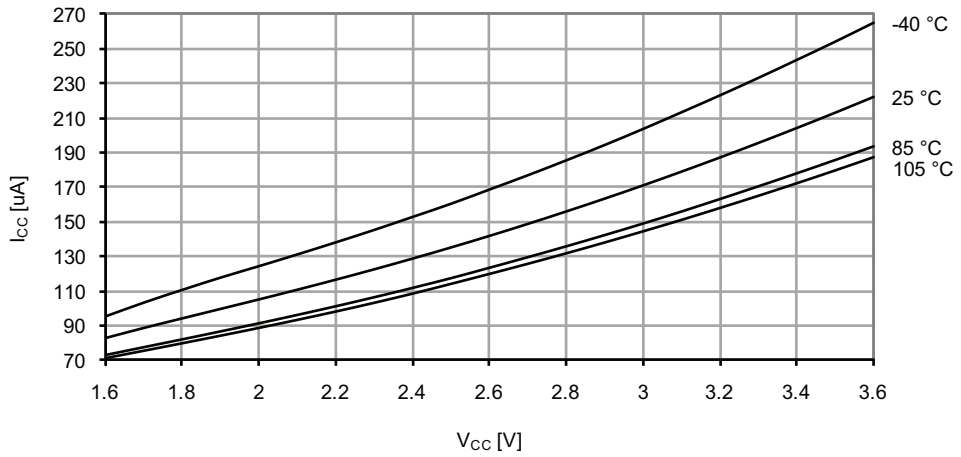



**Figure 37-88.Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock.***

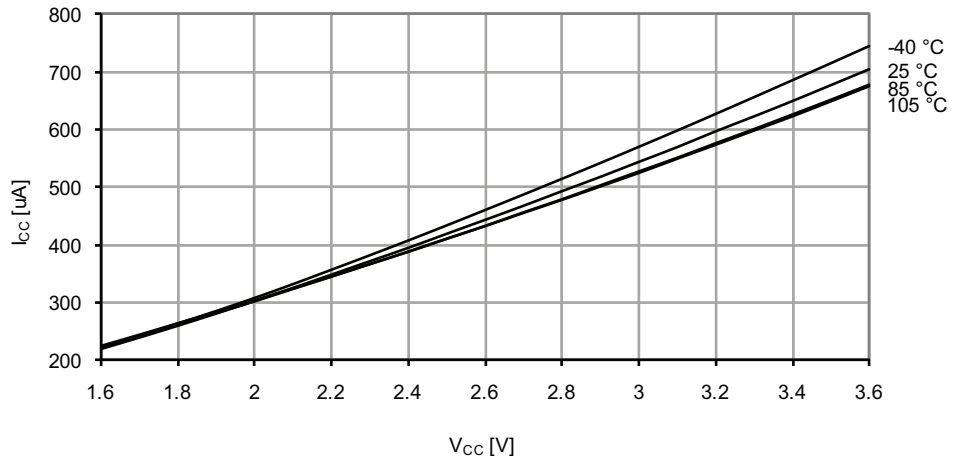


**Figure 37-89.Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator.***

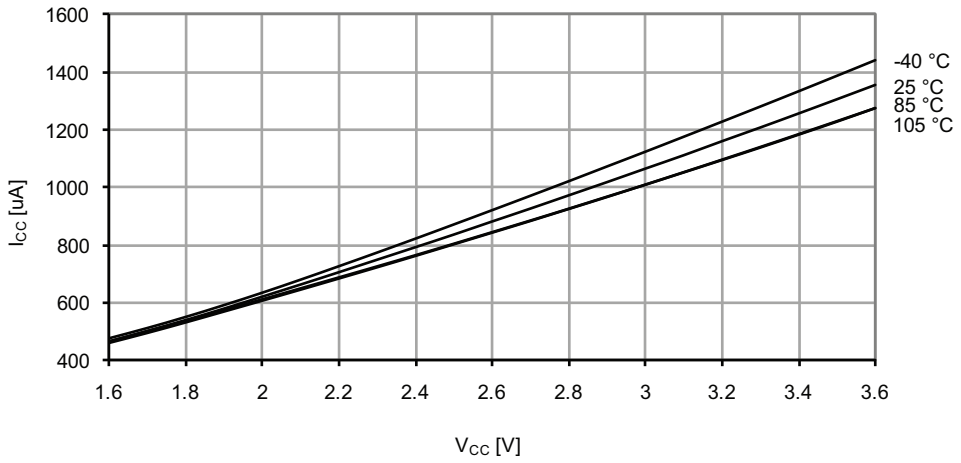



**Figure 37-90.Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz.***

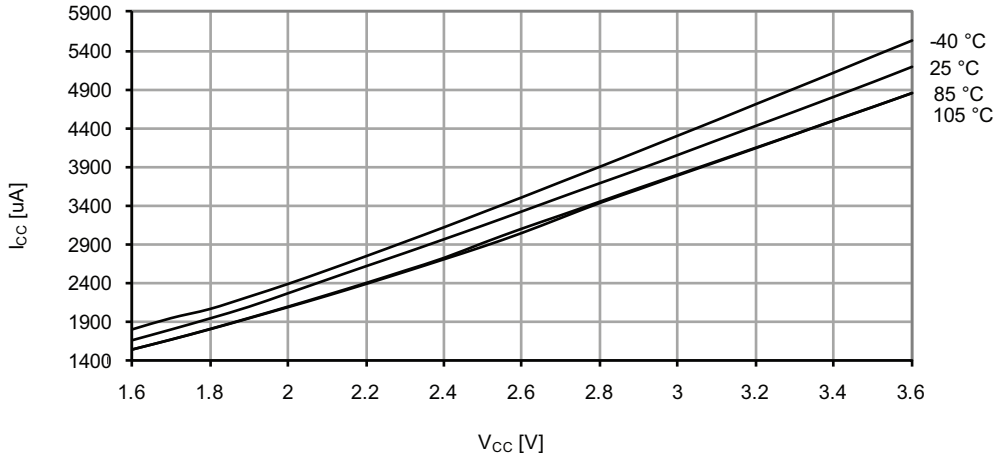
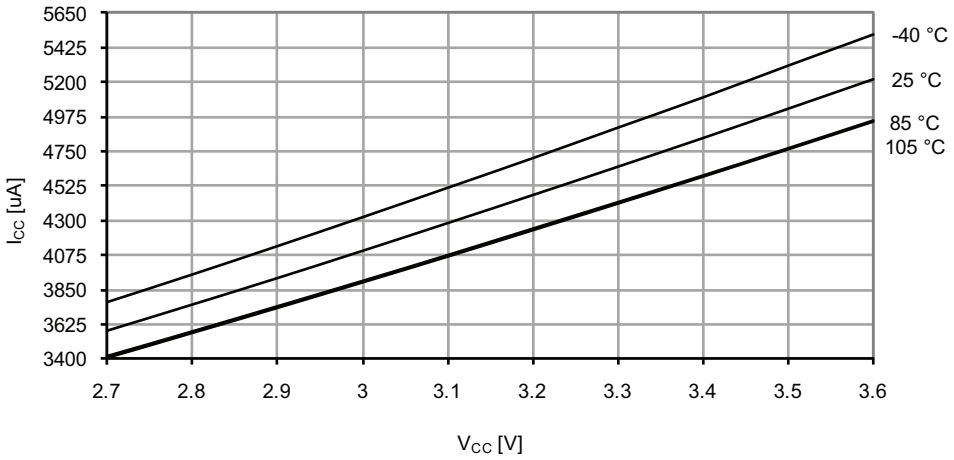


**Figure 37-91.Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator.***




### 37.2.1.2 Idle mode supply current

**Figure 37-92.Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

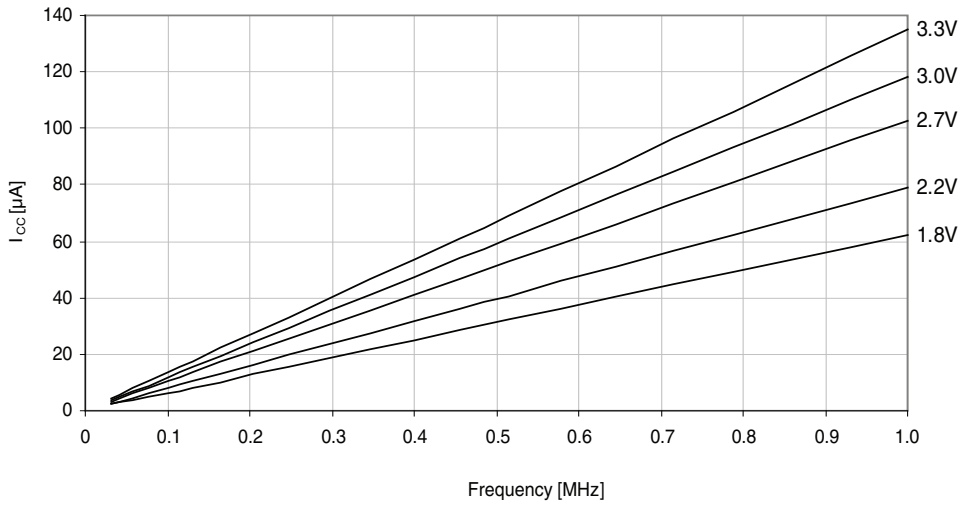


**Figure 37-93.Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C.***

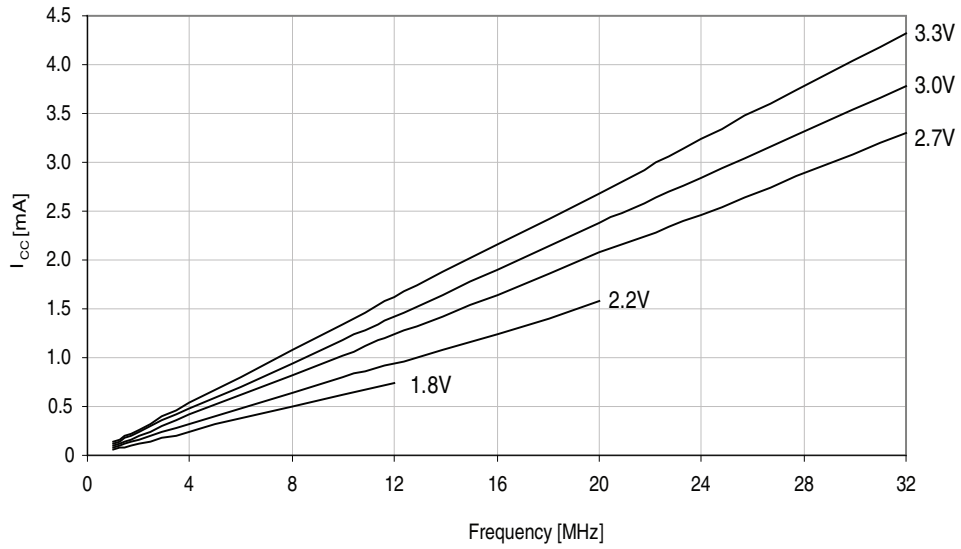



**Figure 37-94. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32.768kHz internal oscillator.***

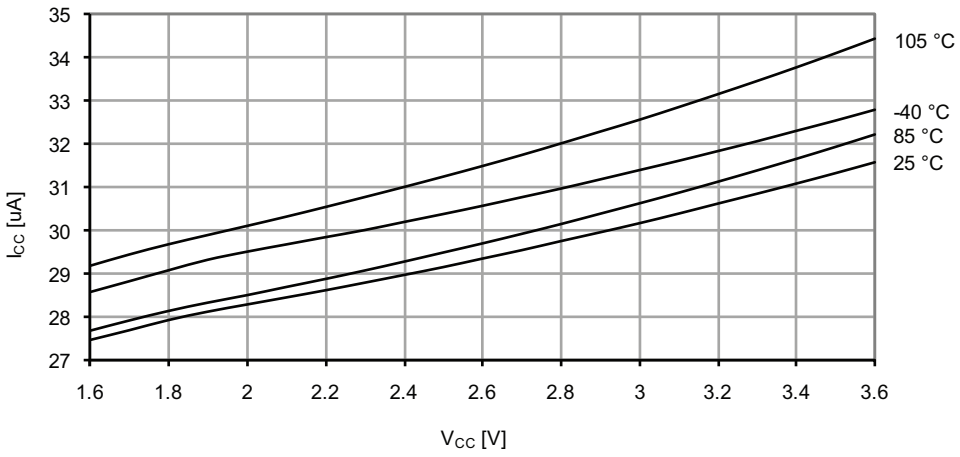


**Figure 37-95. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock.***

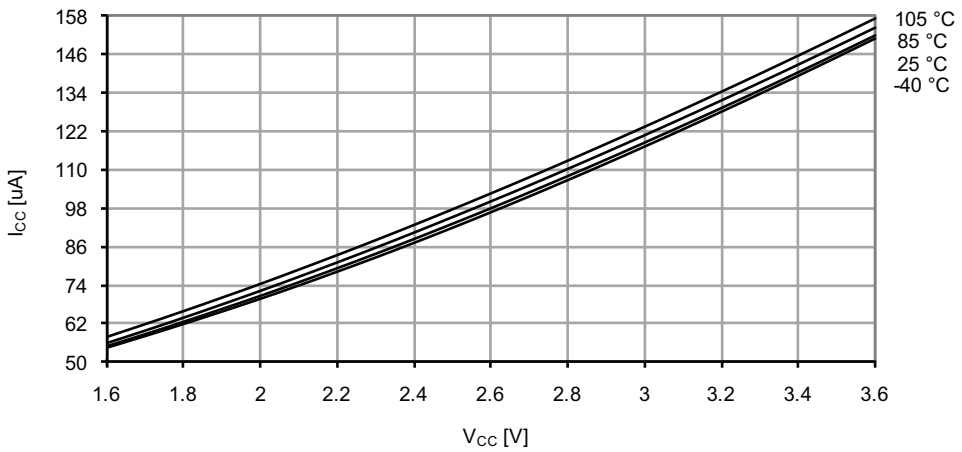



**Figure 37-96. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator.***

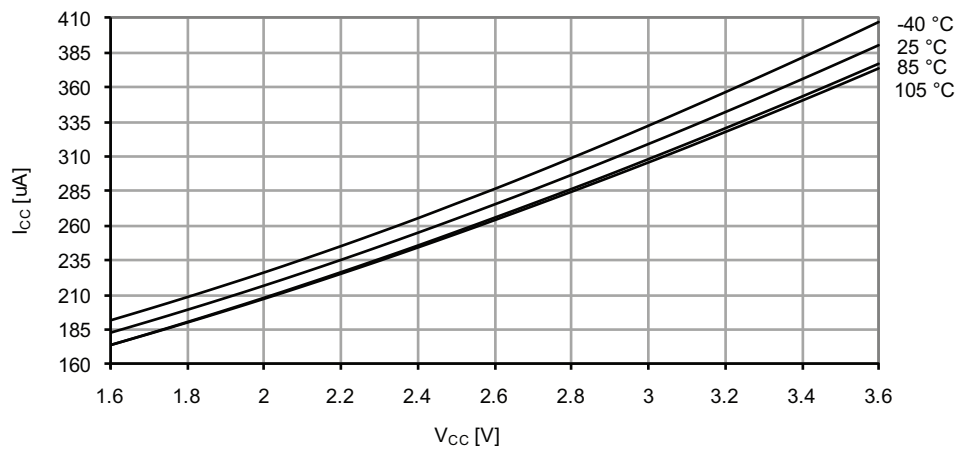


**Figure 37-97. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz.***

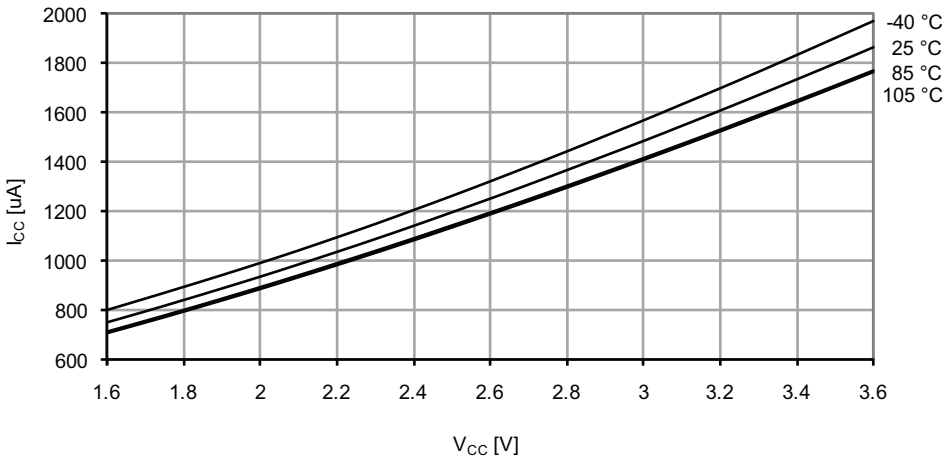
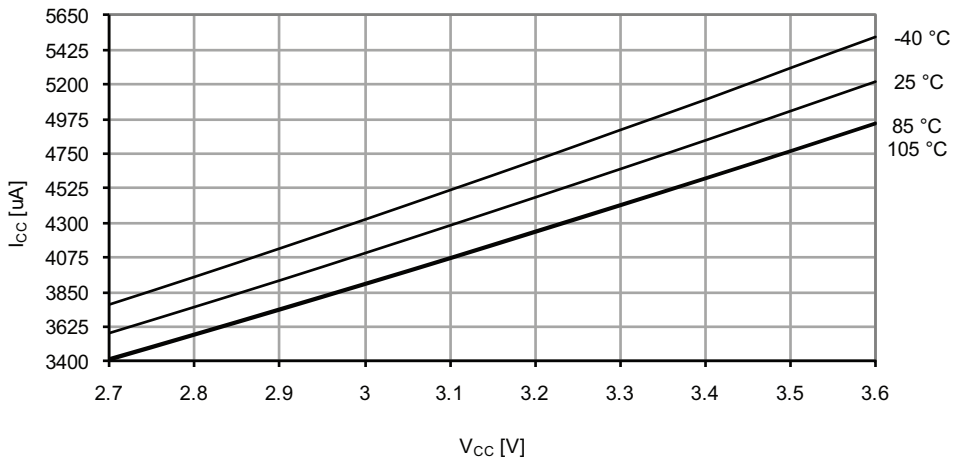



**Figure 37-98. Idle mode current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator.***



### 37.2.1.3 Power-down mode supply current

**Figure 37-99. Power-down mode supply current vs. temperature.**
***All functions disabled.***

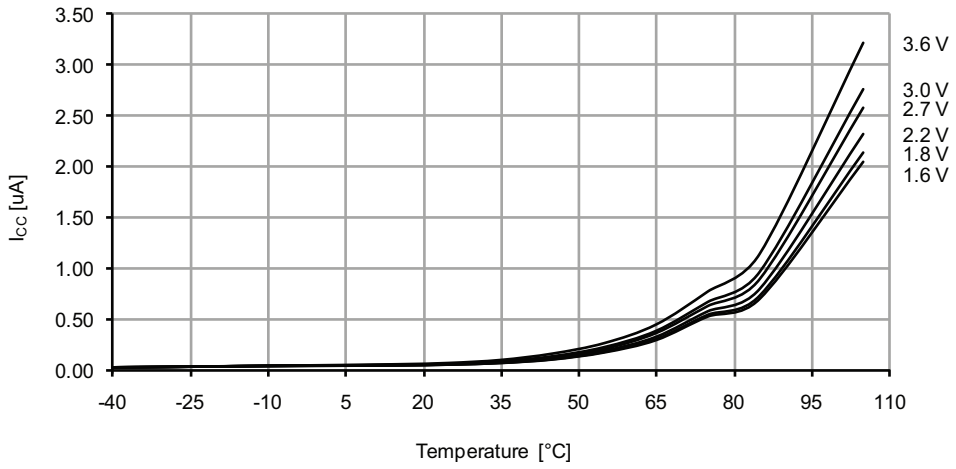



**Figure 37-100. Power-down mode supply current vs. $V_{CC}$.**
***All functions disabled.***

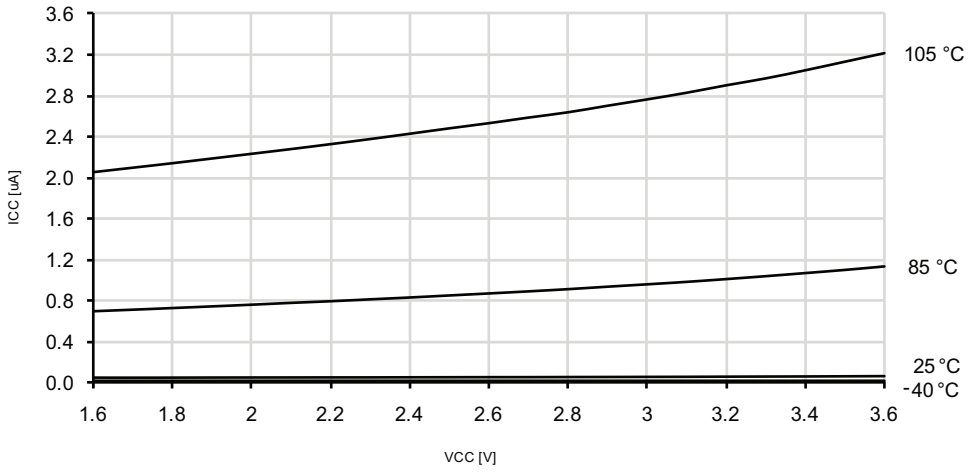
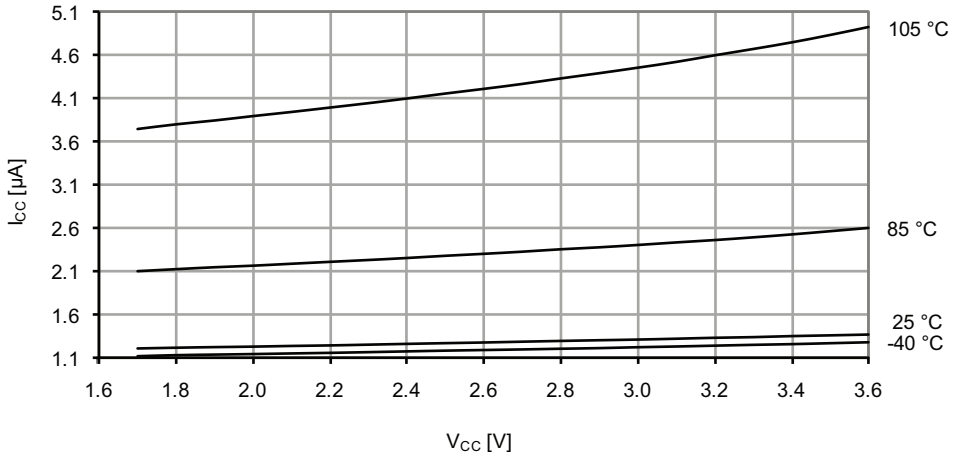


**Figure 37-101. Power-down mode supply current vs. $V_{CC}$.**

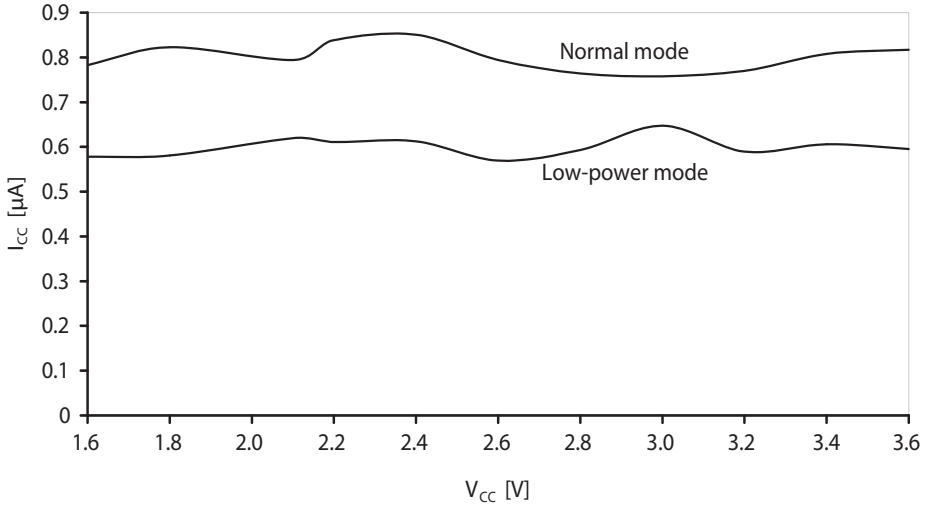
***Watchdog and sampled BOD enabled.***




### 37.2.1.4 Power-save mode supply current

**Figure 37-102. Power-save mode supply current vs.$V_{CC}$.**

***Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.***



### 37.2.1.5 Standby mode supply current

**Figure 37-103. Standby supply current vs. $V_{CC}$.**
***Standby, $f_{SYS}$ = 1MHz.***

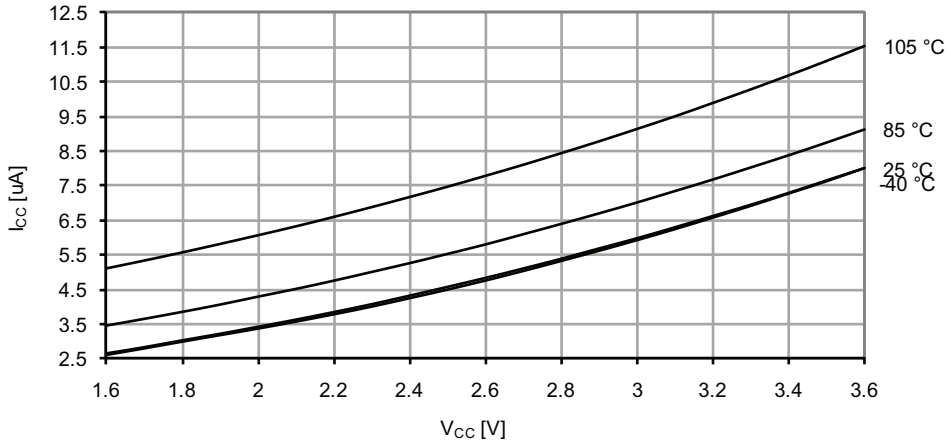
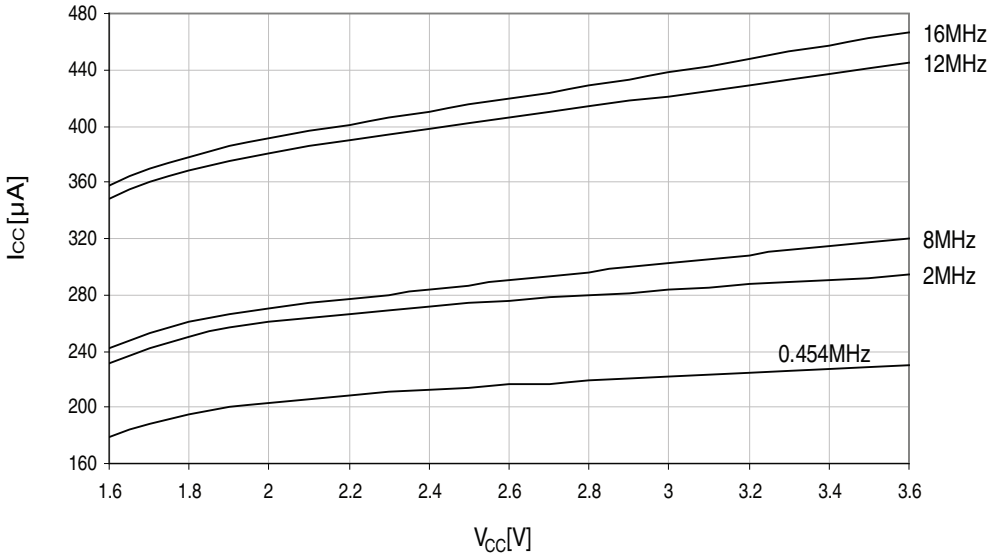



**Figure 37-104. Standby supply current vs. $V_{CC}$.**
***25°C, running from different crystal oscillators.***



### 37.2.2 I/O Pin Characteristics

#### 37.2.2.1 Pull-up

**Figure 37-105. I/O pin pull-up resistor current vs. input voltage.**
***$V_{CC}$ = 1.8V.***

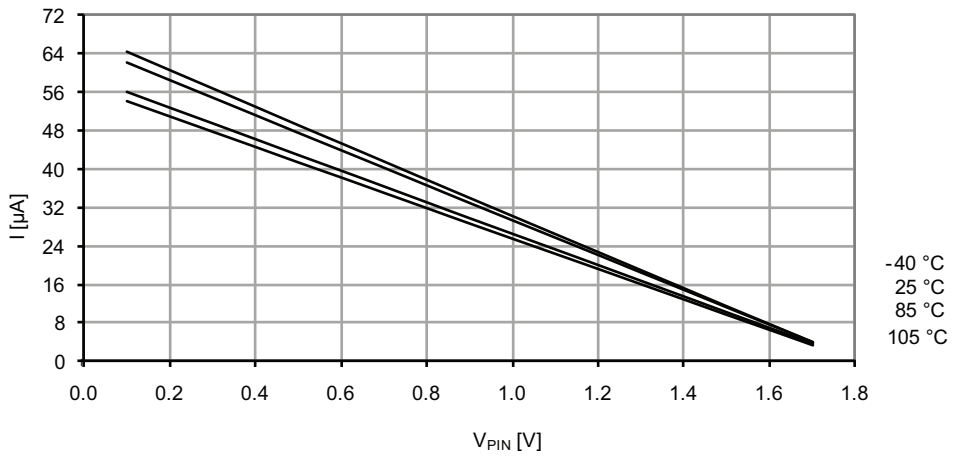



**Figure 37-106. I/O pin pull-up resistor current vs. input voltage.**
***$V_{CC}$ = 3.0V.***

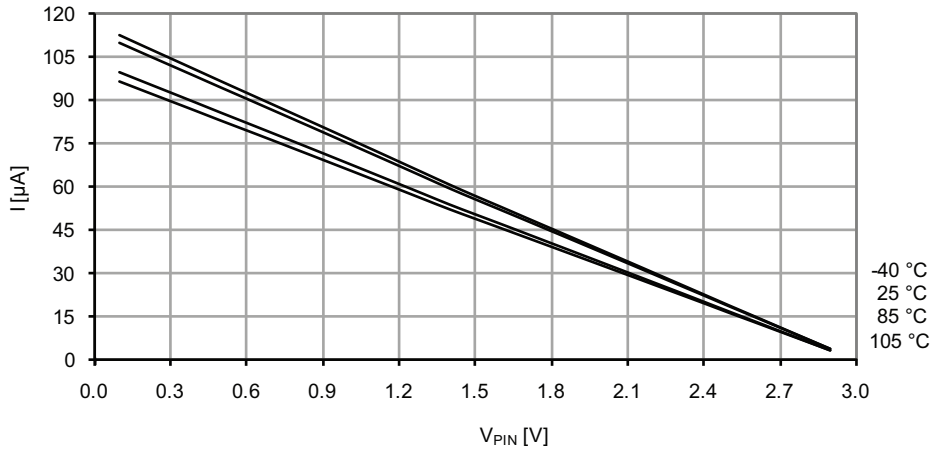
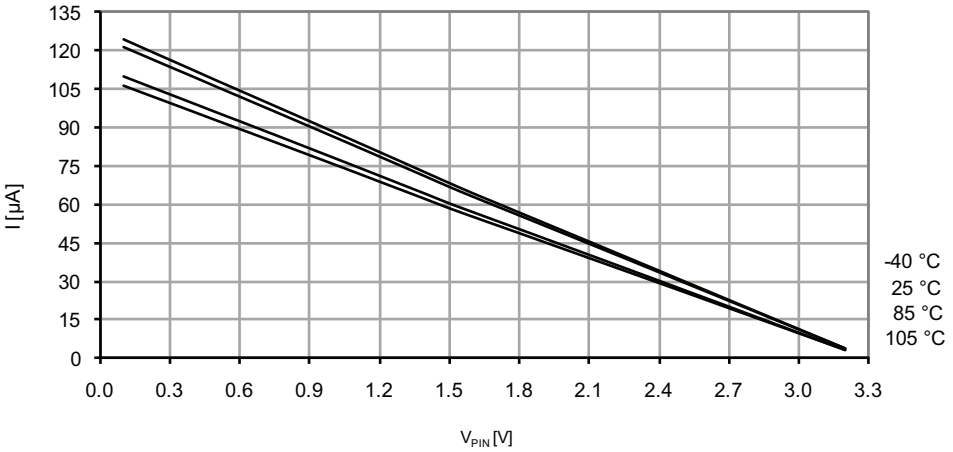


**Figure 37-107. I/O pin pull-up resistor current vs. input voltage.**

***$V_{CC}$ = 3.3V.***




### 37.2.2.2 Output Voltage vs. Sink/Source Current

**Figure 37-108. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 1.8V.***

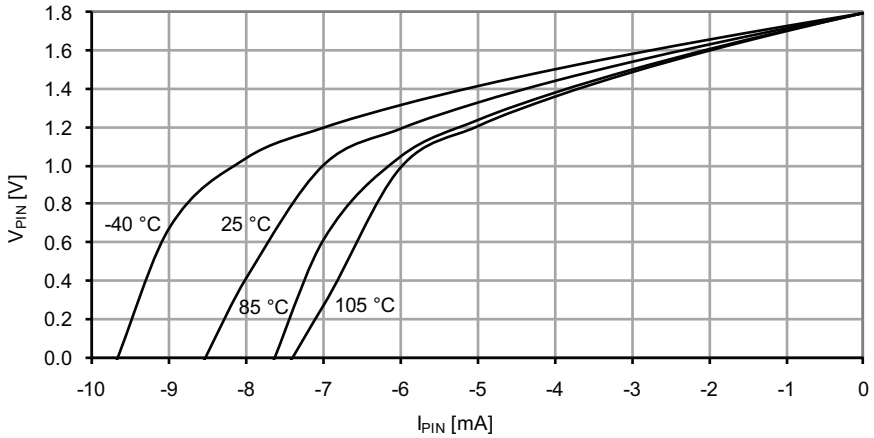


**Figure 37-109. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 3.0V.***

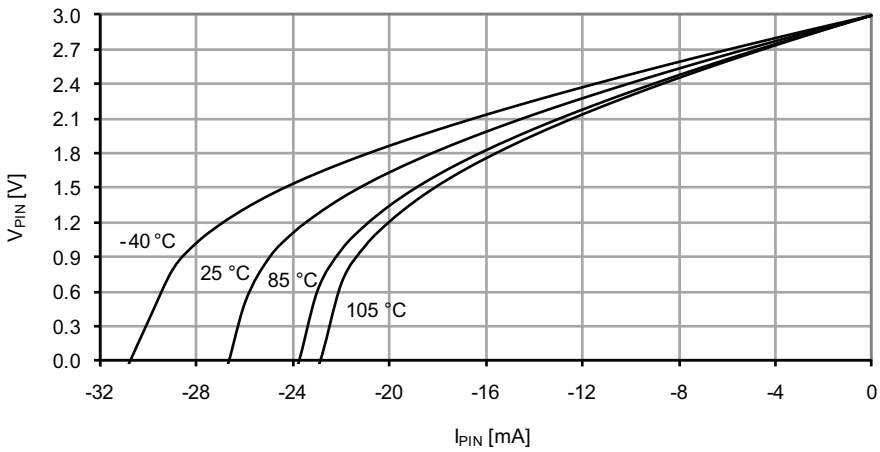



**Figure 37-110. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 3.3V.***

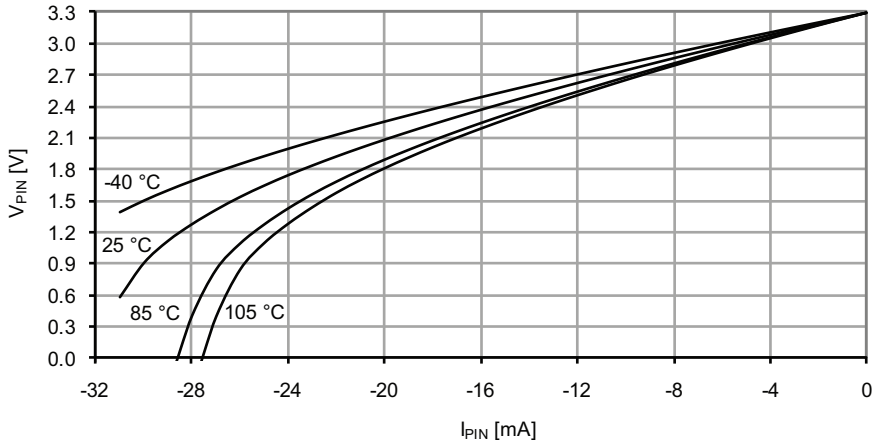


**Figure 37-111. I/O pin output voltage vs. source current.**

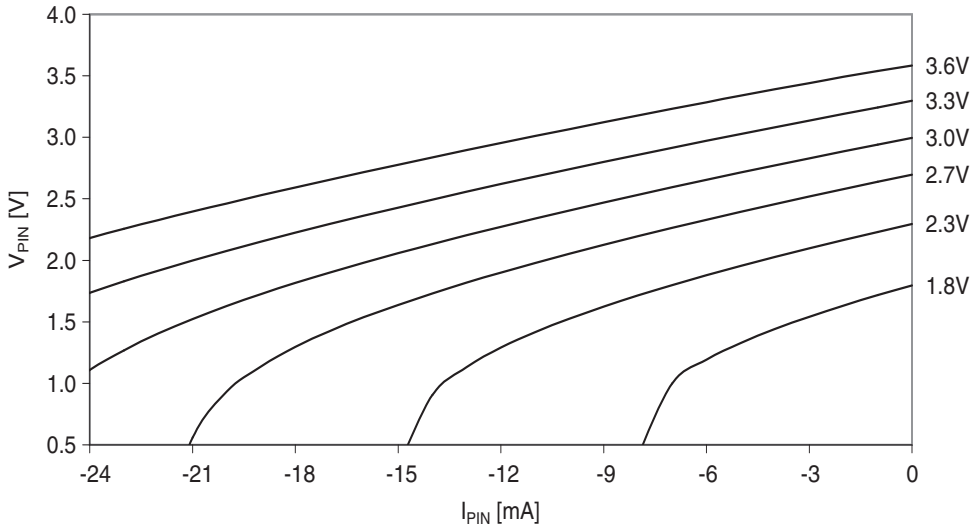



**Figure 37-112. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 1.8V.***

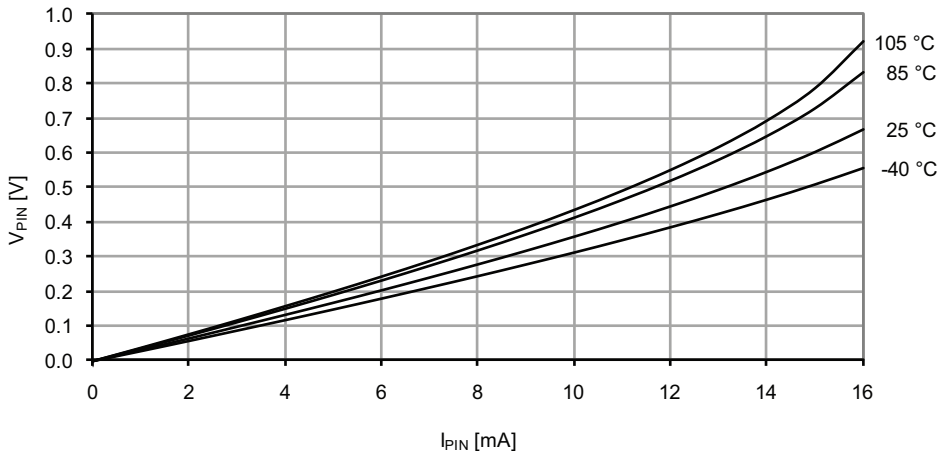


**Figure 37-113. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 3.0V.***

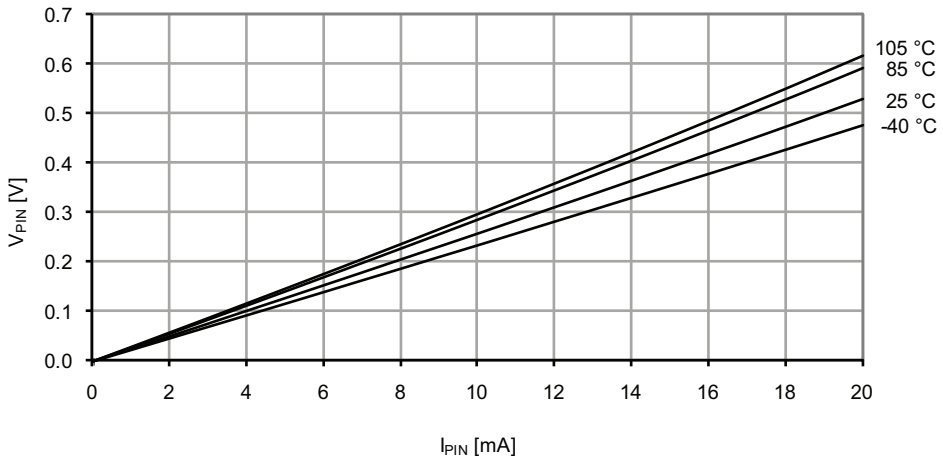



**Figure 37-114. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 3.3V.***

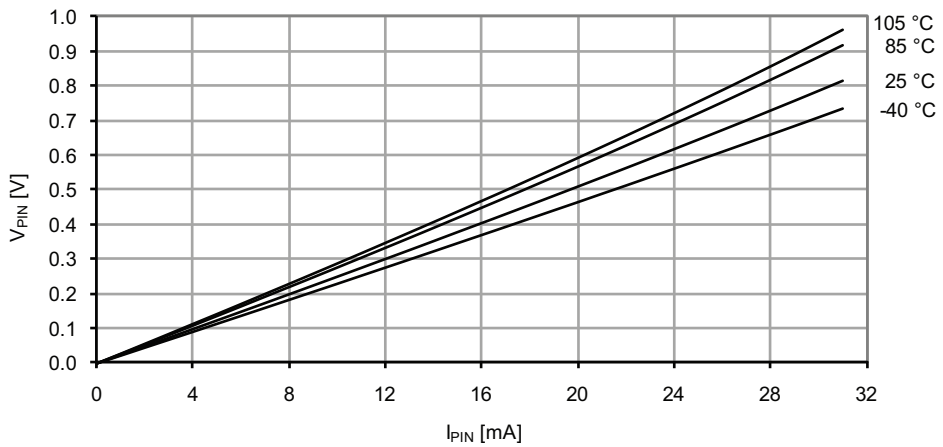
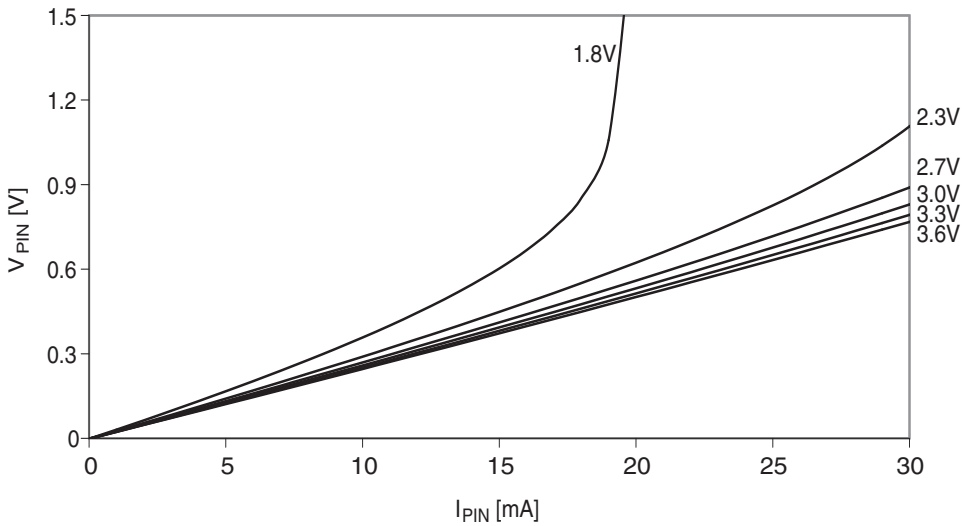



**Figure 37-115. I/O pin output voltage vs. sink current.**



### 37.2.2.3 Thresholds and Hysteresis

**Figure 37-116. I/O pin input threshold voltage vs. $V_{CC}$.**
***T = 25°C.***

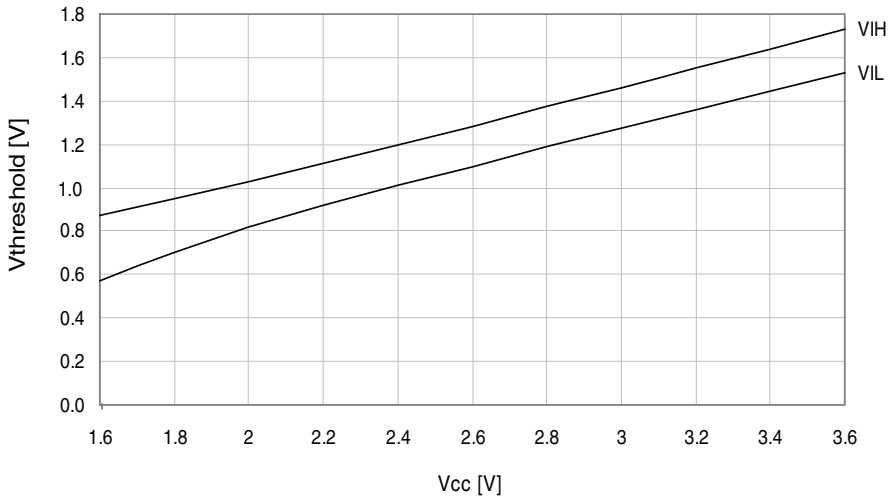



**Figure 37-117. I/O pin input threshold voltage vs. $V_{CC}$.**
***$V_{IH}$ I/O pin read as "1".***

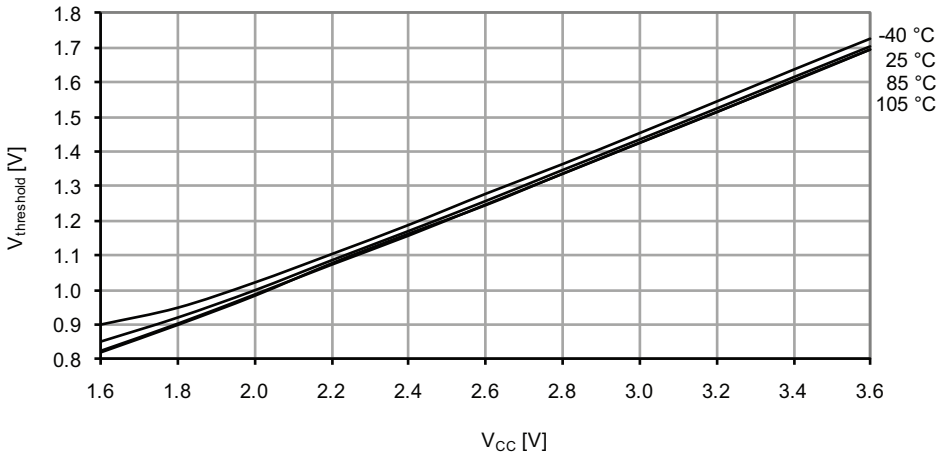


**Figure 37-118. I/O pin input threshold voltage vs. $V_{CC}$.**

***$V_{IL}$ I/O pin read as "0".***

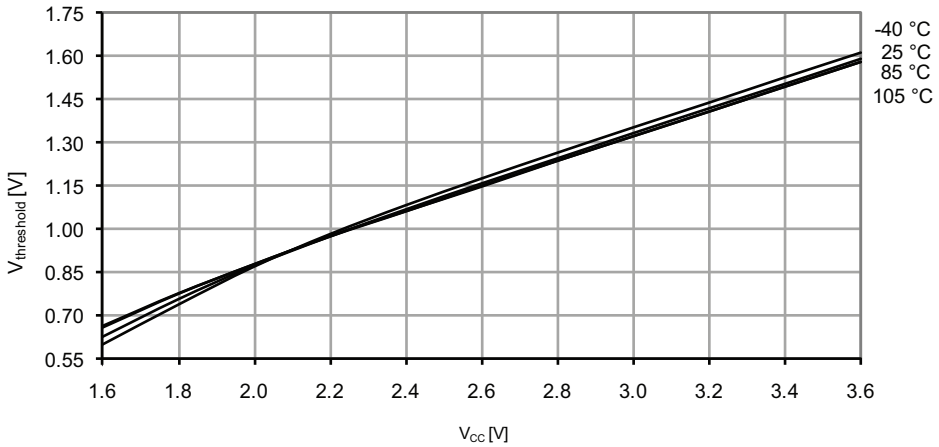
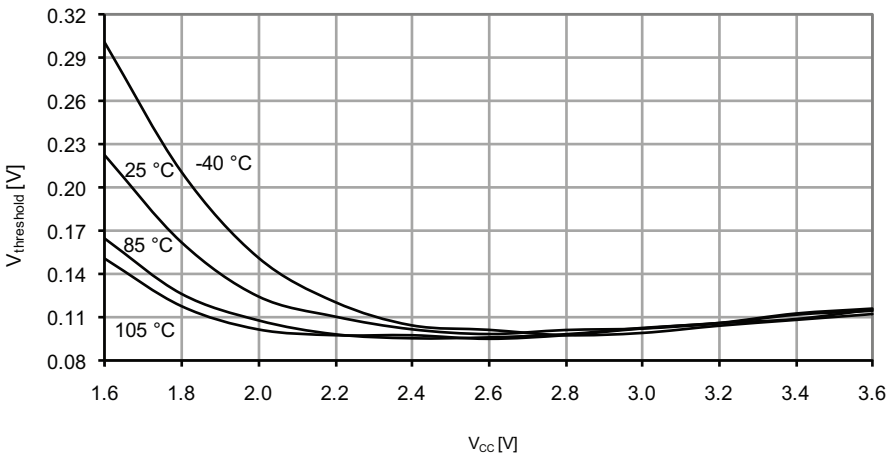



**Figure 37-119. I/O pin input hysteresis vs. $V_{CC}$.**



### 37.2.3 ADC Characteristics

**Figure 37-120. INL error vs. external $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, external reference.***

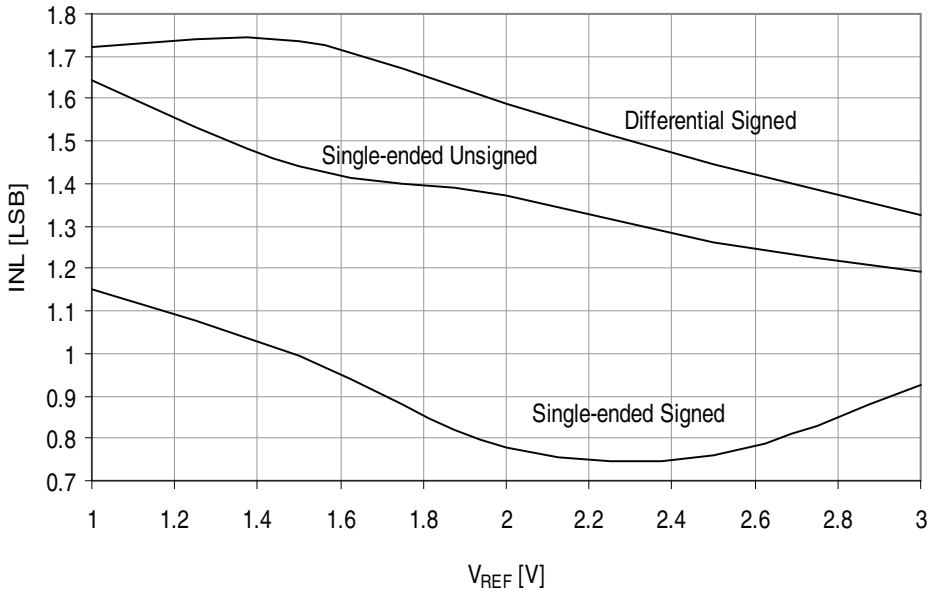



**Figure 37-121. INL error vs. sample rate.**

***T = 25°C, $V_{CC}$ = 3.6V, $V_{REF}$ = 3.0V external.***

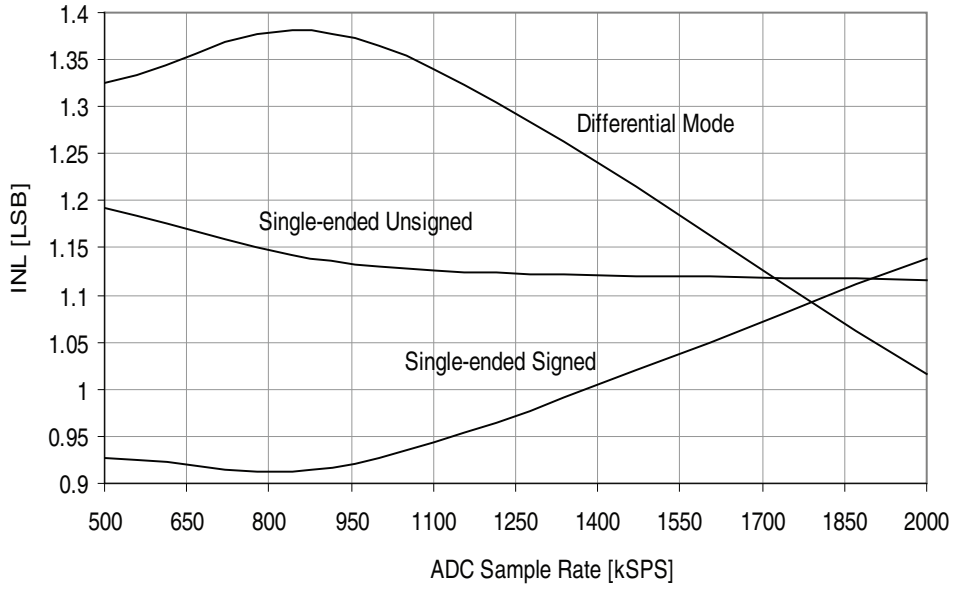


**Figure 37-122. INL error vs. input code**

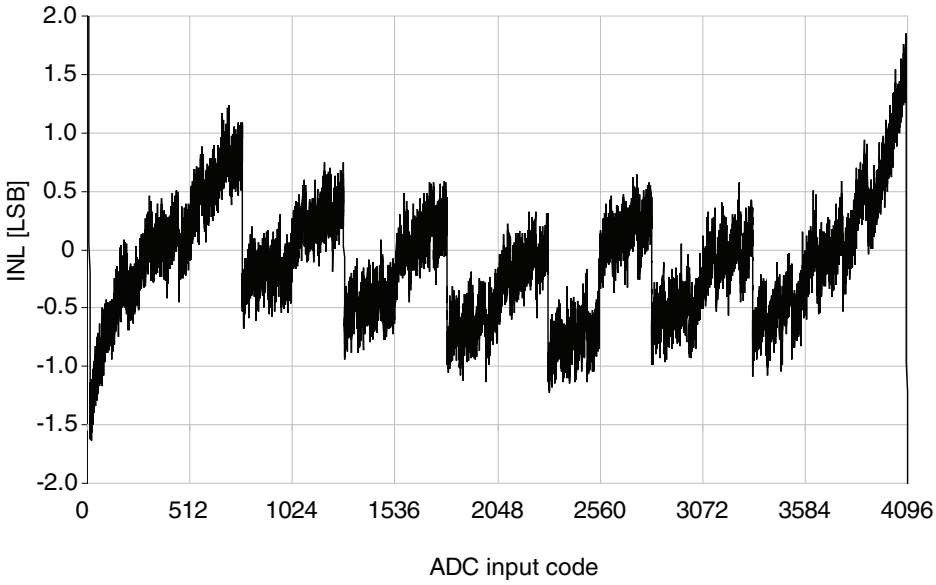



**Figure 37-123. DNL error vs. external $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, external reference.***

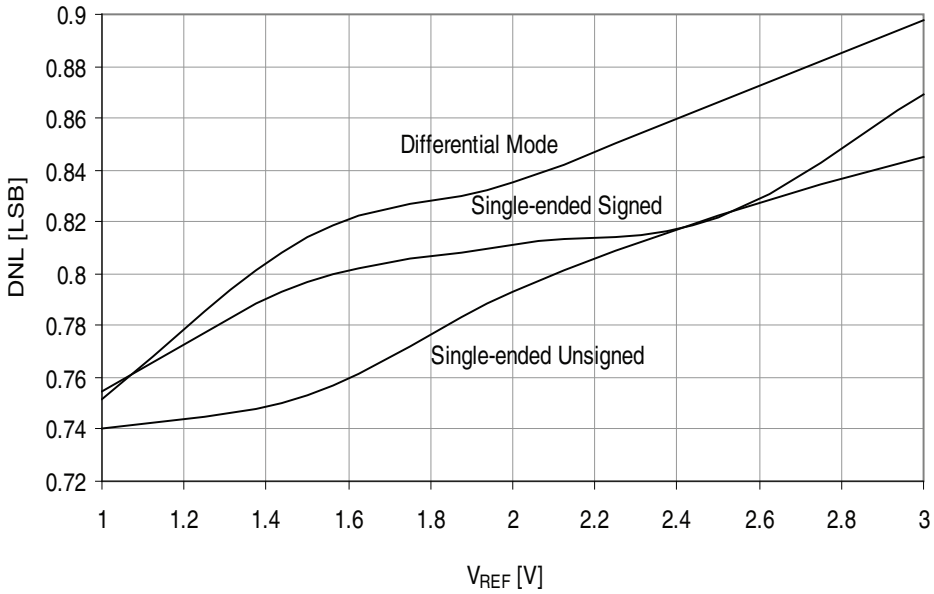


**Figure 37-124. DNL error vs. sample rate.**

***T = 25°C, $V_{CC}$ = 3.6V, $V_{REF}$ = 3.0V external.***

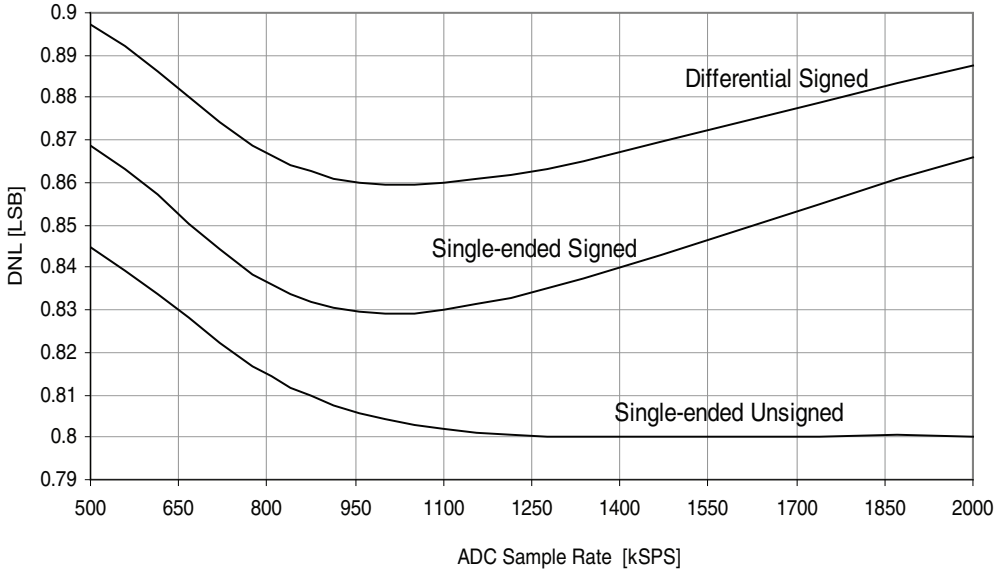



**Figure 37-125. DNL error vs. input code.**

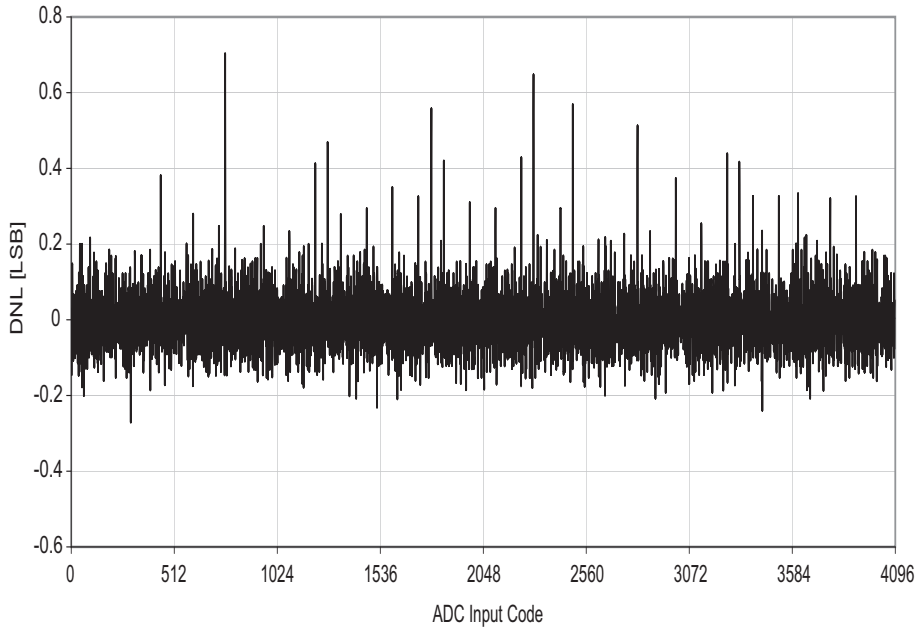


**Figure 37-126. Gain error vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

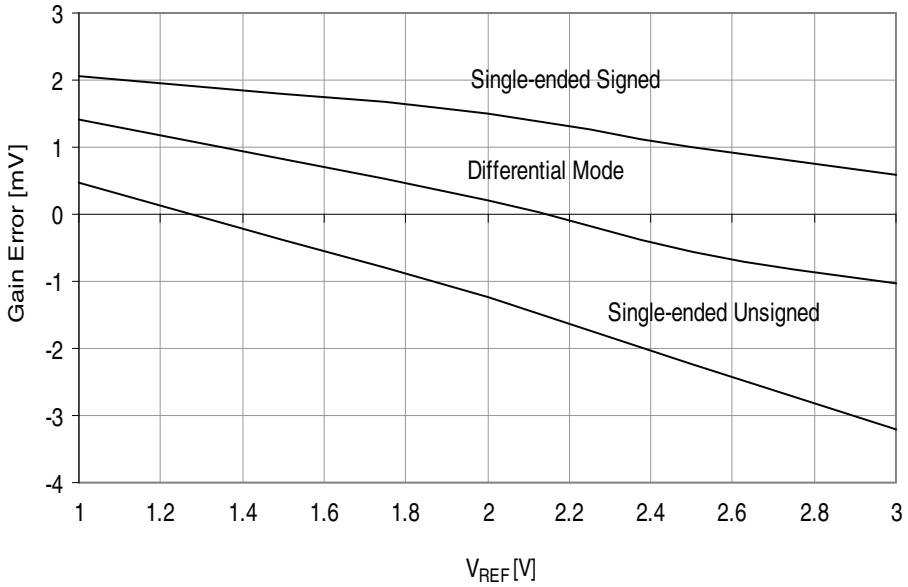



**Figure 37-127. Gain error vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***

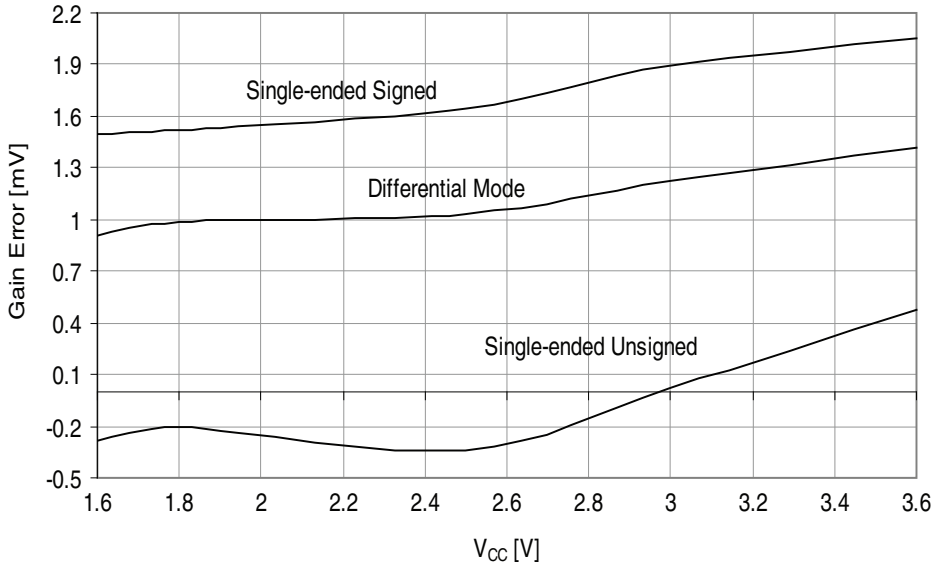


**Figure 37-128. Offset error vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

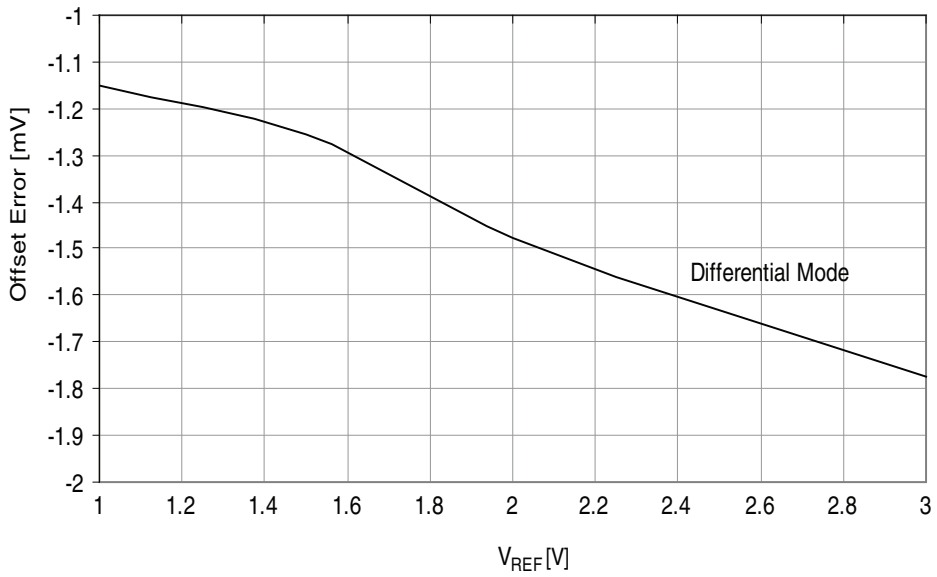



**Figure 37-129. Gain error vs. temperature.**

***$V_{CC}$ = 3.0V, $V_{REF}$ = external 2.0V.***

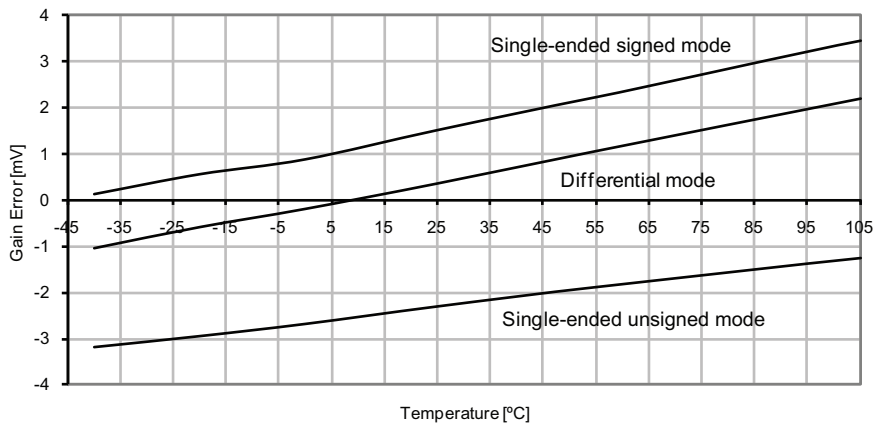


**Figure 37-130. Offset error vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***

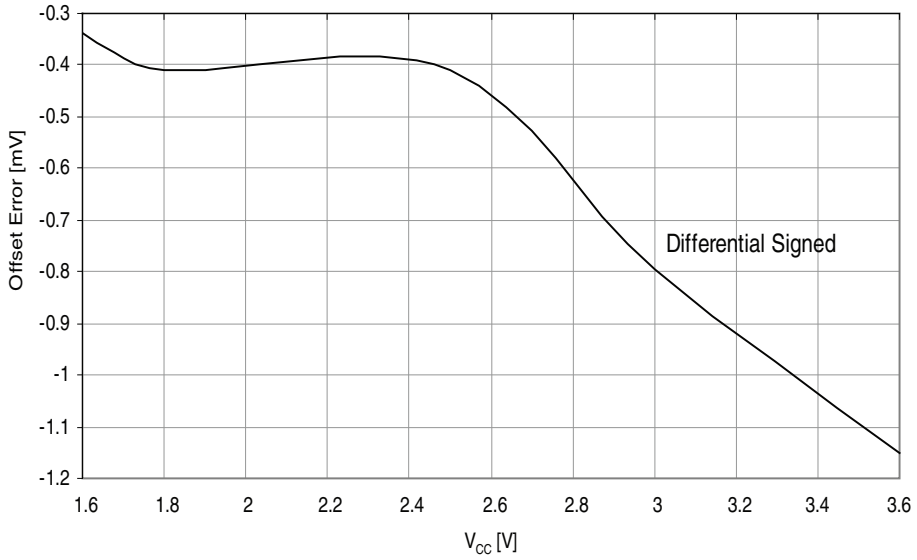



**Figure 37-131. Noise vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

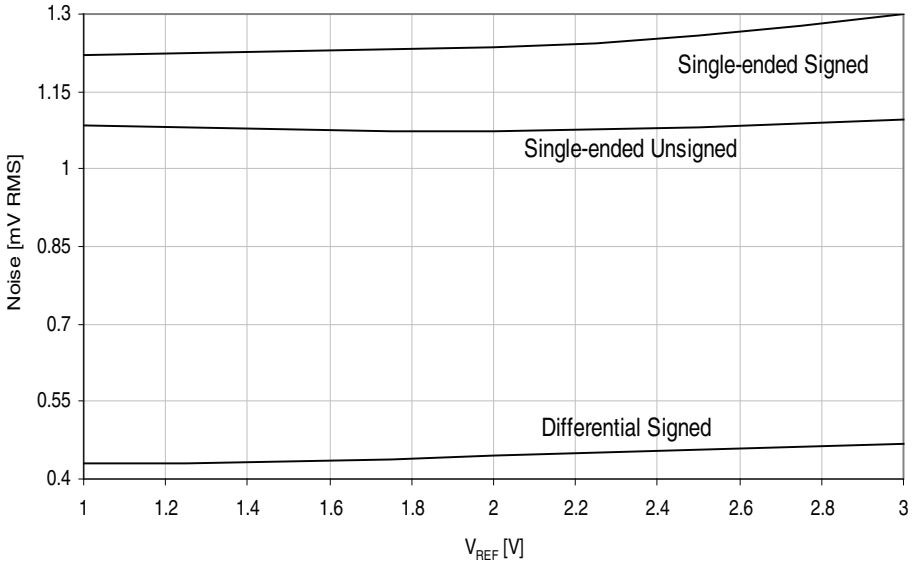
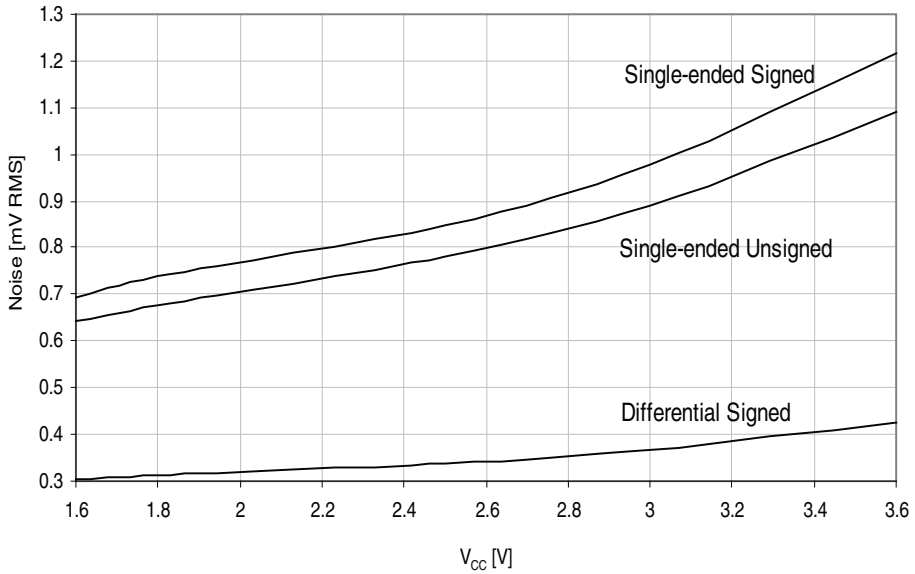


**Figure 37-132. Noise vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***




## 37.2.4 DAC Characteristics

**Figure 37-133. DAC INL error vs. $V_{REF}$.**

***$V_{CC}$ = 3.6V.***

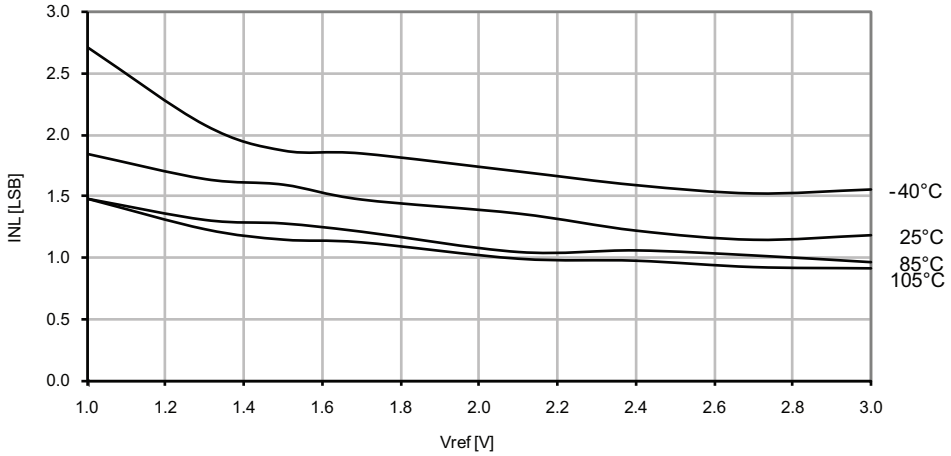


**Figure 37-134. DNL error vs. $V_{REF}$.**

***$V_{CC}$ = 3.6V.***

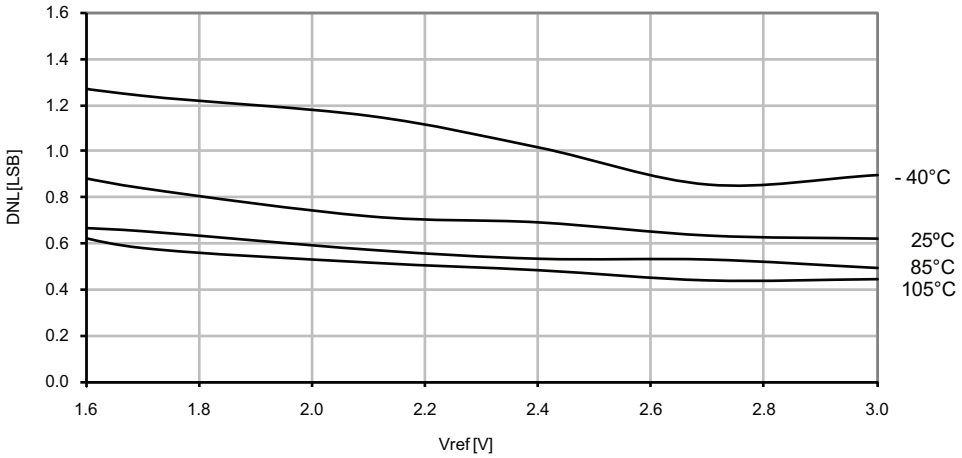
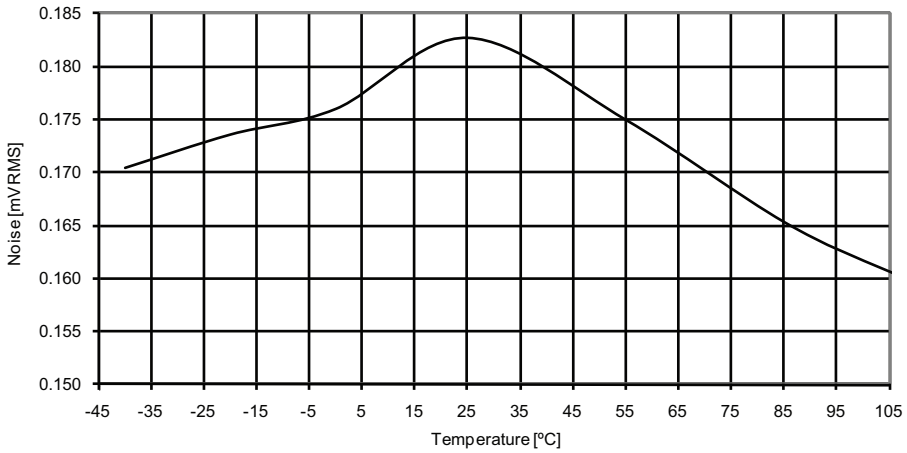



**Figure 37-135. DAC noise vs. temperature.**

***$V_{CC}$ = 3.0V, $V_{REF}$ = 2.4V .***



### 37.2.5 Analog Comparator Characteristics

**Figure 37-136. Analog comparator hysteresis vs. $V_{CC}$.**

***High-speed, small hysteresis.***

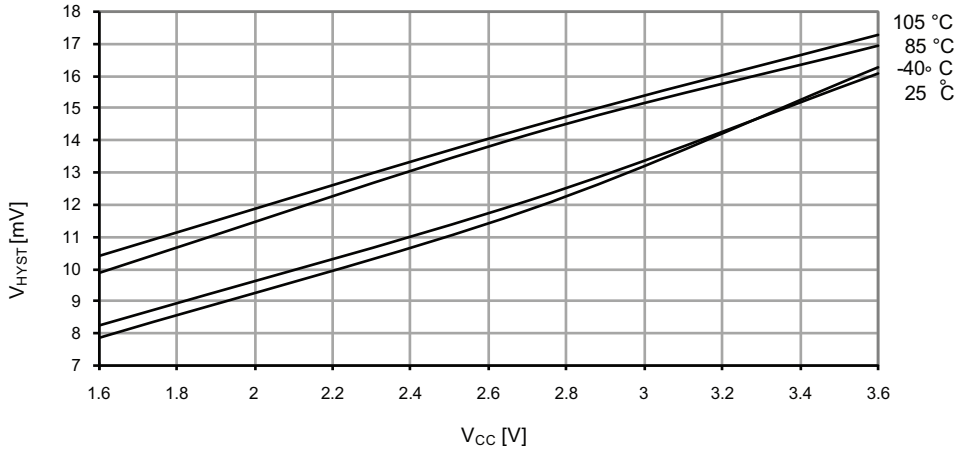



**Figure 37-137. Analog comparator hysteresis vs. $V_{CC}$.**

***Low power, small hysteresis.***

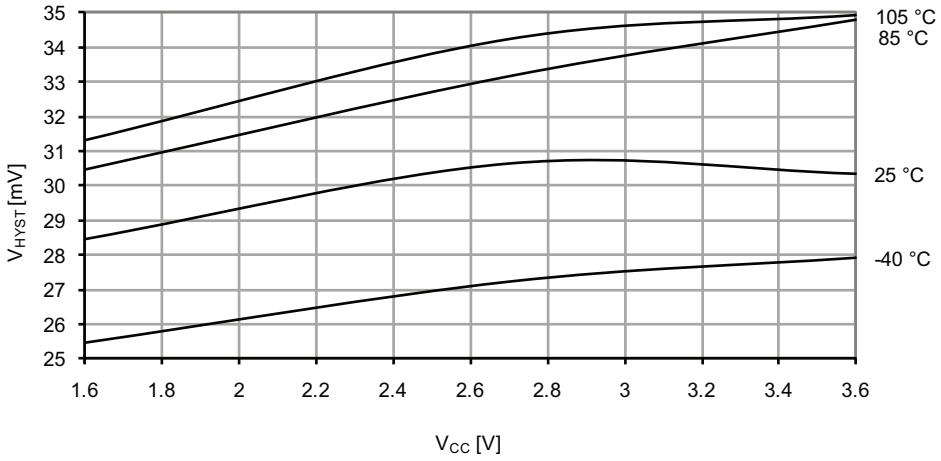


**Figure 37-138. Analog comparator hysteresis vs. $V_{CC}$.**

***High-speed mode, large hysteresis.***

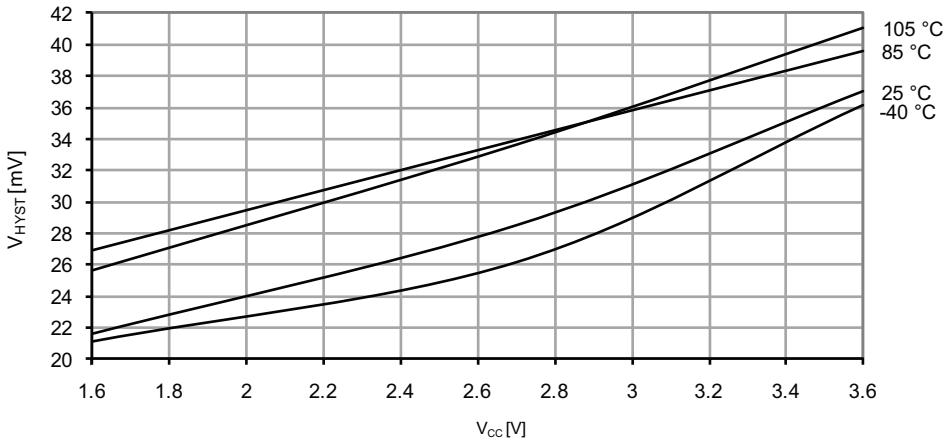



**Figure 37-139. Analog comparator hysteresis vs. $V_{CC}$.**

***Low power, large hysteresis.***

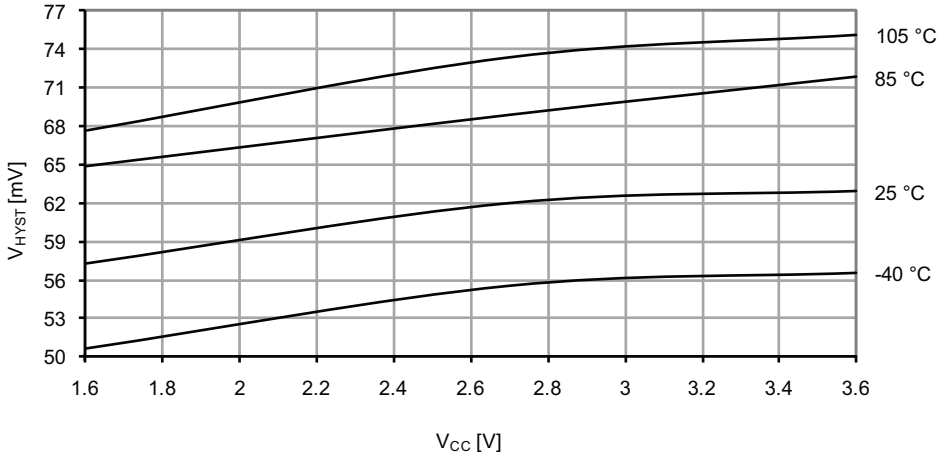


**Figure 37-140. Analog comparator current source vs. calibration value.**

***Temperature = 25°C.***

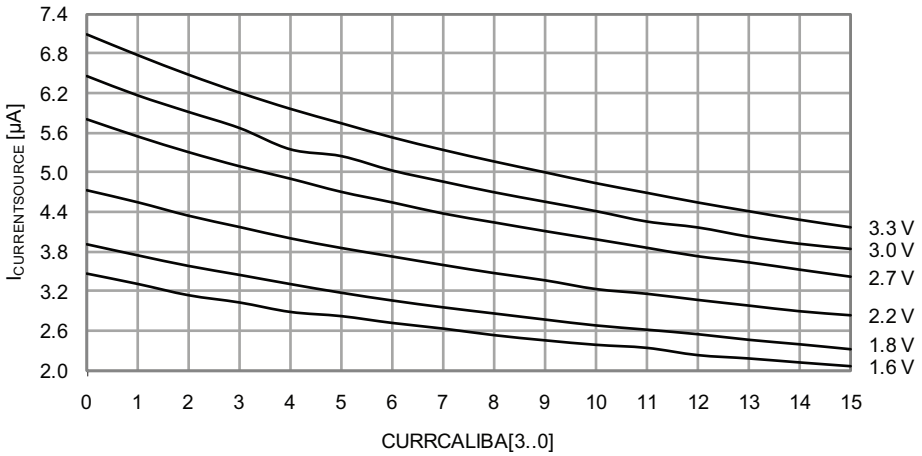



**Figure 37-141. Analog comparator current source vs. calibration value.**

***$V_{CC}$ = 3.0V.***

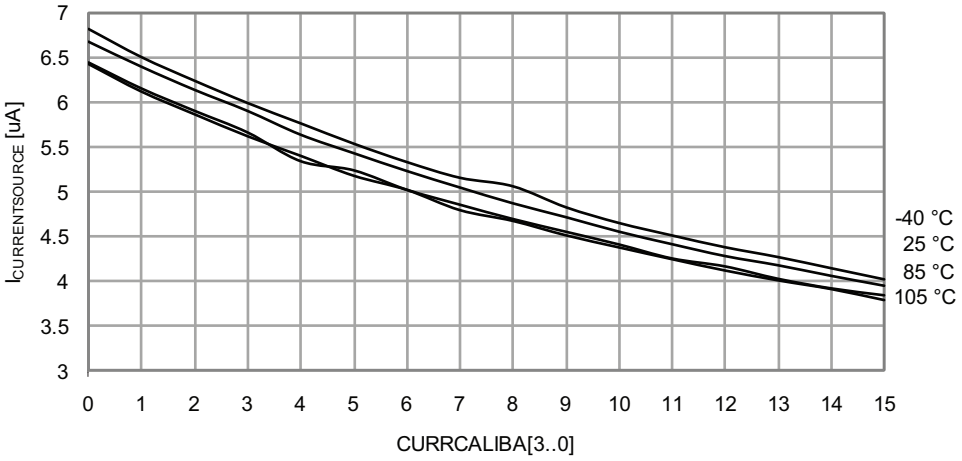
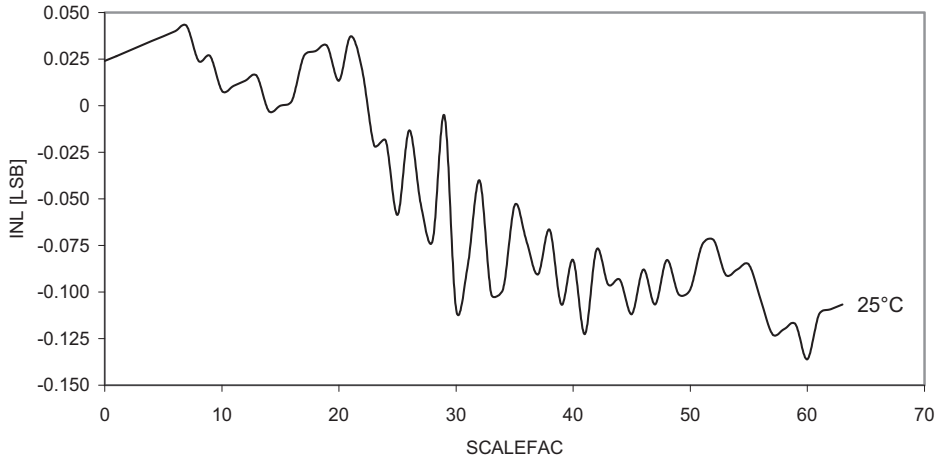


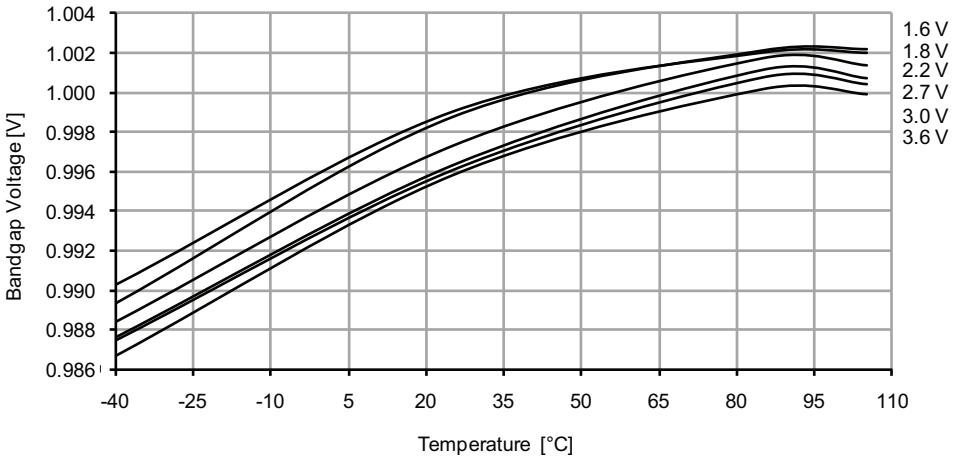
**Figure 37-142. Voltage scaler INL vs. SCALEFAC.**

***T = 25°C, $V_{CC}$ = 3.0V.***




## 37.2.6 Internal 1.0V reference Characteristics

**Figure 37-143. ADC/DAC Internal 1.0V reference vs. temperature.**



### 37.2.7 BOD Characteristics

**Figure 37-144. BOD thresholds vs. temperature.**

***BOD level = 1.6V.***

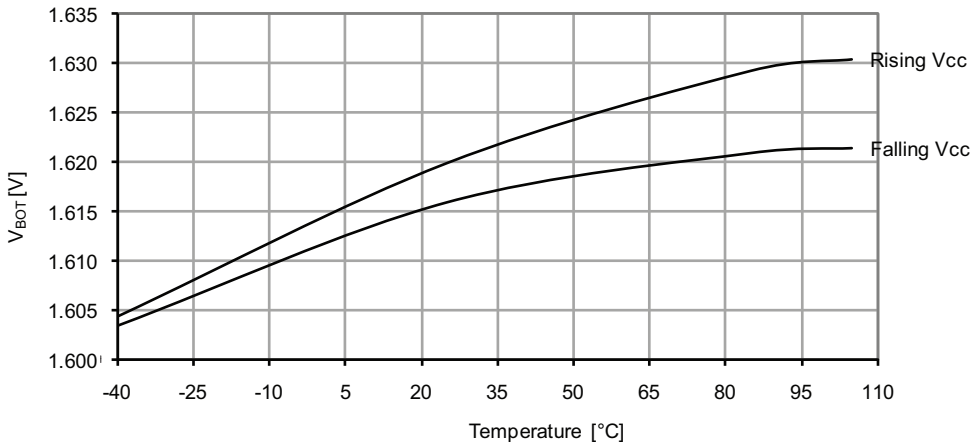
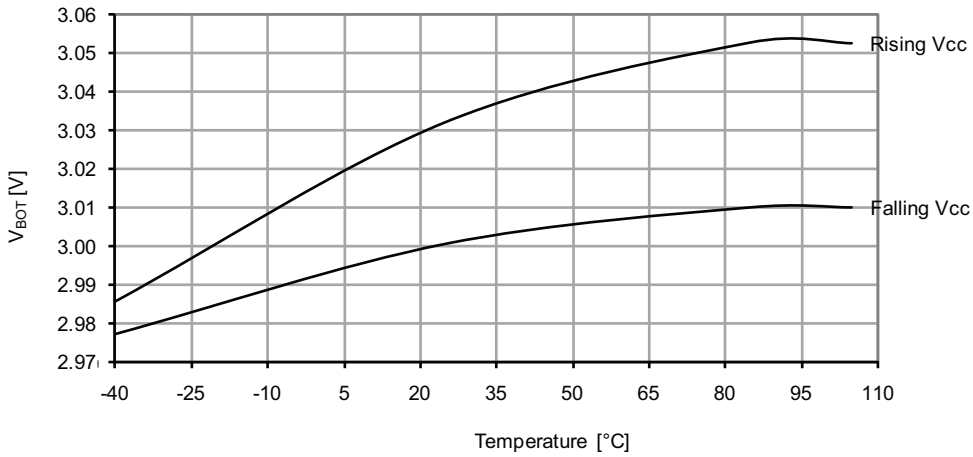



**Figure 37-145. BOD thresholds vs. temperature.**

***BOD level = 3.0V.***



### 37.2.8 External Reset Characteristics

**Figure 37-146. Minimum Reset pin pulse width vs. $V_{CC}$.**

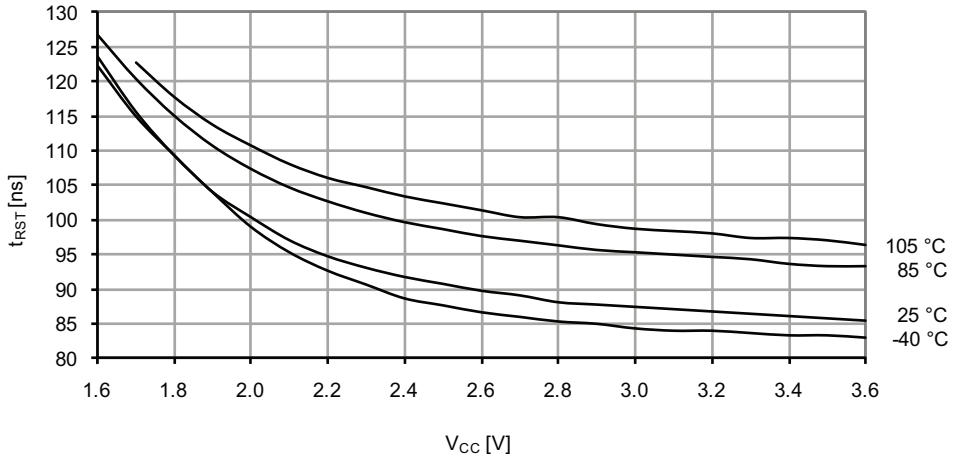



**Figure 37-147. Reset pin pull-up resistor current vs. reset pin voltage.**
***$V_{CC}$ = 1.8V.***

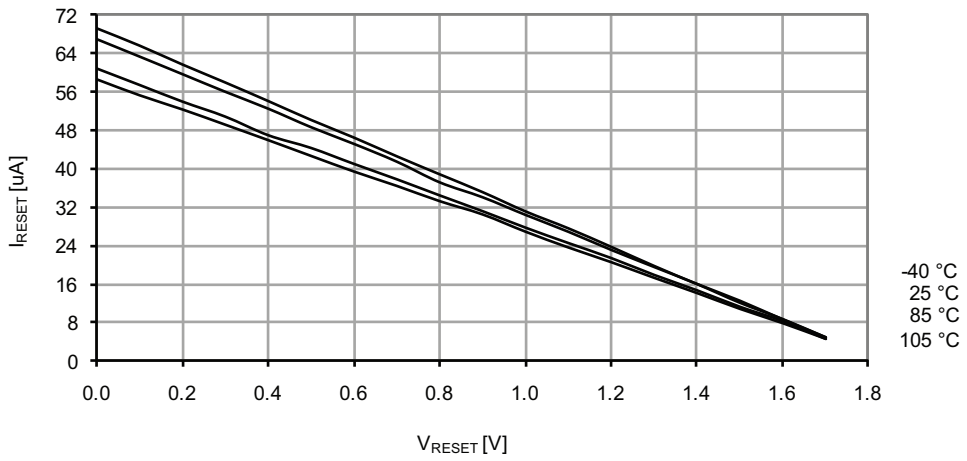


**Figure 37-148. Reset pin pull-up resistor current vs. reset pin voltage.**

***$V_{CC}$ = 3.0V.***

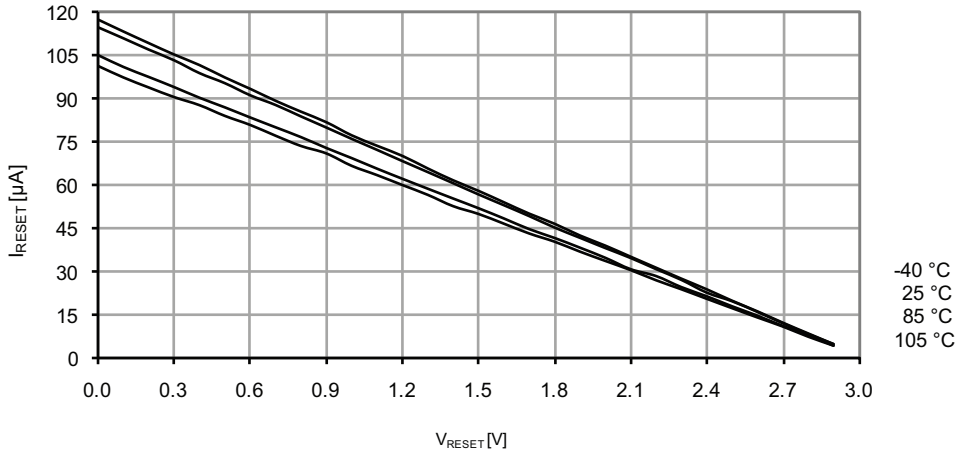



**Figure 37-149. Reset pin pull-up resistor current vs. reset pin voltage.**

***$V_{CC}$ = 3.3V.***

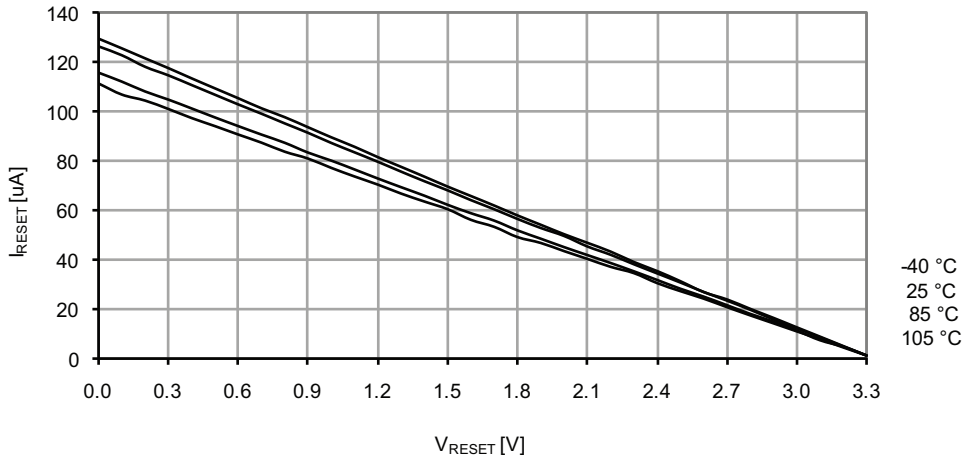


**Figure 37-150. Reset pin input threshold voltage vs. $V_{CC}$.**

***$V_{IH}$ - Reset pin read as "1".***

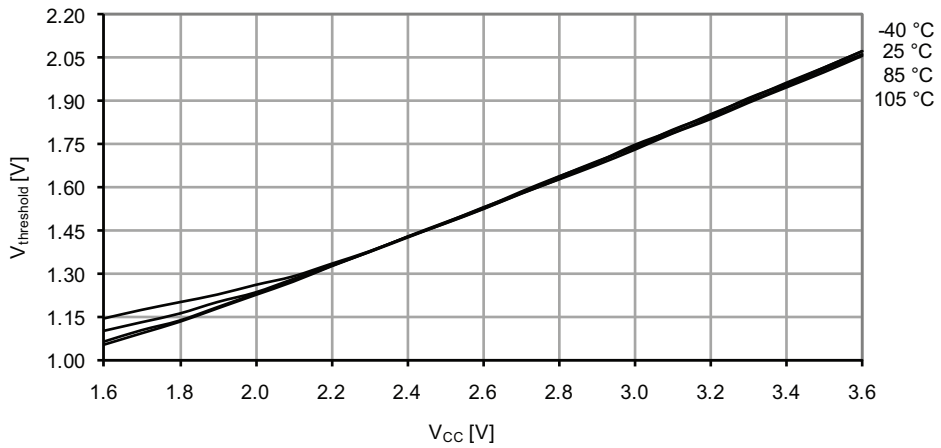
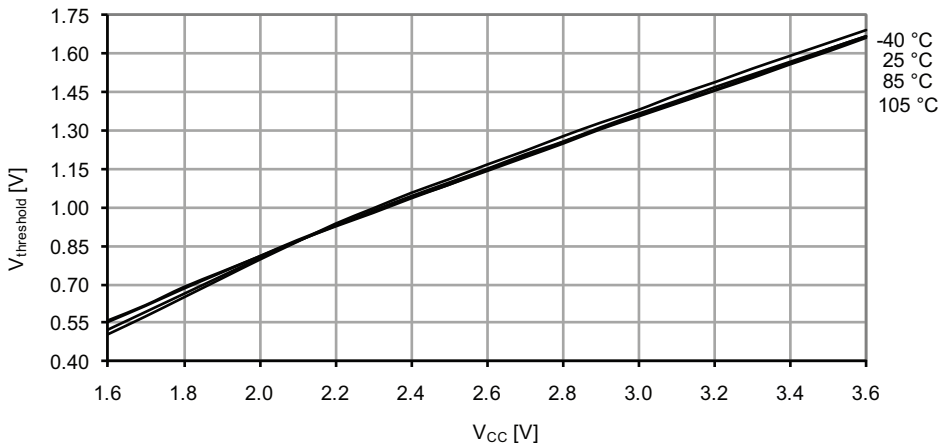



**Figure 37-151. Reset pin input threshold voltage vs. $V_{CC}$.**

***$V_{IL}$ - Reset pin read as "0".***



### 37.2.9 Power-on Reset Characteristics

**Figure 37-152. Power-on reset current consumption vs. $V_{CC}$.**

***BOD level = 3.0V, enabled in continuous mode.***

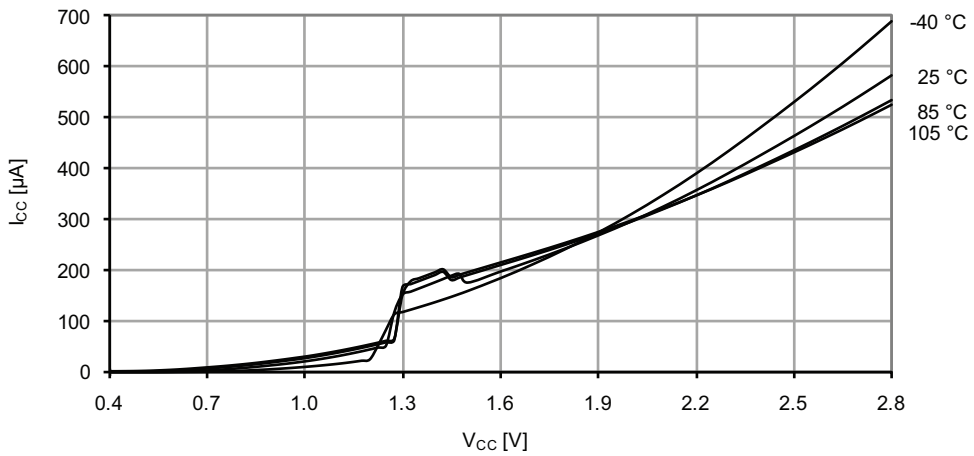
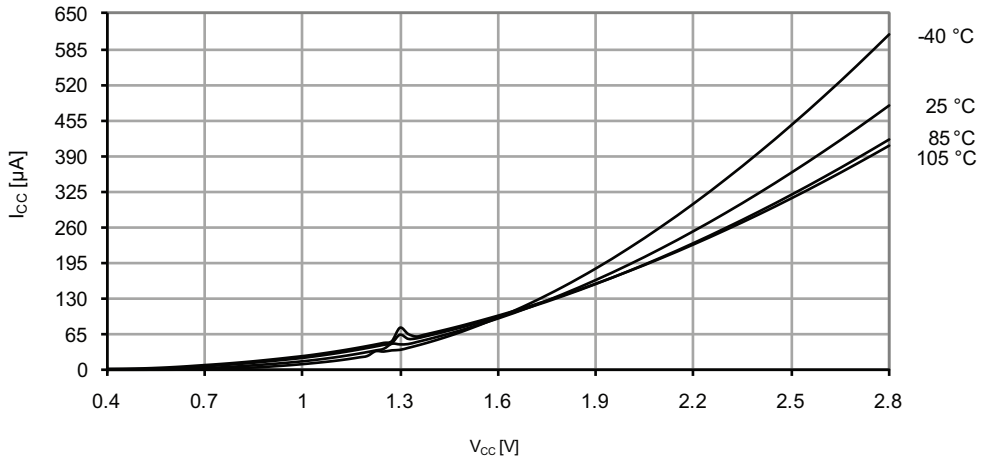



**Figure 37-153. Power-on reset current consumption vs. $V_{CC}$.**

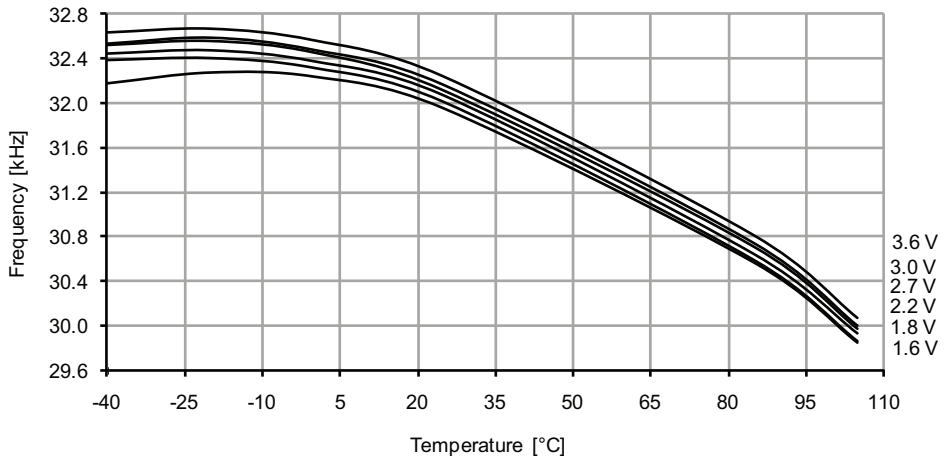
***BOD level = 3.0V, enabled in sampled mode.***



## 37.2.10 Oscillator Characteristics

### 37.2.10.1 Ultra Low-Power internal oscillator

**Figure 37-154. Ultra Low-Power internal oscillator frequency vs. temperature.**




### 37.2.10.2 32.768kHz Internal Oscillator

**Figure 37-155. 32.768kHz internal oscillator frequency vs. temperature.**

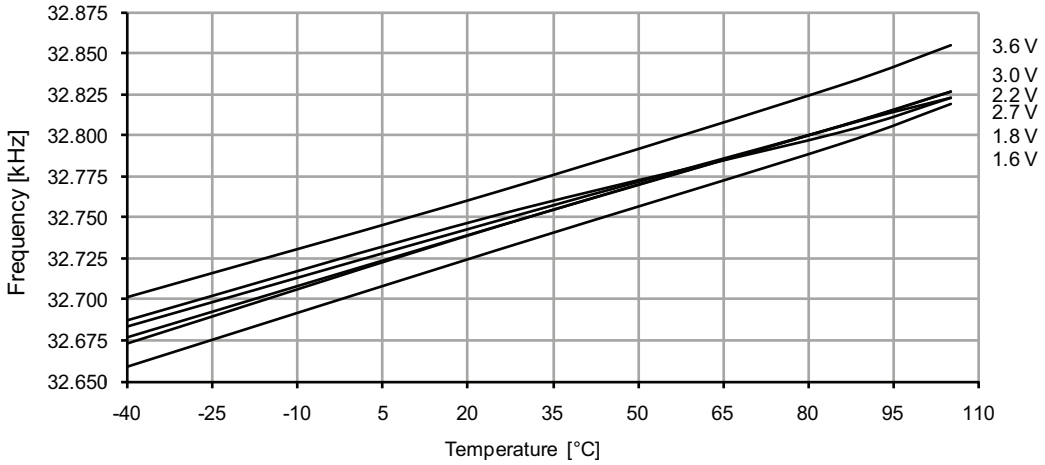
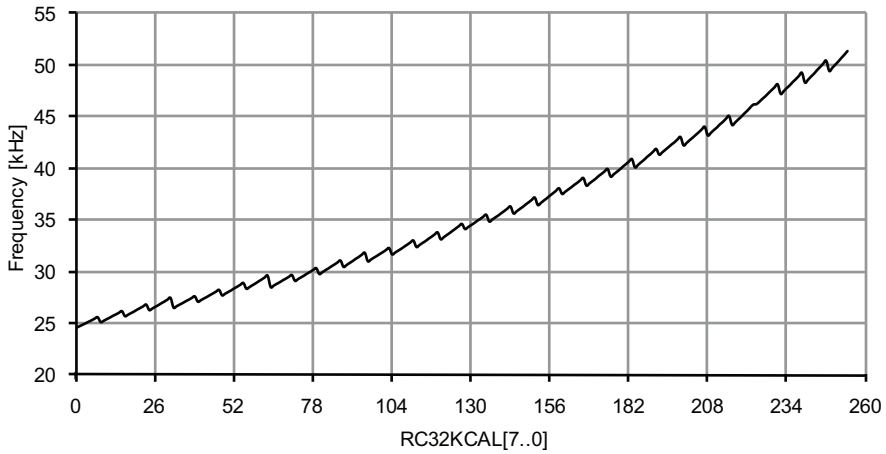


**Figure 37-156. 32.768kHz internal oscillator frequency vs. calibration value.**

***$V_{CC}$ = 3.0V, T = 25°C.***




### 37.2.10.3 2MHz Internal Oscillator

**Figure 37-157. 2MHz internal oscillator frequency vs. temperature.**

***DFLL disabled.***

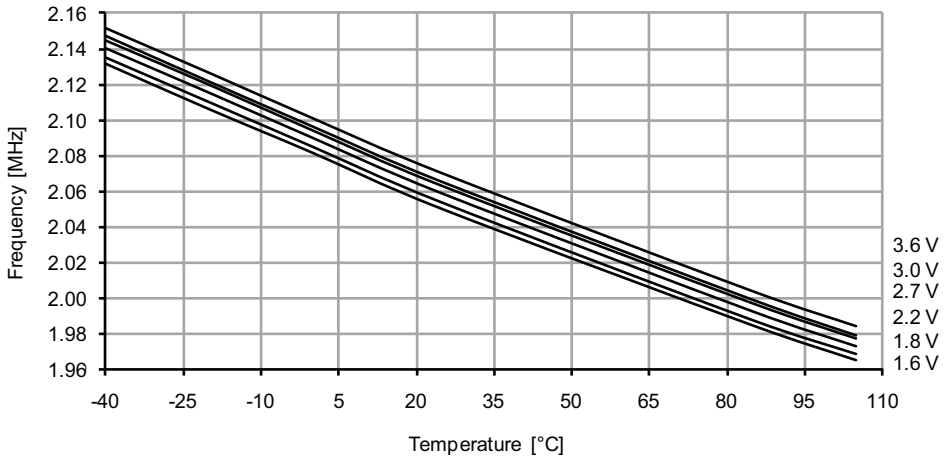


**Figure 37-158. 2MHz internal oscillator frequency vs. temperature.**

***DFLL enabled, from the 32.768kHz internal oscillator .***

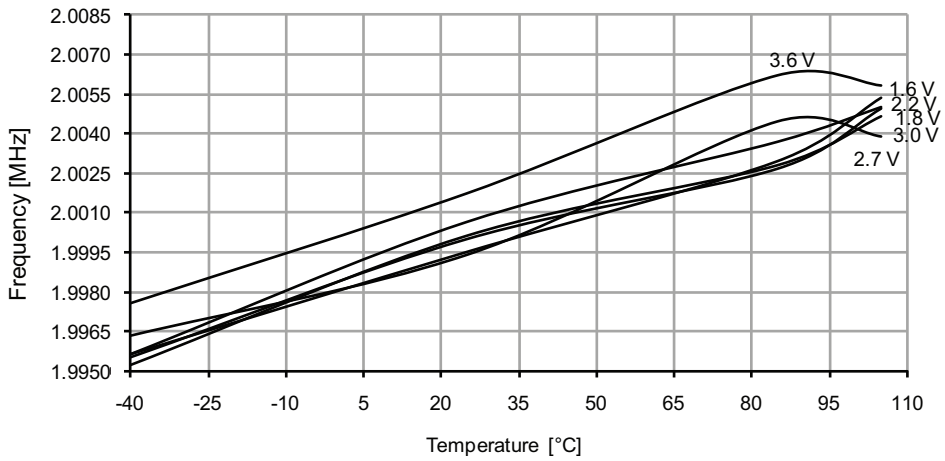
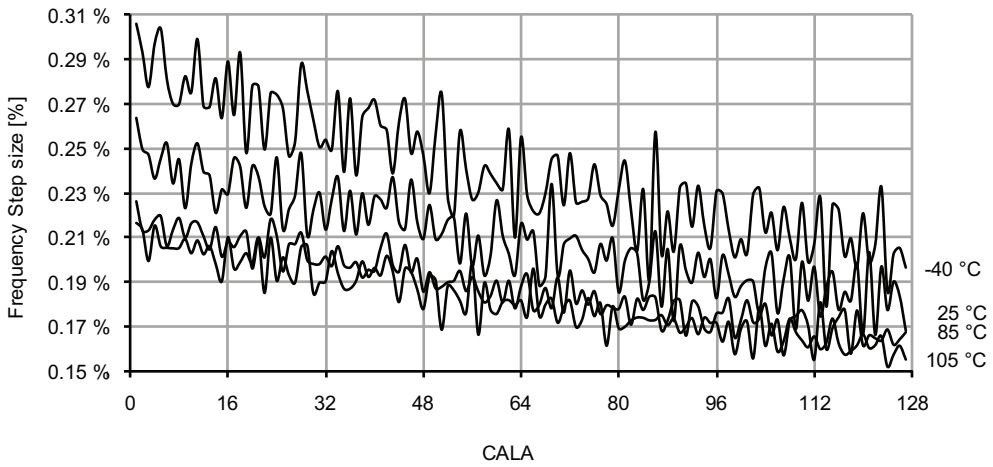



**Figure 37-159. 2MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3V.***



### 37.2.10.4 32MHz Internal Oscillator

**Figure 37-160. 32MHz internal oscillator frequency vs. temperature.**

***DFLL disabled.***

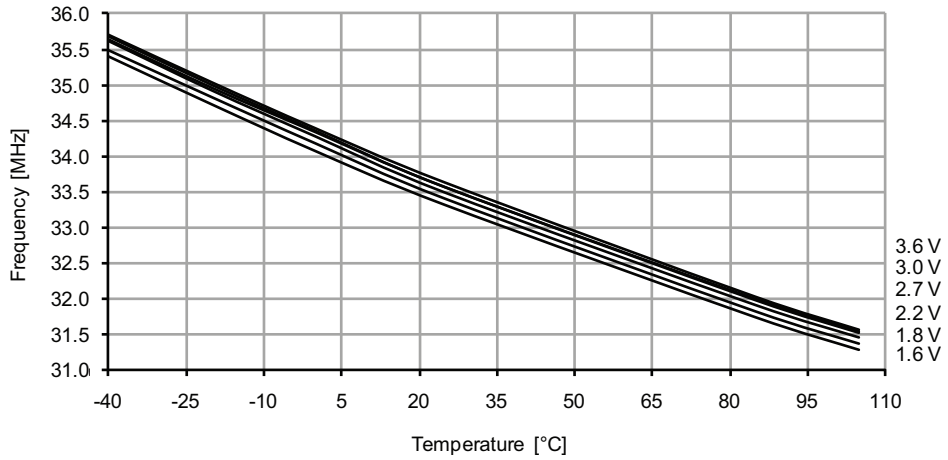



**Figure 37-161. 32MHz internal oscillator frequency vs. temperature.**

***DFLL enabled, from the 32.768kHz internal oscillator.***

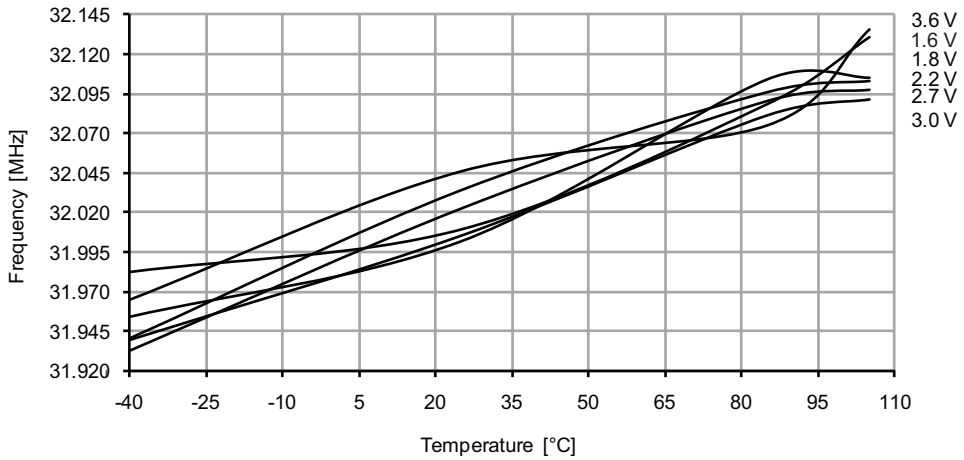


**Figure 37-162. 32MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3.0V.***

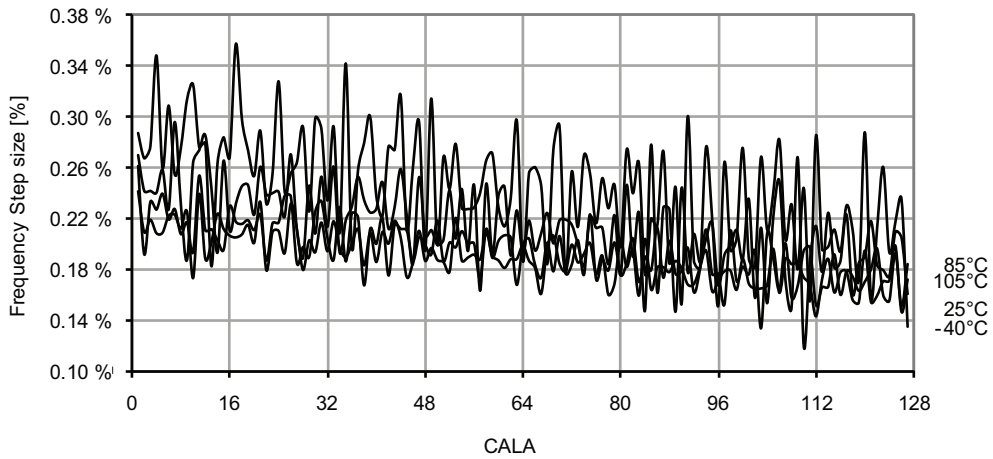
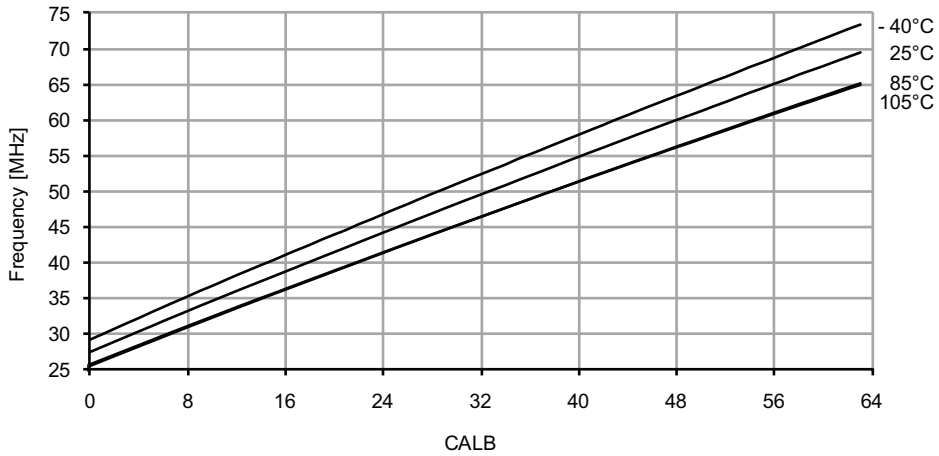



**Figure 37-163. 32MHz internal oscillator frequency vs. CALB calibration value.**

***$V_{CC}$ = 3.0V.***



### 37.2.10.5 32MHz internal oscillator calibrated to 48MHz

**Figure 37-164. 48MHz internal oscillator frequency vs. temperature.**
***DFLL disabled.***

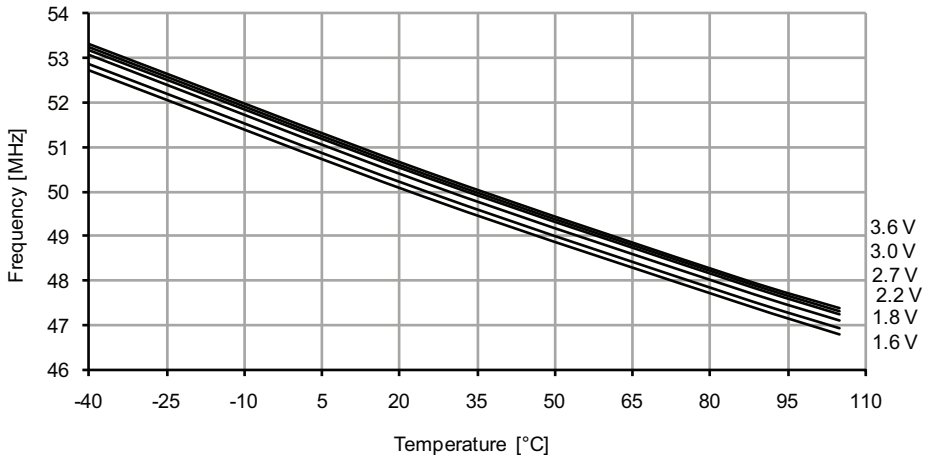



**Figure 37-165. 48MHz internal oscillator frequency vs. temperature.**
***DFLL enabled, from the 32.768kHz internal oscillator.***

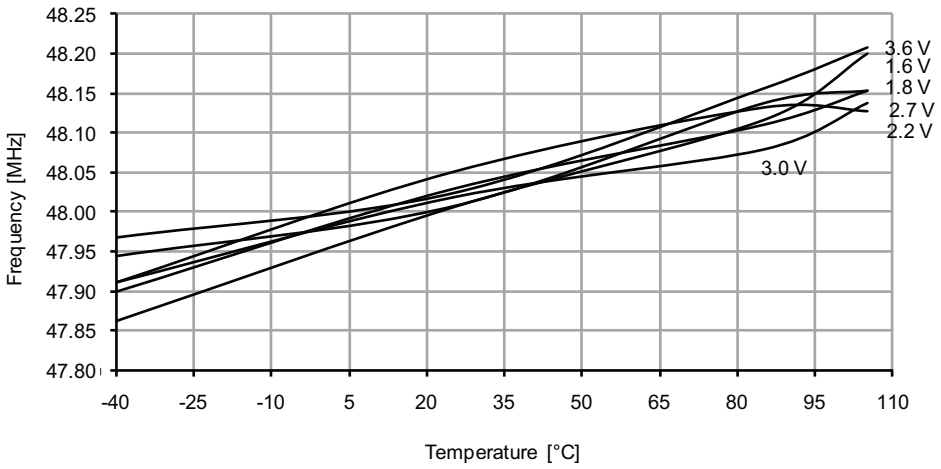
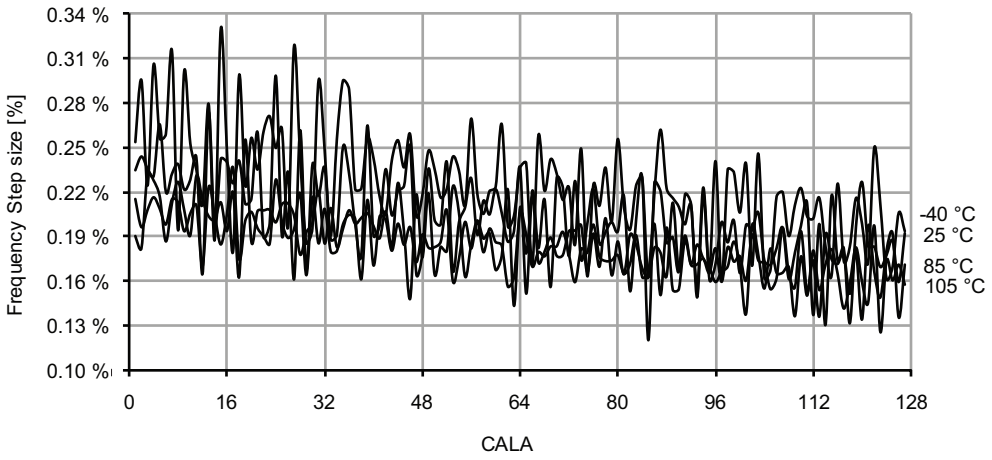


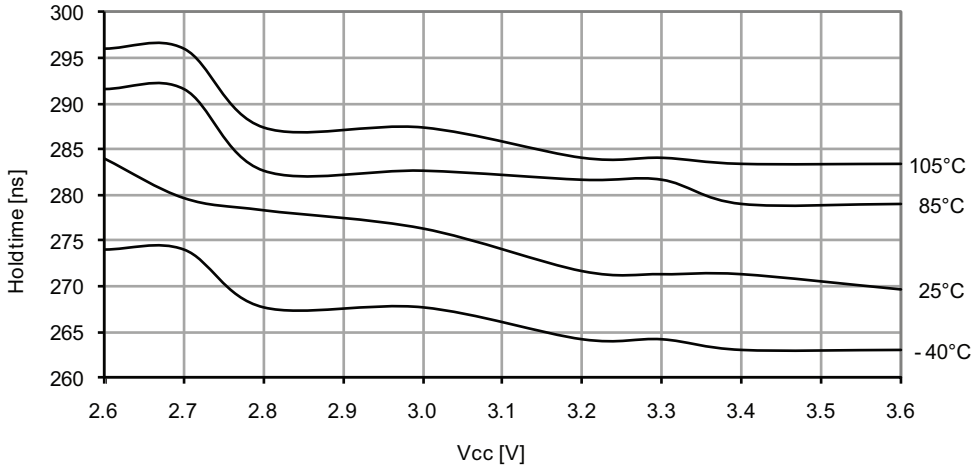
**Figure 37-166. 48MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3.0V.***



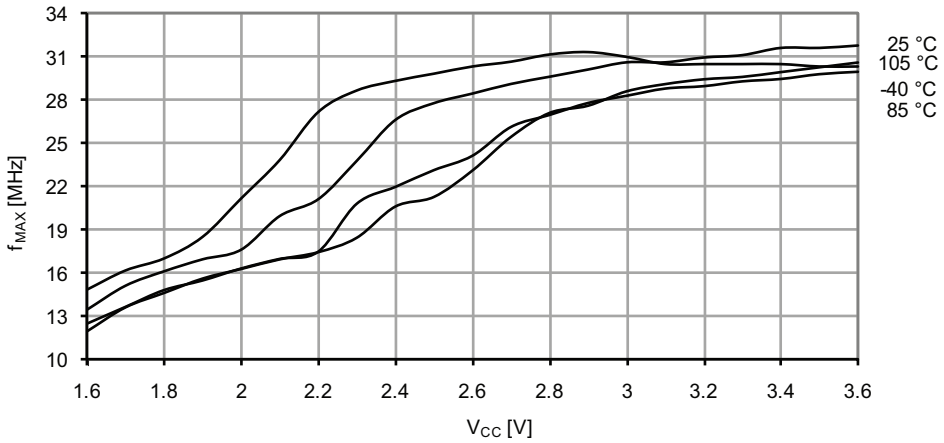

## 37.2.11 Two-Wire Interface characteristics

**Figure 37-167. SDA hold time vs. supply voltage.**



### 37.2.12 PDI characteristics

**Figure 37-168. Maximum PDI frequency vs. $V_{CC}$.**



## 37.3 ATxmega64A4U

### 37.3.1 Current consumption

#### 37.3.1.1 Active mode supply current

**Figure 37-169. Active supply current vs. frequency.**
***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

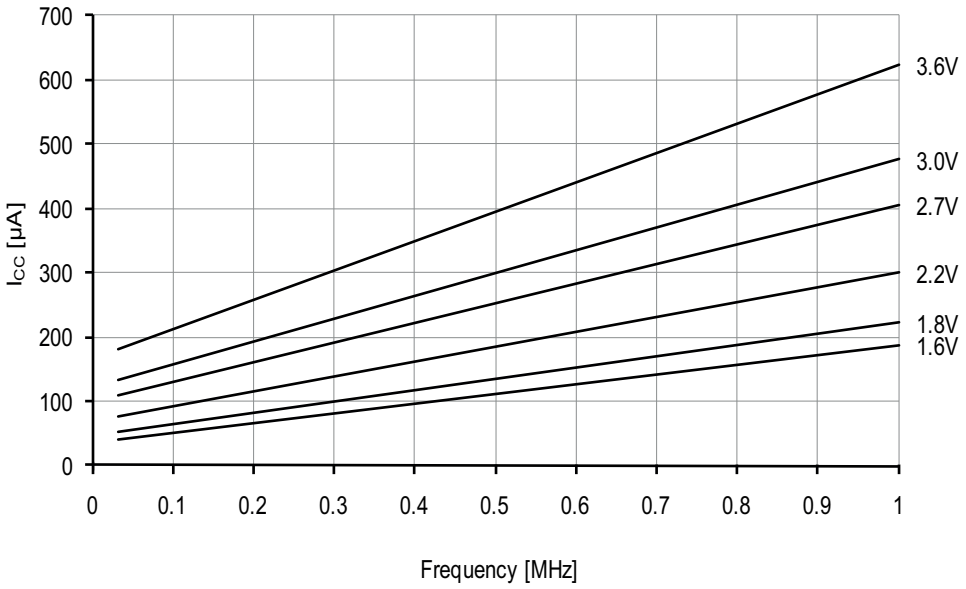



**Figure 37-170. Active supply current vs. frequency.**
***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C.***

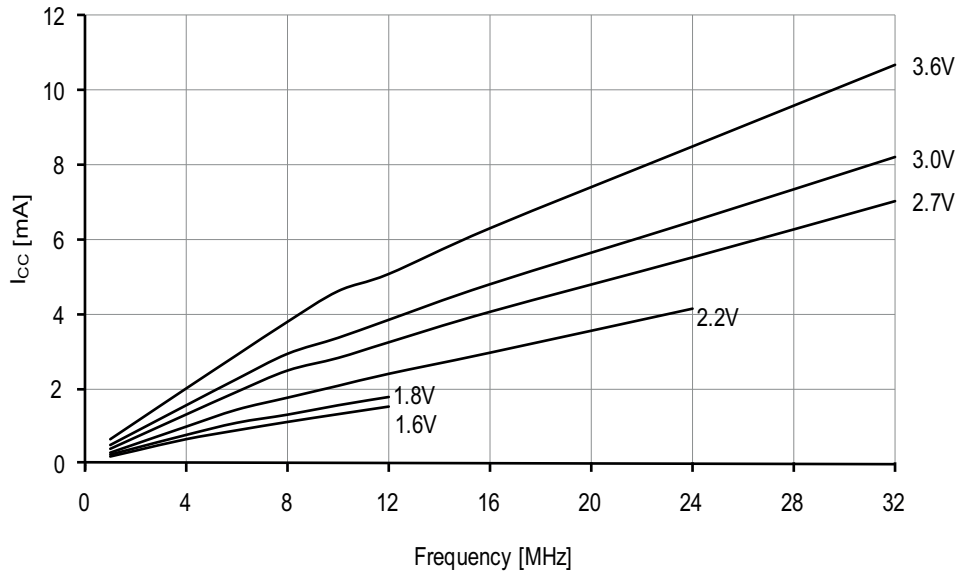


**Figure 37-171. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32.768kHz internal oscillator.***

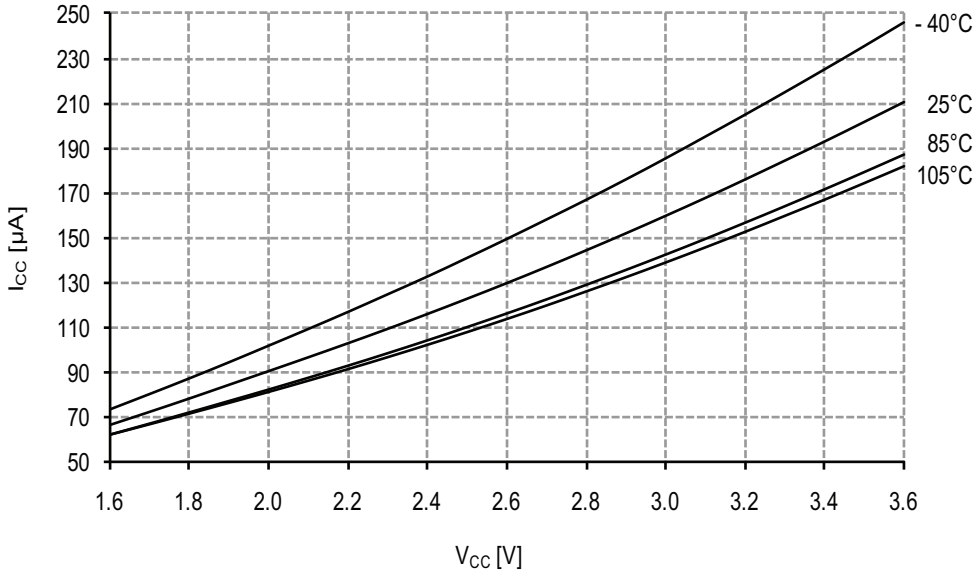



**Figure 37-172. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock.***

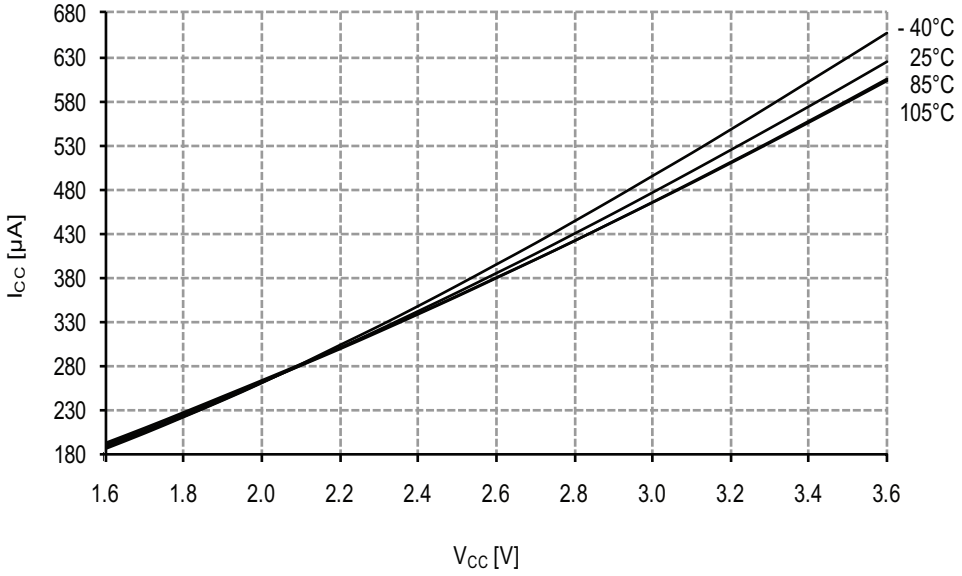


**Figure 37-173. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator.***

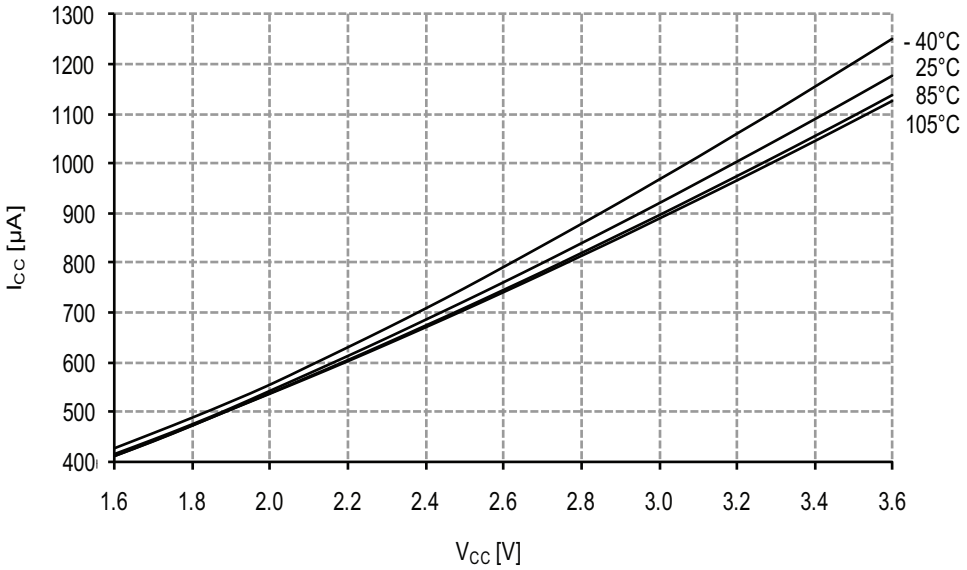



**Figure 37-174. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz.***

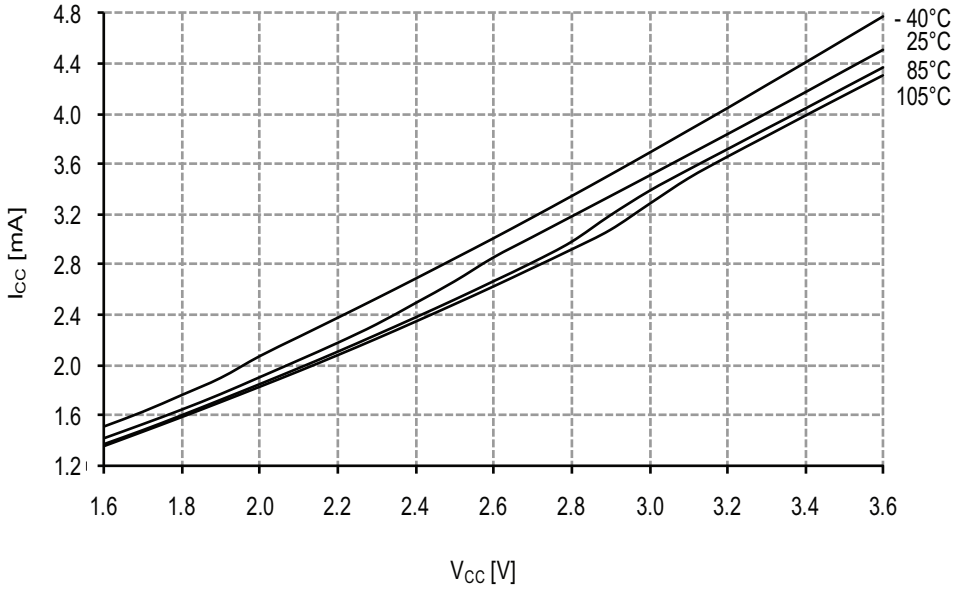
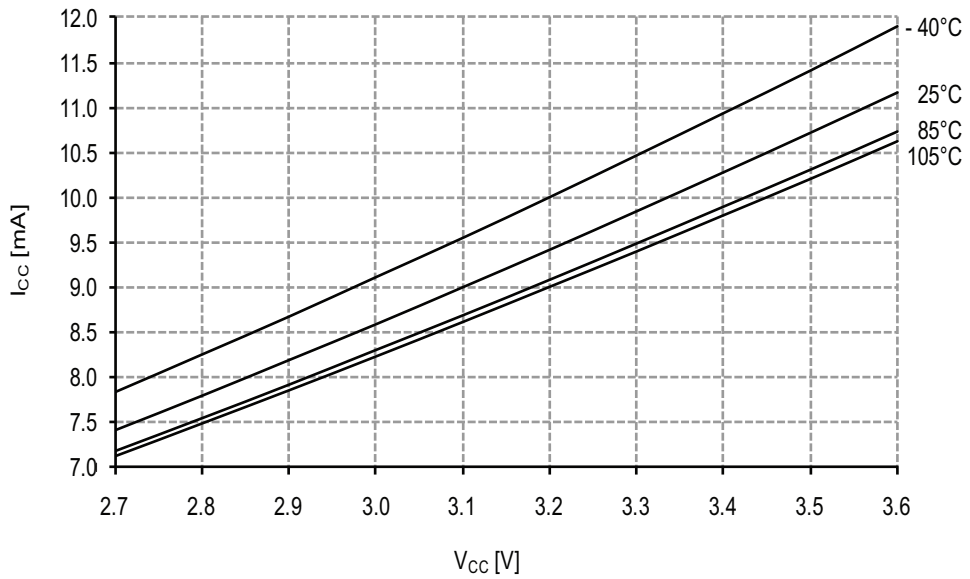


**Figure 37-175. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator.***




### 37.3.1.2 Idle mode supply current

**Figure 37-176. Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

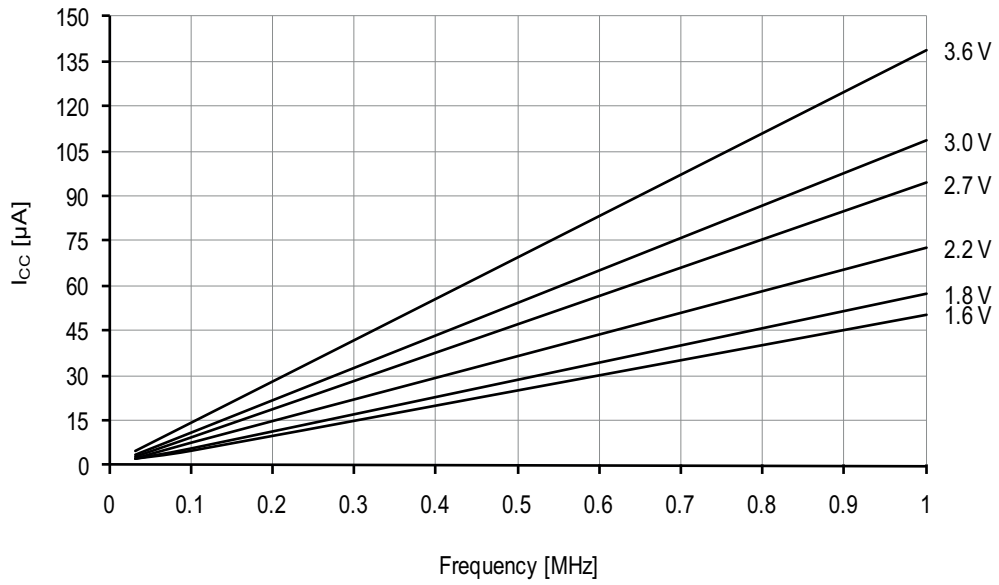


**Figure 37-177. Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C.***

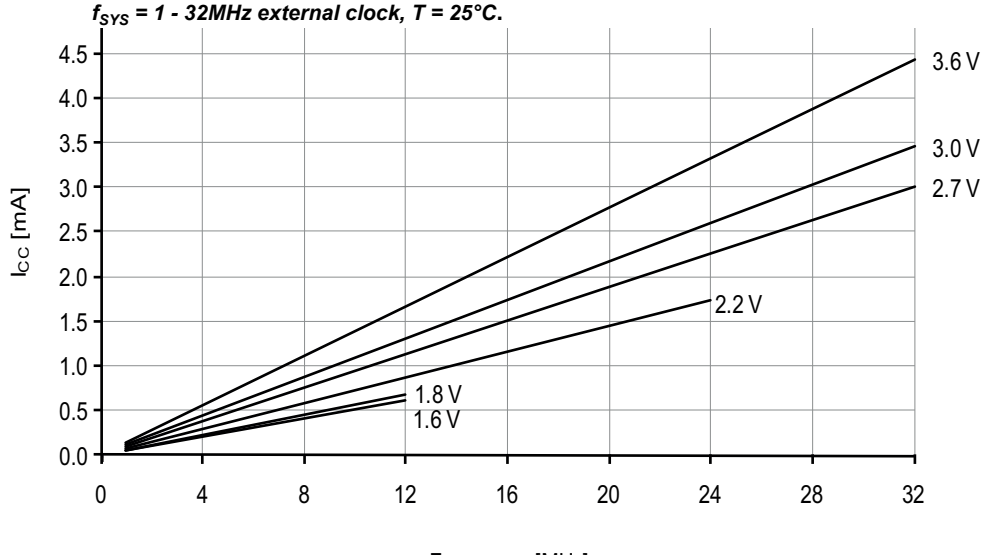



**Figure 37-178. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32.768kHz internal oscillator.***

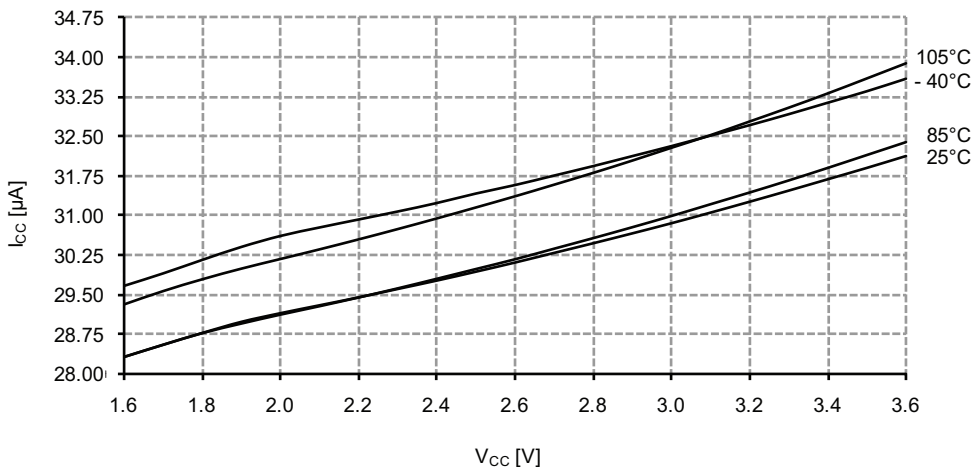


**Figure 37-179. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock.***

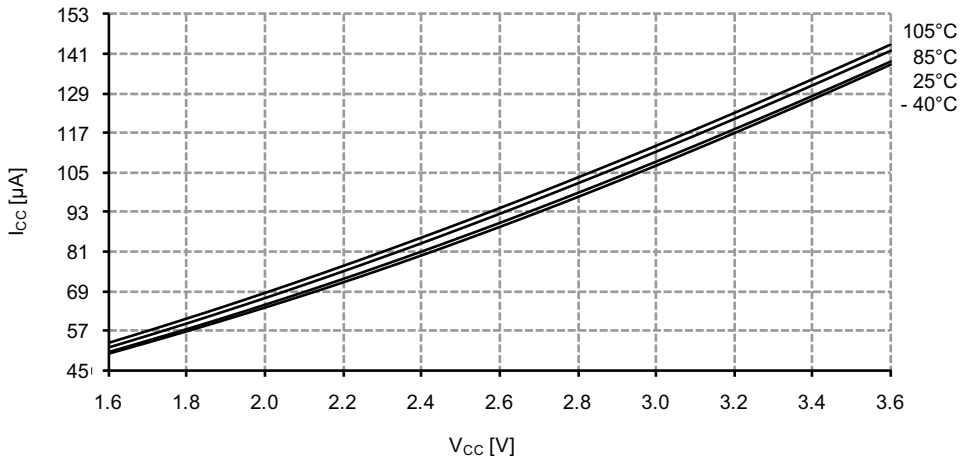



**Figure 37-180. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator.***

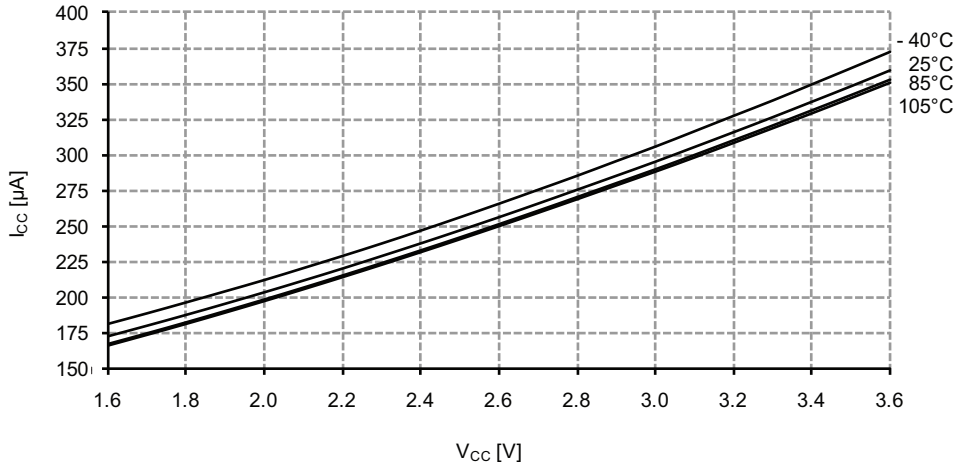


**Figure 37-181. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz.***

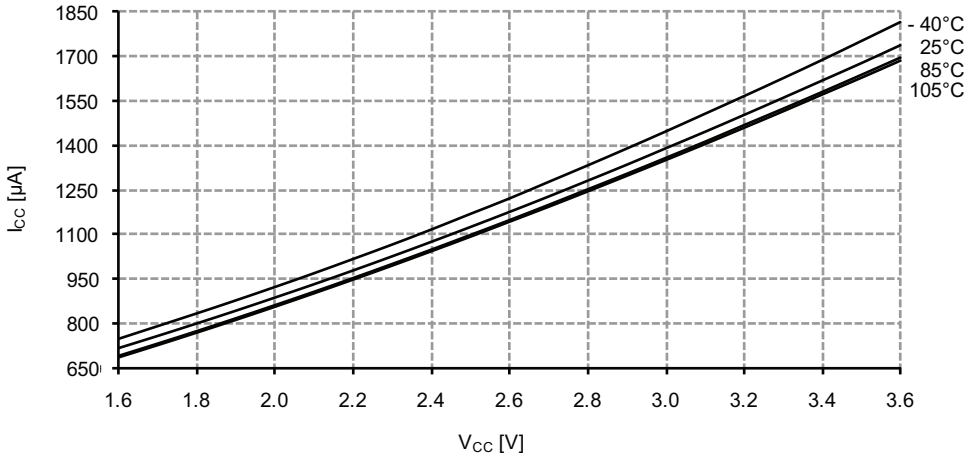
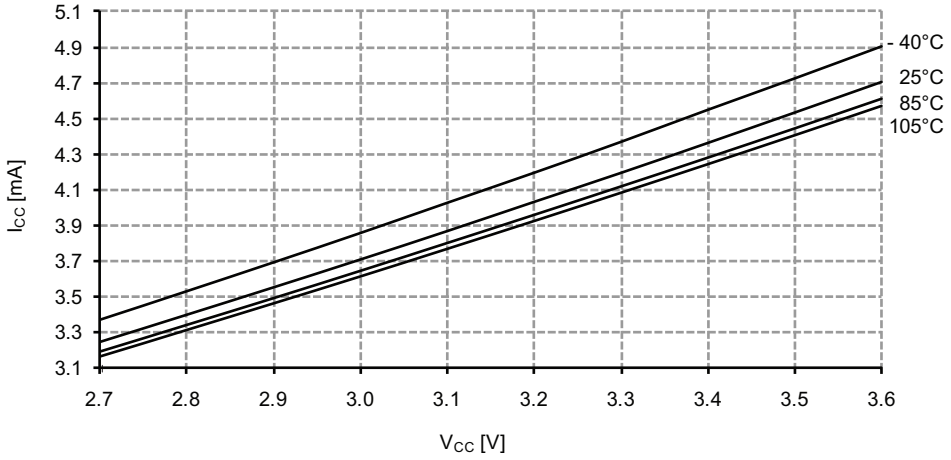



**Figure 37-182. Idle mode current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator.***



### 37.3.1.3 Power-down mode supply current

**Figure 37-183. Power-down mode supply current vs. temperature.**

***All functions disabled.***

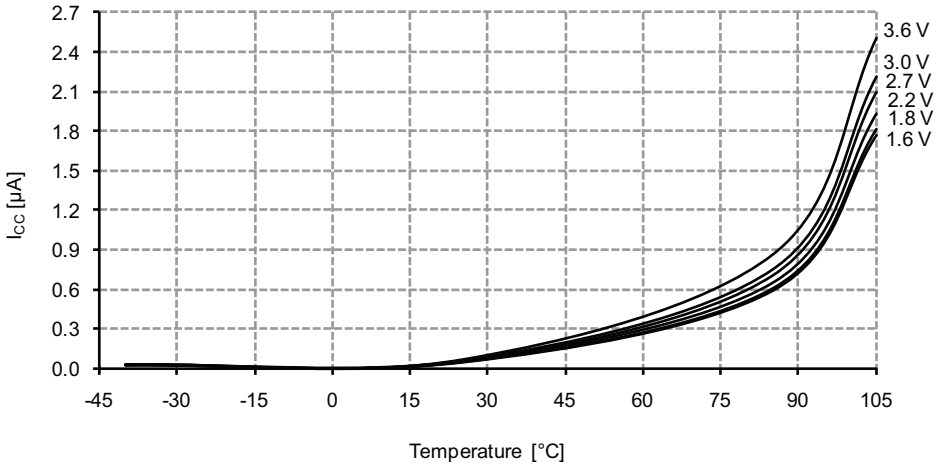



**Figure 37-184. Power-down mode supply current vs. $V_{CC}$.**

***All functions disabled.***

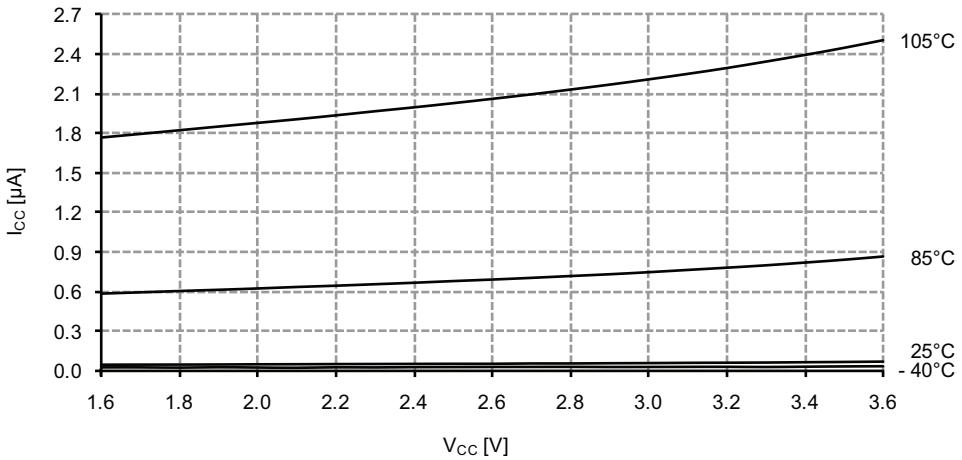
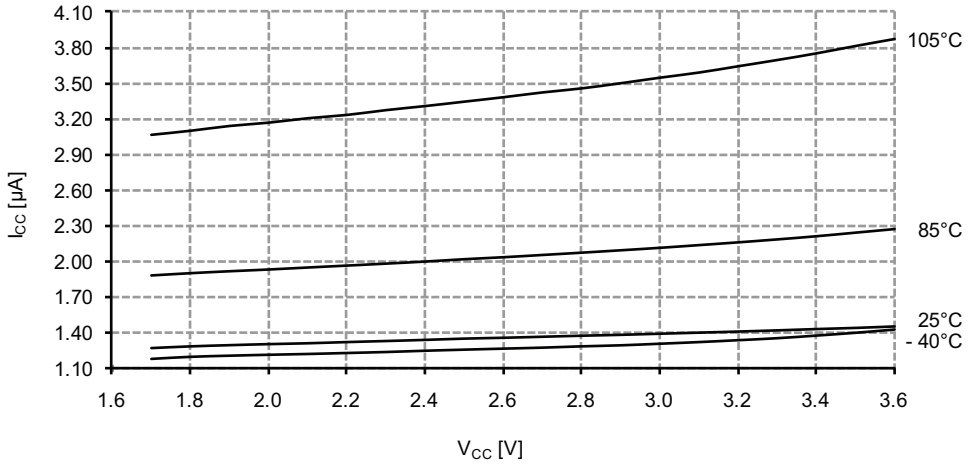


**Figure 37-185. Power-down mode supply current vs. $V_{CC}$.**

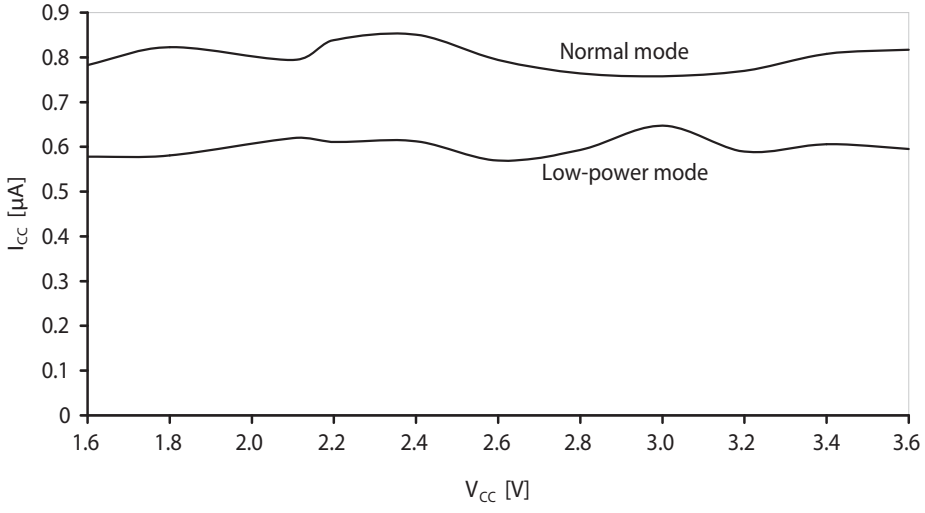
***Watchdog and sampled BOD enabled.***




### 37.3.1.4 Power-save mode supply current

**Figure 37-186. Power-save mode supply current vs.$V_{CC}$.**

***Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.***



### 37.3.1.5 Standby mode supply current

**Figure 37-187. Standby supply current vs. $V_{CC}$.**
***Standby, $f_{SYS}$ = 1MHz.***

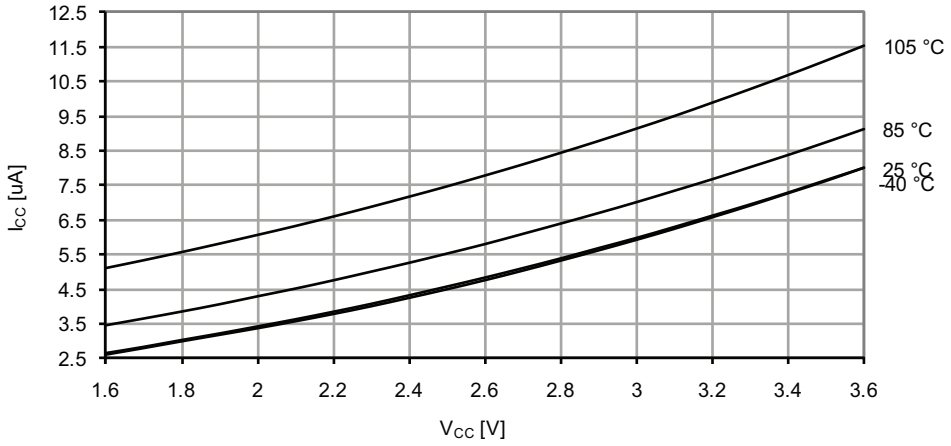
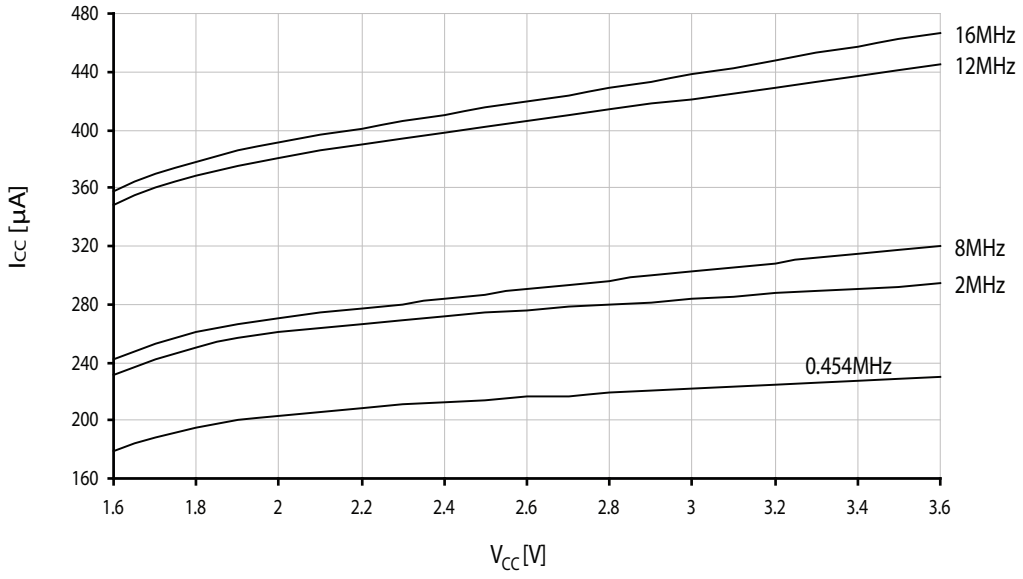



**Figure 37-188. Standby supply current vs. $V_{CC}$.**
***25°C, running from different crystal oscillators.***



### 37.3.2 I/O Pin Characteristics

#### 37.3.2.1 Pull-up

**Figure 37-189. I/O pin pull-up resistor current vs. input voltage.**

***$V_{CC}$ = 1.8V.***

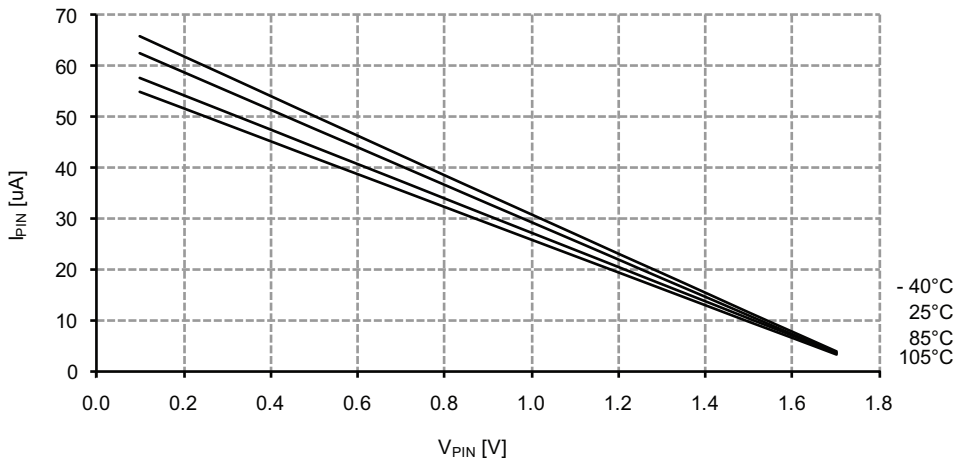



**Figure 37-190. I/O pin pull-up resistor current vs. input voltage.**

***$V_{CC}$ = 3.0V.***

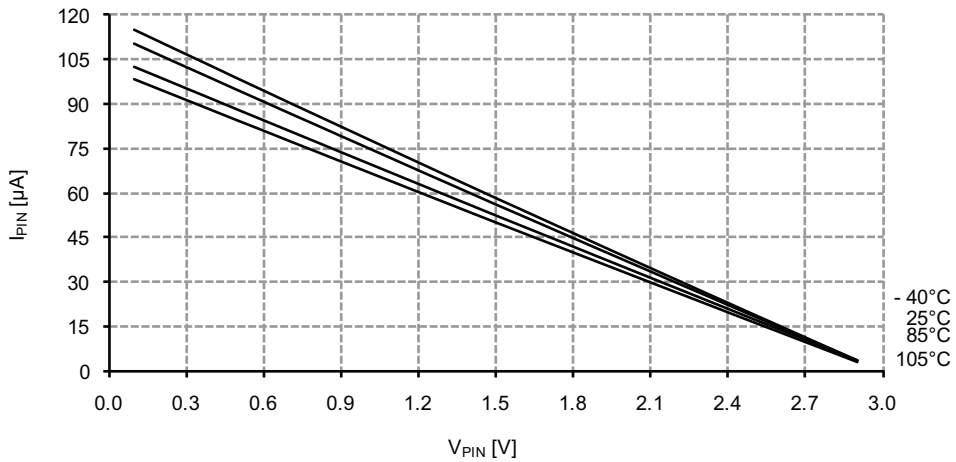
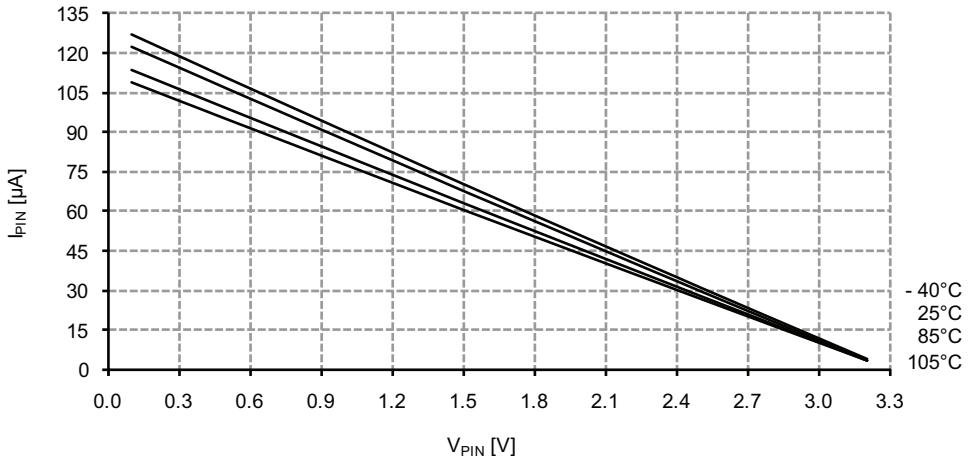


**Figure 37-191. I/O pin pull-up resistor current vs. input voltage.**

***$V_{CC}$ = 3.3V.***




### 37.3.2.2 Output Voltage vs. Sink/Source Current

**Figure 37-192. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 1.8V.***

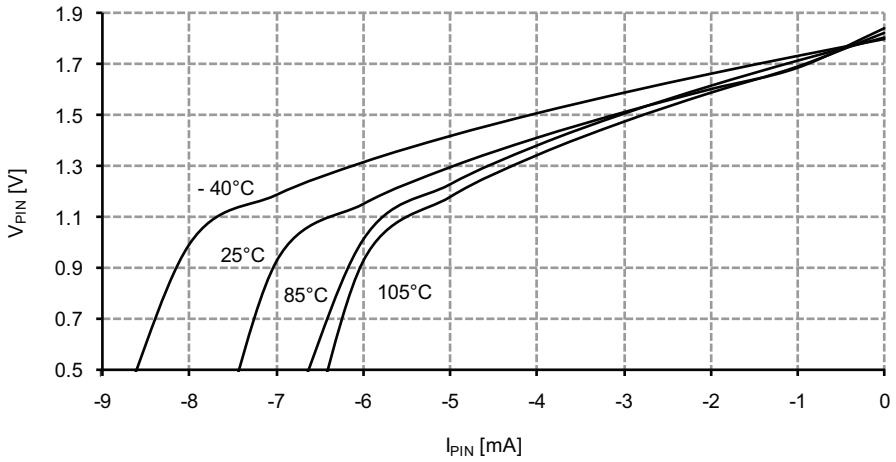


**Figure 37-193. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 3.0V.***

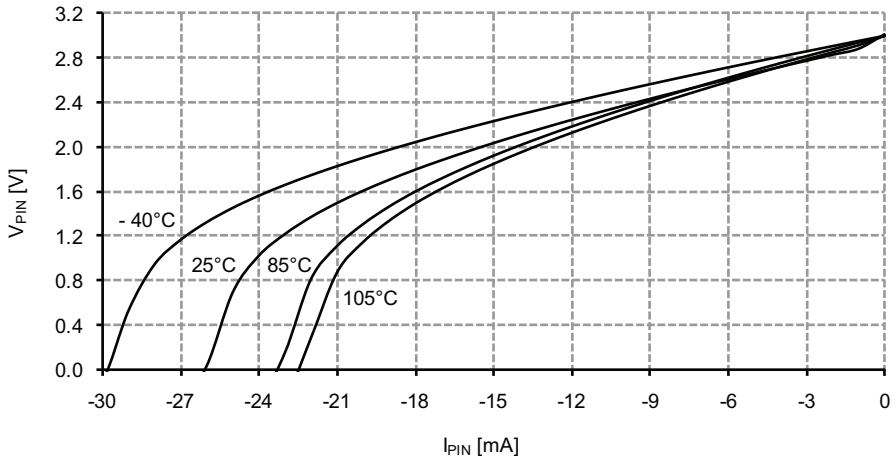



**Figure 37-194. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 3.3V.***

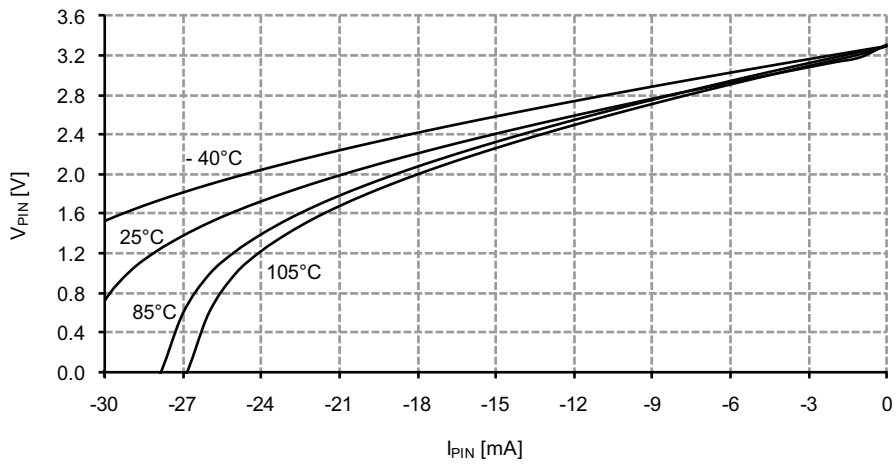


**Figure 37-195. I/O pin output voltage vs. source current.**

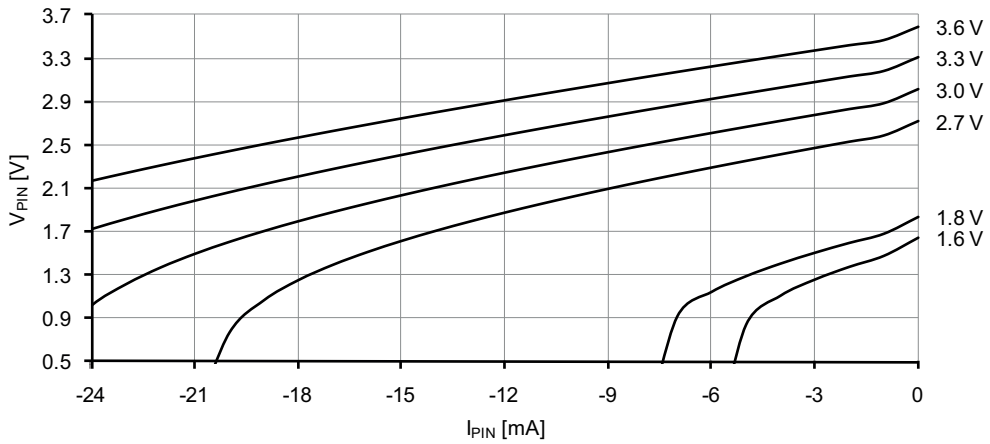



**Figure 37-196. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 1.8V.***

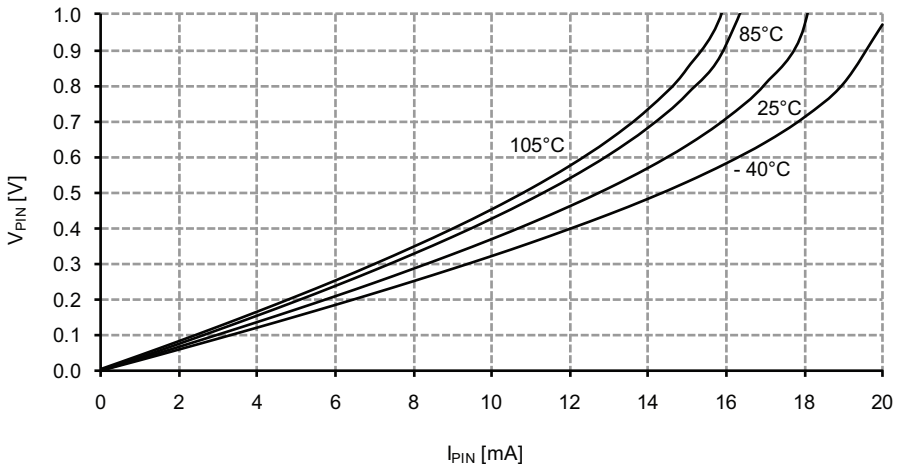


**Figure 37-197. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 3.0V.***

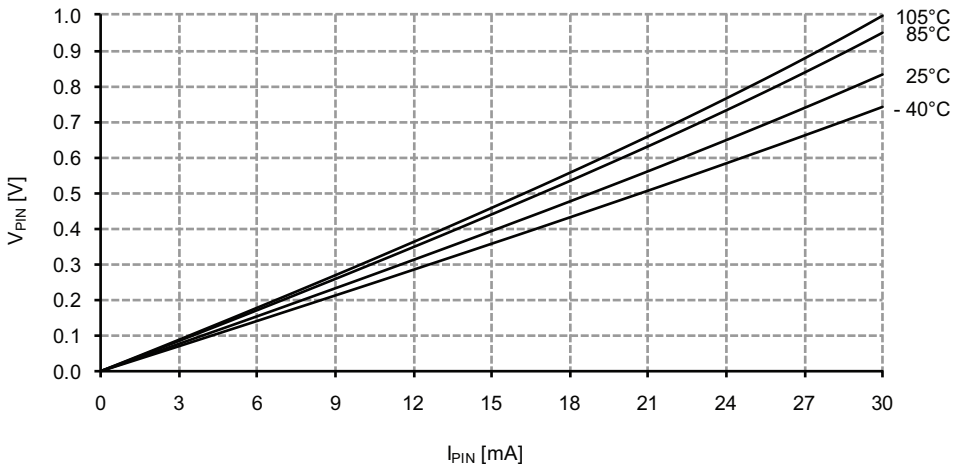



**Figure 37-198. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 3.3V.***

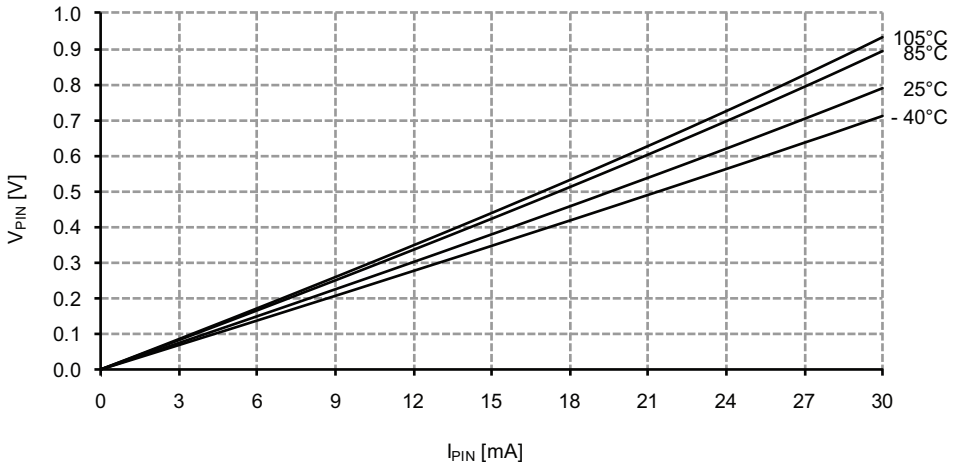
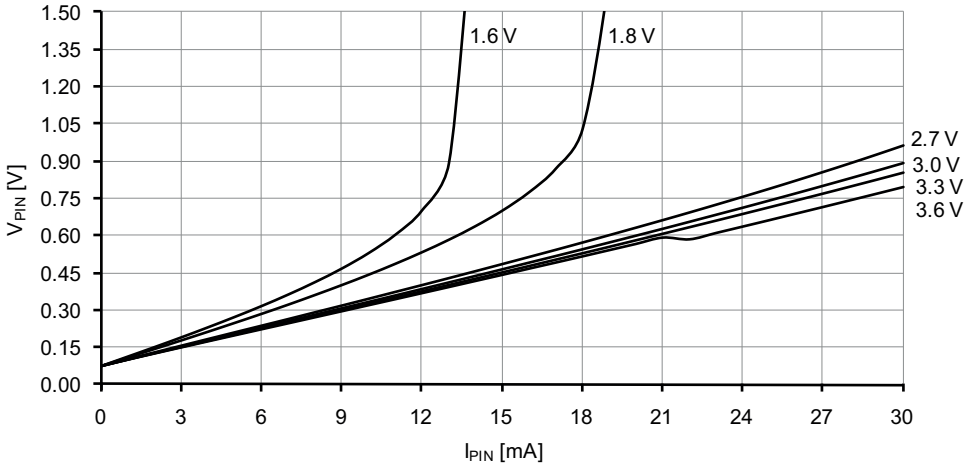


**Figure 37-199. I/O pin output voltage vs. sink current.**




### 37.3.2.3 Thresholds and Hysteresis

**Figure 37-200. I/O pin input threshold voltage vs. $V_{CC}$.**
***T = 25°C.***

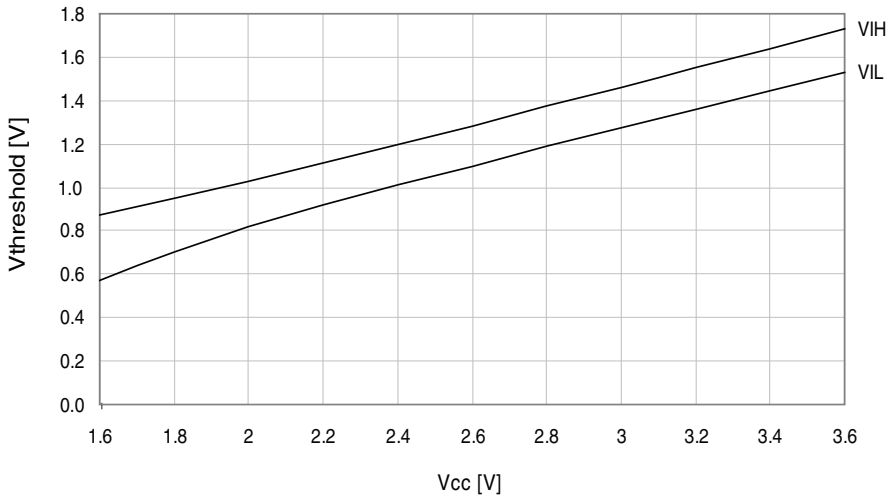


**Figure 37-201. I/O pin input threshold voltage vs. $V_{CC}$.**

***$V_{IH}$ I/O pin read as "1".***

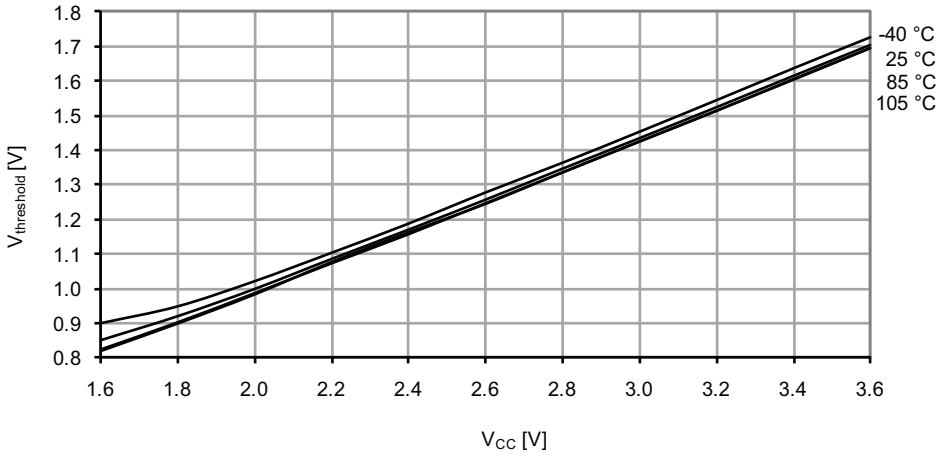



**Figure 37-202. I/O pin input threshold voltage vs. $V_{CC}$.**

***$V_{IL}$ I/O pin read as "0".***

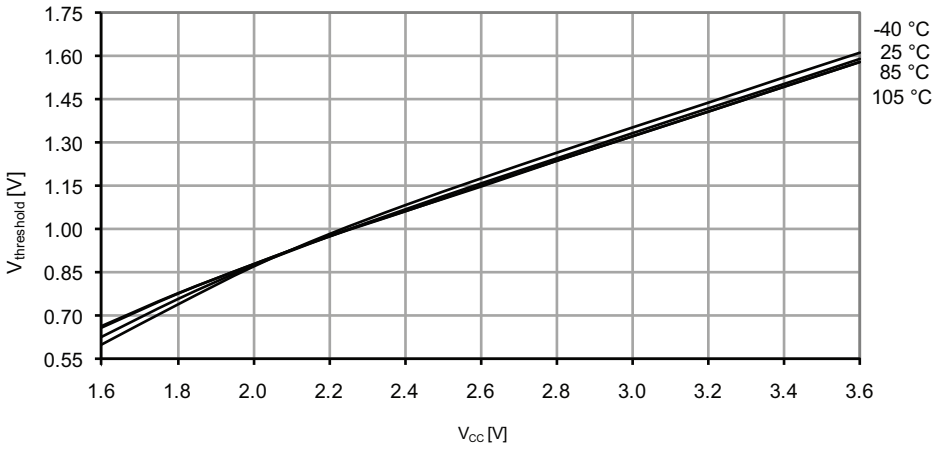
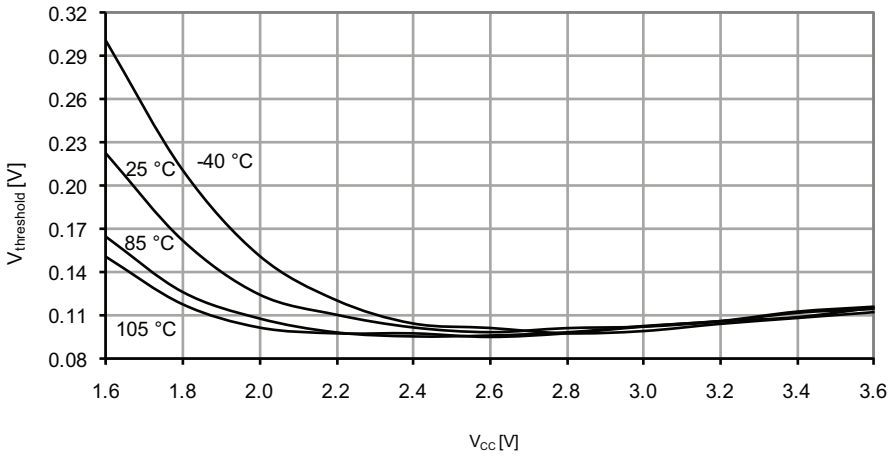


**Figure 37-203. I/O pin input hysteresis vs. $V_{CC}$.**




## 37.3.3 ADC Characteristics

**Figure 37-204. INL error vs. external $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, external reference.***

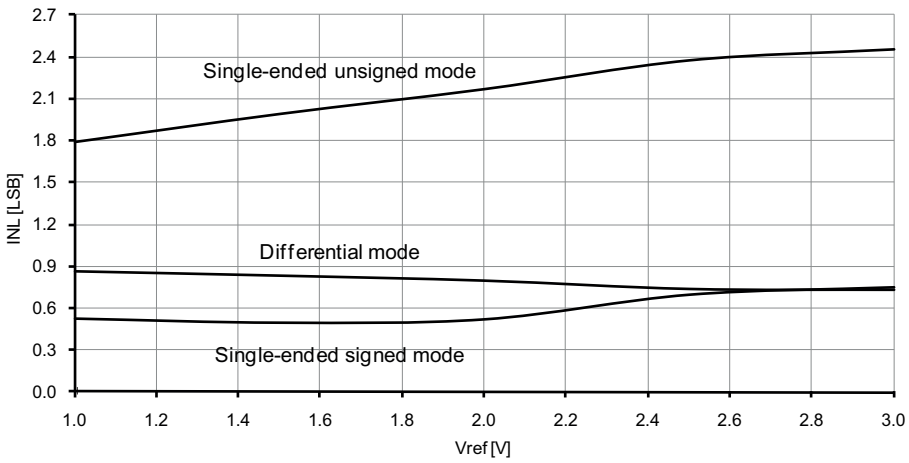


**Figure 37-205. INL error vs. sample rate.**

***T = 25°C, $V_{CC}$ = 2.7V, $V_{REF}$ = 1.0V external.***

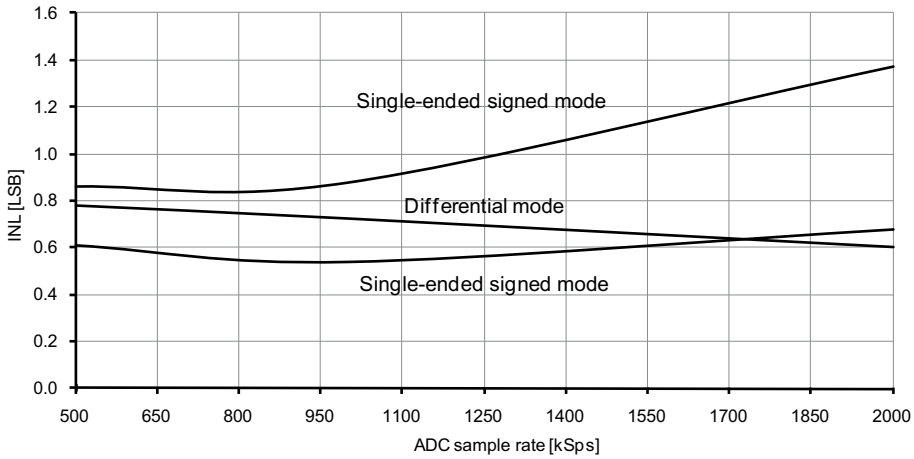



**Figure 37-206. INL error vs. input code**

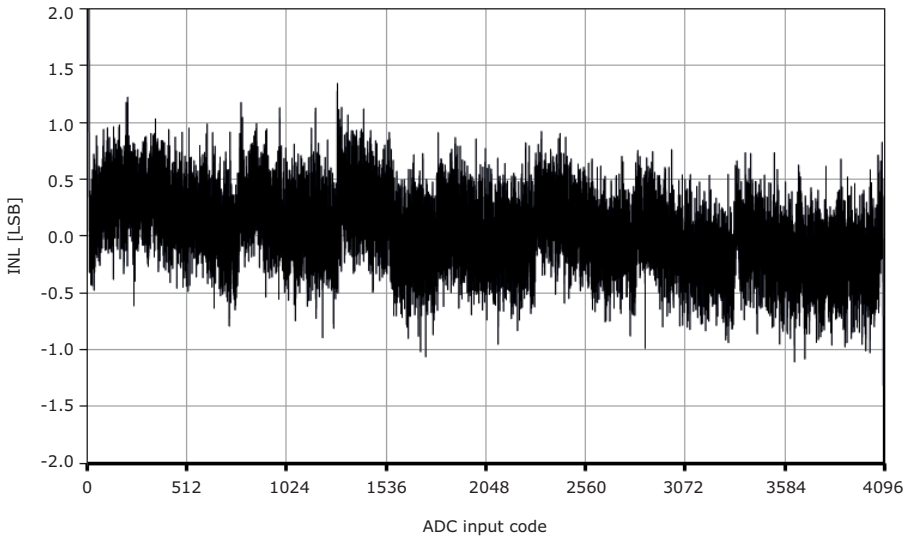


**Figure 37-207. DNL error vs. external $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, external reference.***

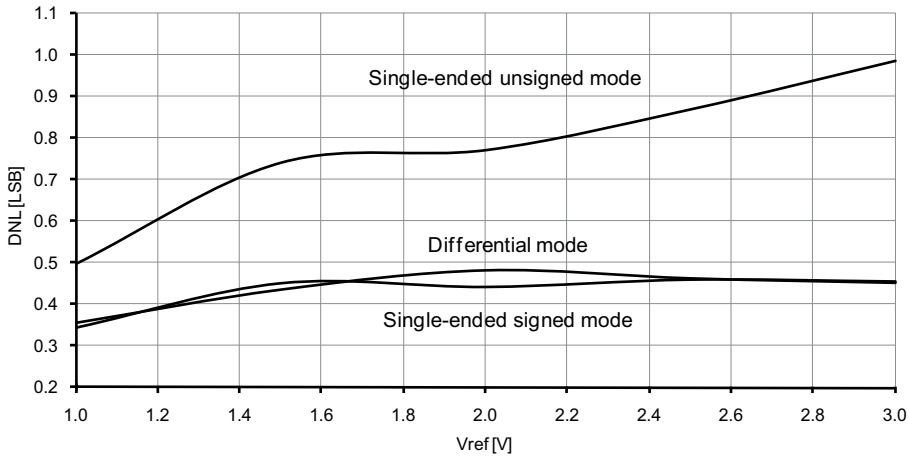



**Figure 37-208. DNL error vs. sample rate.**

***T = 25°C, $V_{CC}$ = 2.7V, $V_{REF}$ = 1.0V external.***

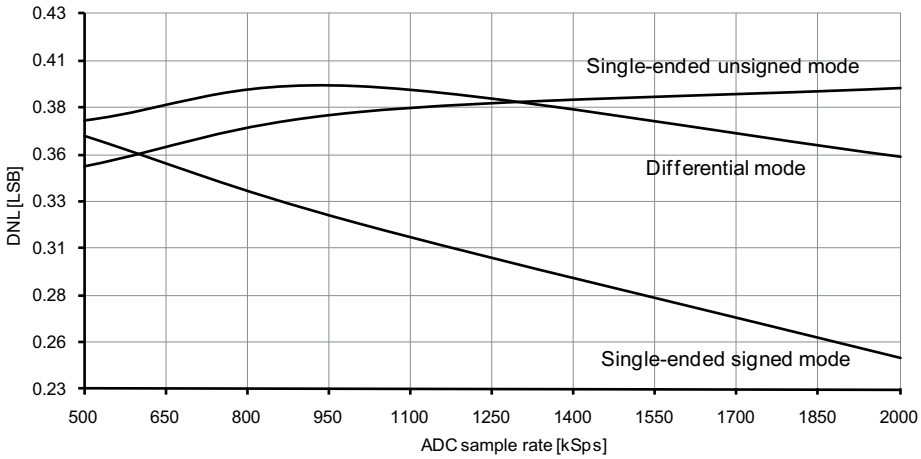


**Figure 37-209. DNL error vs. input code.**

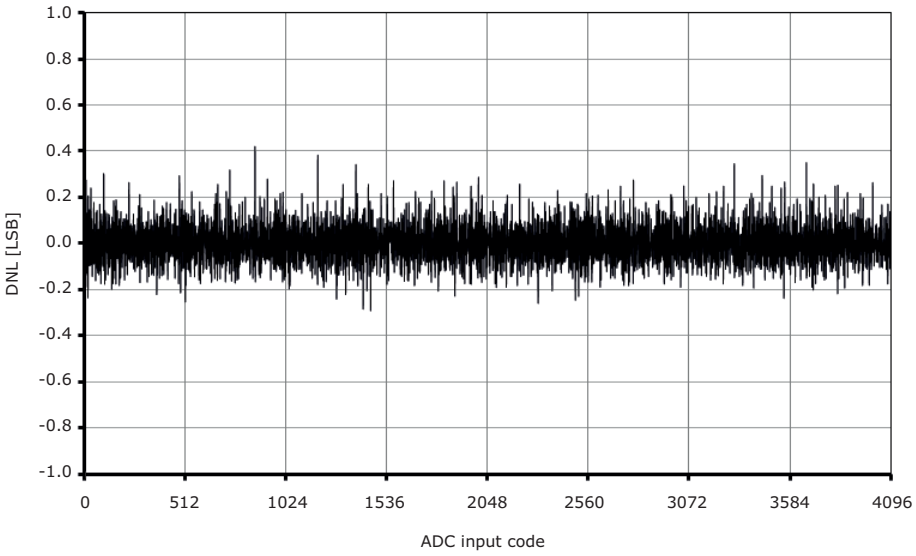



**Figure 37-210. Gain error vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

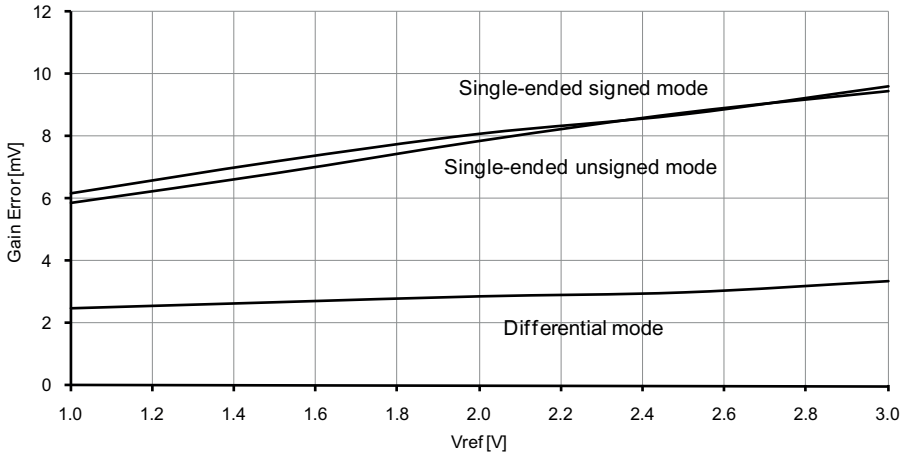


**Figure 37-211. Gain error vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***

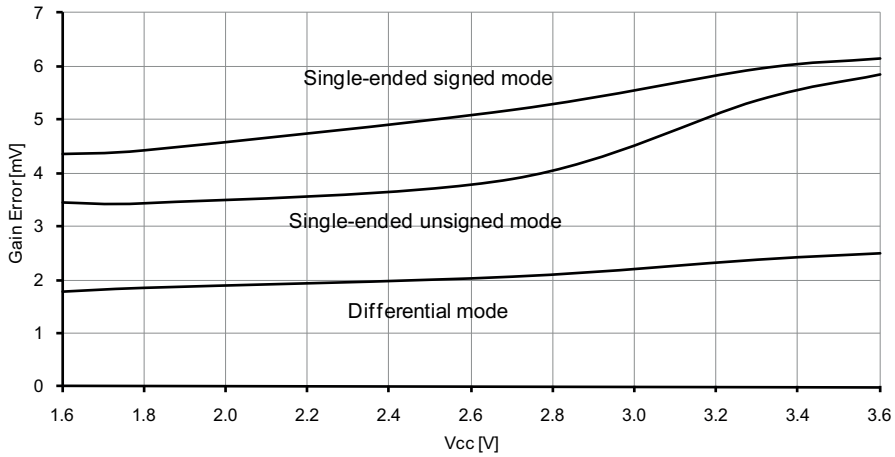



**Figure 37-212. Offset error vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

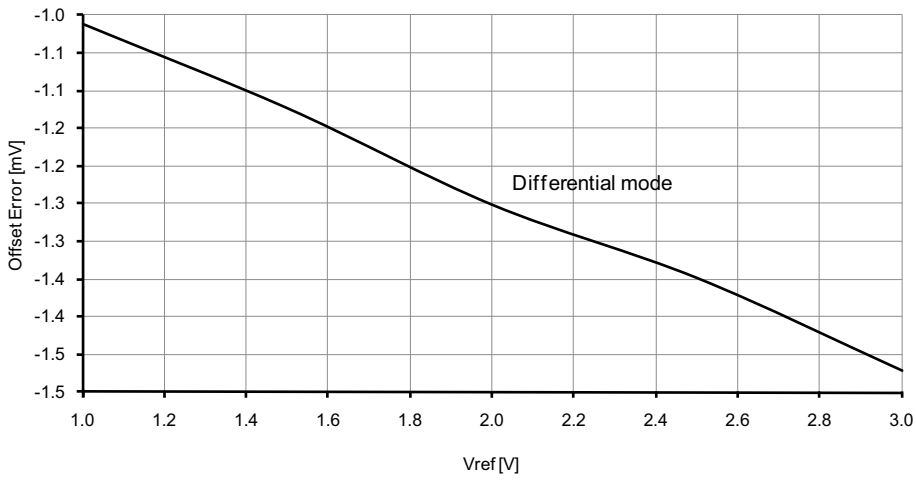


**Figure 37-213. Gain error vs. temperature.**

***$V_{CC}$ = 2.7V, $V_{REF}$ = external 1.0V.***

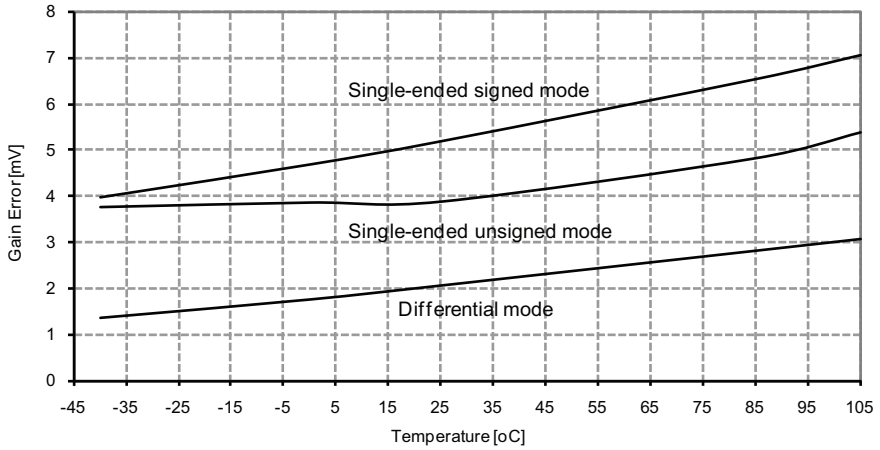



**Figure 37-214. Offset error vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***

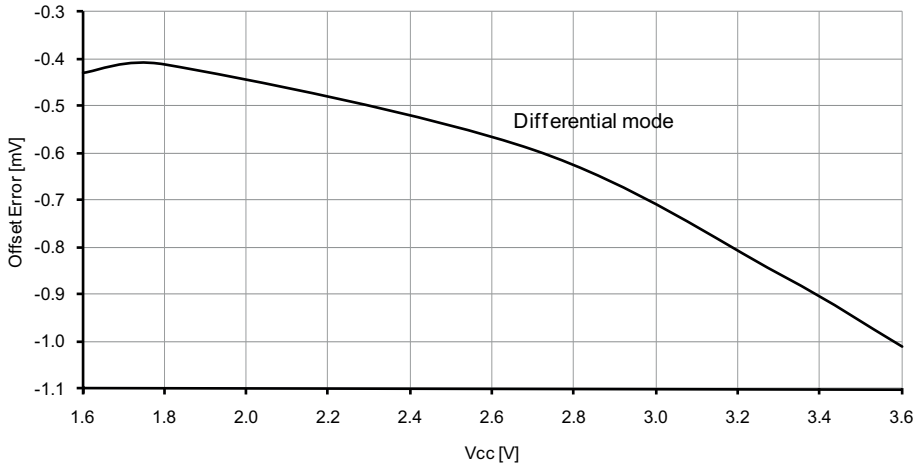


**Figure 37-215. Noise vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps.***

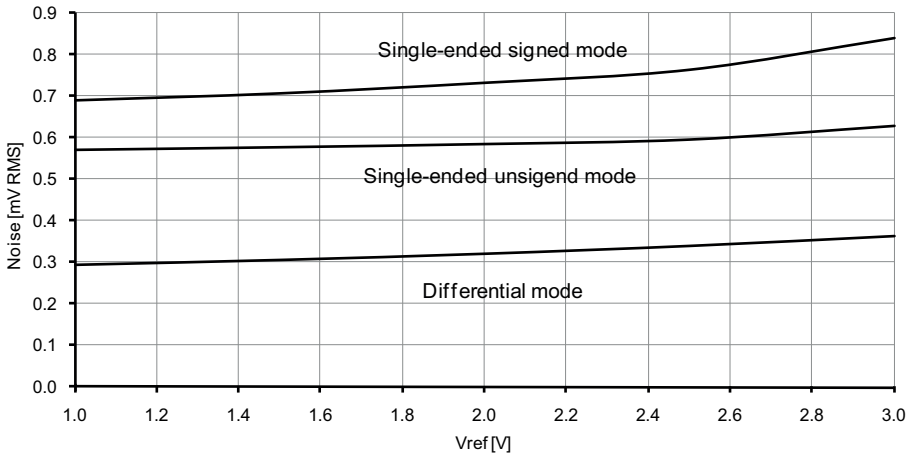
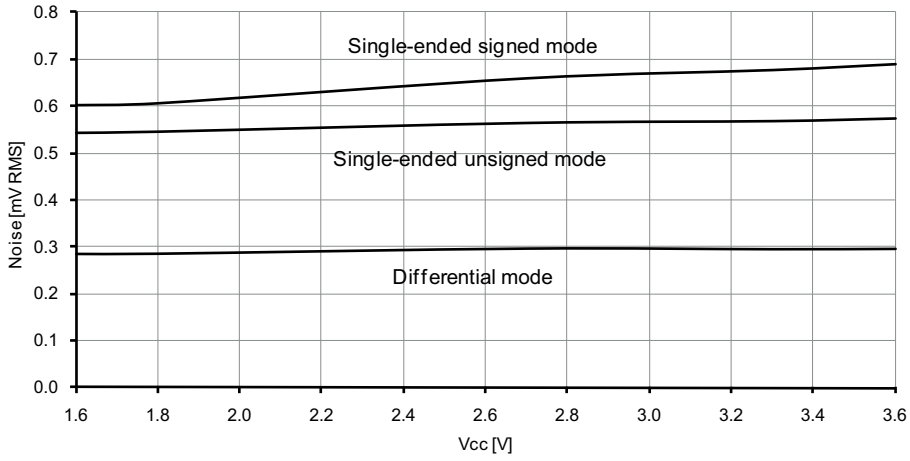



**Figure 37-216. Noise vs. $V_{CC}$.**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps.***



### 37.3.4 DAC Characteristics

**Figure 37-217. DAC INL error vs. $V_{REF}$.**
***$V_{CC}$ = 3.6V.***

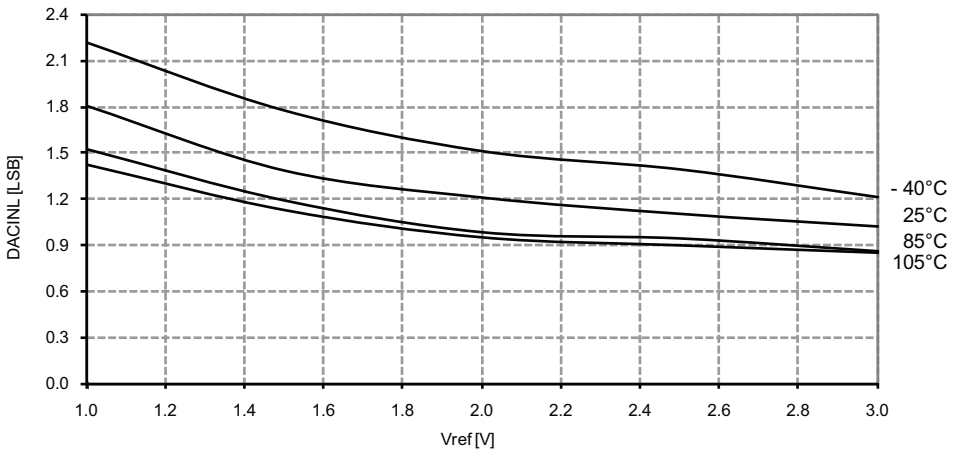



**Figure 37-218. DNL error vs. $V_{REF}$.**
***$V_{CC}$ = 3.6V.***

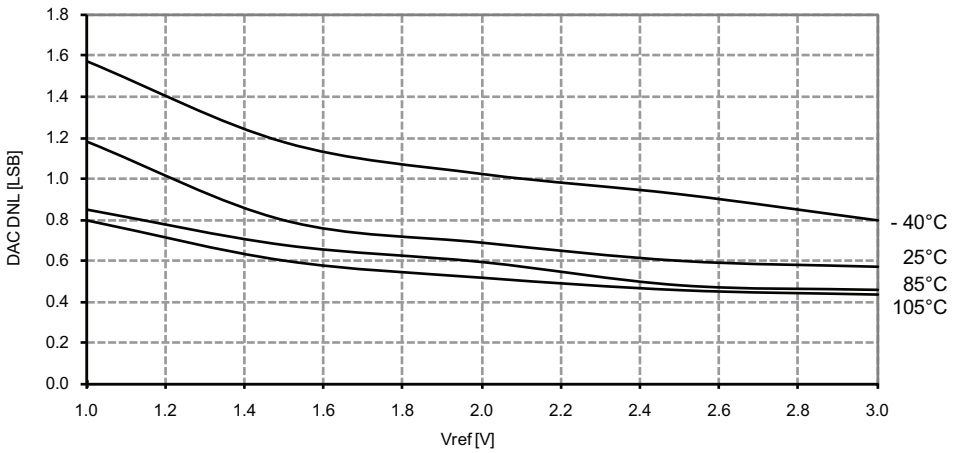
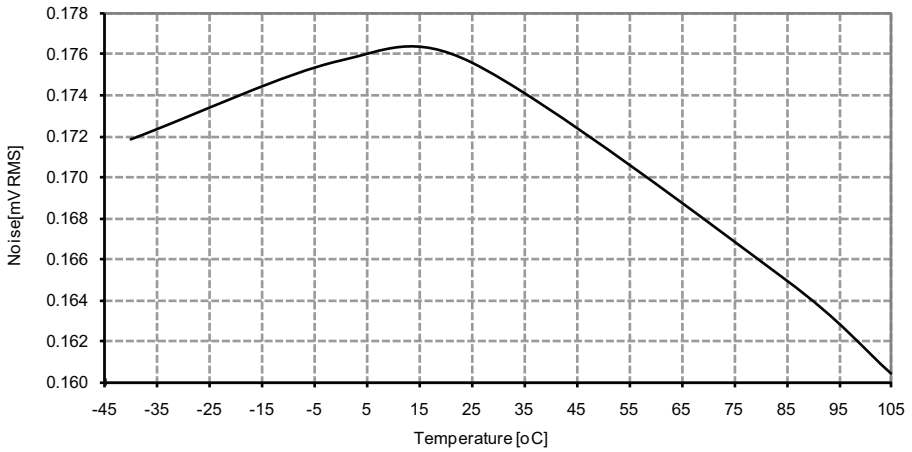


**Figure 37-219. DAC noise vs. temperature.**

***$V_{CC}$ = 2.7V, $V_{REF}$ = 1.0V .***




## 37.3.5 Analog Comparator Characteristics

**Figure 37-220. Analog comparator hysteresis vs. $V_{CC}$.**

***High-speed, small hysteresis.***

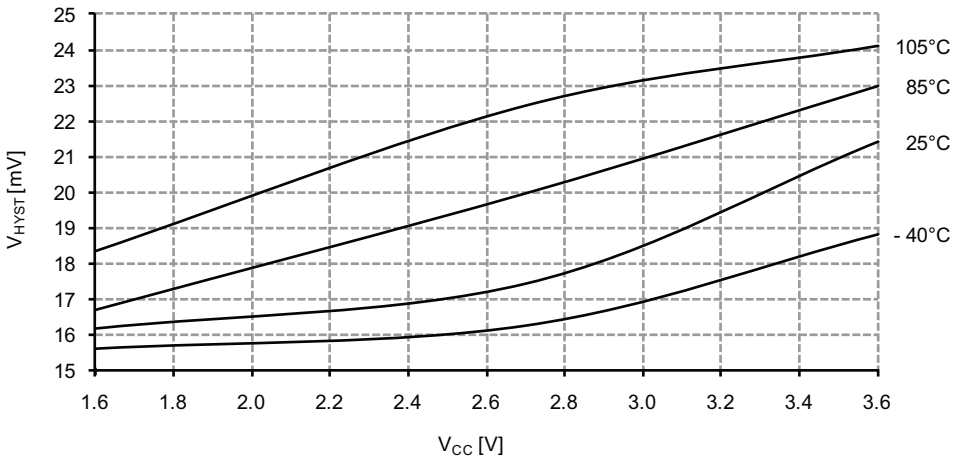


**Figure 37-221. Analog comparator hysteresis vs. $V_{CC}$.**

***Low power, small hysteresis.***

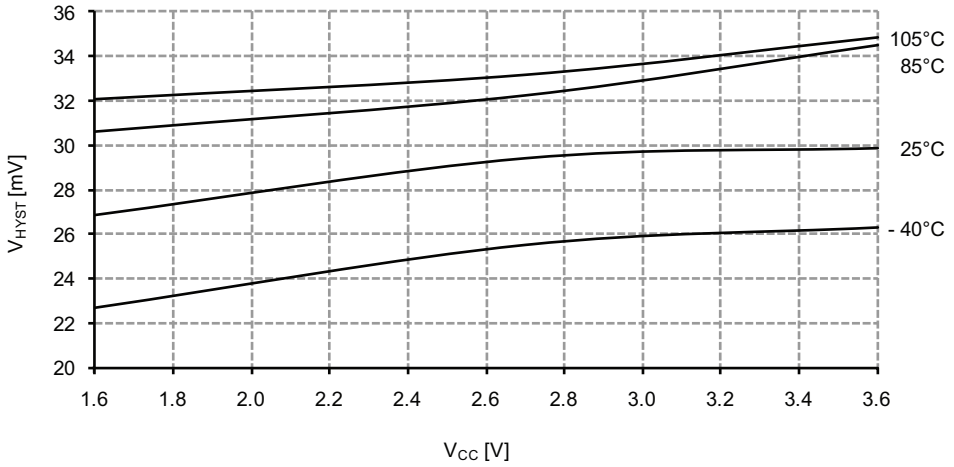



**Figure 37-222. Analog comparator hysteresis vs. $V_{CC}$.**

***High-speed mode, large hysteresis.***

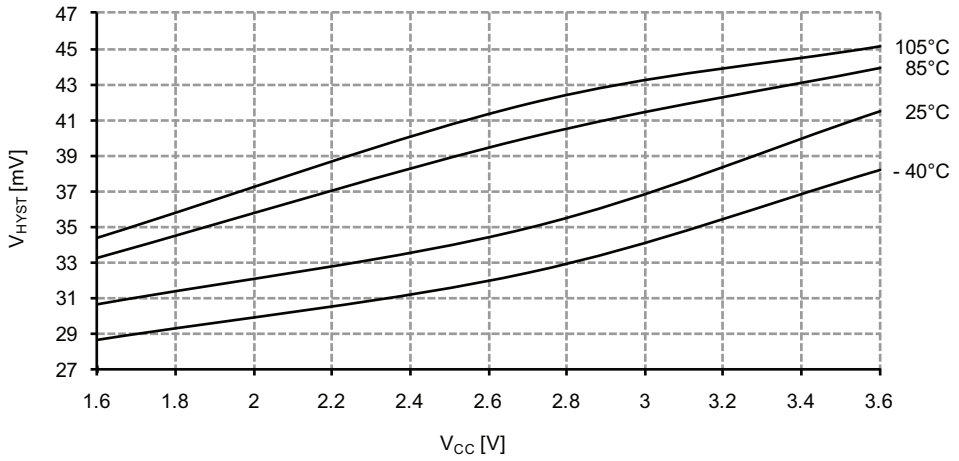


**Figure 37-223. Analog comparator hysteresis vs. $V_{CC}$.**

***Low power, large hysteresis.***

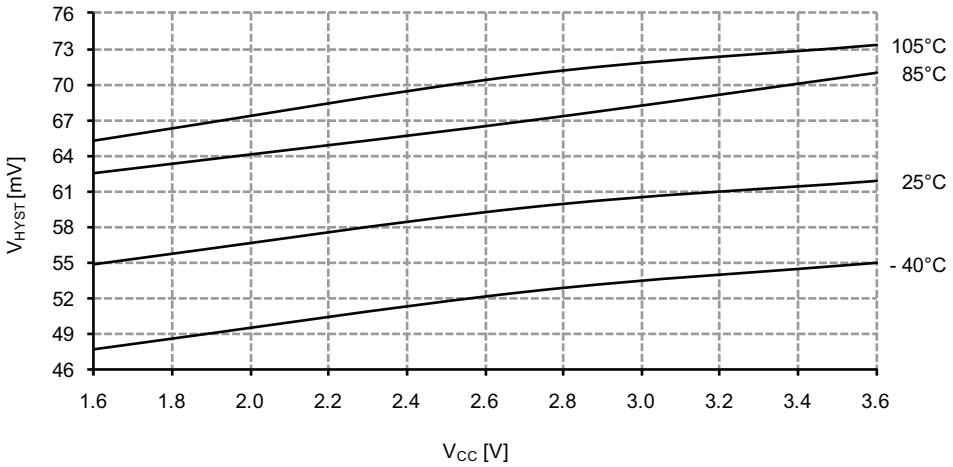



**Figure 37-224. Analog comparator current source vs. calibration value.**

***Temperature = 25°C.***

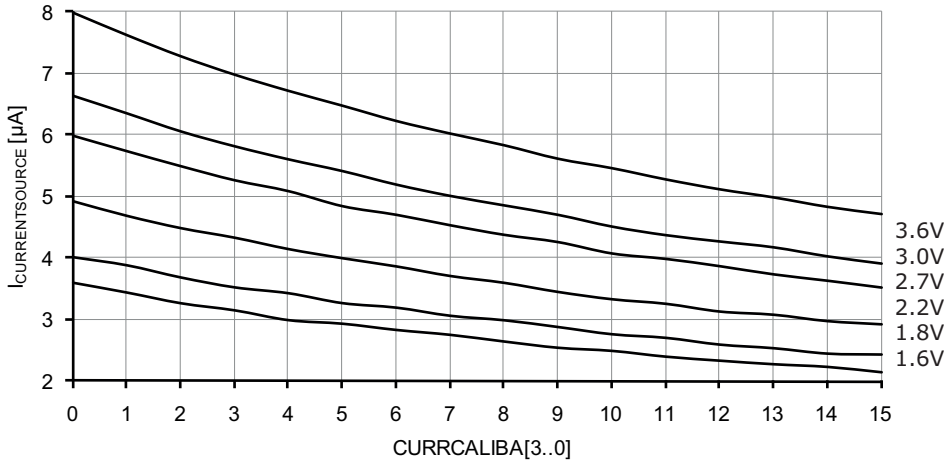


**Figure 37-225. Analog comparator current source vs. calibration value.**

***$V_{CC}$ = 3.0V.***

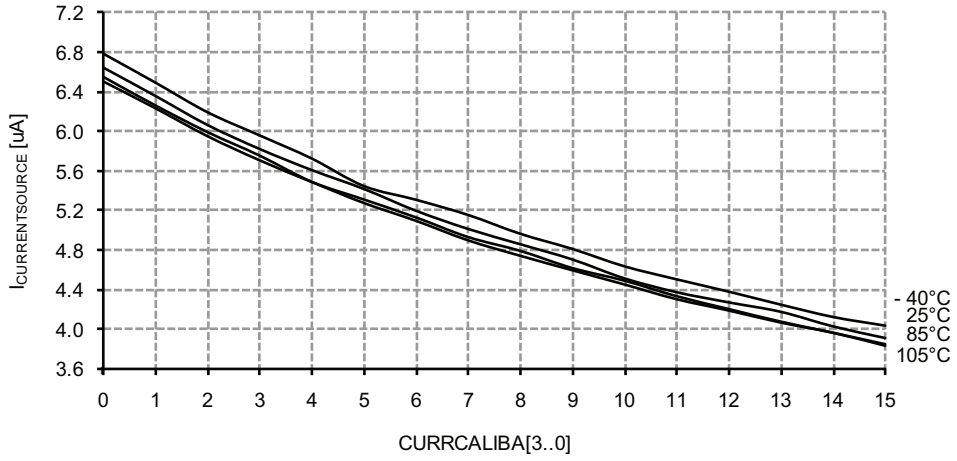
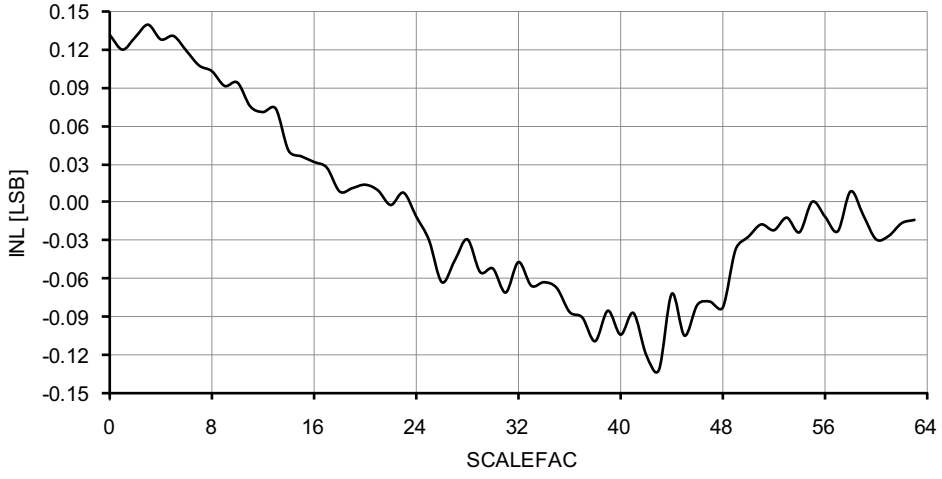


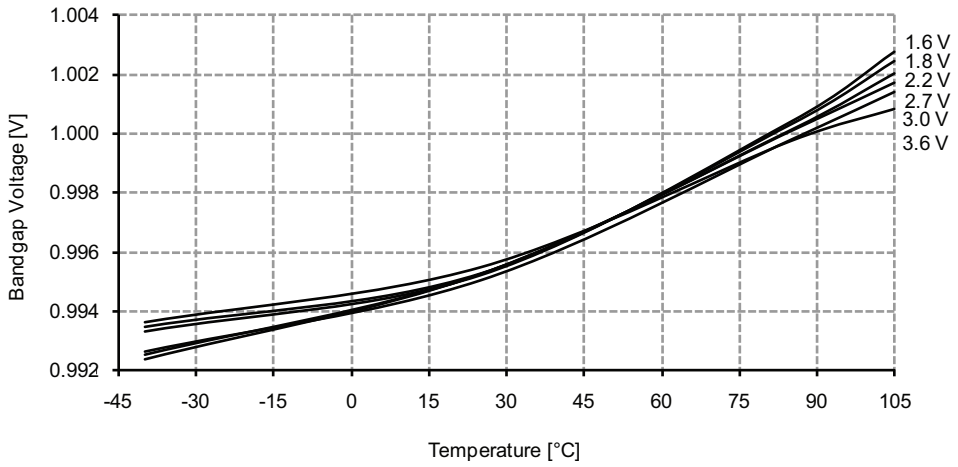

**Figure 37-226. Voltage scaler INL vs. SCALEFAC.**

***T = 25°C, $V_{CC}$ = 3.0V.***



### 37.3.6 Internal 1.0V reference Characteristics

**Figure 37-227. ADC/DAC Internal 1.0V reference vs. temperature.**




### 37.3.7 BOD Characteristics

**Figure 37-228. BOD thresholds vs. temperature.**

***BOD level = 1.6V.***

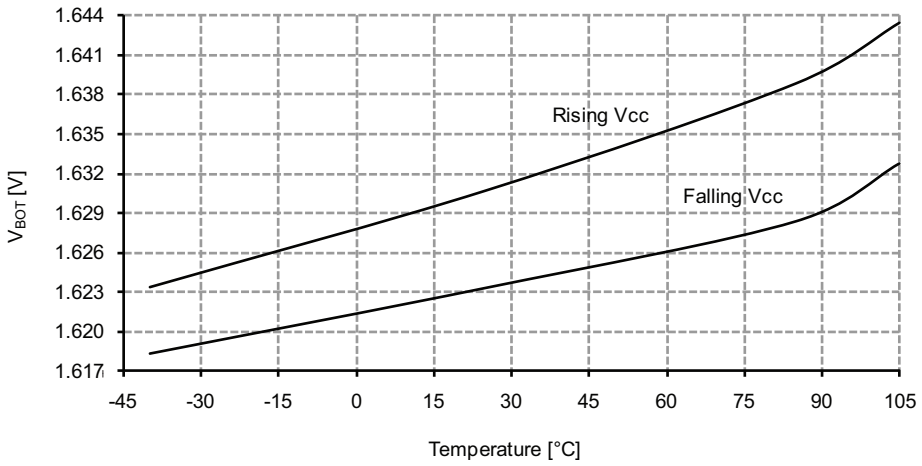
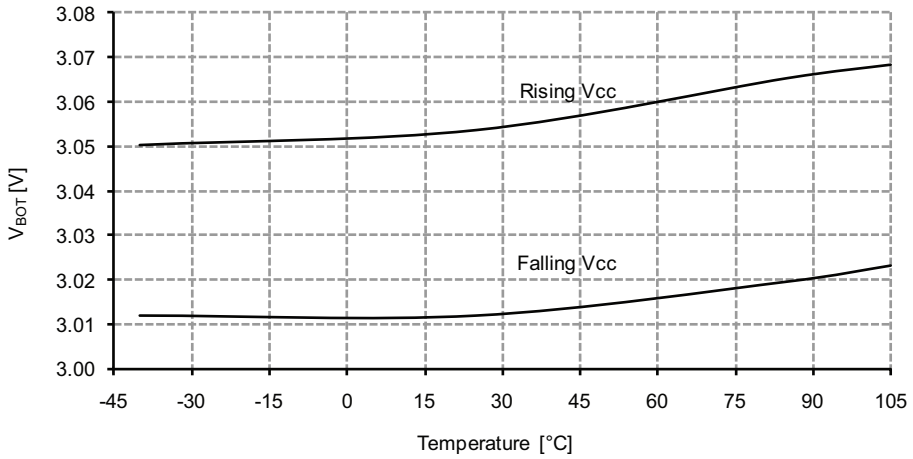


**Figure 37-229. BOD thresholds vs. temperature.**

***BOD level = 3.0V.***




## 37.3.8 External Reset Characteristics

**Figure 37-230. Minimum Reset pin pulse width vs. $V_{CC}$.**

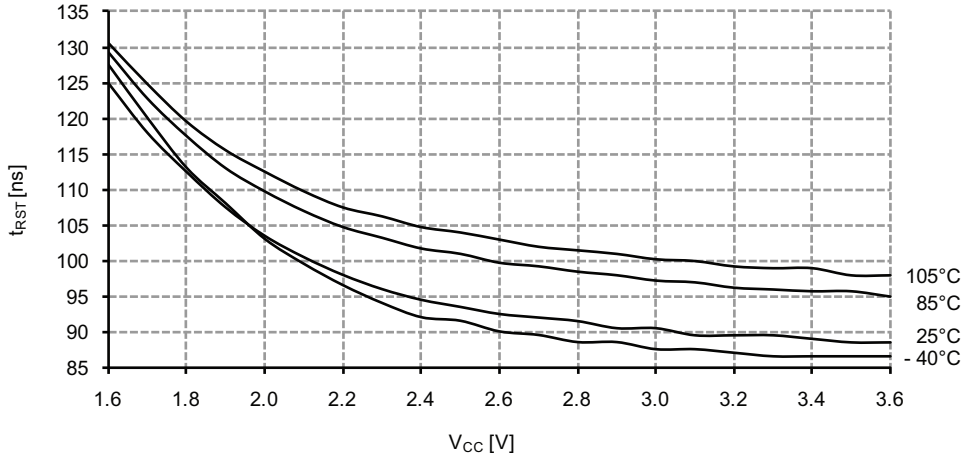


**Figure 37-231. Reset pin pull-up resistor current vs. reset pin voltage.**

***$V_{CC}$ = 1.8V.***

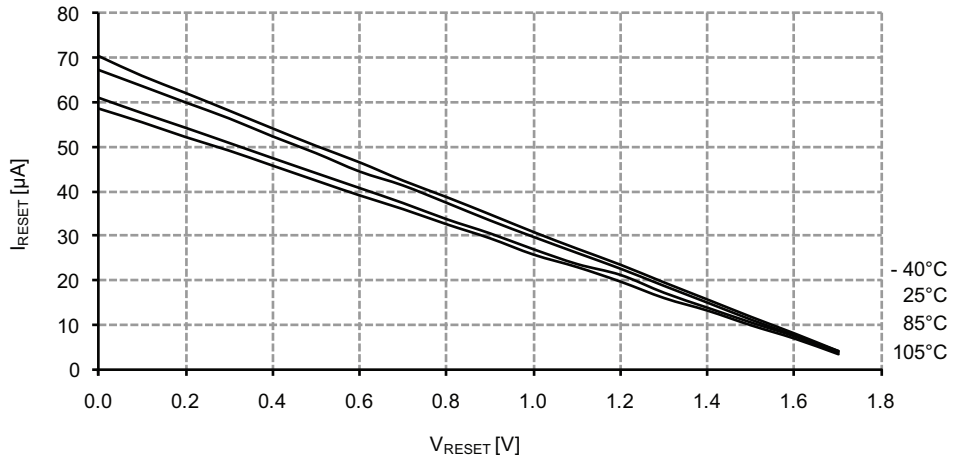



**Figure 37-232. Reset pin pull-up resistor current vs. reset pin voltage.**

***$V_{CC}$ = 3.0V.***

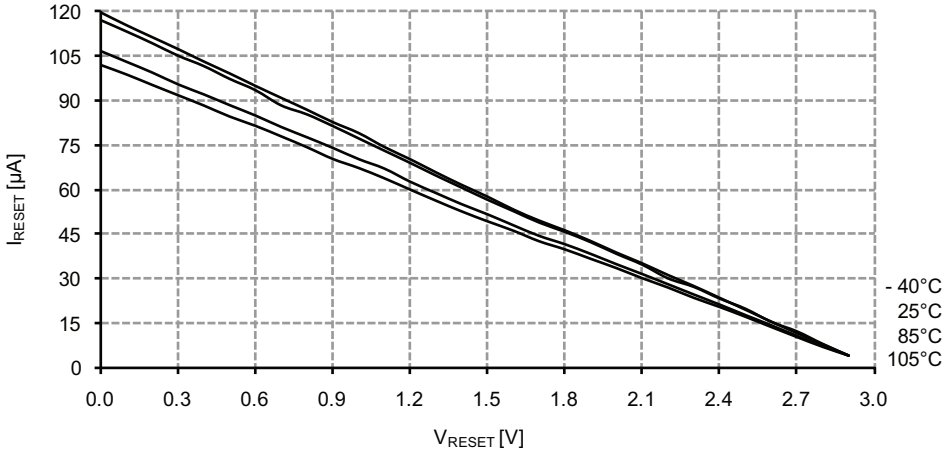


**Figure 37-233. Reset pin pull-up resistor current vs. reset pin voltage.**

***$V_{CC}$ = 3.3V.***

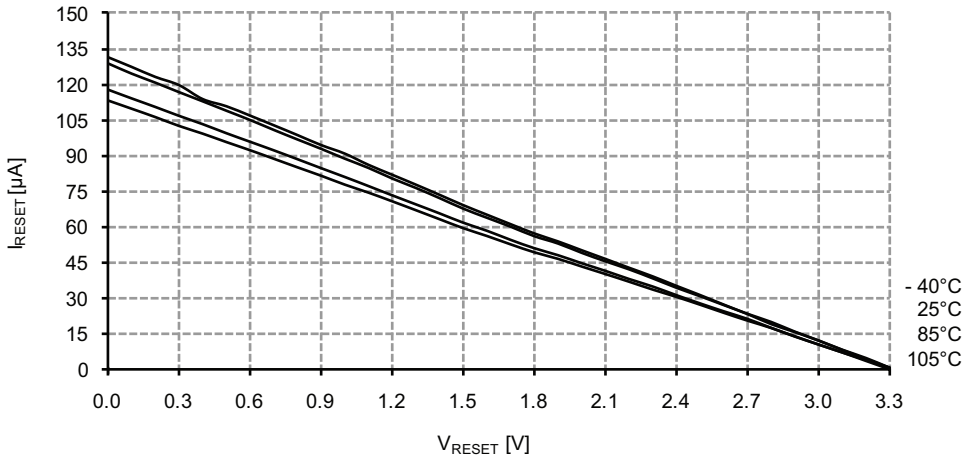



**Figure 37-234. Reset pin input threshold voltage vs. $V_{CC}$.**

***$V_{IH}$ - Reset pin read as "1".***

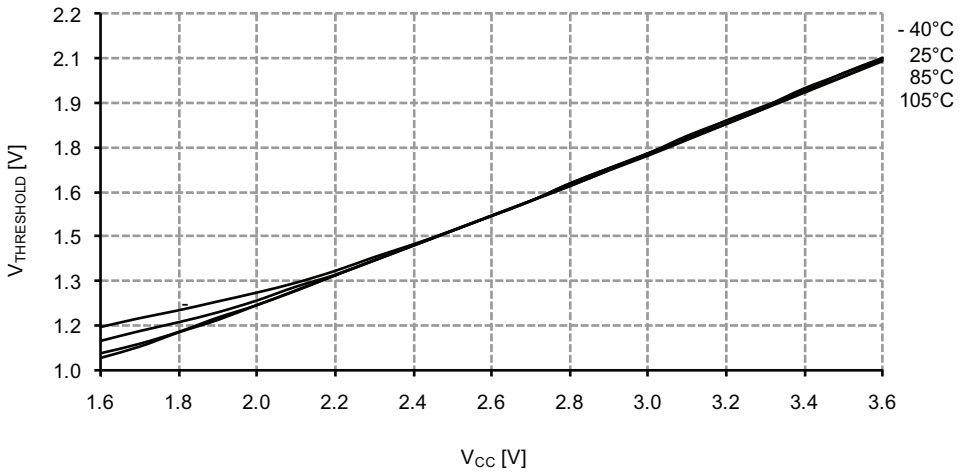
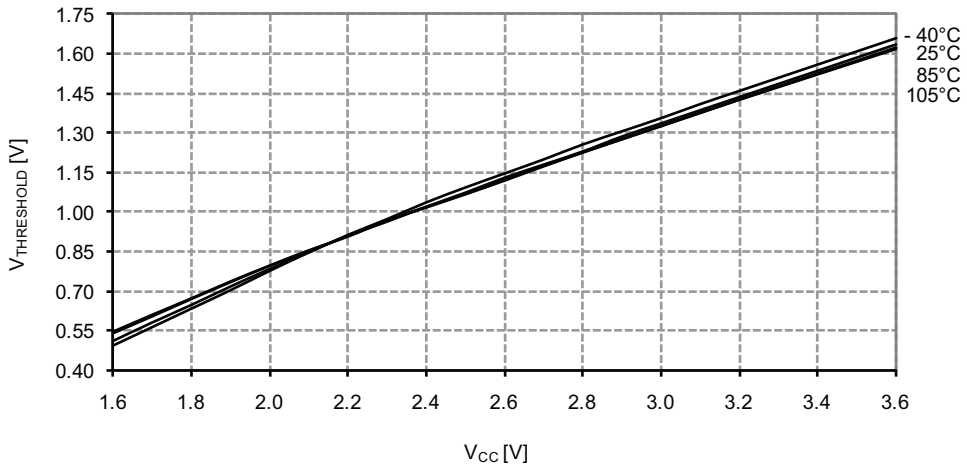


**Figure 37-235. Reset pin input threshold voltage vs. $V_{CC}$.**

***$V_{IL}$ - Reset pin read as "0".***




## 37.3.9 Power-on Reset Characteristics

**Figure 37-236. Power-on reset current consumption vs. $V_{CC}$.**

***BOD level = 3.0V, enabled in continuous mode.***

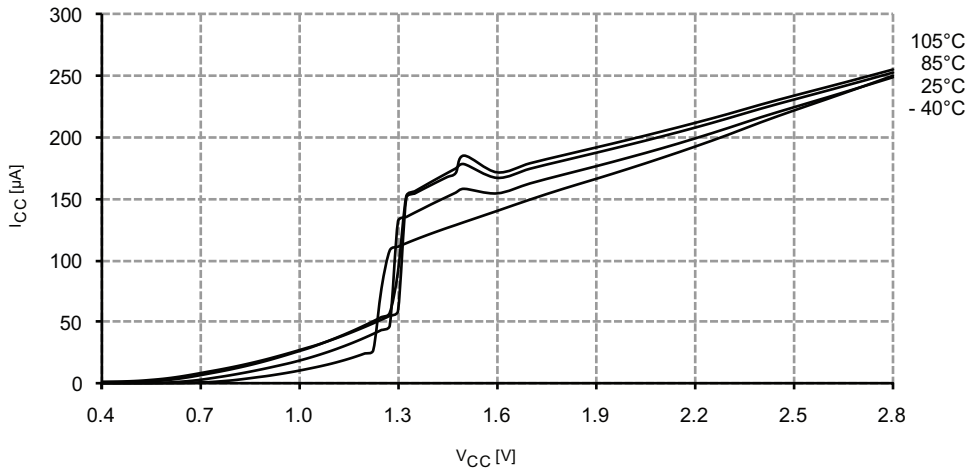
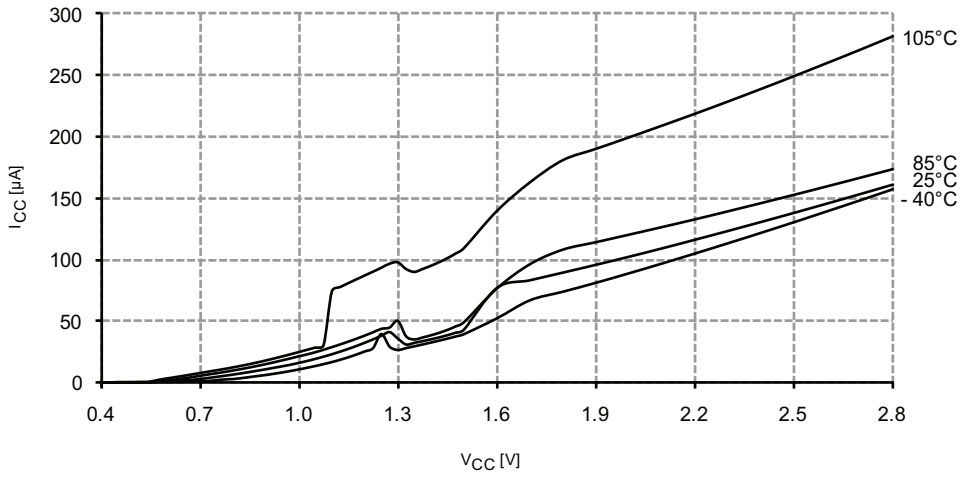


**Figure 37-237. Power-on reset current consumption vs. $V_{CC}$.**

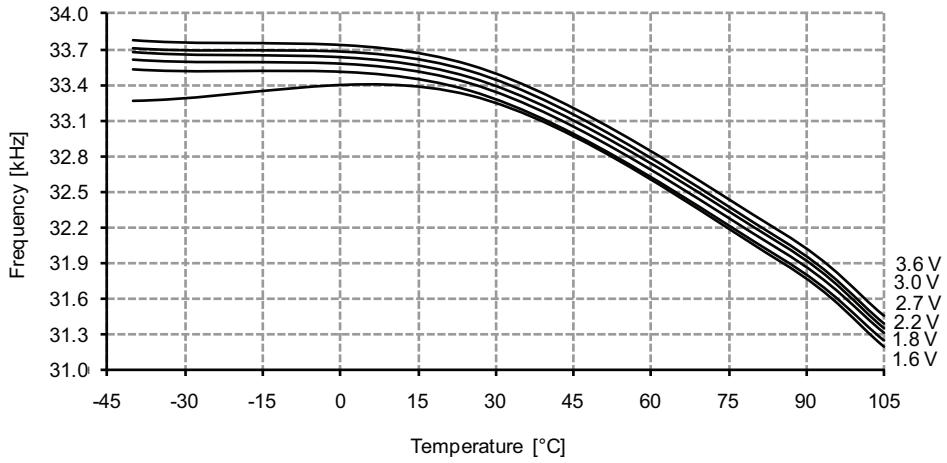
***BOD level = 3.0V, enabled in sampled mode.***




## 37.3.10 Oscillator Characteristics

### 37.3.10.1 Ultra Low-Power internal oscillator

**Figure 37-238. Ultra Low-Power internal oscillator frequency vs. temperature.**



### 37.3.10.2 32.768kHz Internal Oscillator

**Figure 37-239. 32.768kHz internal oscillator frequency vs. temperature.**

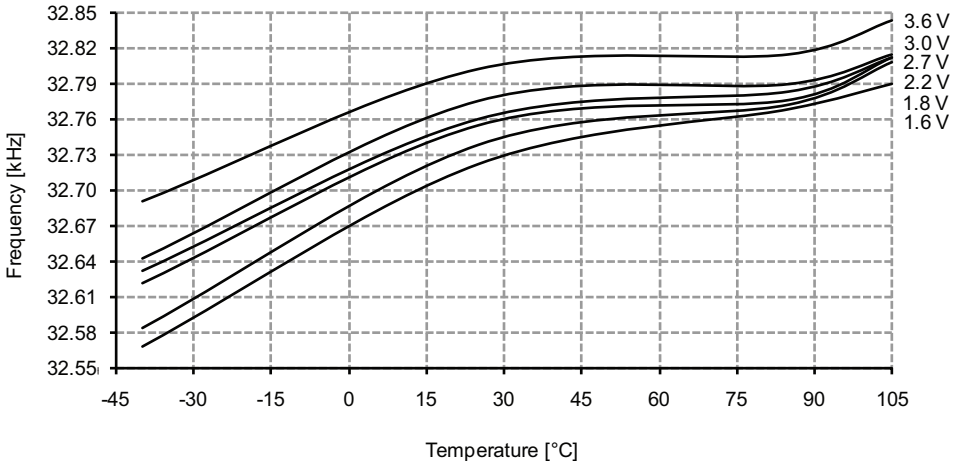
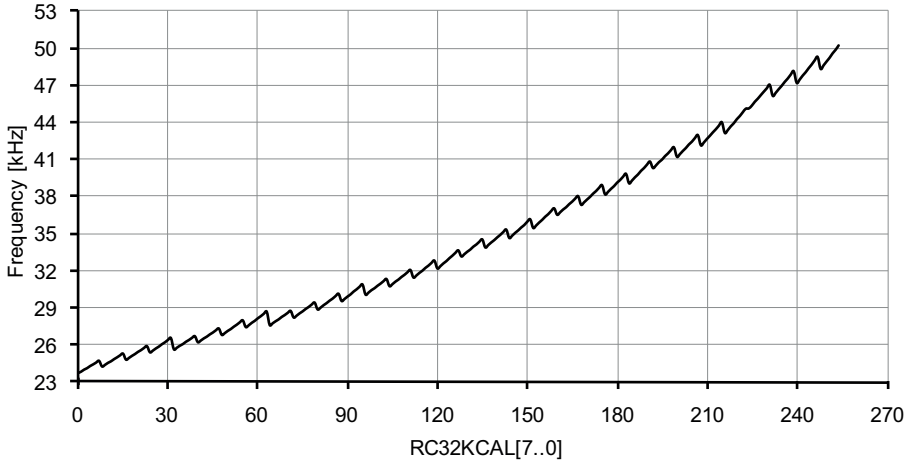



**Figure 37-240. 32.768kHz internal oscillator frequency vs. calibration value.**
***$V_{CC}$ = 3.0V, T = 25°C.***



### 37.3.10.3 2MHz Internal Oscillator

**Figure 37-241. 2MHz internal oscillator frequency vs. temperature.**
***DFLL disabled.***

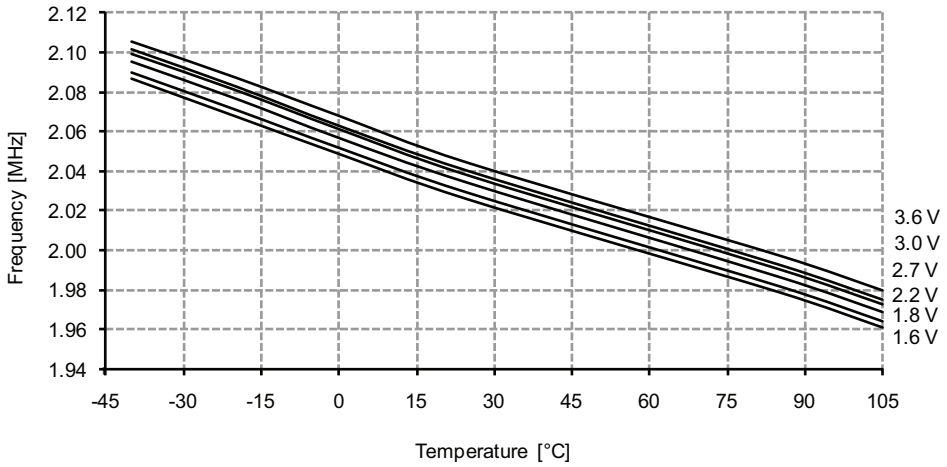



**Figure 37-242. 2MHz internal oscillator frequency vs. temperature.**
***DFLL enabled, from the 32.768kHz internal oscillator .***

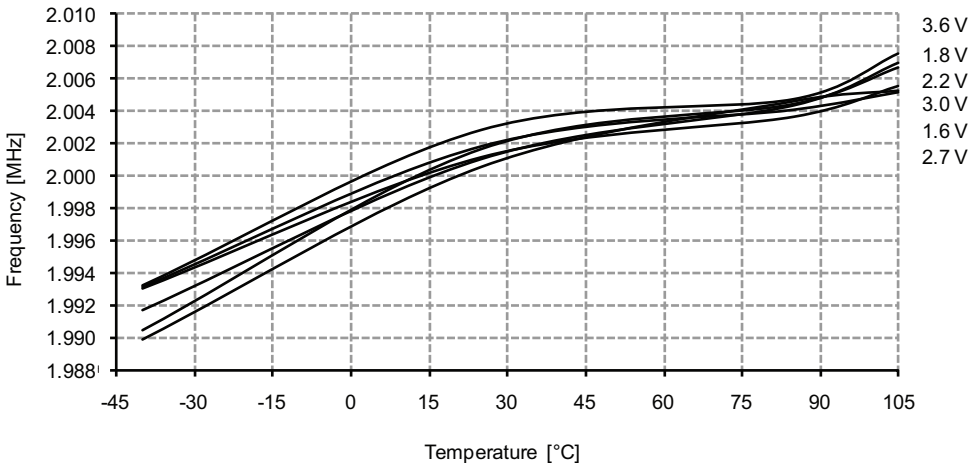
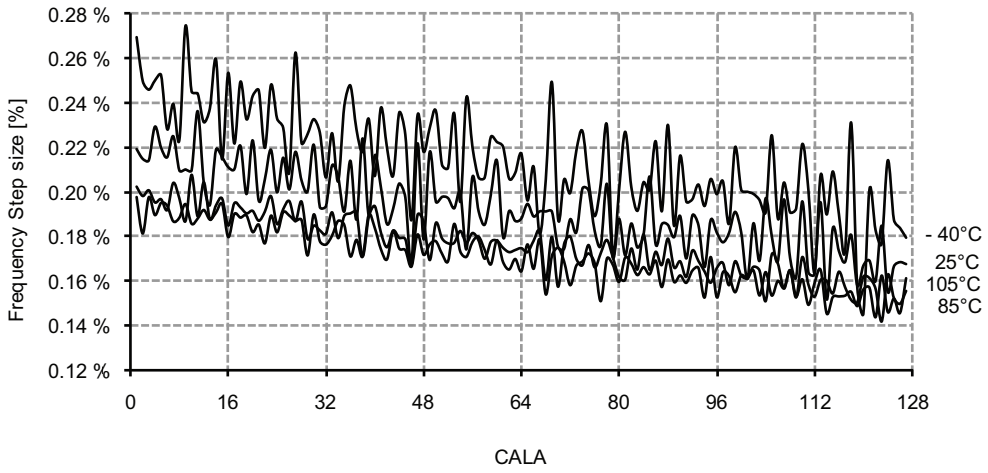


**Figure 37-243. 2MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3V.***




### 37.3.10.4 32MHz Internal Oscillator

**Figure 37-244. 32MHz internal oscillator frequency vs. temperature.**

***DFLL disabled.***

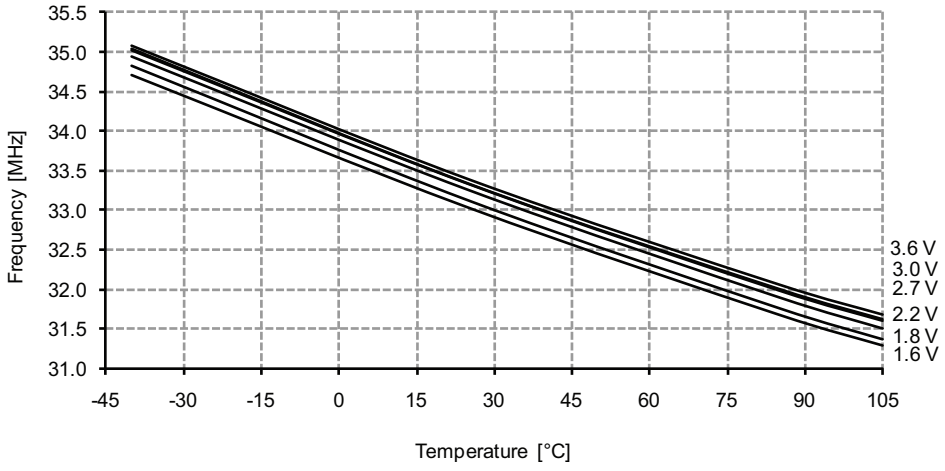


**Figure 37-245. 32MHz internal oscillator frequency vs. temperature.**

***DFLL enabled, from the 32.768kHz internal oscillator.***

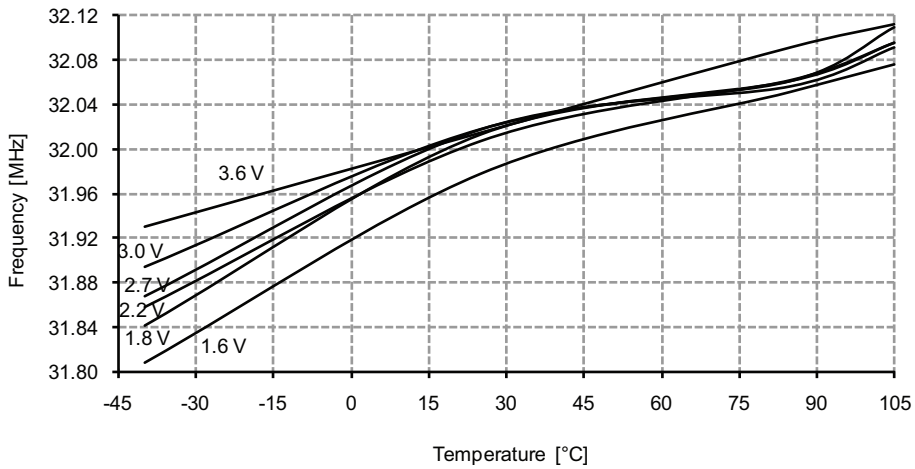



**Figure 37-246. 32MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3.0V.***

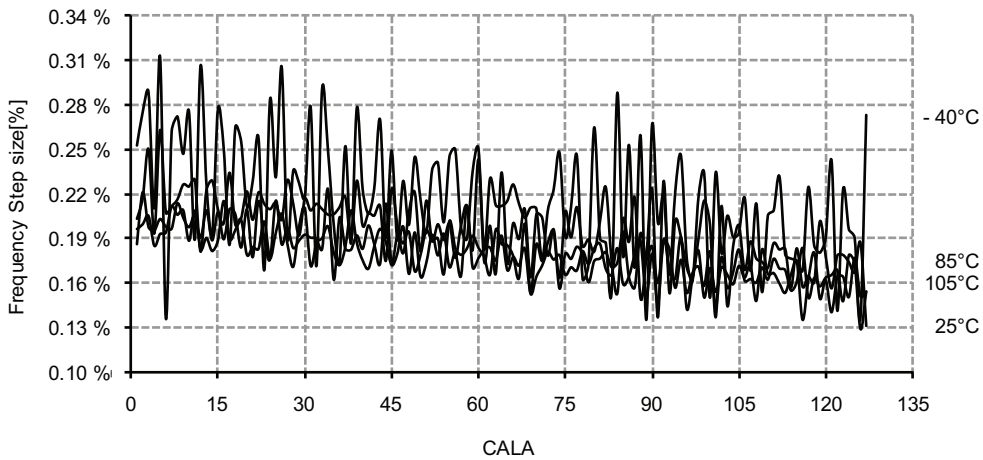
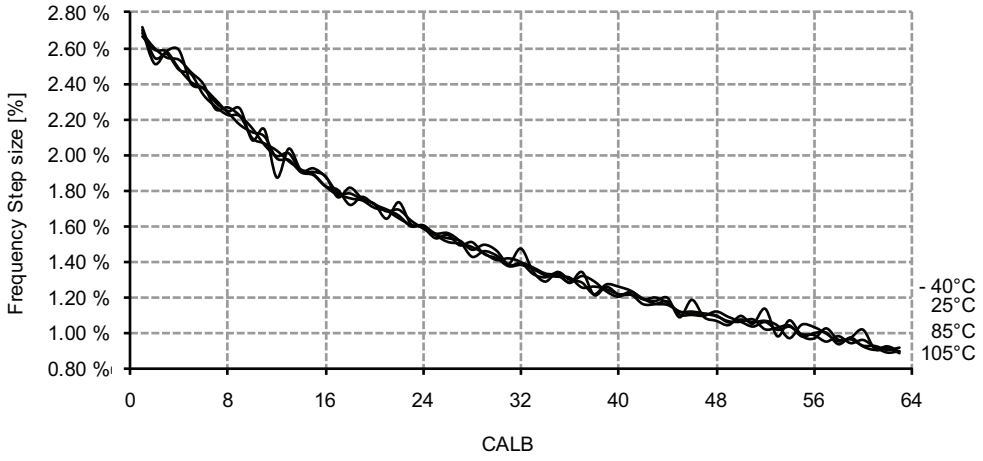


**Figure 37-247. 32MHz internal oscillator CALB calibration step size.**

***$V_{CC}$ = 3.0V***




### 37.3.10.5 32MHz internal oscillator calibrated to 48MHz

**Figure 37-248. 48MHz internal oscillator frequency vs. temperature.**

***DFLL disabled.***

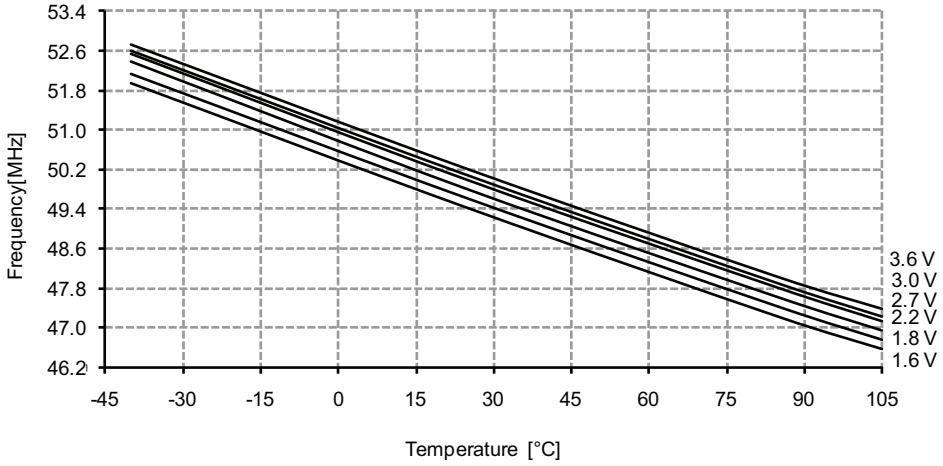


**Figure 37-249. 48MHz internal oscillator frequency vs. temperature.**

***DFLL enabled, from the 32.768kHz internal oscillator.***

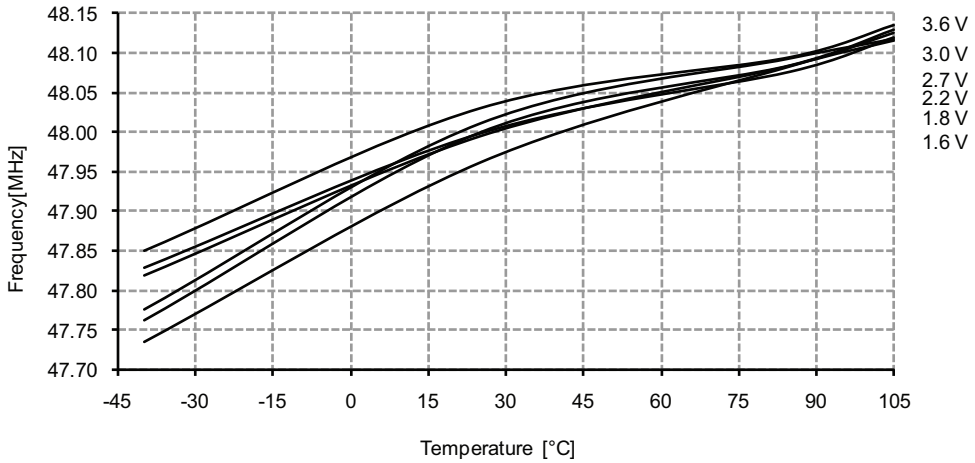
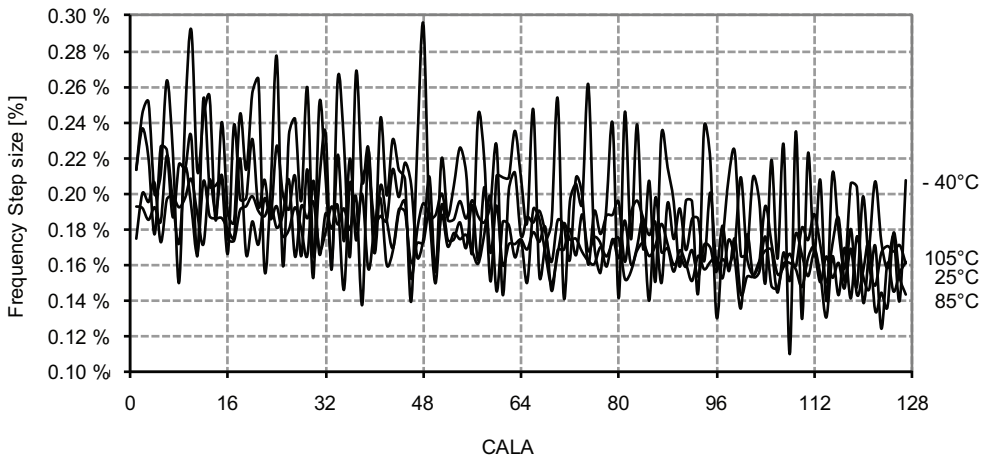


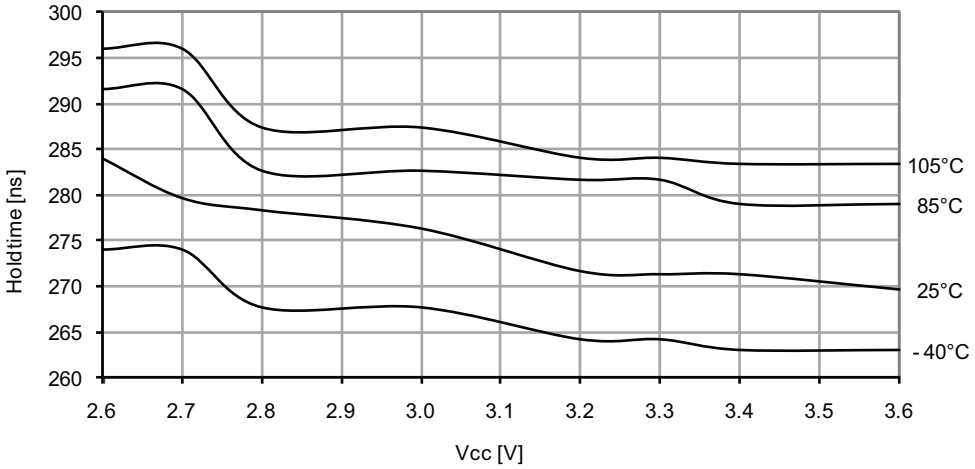

**Figure 37-250. 48MHz internal oscillator CALA calibration step size.**

***$V_{CC}$ = 3.0V***



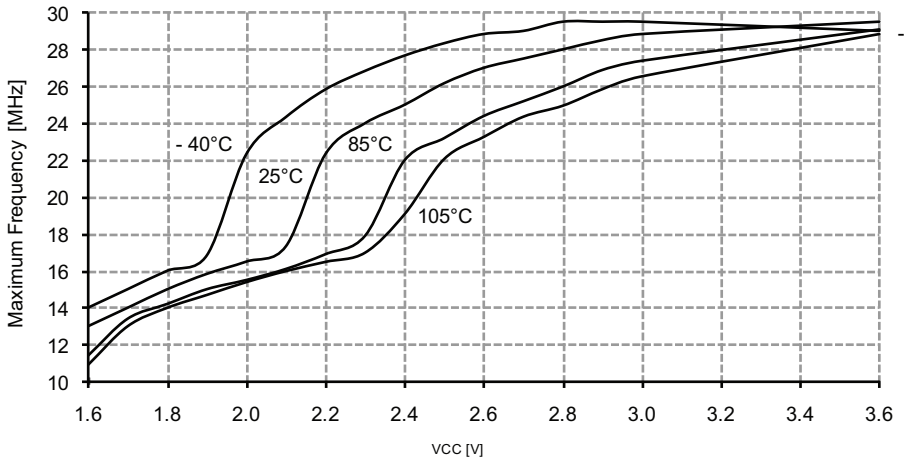
### 37.3.11 Two-Wire Interface characteristics

**Figure 37-251. SDA hold time vs. supply voltage.**




### 37.3.12 PDI characteristics

**Figure 37-252. Maximum PDI frequency vs. $V_{CC}$.**



## 37.4 ATxmega128A4U

### 37.4.1 Current consumption

#### 37.4.1.1 Active mode supply current

**Figure 37-253. Active supply current vs. frequency.**

***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

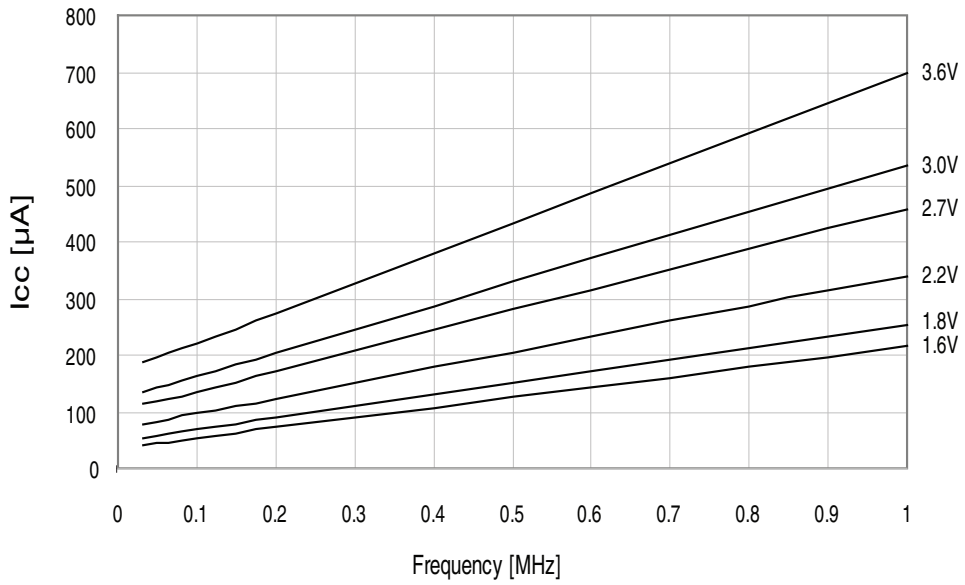



**Figure 37-254. Active supply current vs. frequency.**

***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C.***

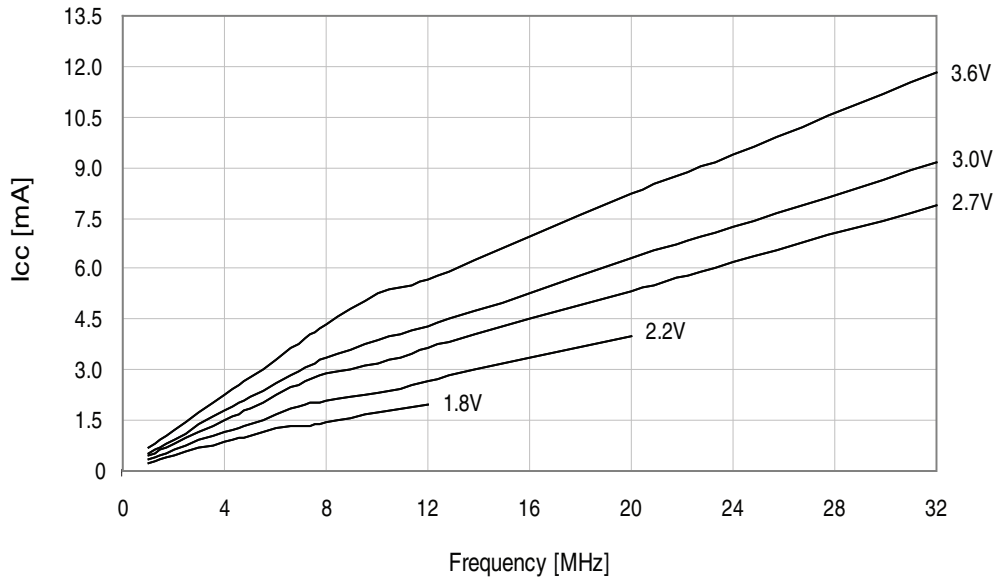


**Figure 37-255. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32.768kHz internal oscillator***

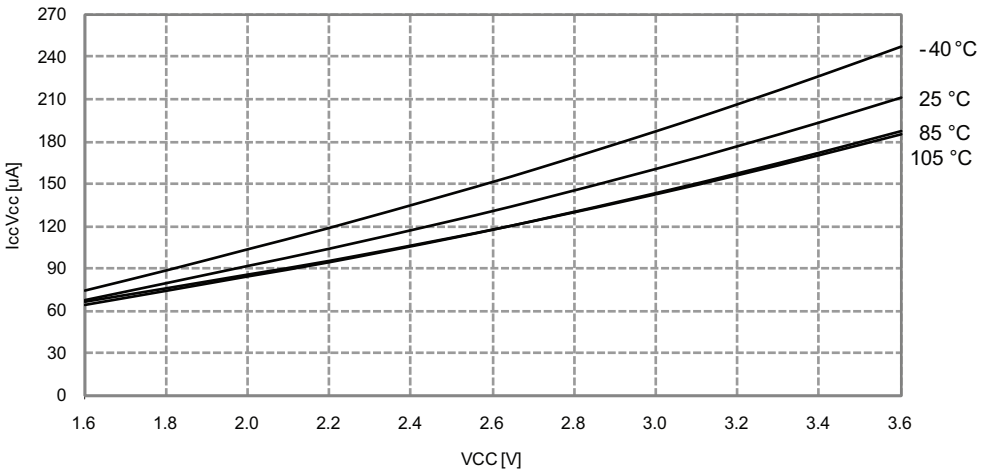



**Figure 37-256. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock.***

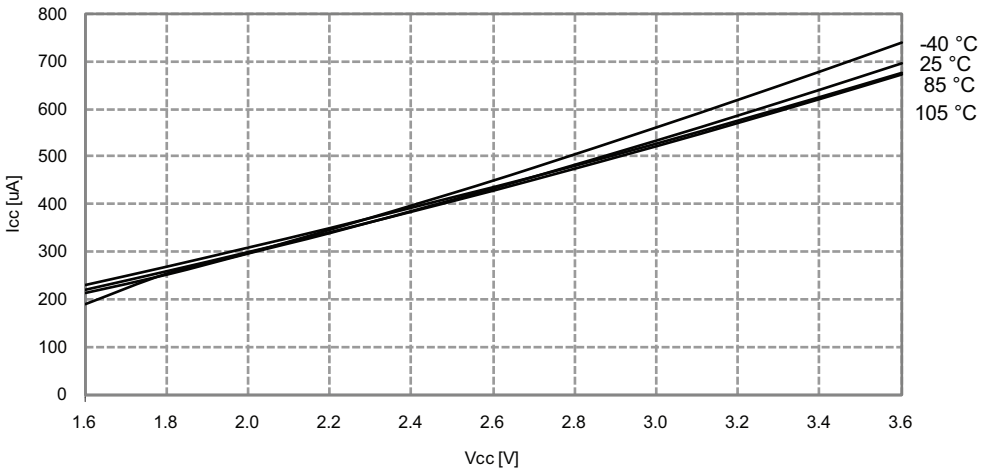


**Figure 37-257. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator***

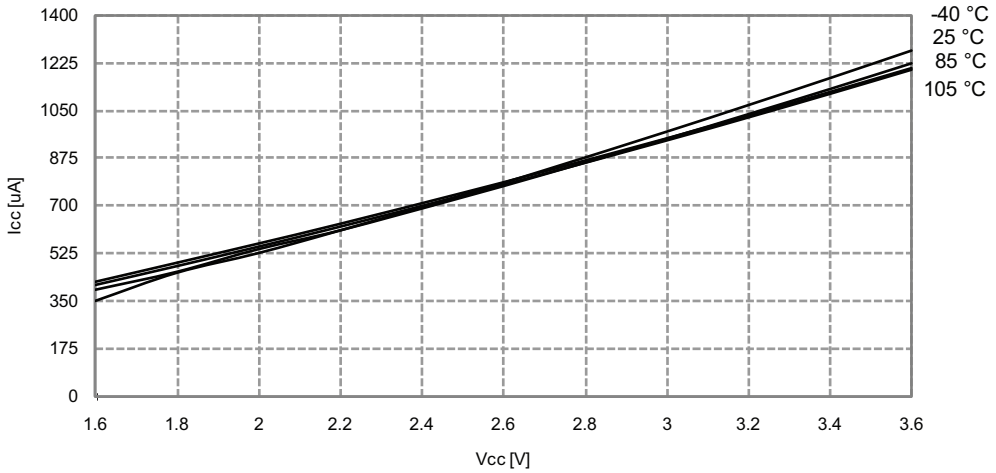



**Figure 37-258. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz.***

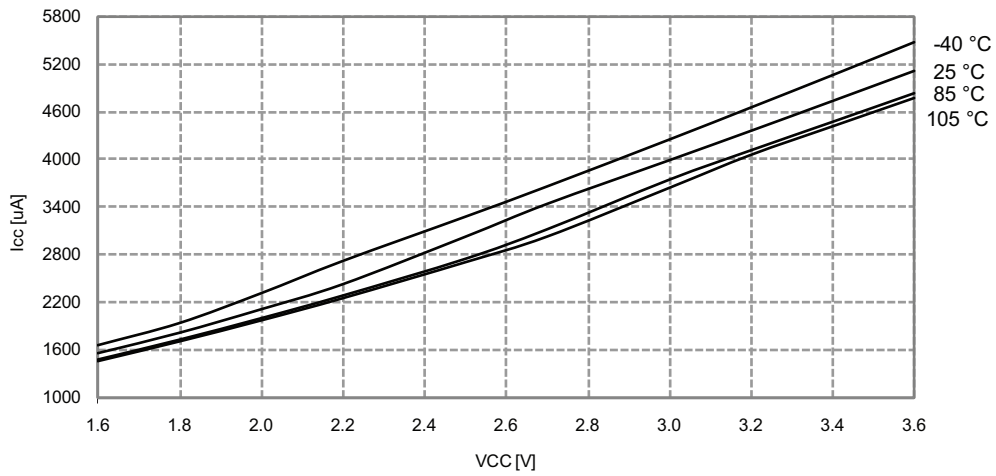
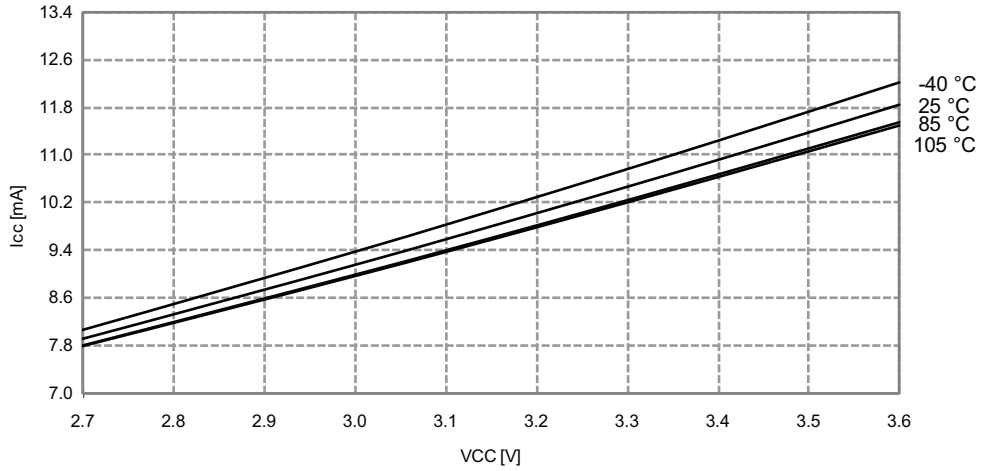


**Figure 37-259. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator.***




### 37.4.1.2 Idle mode supply current

**Figure 37-260. Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C***

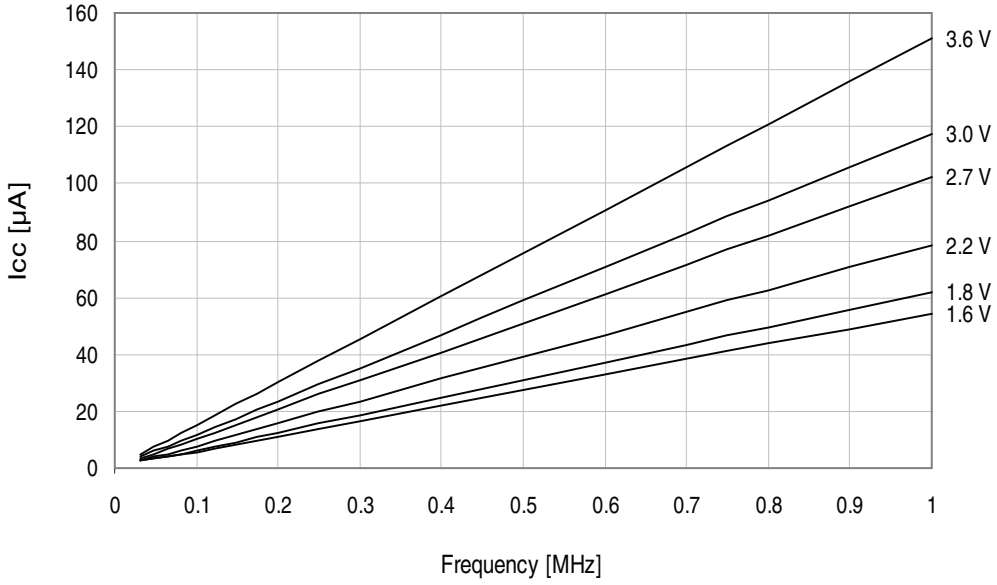


**Figure 37-261. Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 1 - 32MHz external clock, T = 25°C***

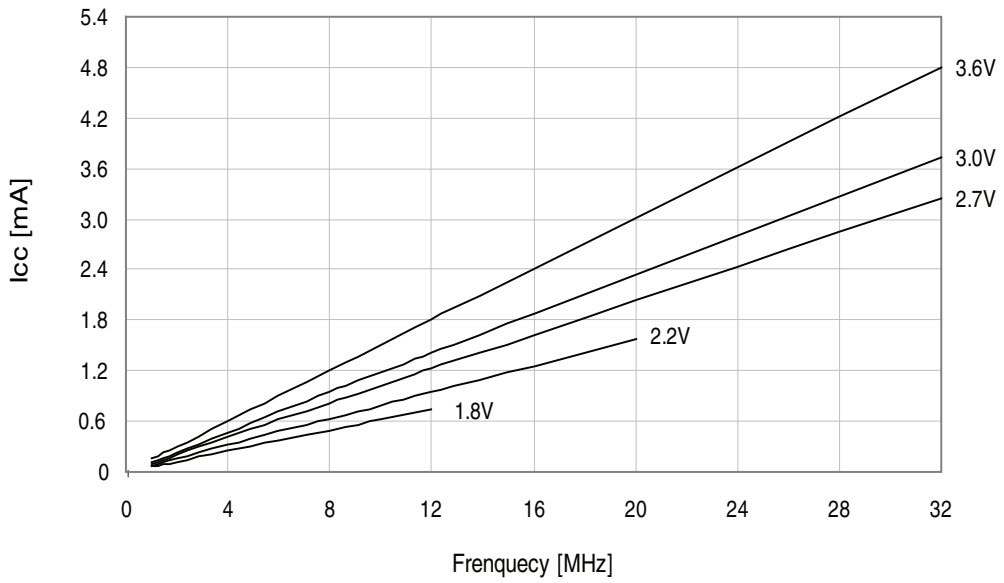



**Figure 37-262. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32.768kHz internal oscillator.***

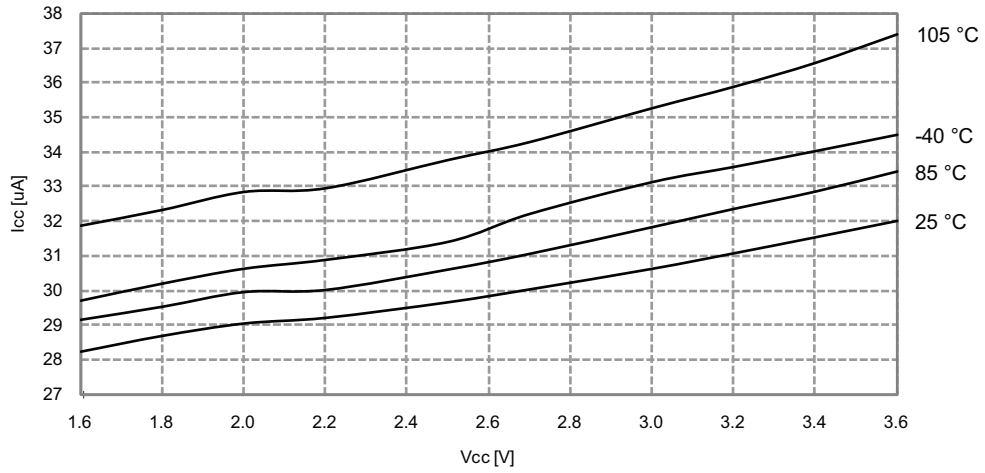


**Figure 37-263. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock***

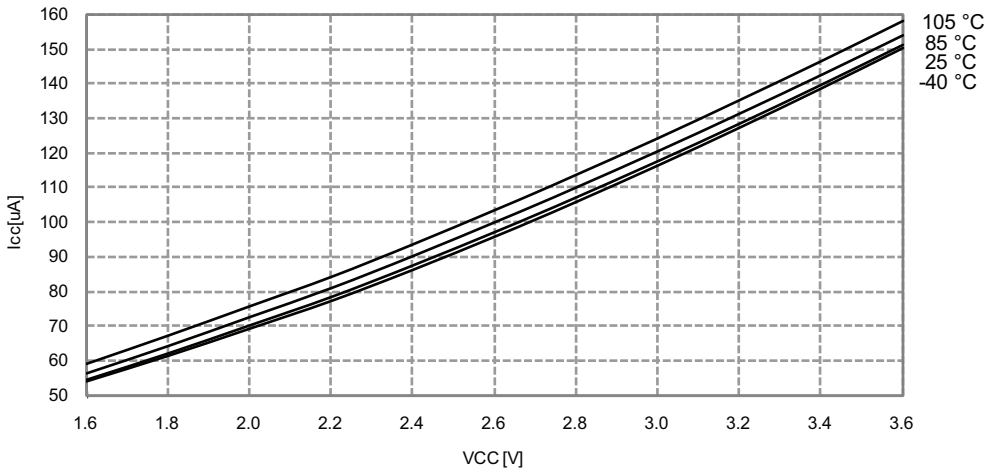



**Figure 37-264. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator***

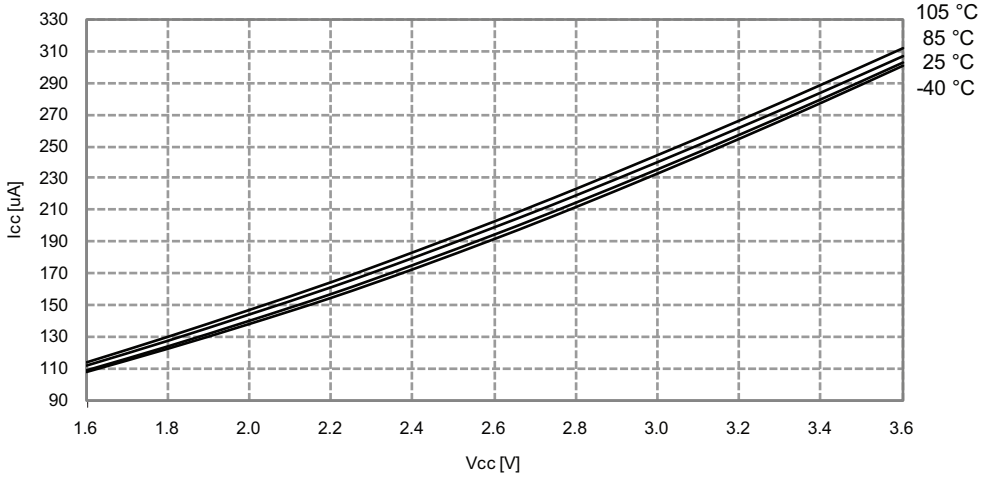


**Figure 37-265. Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator prescaled to 8MHz***

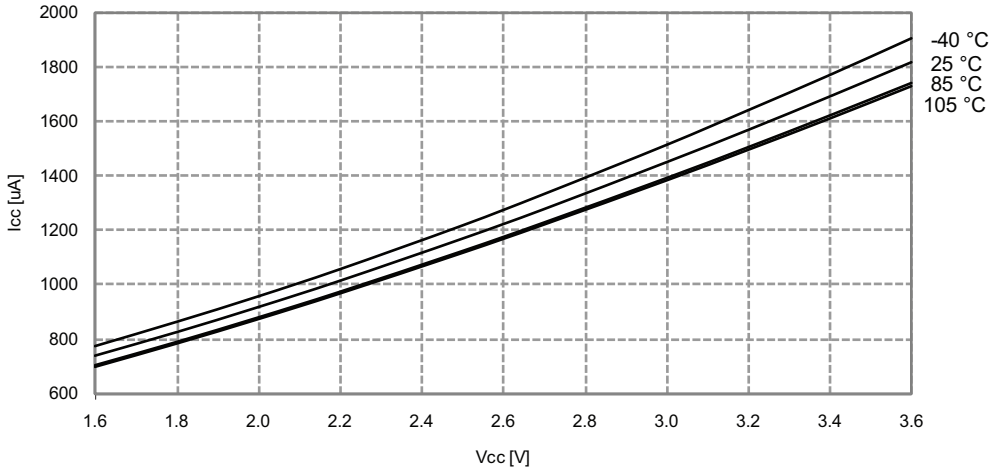
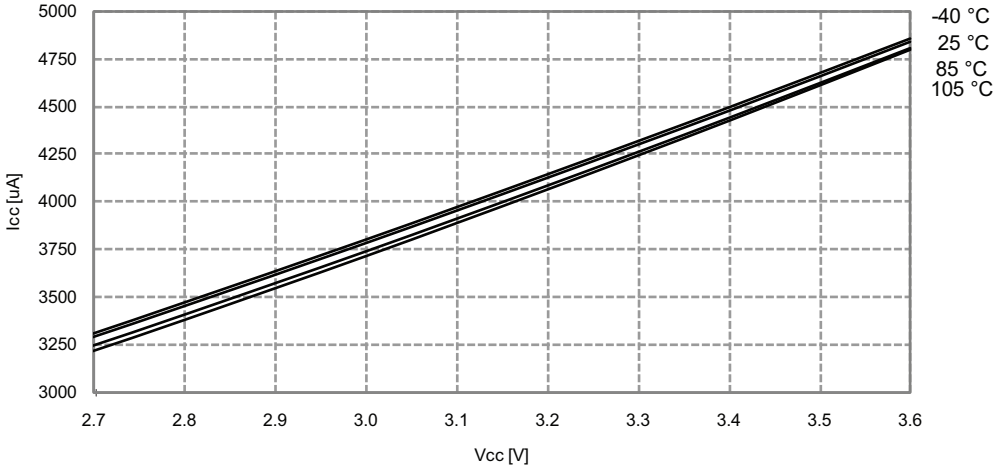



**Figure 37-266. Idle mode current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator***



### 37.4.1.3 Power-down mode supply current

**Figure 37-267. Power-down mode supply current vs. temperature.**

***All functions disabled***

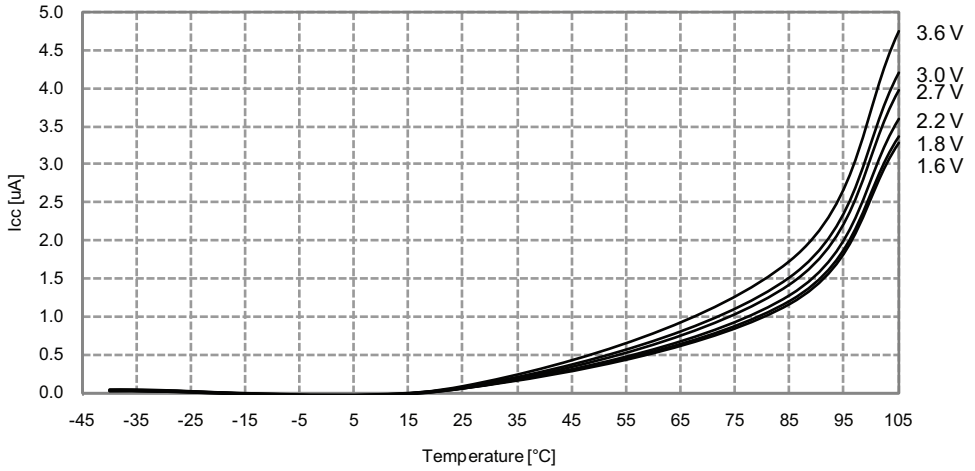



**Figure 37-268. Power-down mode supply current vs. $V_{CC}$.**

***All functions disabled***

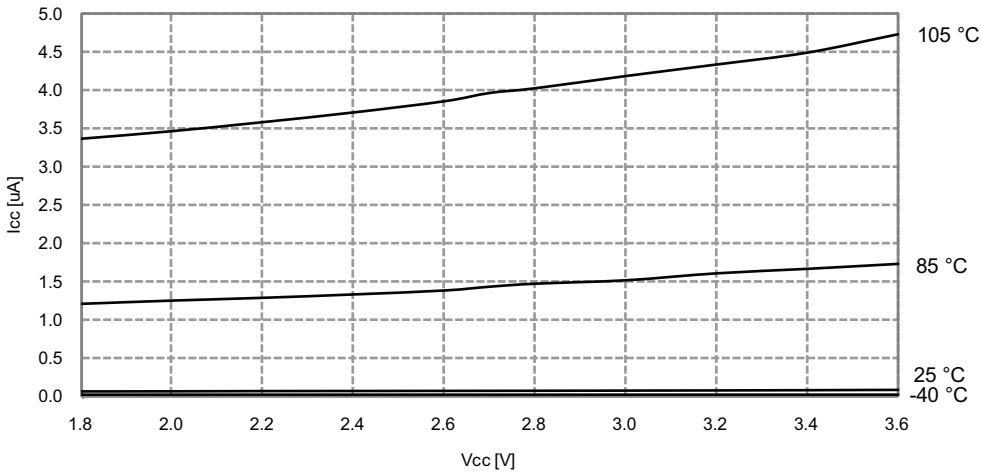
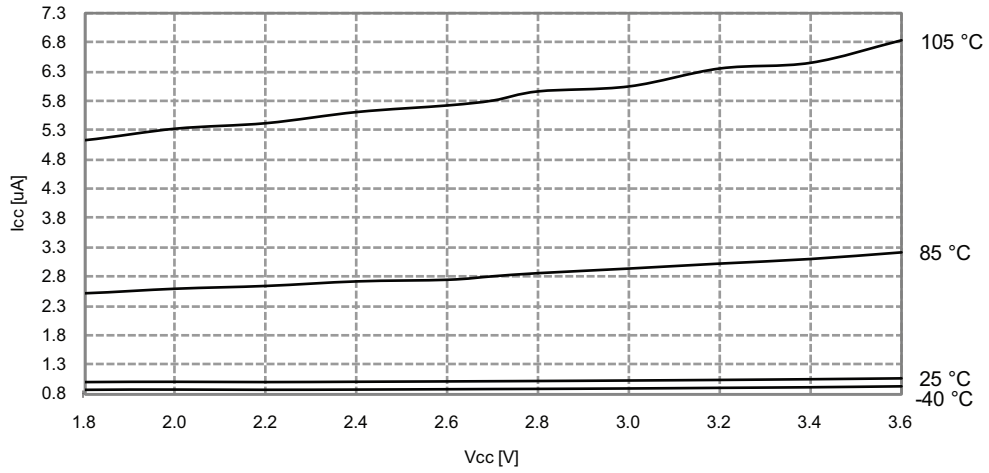


**Figure 37-269. Power-down mode supply current vs. $V_{CC}$.**

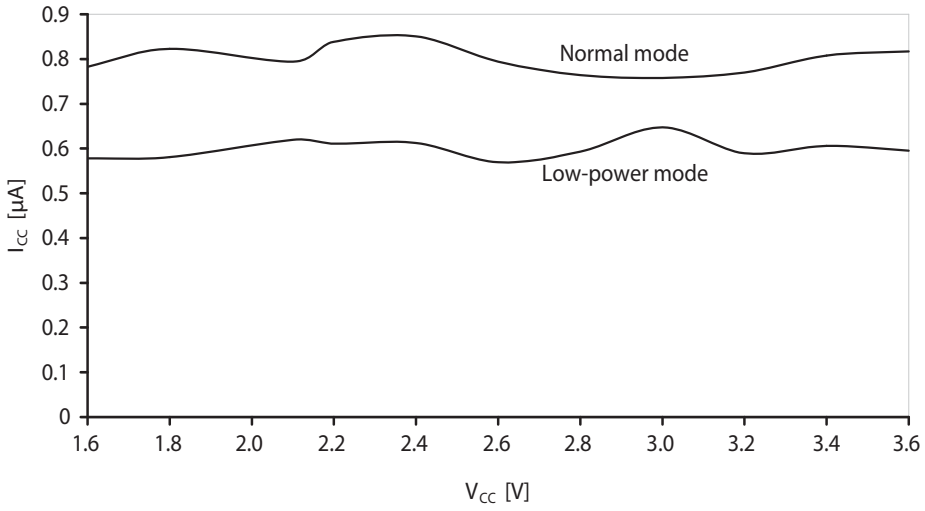
***Watchdog and sampled BOD enabled***




### 37.4.1.4 Power-save mode supply current

**Figure 37-270. Power-save mode supply current vs.$V_{CC}$.**

***Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.***



### 37.4.1.5 Standby mode supply current

**Figure 37-271. Standby supply current vs. $V_{CC}$.**

***Standby, $f_{SYS}$ = 1MHz***

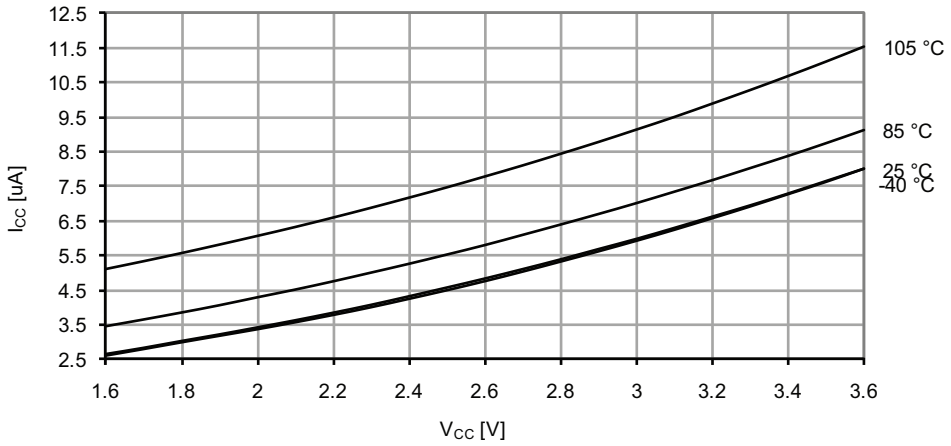
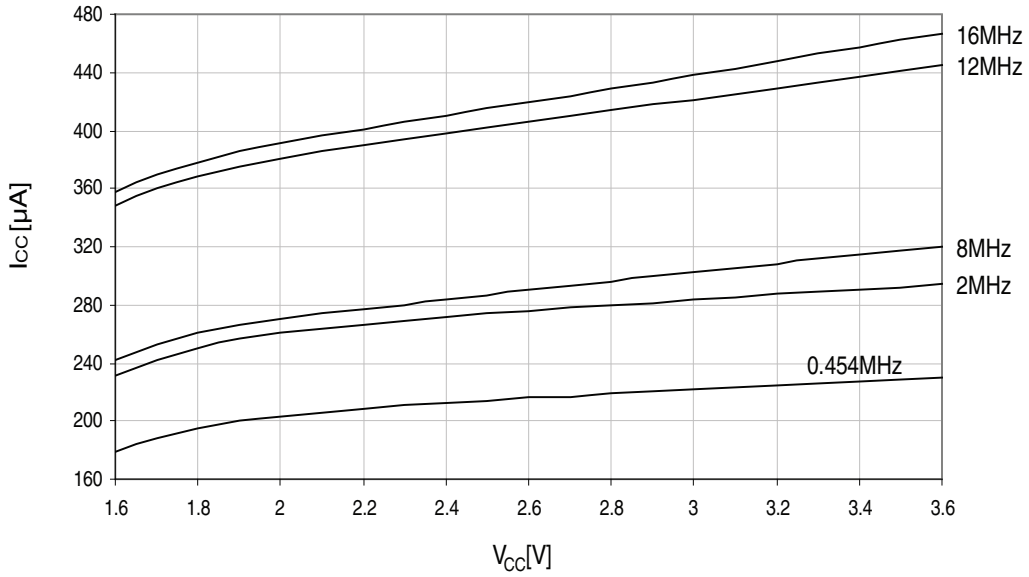



**Figure 37-272. Standby supply current vs. $V_{CC}$.**

***T = 25°C, running from different crystal oscillators***



### 37.4.2 I/O Pin Characteristics

#### 37.4.2.1 Pull-up

**Figure 37-273. I/O pin pull-up resistor current vs. input voltage.**
***$V_{CC}$ = 1.8V***

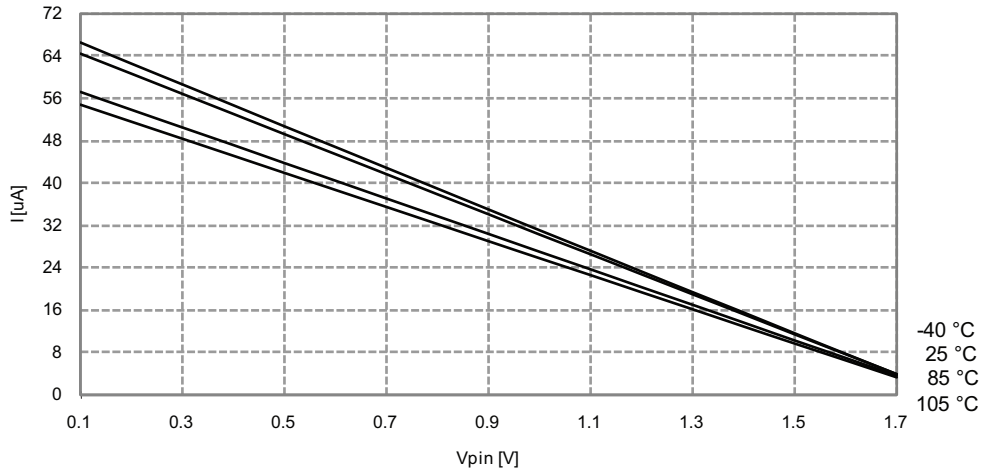



**Figure 37-274. I/O pin pull-up resistor current vs. input voltage.**
***$V_{CC}$ = 3.0V***

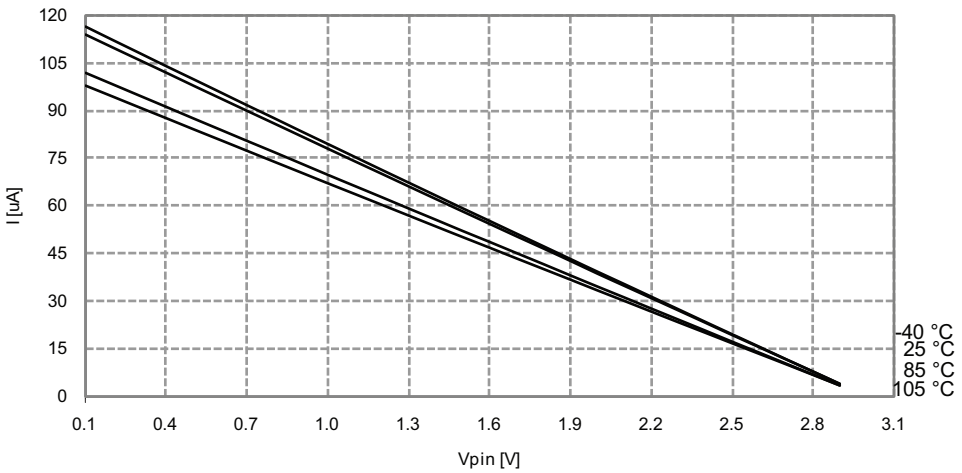
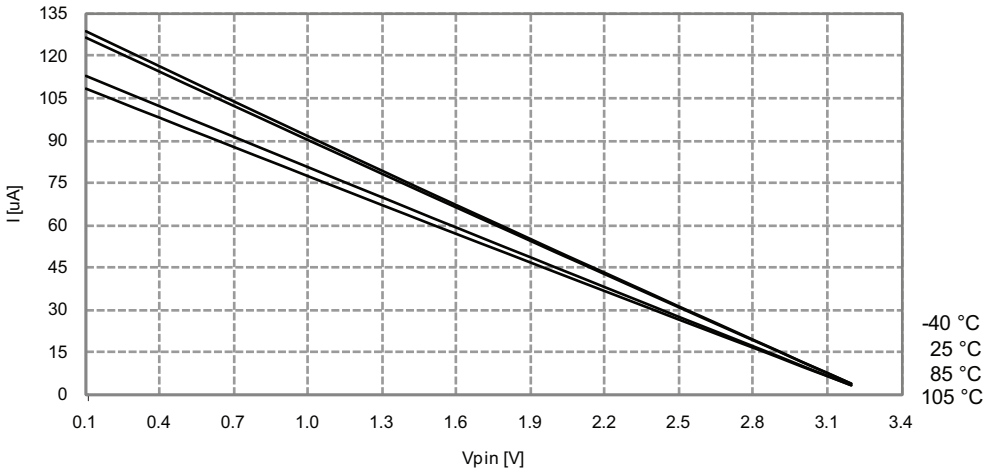


**Figure 37-275. I/O pin pull-up resistor current vs. input voltage.**

***$V_{CC}$ = 3.3V.***




### 37.4.2.2 Output Voltage vs. Sink/Source Current

**Figure 37-276. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 1.8V***

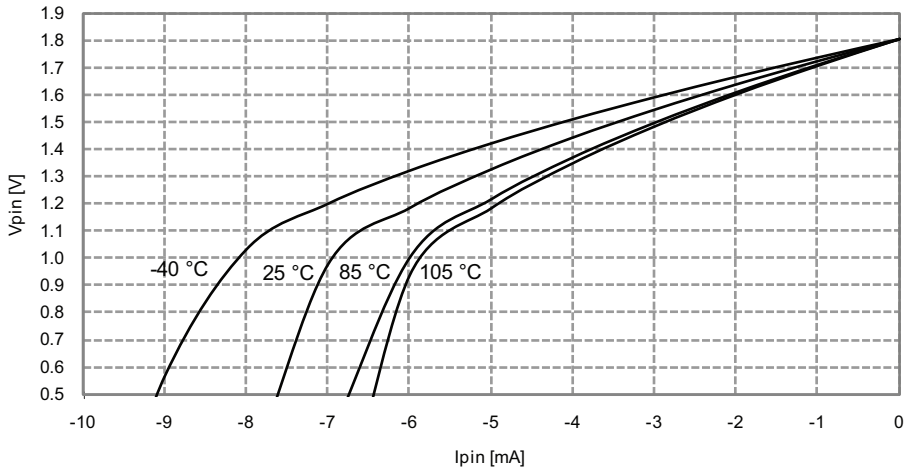


**Figure 37-277. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 3.0V***

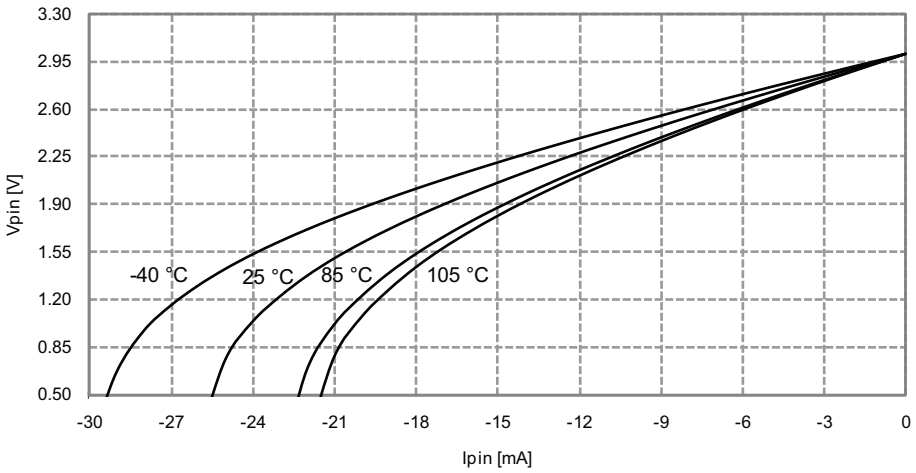



**Figure 37-278. I/O pin output voltage vs. source current.**

***$V_{CC}$ = 3.3V***

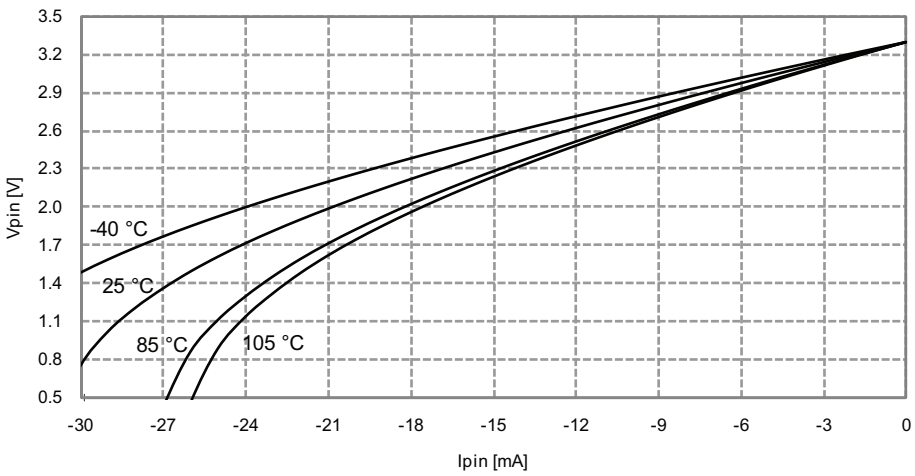


**Figure 37-279. I/O pin output voltage vs. source current**

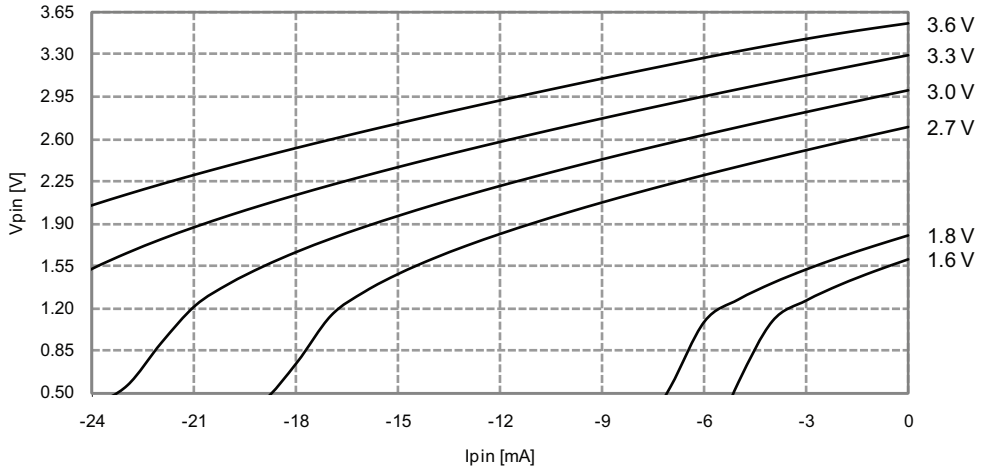



**Figure 37-280. I/O pin output voltage vs. sink current.**
***$V_{CC}$ = 1.8V***

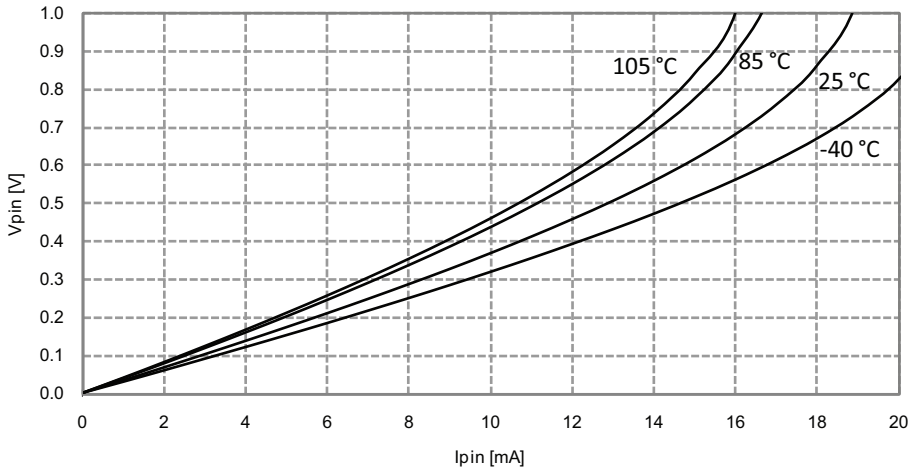


**Figure 37-281. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 3.0V***

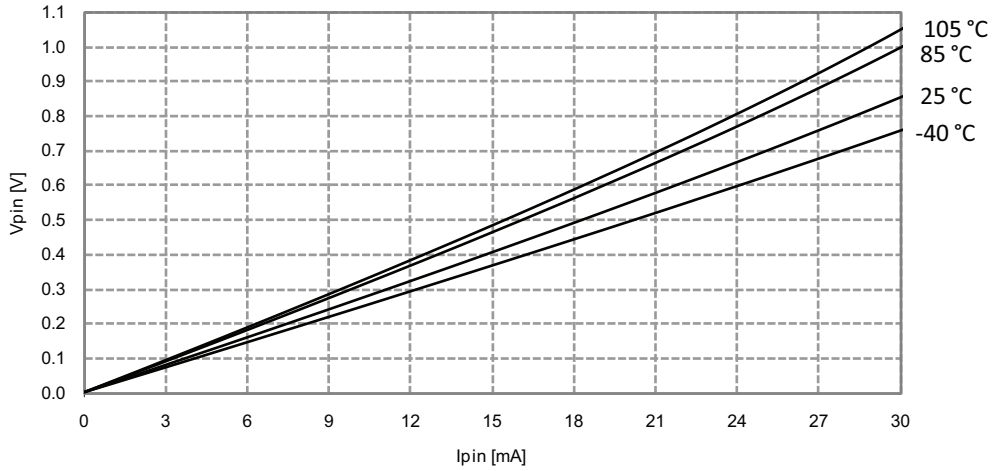



**Figure 37-282. I/O pin output voltage vs. sink current.**

***$V_{CC}$ = 3.3V***

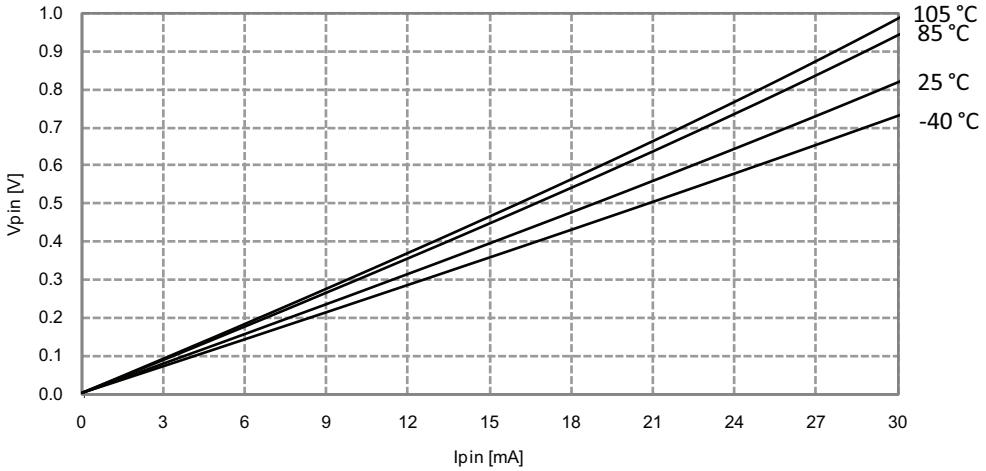
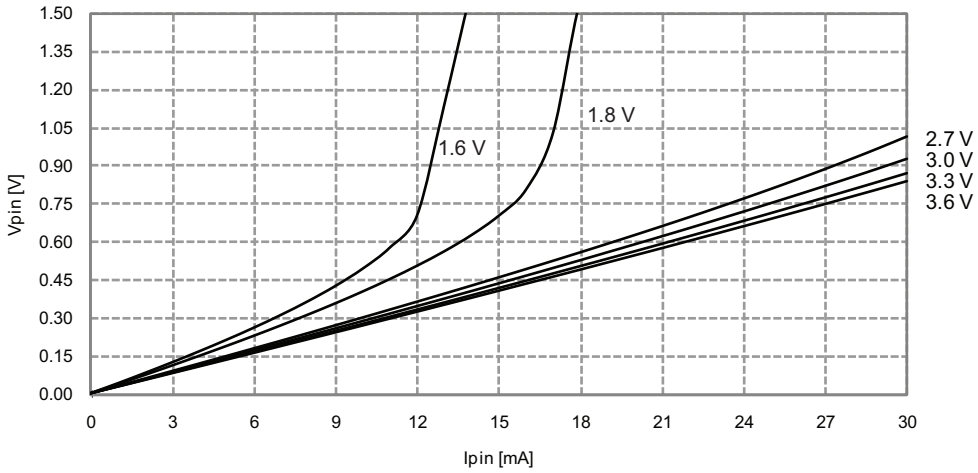


**Figure 37-283. I/O pin output voltage vs. sink current**




### 37.4.2.3 Thresholds and Hysteresis

**Figure 37-284. I/O pin input threshold voltage vs. $V_{CC}$.**
***T = 25°C***

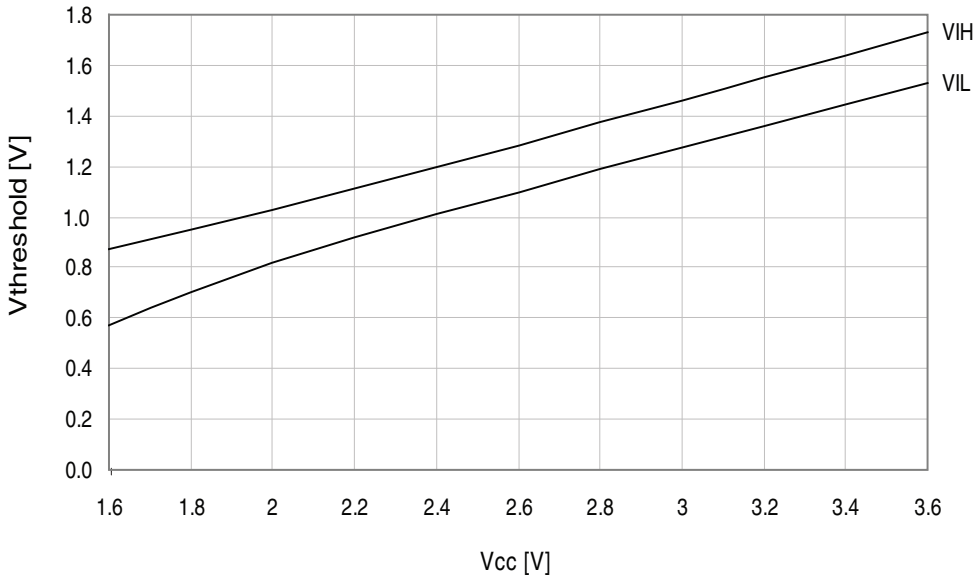


**Figure 37-285. I/O pin input threshold voltage vs. $V_{CC}$.**

***$V_{IH}$ I/O pin read as "1"***

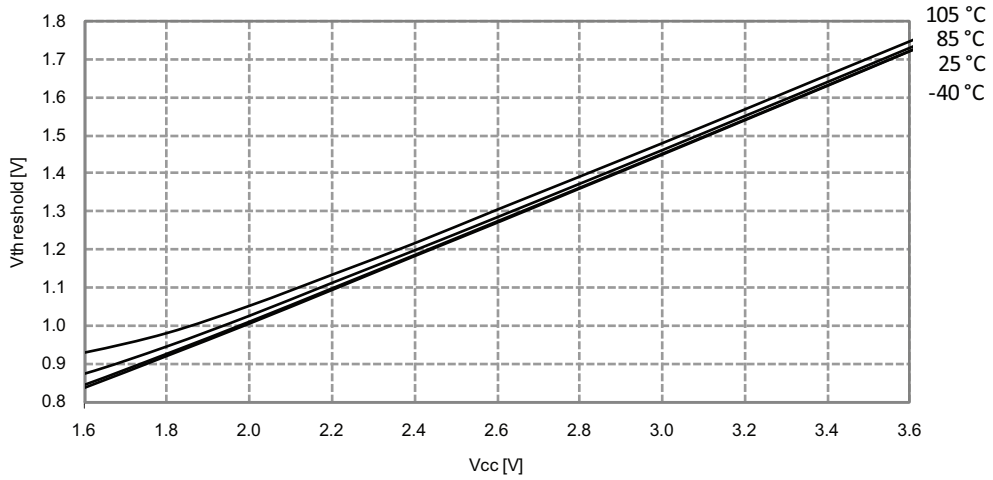



**Figure 37-286. I/O pin input threshold voltage vs. $V_{CC}$.**

***$V_{IL}$ I/O pin read as "0"***

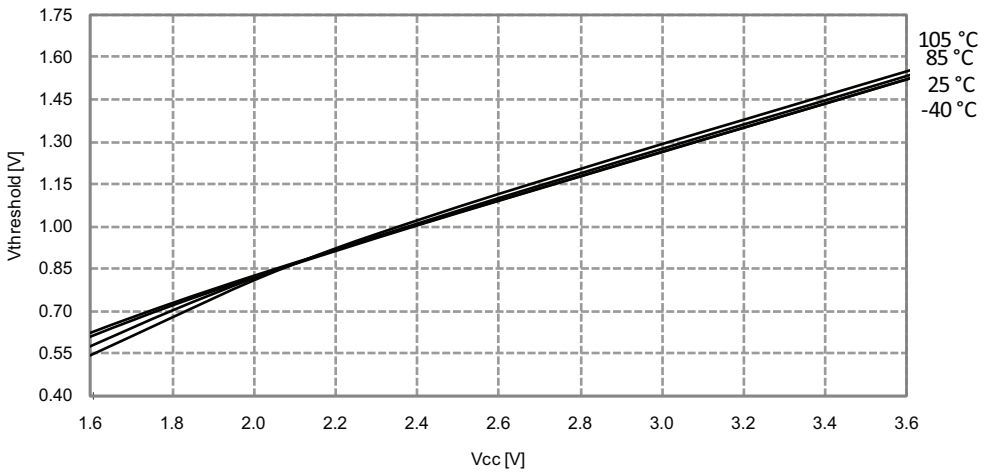
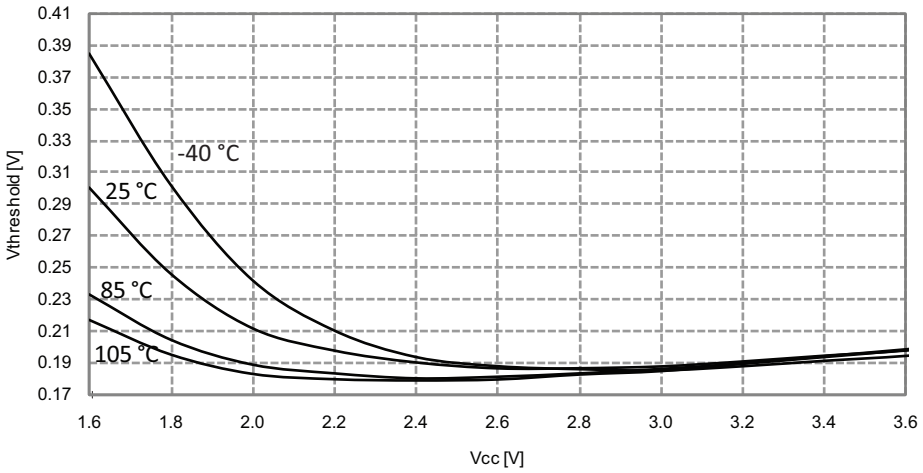


**Figure 37-287. I/O pin input hysteresis vs. $V_{CC}$**




## 37.4.3 ADC Characteristics

**Figure 37-288. INL error vs. external $V_{REF}$**

***T = 25°C, $V_{CC}$ = 3.6V, external reference***

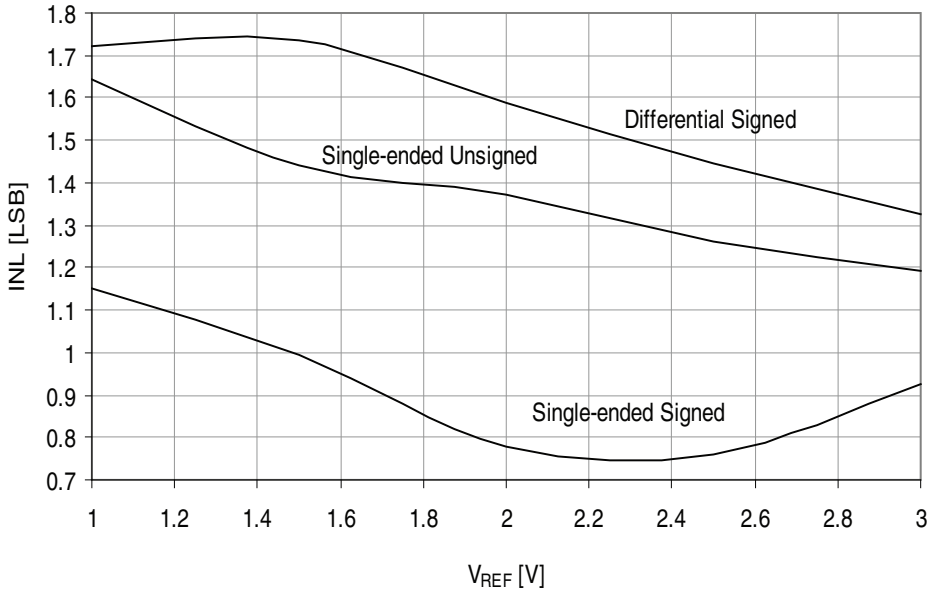


**Figure 37-289. INL error vs. sample rate**

*$T = 25°C$, $V_{CC} = 3.6V$, $V_{REF} = 3.0V$ external*

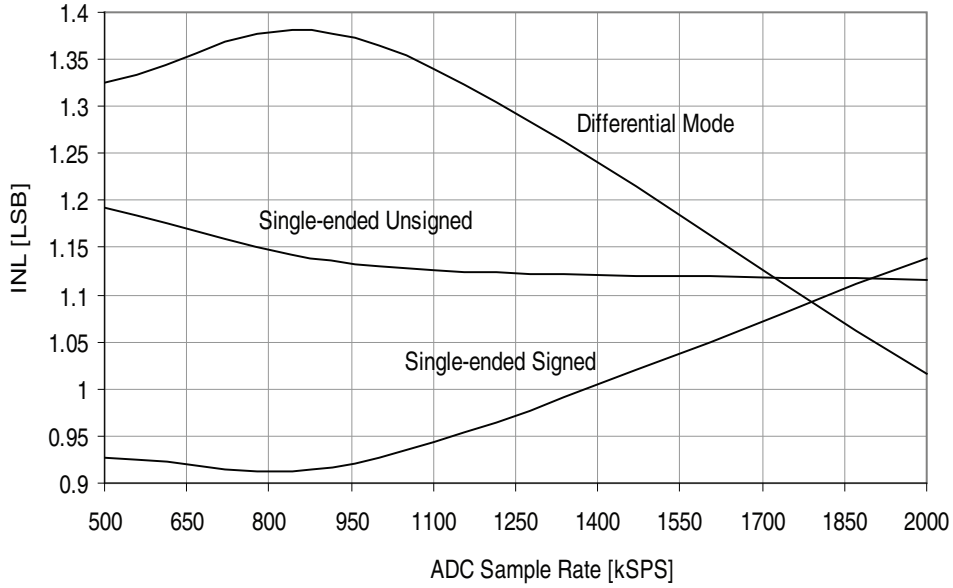



**Figure 37-290. INL error vs. input code**

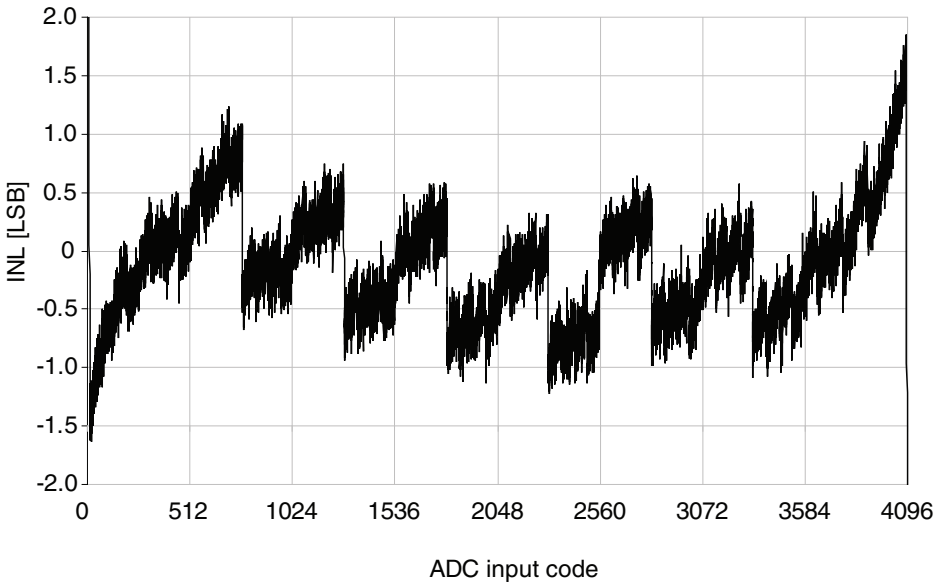


**Figure 37-291. DNL error vs. external $V_{REF}$**

***T = 25°C, $V_{CC}$ = 3.6V, external reference***

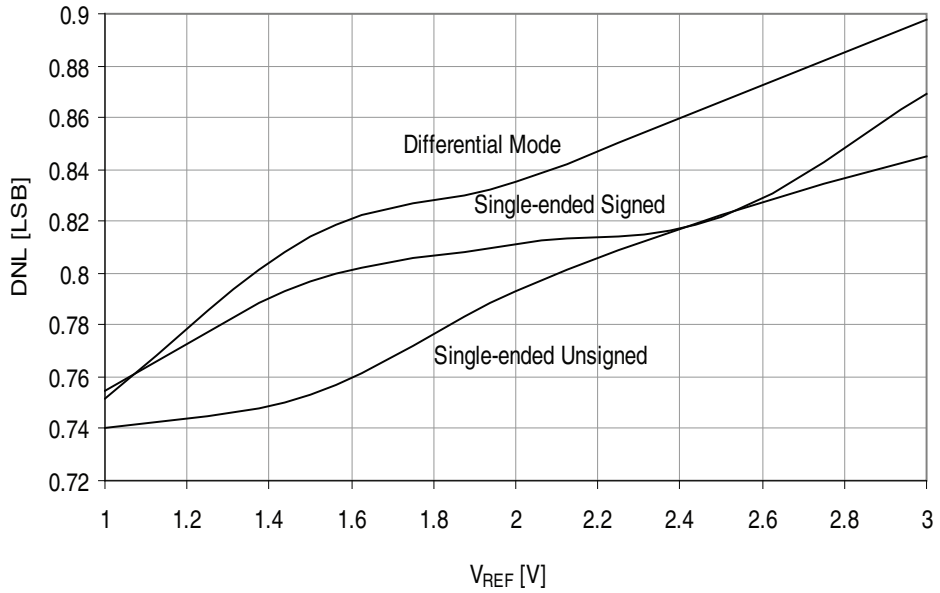



**Figure 37-292. DNL error vs. sample rate**

***T = 25°C, $V_{CC}$ = 3.6V, $V_{REF}$ = 3.0V external***

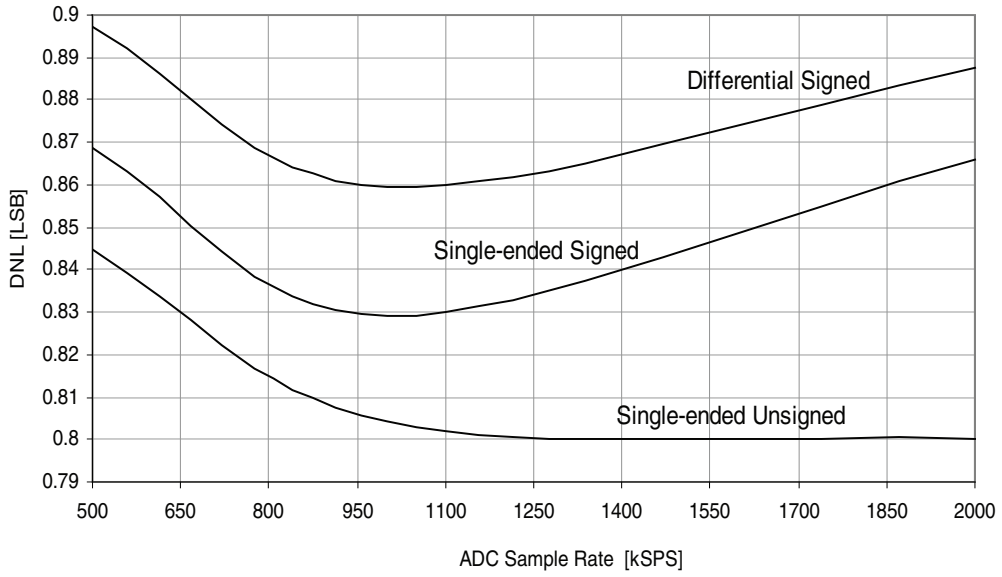


**Figure 37-293. DNL error vs. input code**

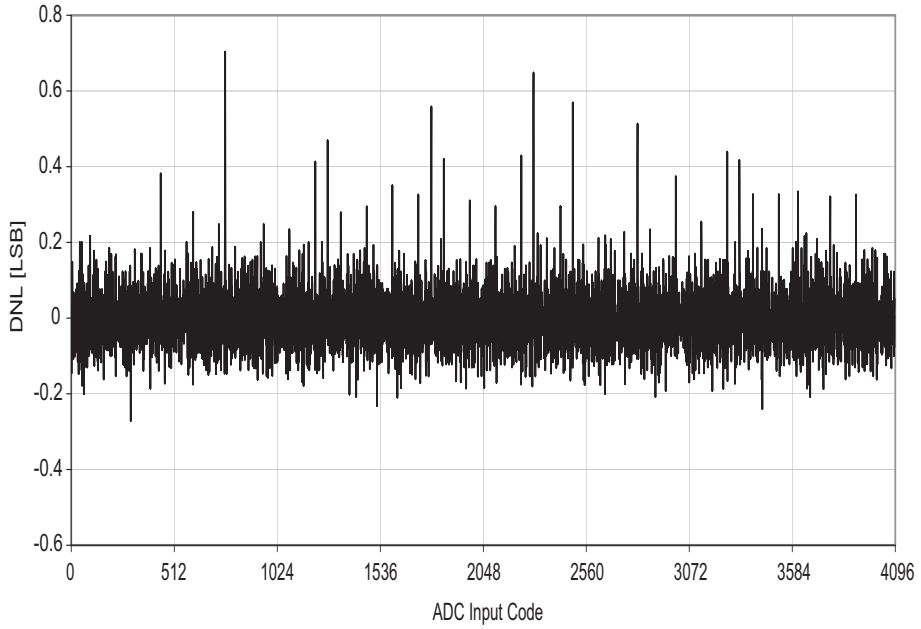



**Figure 37-294. Gain error vs. $V_{REF}$**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps***

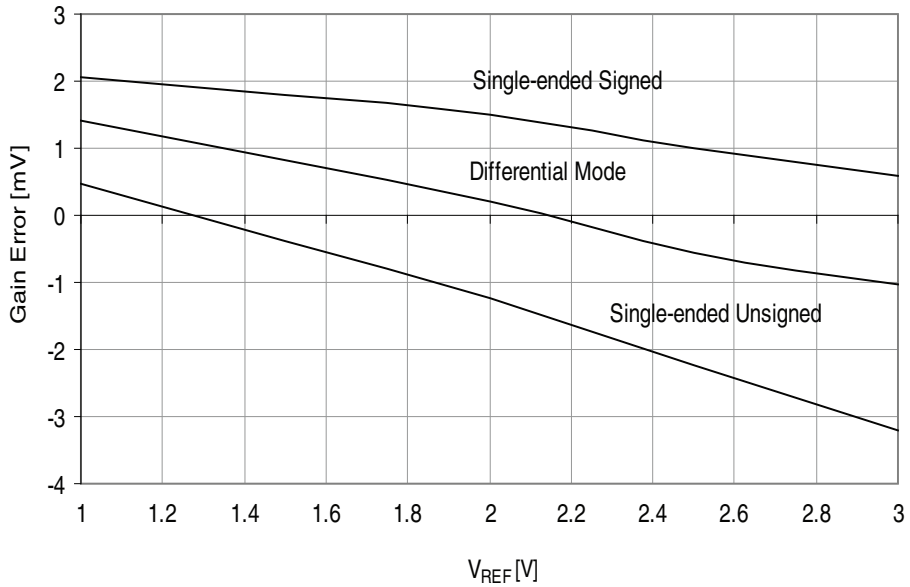


**Figure 37-295. Gain error vs. $V_{CC}$**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps***

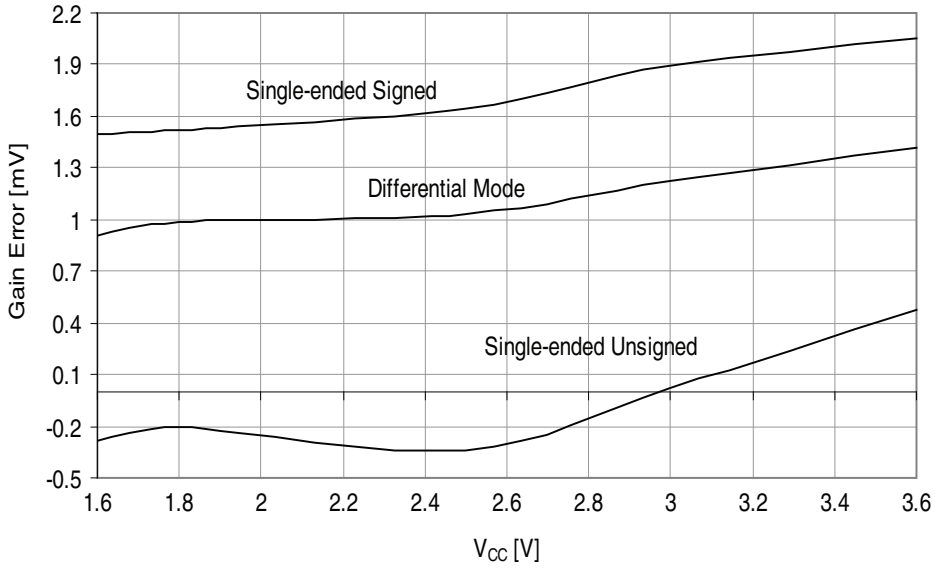



**Figure 37-296. Offset error vs. $V_{REF}$**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps***

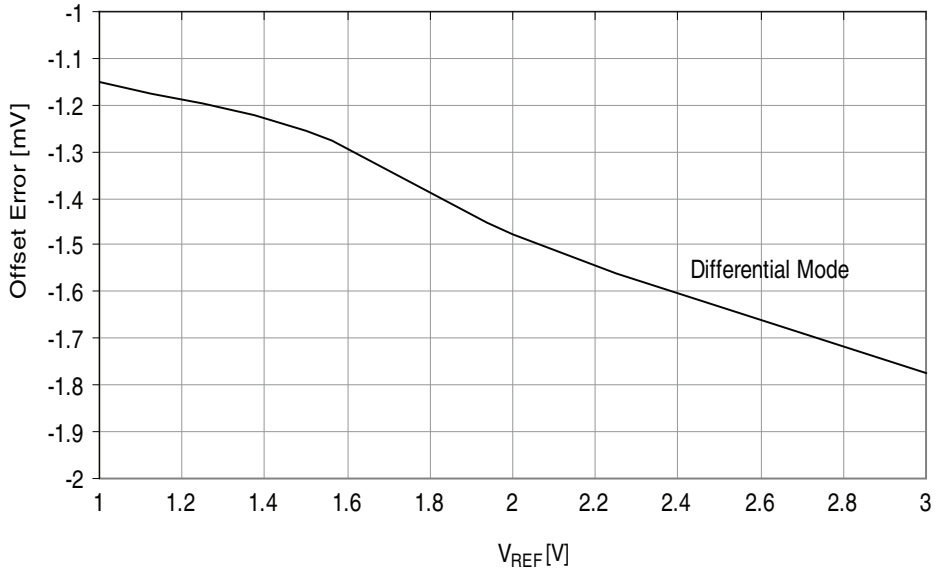


**Figure 37-297. Gain error vs. temperature**

***$V_{CC}$ = 3.0V, $V_{REF}$ = external 2.0V***

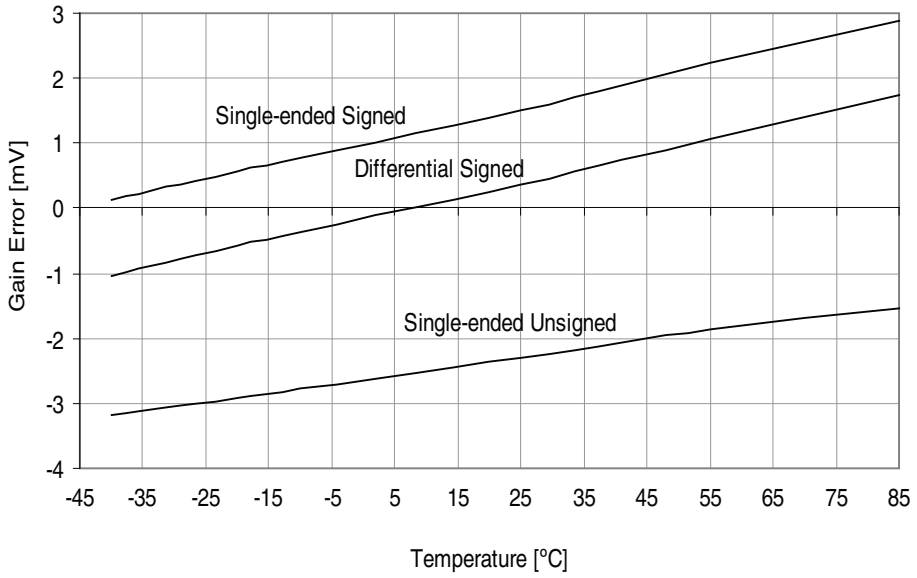



**Figure 37-298. Offset error vs. $V_{CC}$**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps***

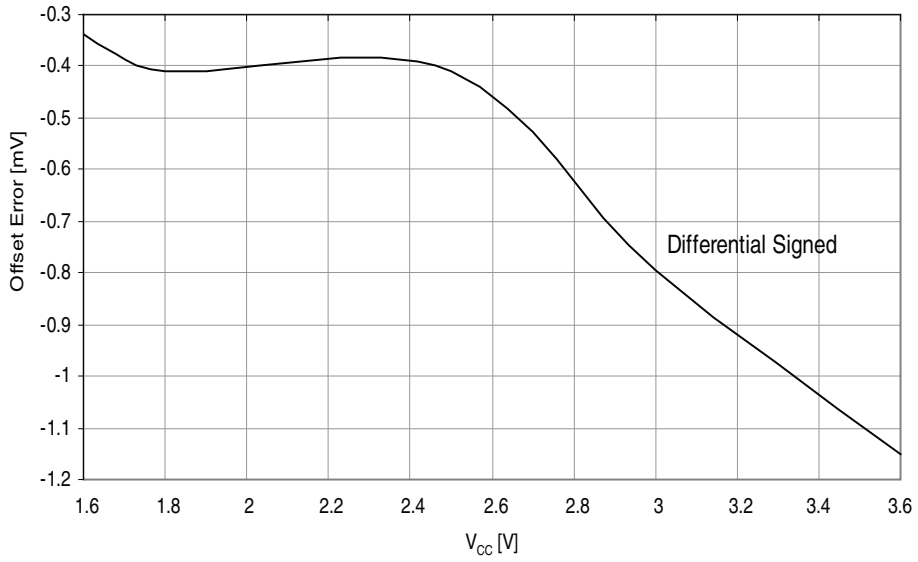


**Figure 37-299. Noise vs. $V_{REF}$**

***T = 25°C, $V_{CC}$ = 3.6V, ADC sampling speed = 500ksps***

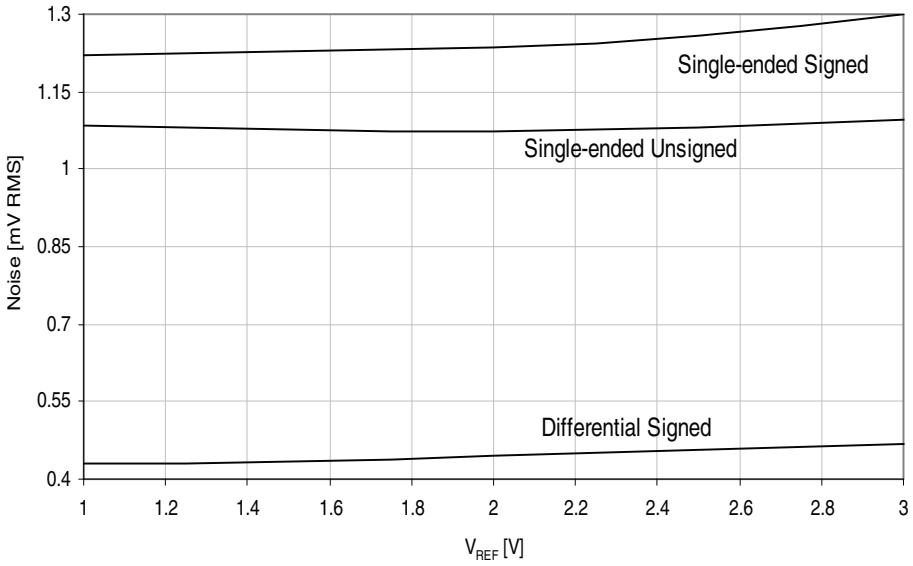
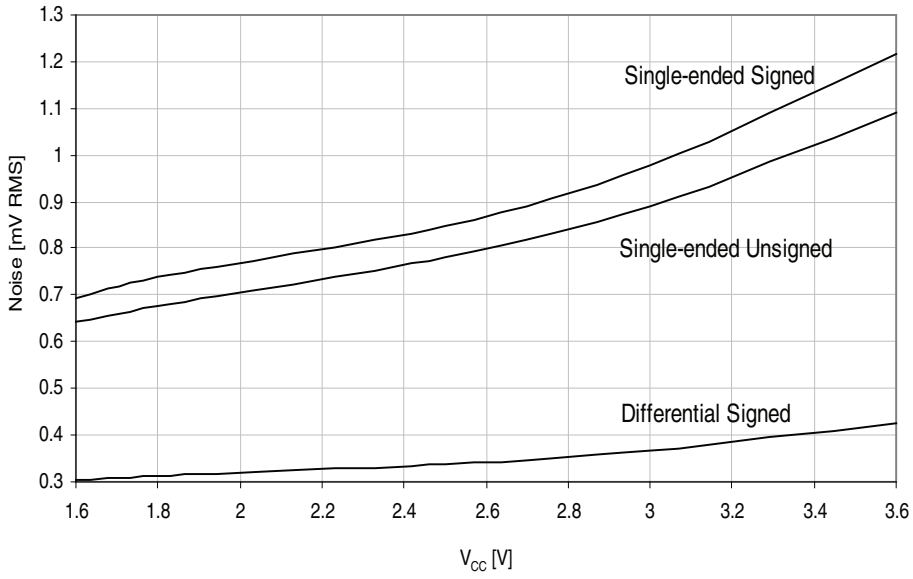



**Figure 37-300. Noise vs. $V_{CC}$**

***T = 25°C, $V_{REF}$ = external 1.0V, ADC sampling speed = 500ksps***



### 37.4.4 DAC Characteristics

**Figure 37-301. DAC INL error vs. $V_{REF}$**

***$V_{CC}$ = 3.6V***

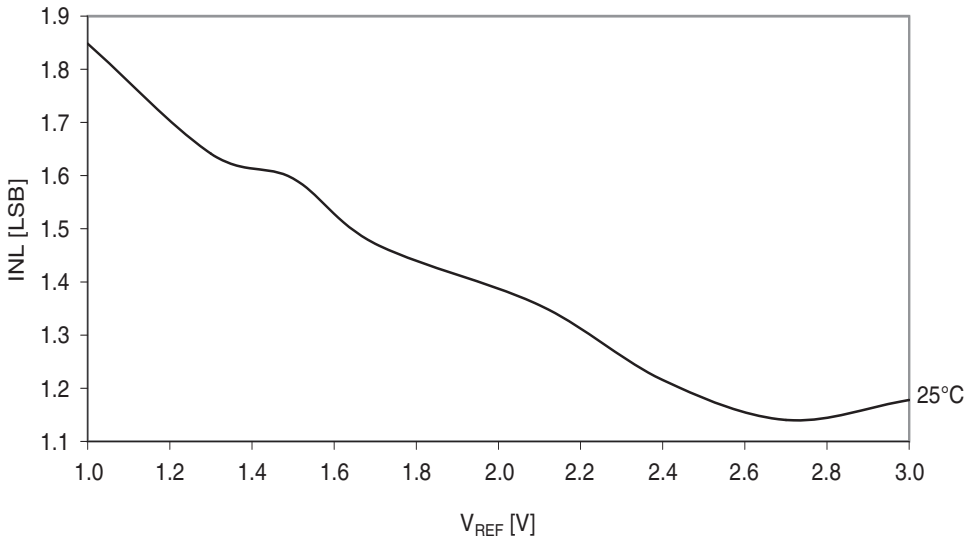



**Figure 37-302. DNL error vs. $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V.***

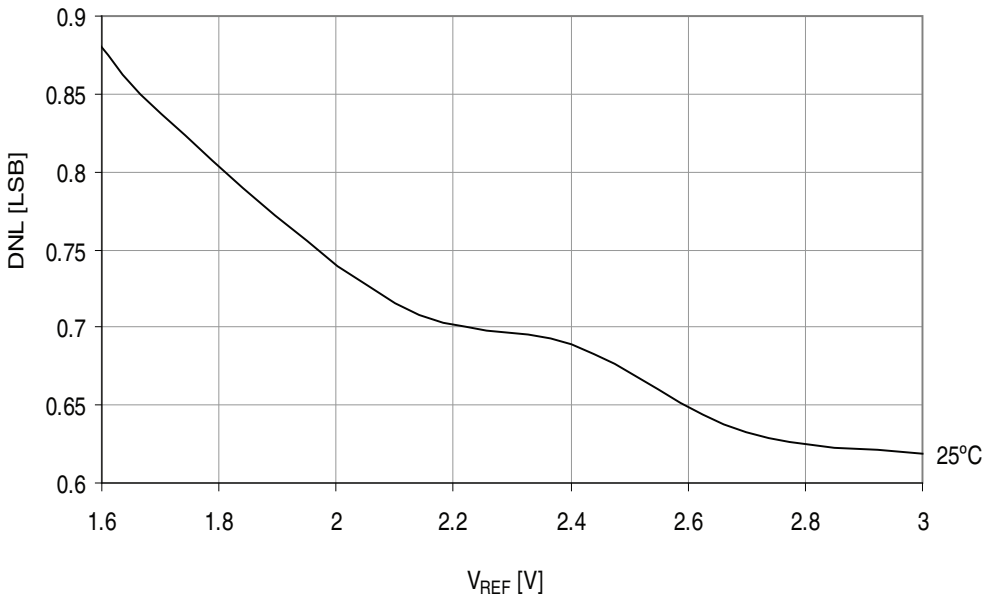
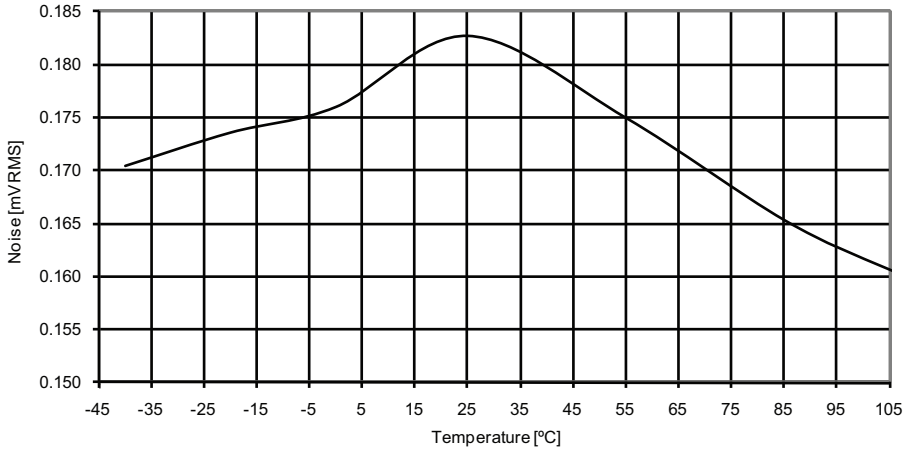


**Figure 37-303. DAC noise vs. temperature**

***$V_{CC}$ = 3.0V, $V_{REF}$ = 2.4V***




## 37.4.5 Analog Comparator Characteristics

**Figure 37-304. Analog comparator hysteresis vs. $V_{CC}$.**

***High-speed, small hysteresis***

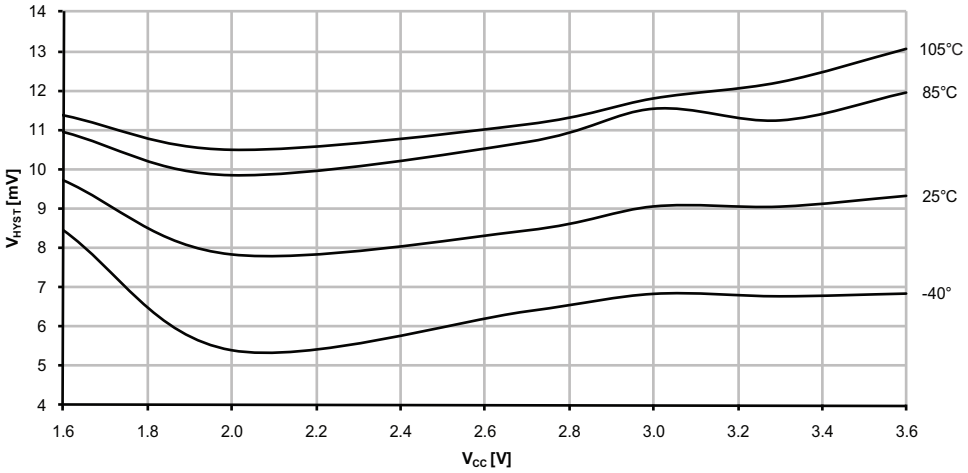


**Figure 37-305. Analog comparator hysteresis vs. $V_{CC}$.**

***Low power, small hysteresis***

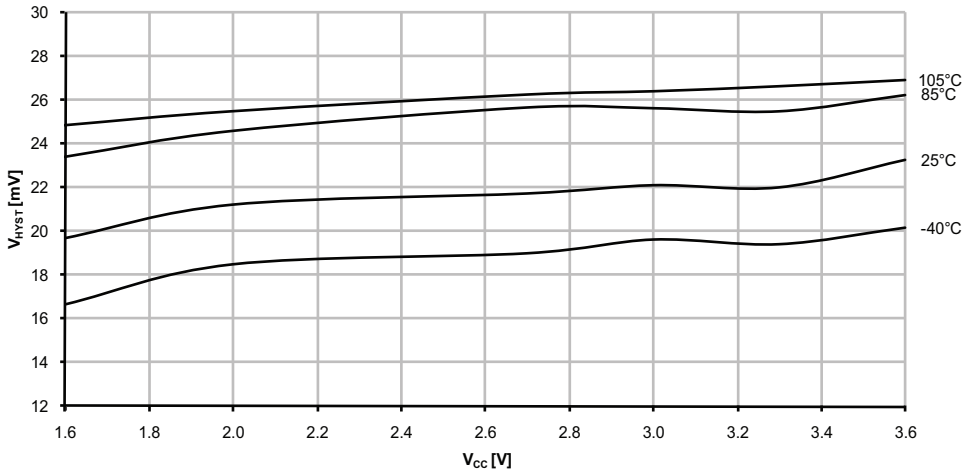



**Figure 37-306. Analog comparator hysteresis vs. $V_{CC}$.**

***High-speed mode, large hysteresis***

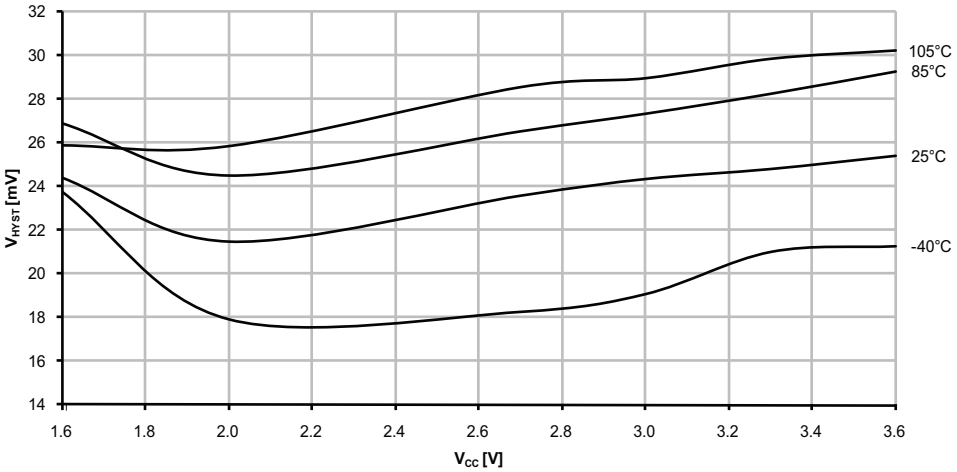


**Figure 37-307. Analog comparator hysteresis vs. $V_{CC}$.**

***Low power, large hysteresis***

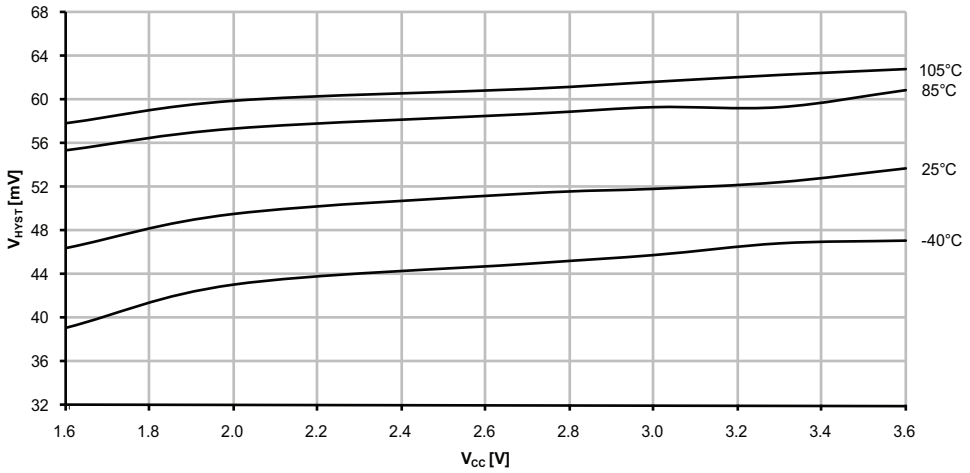



**Figure 37-308. Analog comparator current source vs. calibration value.**

***Temperature = 25°C***

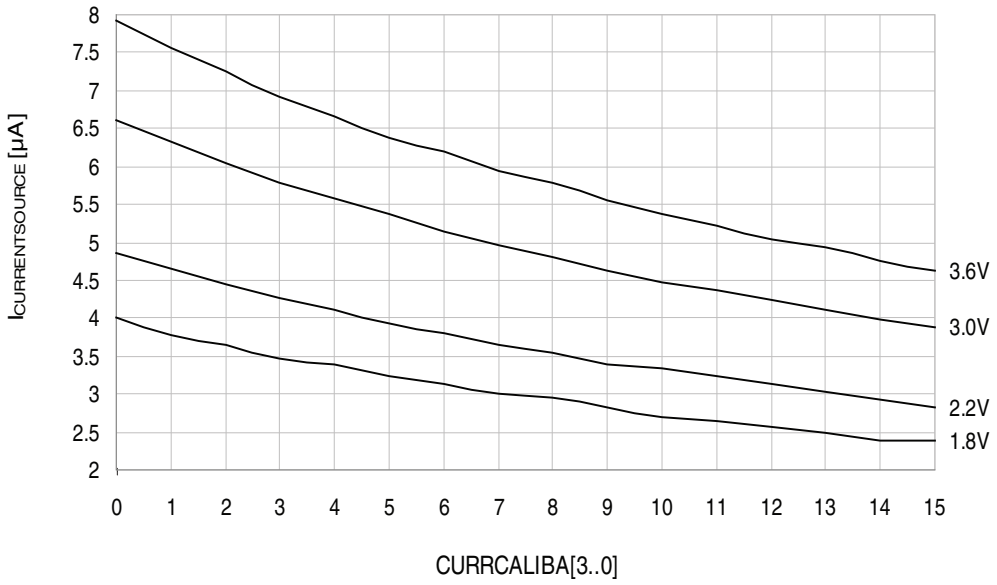


**Figure 37-309. Analog comparator current source vs. calibration value.**

***$V_{CC}$ = 3.0V.***

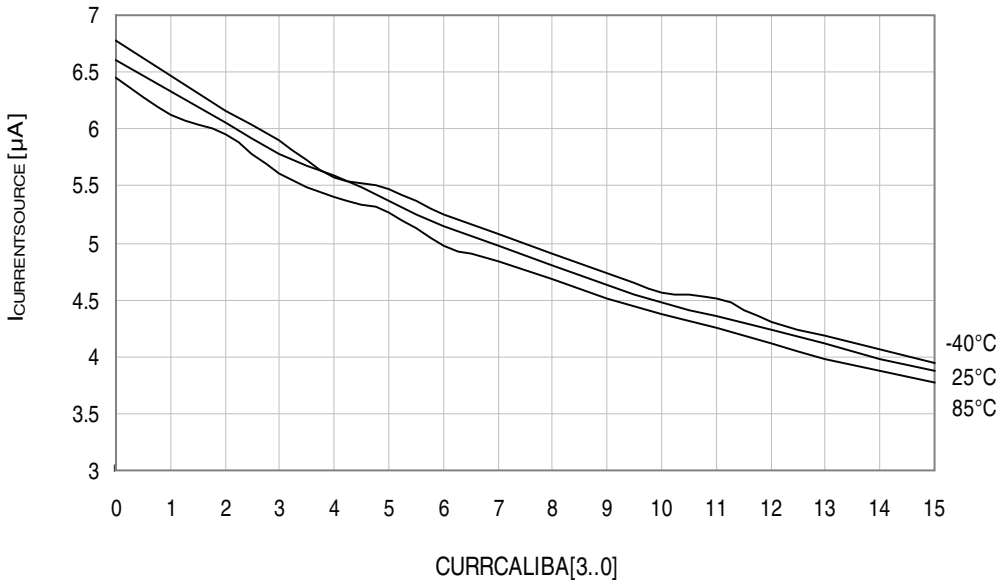
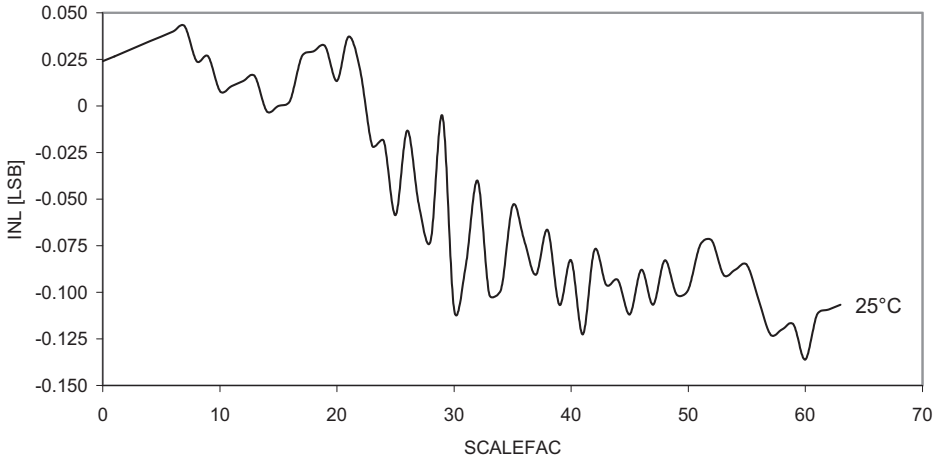


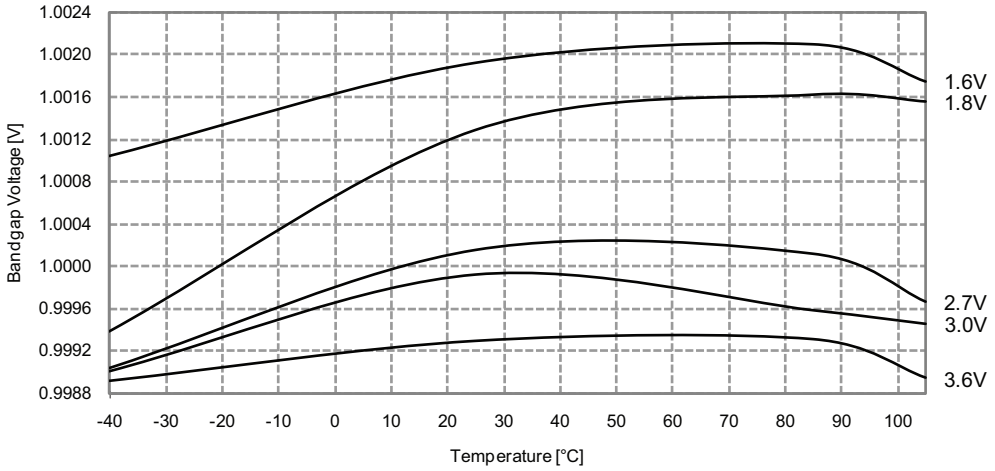

**Figure 37-310. Voltage scaler INL vs. SCALEFAC.**

***T = 25°C, $V_{CC}$ = 3.0V.***



### 37.4.6 Internal 1.0V reference Characteristics

**Figure 37-311. ADC/DAC Internal 1.0V reference vs. temperature**




### 37.4.7 BOD Characteristics

**Figure 37-312. BOD thresholds vs. temperature.**
***BOD level = 1.6V***

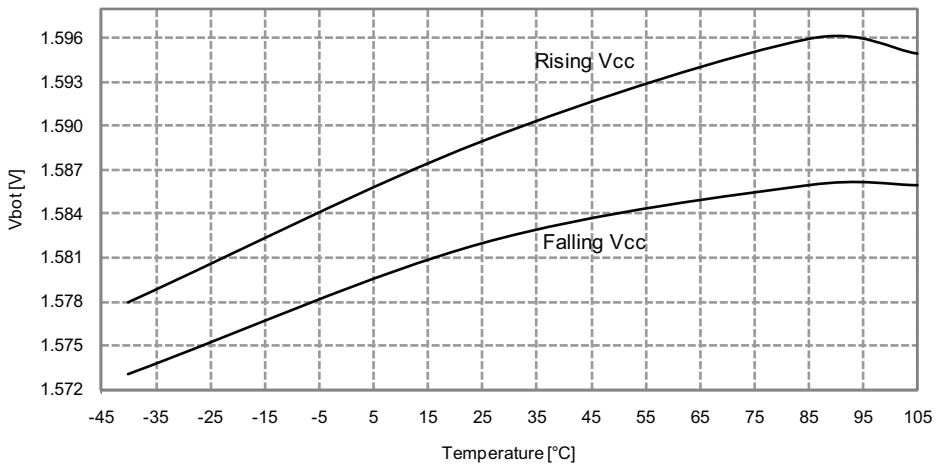
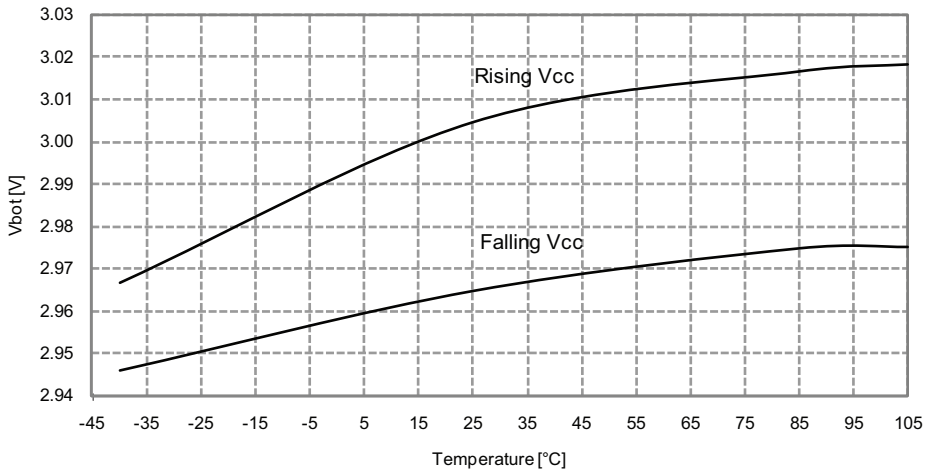


**Figure 37-313. BOD thresholds vs. temperature.**

***BOD level = 3.0V***




## 37.4.8 External Reset Characteristics

**Figure 37-314. Minimum Reset pin pulse width vs. $V_{CC}$**

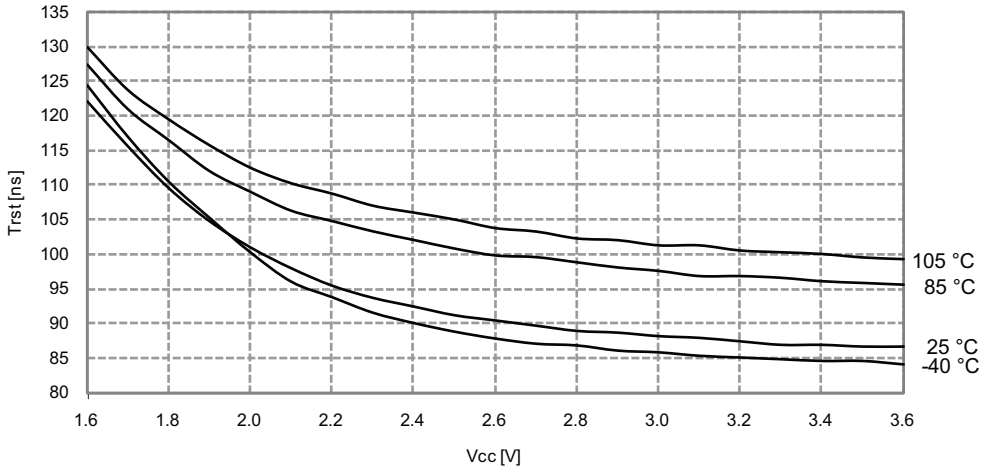


**Figure 37-315. Reset pin pull-up resistor current vs. reset pin voltage**

***$V_{CC}$ = 1.8V***

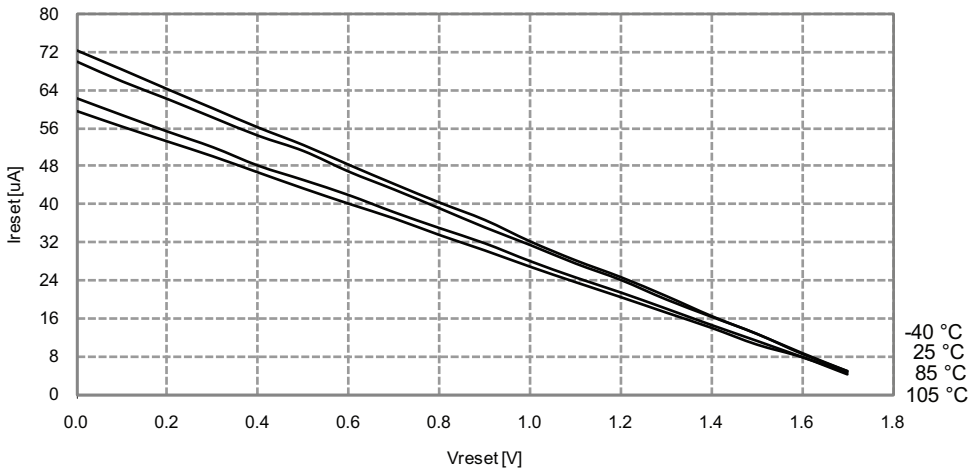



**Figure 37-316. Reset pin pull-up resistor current vs. reset pin voltage**

***$V_{CC}$ = 3.0V***

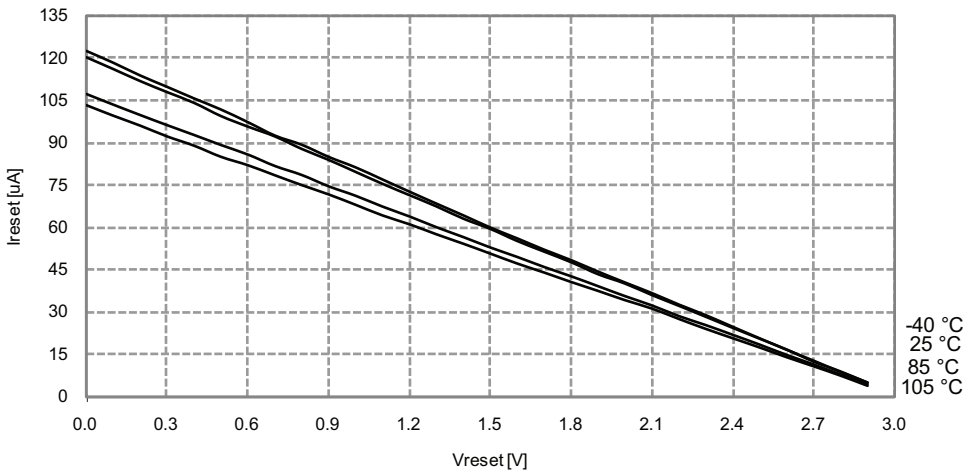


**Figure 37-317. Reset pin pull-up resistor current vs. reset pin voltage**

***$V_{CC}$ = 3.3V***

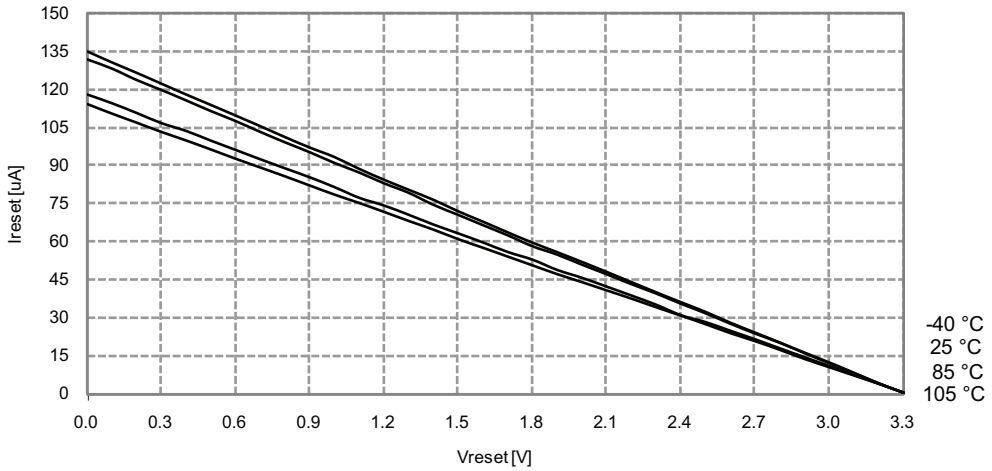



**Figure 37-318. Reset pin input threshold voltage vs. $V_{CC}$**

***$V_{IH}$ - Reset pin read as "1"***

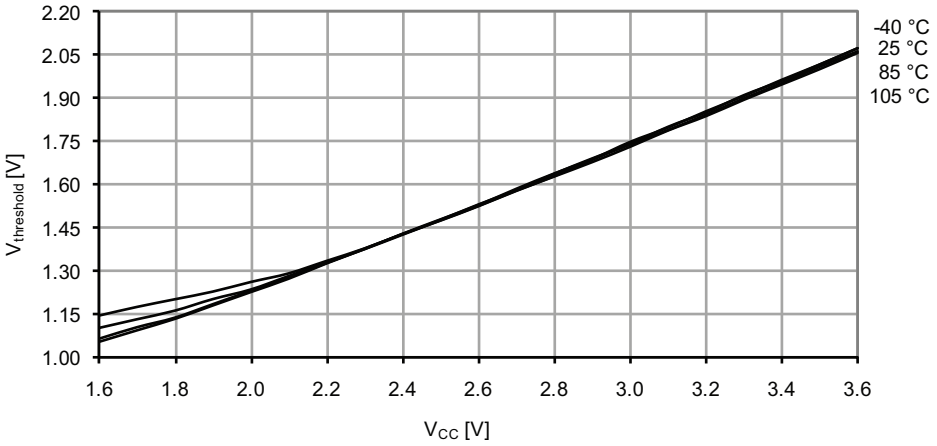
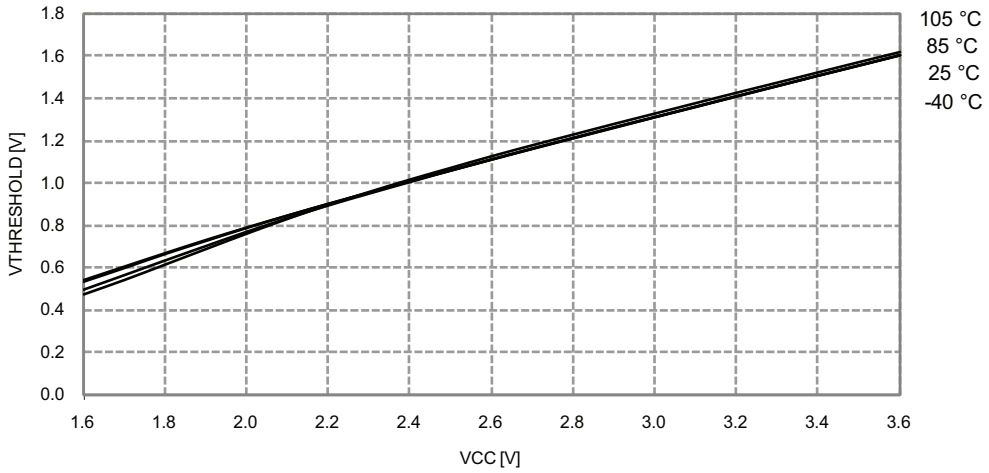


**Figure 37-319. Reset pin input threshold voltage vs. $V_{CC}$**

***$V_{IL}$ - Reset pin read as "0"***




## 37.4.9 Power-on Reset Characteristics

**Figure 37-320. Power-on reset current consumption vs. $V_{CC}$**

***BOD level = 3.0V, enabled in continuous mode***

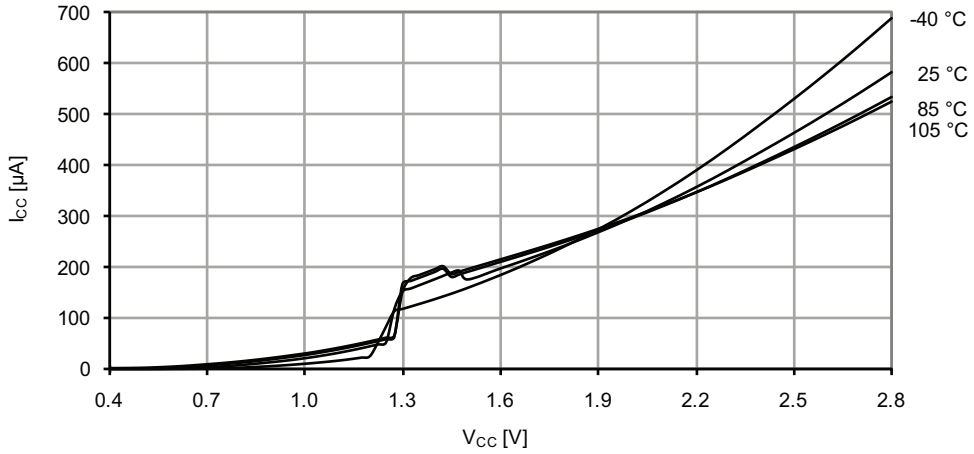
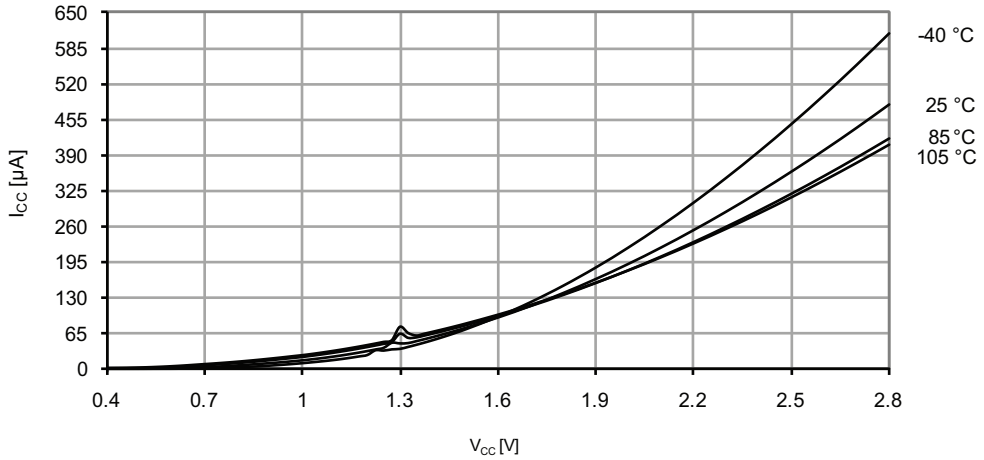


**Figure 37-321. Power-on reset current consumption vs. $V_{CC}$**

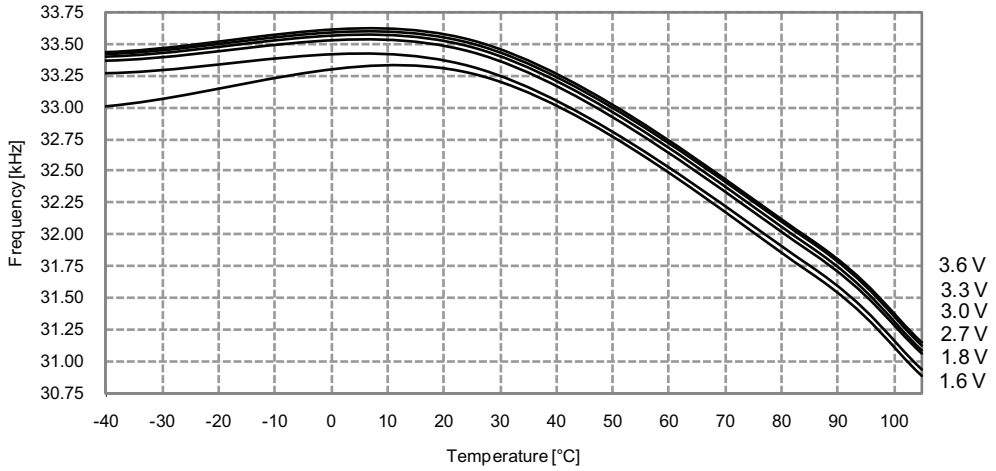
***BOD level = 3.0V, enabled in sampled mode***




## 37.4.10 Oscillator Characteristics

### 37.4.10.1 Ultra Low-Power internal oscillator

**Figure 37-322. Ultra Low-Power internal oscillator frequency vs. temperature.**



### 37.4.10.2 32.768kHz Internal Oscillator

**Figure 37-323. 32.768kHz internal oscillator frequency vs. temperature**

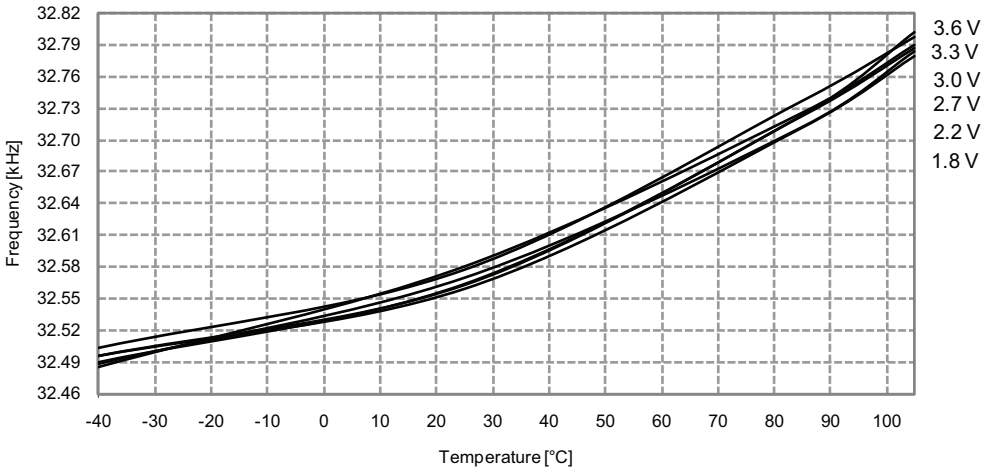
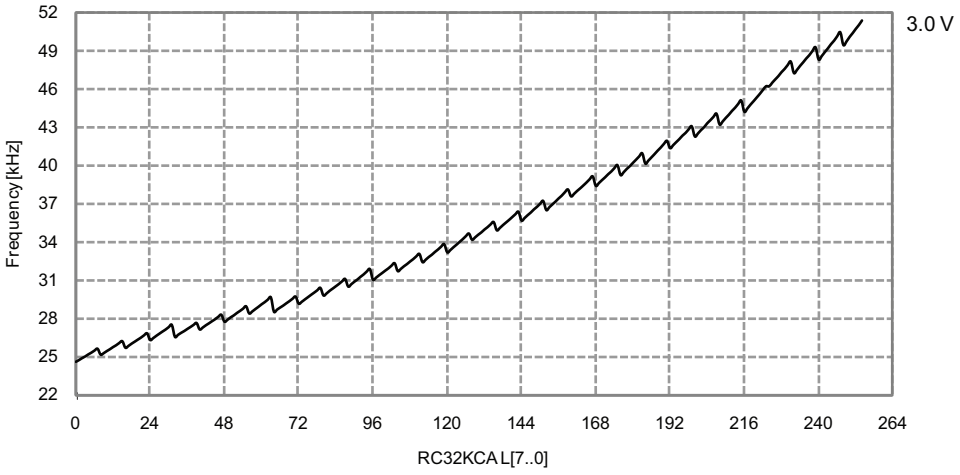



**Figure 37-324. 32.768kHz internal oscillator frequency vs. calibration value**

***$V_{CC}$ = 3.0V, T = 25°C***



### 37.4.10.3 2MHz Internal Oscillator

**Figure 37-325. 2MHz internal oscillator frequency vs. temperature**

***DFLL disabled***

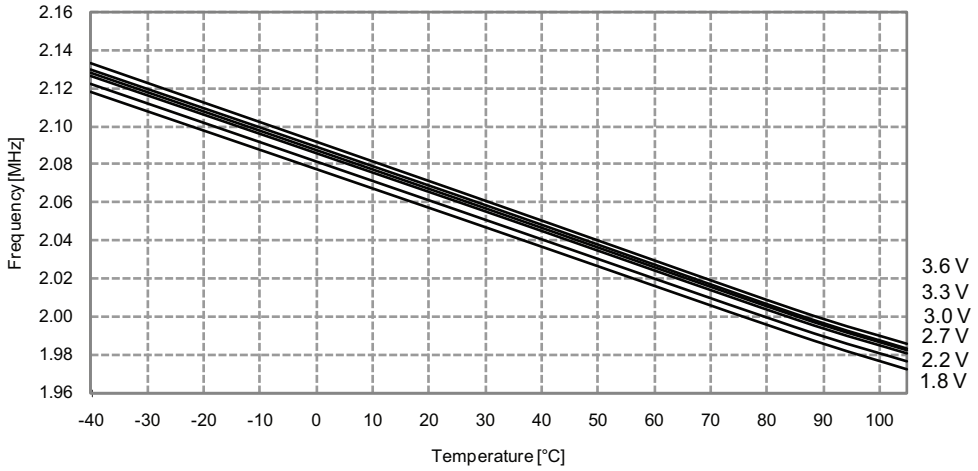



**Figure 37-326. 2MHz internal oscillator frequency vs. temperature**

***DFLL enabled, from the 32.768kHz internal oscillator***

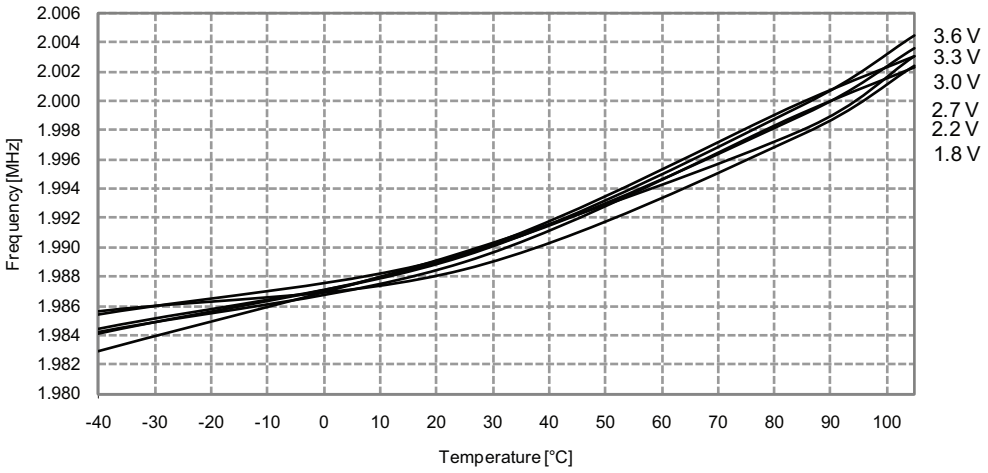
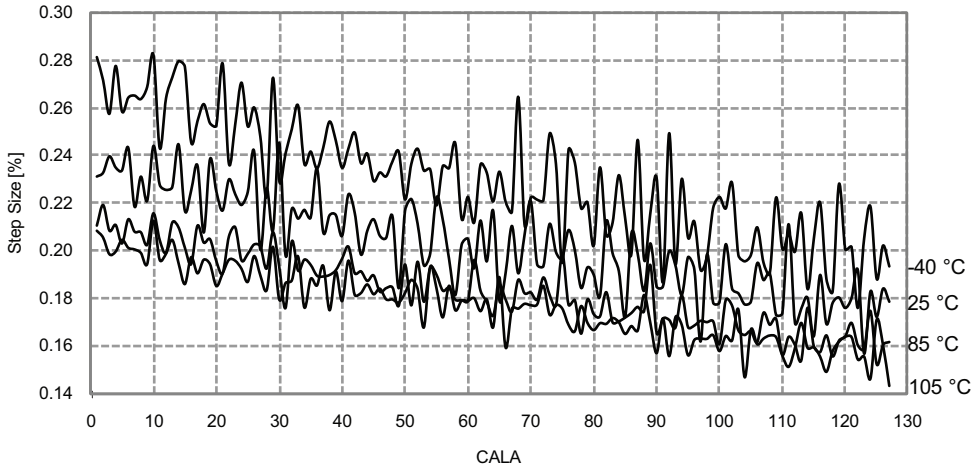


**Figure 37-327. 2MHz internal oscillator CALA calibration step size**

***$V_{CC}$ = 3V***




### 37.4.10.4 32MHz Internal Oscillator

**Figure 37-328. 32MHz internal oscillator frequency vs. temperature**

***DFLL disabled***

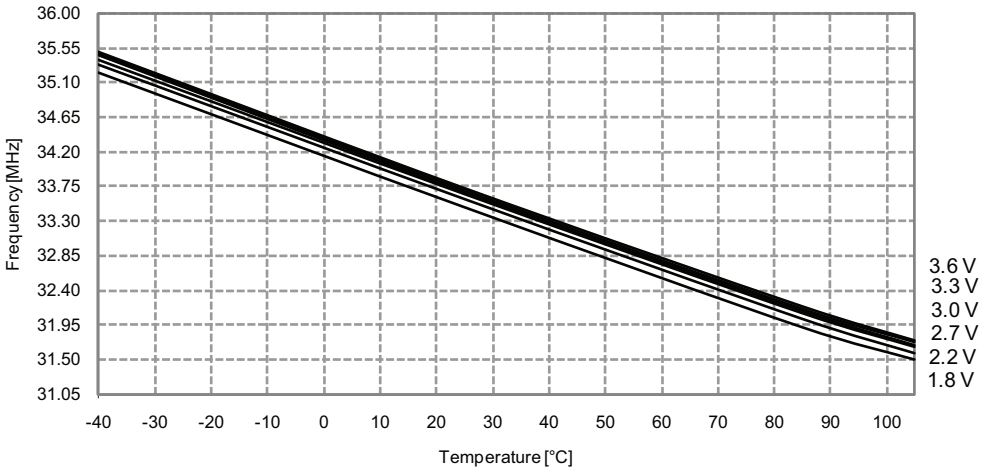


**Figure 37-329. 32MHz internal oscillator frequency vs. temperature**

***DFLL enabled, from the 32.768kHz internal oscillator***

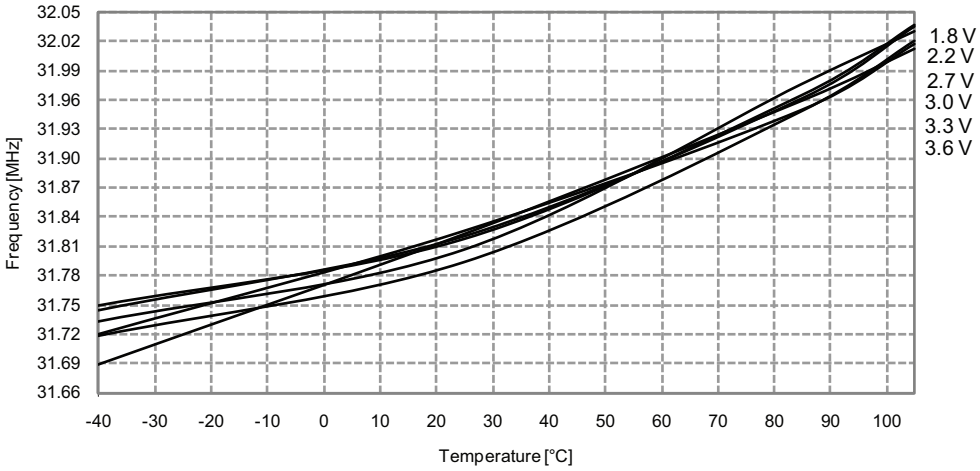
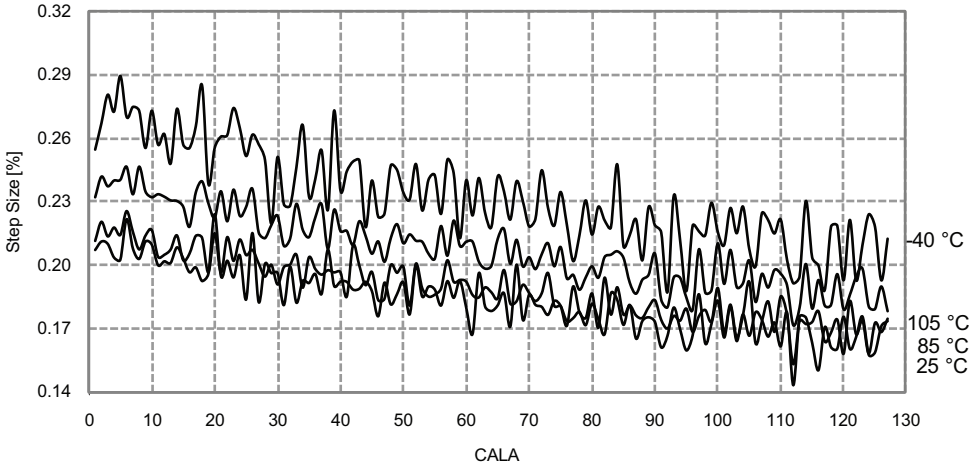



**Figure 37-330. 32MHz internal oscillator CALA calibration step size**

***$V_{CC}$ = 3.0V***



### 37.4.10.5 32MHz internal oscillator calibrated to 48MHz

**Figure 37-331. 48MHz internal oscillator frequency vs. temperature**

***DFLL disabled***

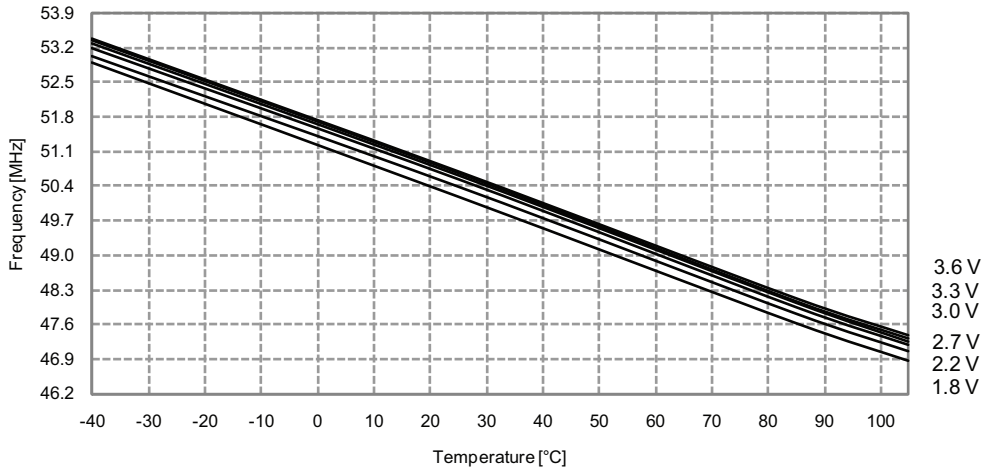



**Figure 37-332. 48MHz internal oscillator frequency vs. temperature**

***DFLL enabled, from the 32.768kHz internal oscillator***

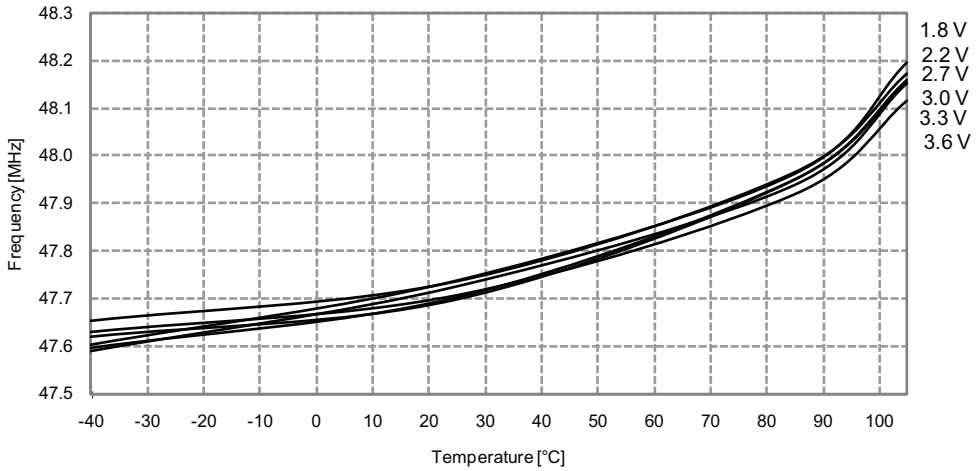
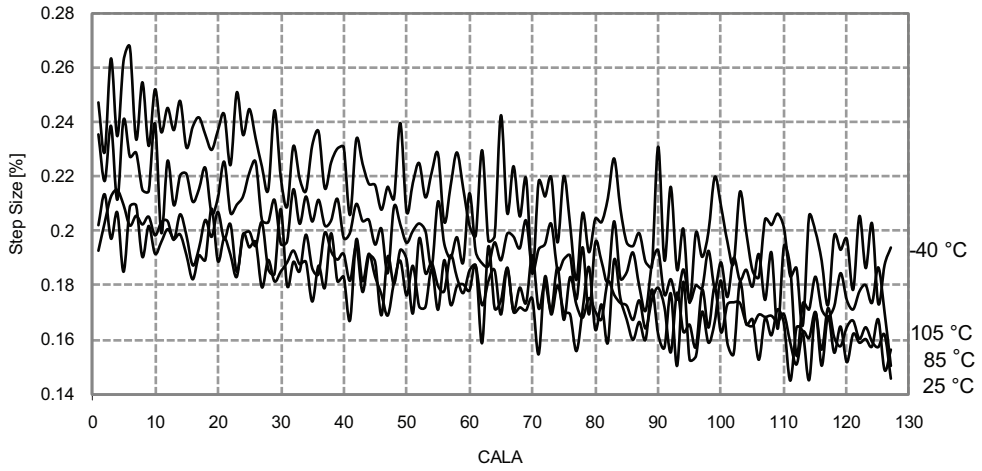


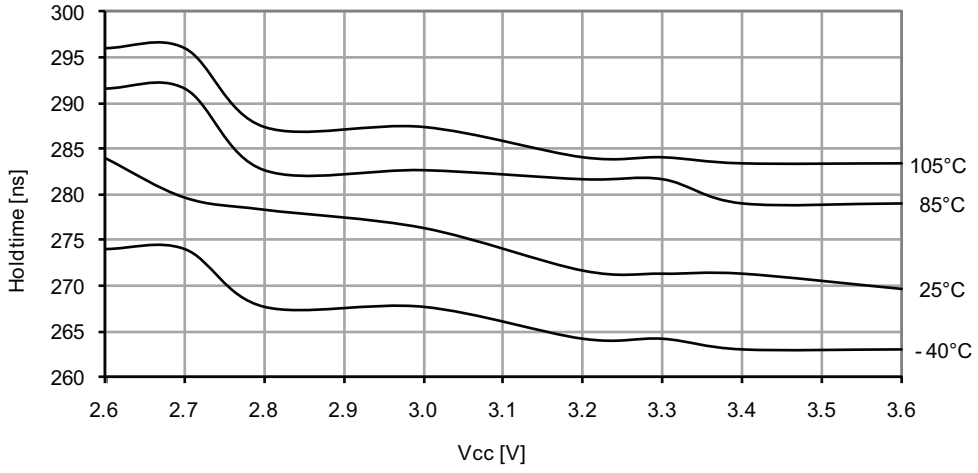
**Figure 37-333. 48MHz internal oscillator CALA calibration step size**

$V_{CC} = 3V$



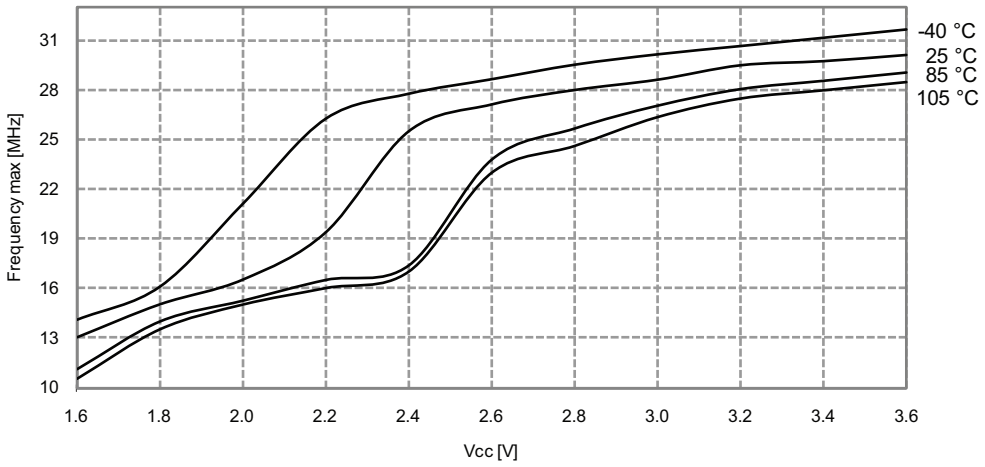

## 37.4.11 Two-Wire Interface characteristics

**Figure 37-334. SDA hold time vs. supply voltage**



### 37.4.12 PDI characteristics

**Figure 37-335. Maximum PDI frequency vs. $V_{CC}$**



# 38. Errata

## 38.1 ATxmega16A4U

### 38.1.1 Rev. E

- ADC may have missing codes in SE unsigned mode at low temp and low Vcc
- CRC fails for Range CRC when end address is the last word address of a flash section
- AWeX fault protection restore is not done correct in Pattern Generation Mode

1. **ADC may have missing codes in SE unsigned mode at low temp and low Vcc**
   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   **Problem fix/Workaround**
   Use the ADC in SE signed mode.

2. **CRC fails for Range CRC when end address is the last word address of a flash section**
   If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

   **Problem fix/Workaround**
   Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

3. **AWeX fault protection restore is not done correct in Pattern Generation Mode**
   When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTLSBUF register.

   **Problem fix/Workaround**
   For CWCM no workaround is required.

   For PGM in latched mode, disable the DTI channels before returning from the fault condition. Then, set correct OUTOVEN value and enable the DTI channels, before the direction (DIR) register is written to enable the correct outputs again.

### 38.1.2 Rev. A - D

Not sampled.

## 38.2 ATxmega32A4U

### 38.2.1 Rev. E

- ADC may have missing codes in SE unsigned mode at low temp and low Vcc
- CRC fails for Range CRC when end address is the last word address of a flash section
- AWeX fault protection restore is not done correct in Pattern Generation Mode

1. **ADC may have missing codes in SE unsigned mode at low temp and low Vcc**

   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   **Problem fix/Workaround**

   Use the ADC in SE signed mode.

2. **CRC fails for Range CRC when end address is the last word address of a flash section**

   If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

   **Problem fix/Workaround**

   Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

3. **AWeX fault protection restore is not done correct in Pattern Generation Mode**

   When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTLSBUF register.

   **Problem fix/Workaround**

   For CWCM no workaround is required.

   For PGM in latched mode, disable the DTI channels before returning from the fault condition. Then, set correct OUTOVEN value and enable the DTI channels, before the direction (DIR) register is written to enable the correct outputs again.

### 38.2.2 Rev. A - D

Not sampled.

## 38.3 ATxmega64A4U

### 38.3.1 Rev. D

- ADC may have missing codes in SE unsigned mode at low temp and low Vcc
- CRC fails for Range CRC when end address is the last word address of a flash section

1. **ADC may have missing codes in SE unsigned mode at low temp and low Vcc**
   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   **Problem fix/Workaround**
   Use the ADC in SE signed mode.

2. **CRC fails for Range CRC when end address is the last word address of a flash section**
   If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

   **Problem fix/Workaround**
   Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

### 38.3.2 Rev. C

- ADC may have missing codes in SE unsigned mode at low temp and low Vcc
- CRC fails for Range CRC when end address is the last word address of a flash section
- AWeX fault protection restore is not done correct in Pattern Generation Mode

1. **ADC may have missing codes in SE unsigned mode at low temp and low Vcc**
   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   **Problem fix/Workaround**
   Use the ADC in SE signed mode.

2. **CRC fails for Range CRC when end address is the last word address of a flash section**
   If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

   **Problem fix/Workaround**
   Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

3. **AWeX fault protection restore is not done correct in Pattern Generation Mode**

When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTLSBUF register.

**Problem fix/Workaround**

For CWCM no workaround is required.

For PGM in latched mode, disable the DTI channels before returning from the fault condition. Then, set correct OUTOVEN value and enable the DTI channels, before the direction (DIR) register is written to enable the correct outputs again.

### 38.3.3 Rev. A - B

Not sampled.

## 38.4 ATxmega128A4U

### 38.4.1 rev. A

- ADC may have missing codes in SE unsigned mode at low temp and low Vcc

1. **ADC may have missing codes in SE unsigned mode at low temp and low Vcc**

   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   **Problem fix/Workaround**

   Use the ADC in SE signed mode.

# 39. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

## 39.1 8387H –09/2014

| | |
|---|---|
| 1. | Updated "Ordering Information" on page 2. Added ordering information for ATxmega16A4U/32A4U/64A4U/128A4U @ 105°C |
| 2. | Updated the Application Table Section from 4K/4K/4K/4K to 8K/4K/4K/4K in the Figure 7-1 on page 14 |
| 3. | Updated Table 36-4 on page 74, Table 36-36 on page 95, Table 36-68 on page 117 and Table 36-100 on page 139. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled |
| 4. | Updated Table 36-20 on page 84, Table 36-52 on page 105, Table 36-84 on page 127 and Table 36-116 on page 149. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C |
| 5. | Added 105°C Typical Characterization plots for:<br>ATxmega16A4U<br>ATxmega32A4U<br>ATxmega64A4U<br>ATxmega128A4U |
| 6. | Changed Vcc to AVcc in Figure 28-1 on page 50 and in the text in Section 28. "ADC – 12-bit Analog to Digital Converter" on page 49 andSection 30. "AC – Analog Comparator" on page 53. |
| 7. | Changed values for 128A4U in Table 7-3 on page 17. Page size = 128, FWORD = Z(6:0) |
| 8. | Changed unit notation for parameter $t_{SU;DAT}$ to ns in Table 36-32 on page 92, Table 36-64 on page 113, and Table 36-128 on page 157. |

## 39.2 8387G – 03/2014

| | |
|---|---|
| 1. | Removed "Preliminary" from the datasheet |
| 2. | Updated "Errata" on page 327: added ERRATA "Rev. D" and "Rev. C" for "ATxmega64A4U" on page 329 |

## 39.3 8387F – 01/2014

| | |
|---|---|
| 1. | Removed JTAG references from the datasheet |
| 2. | Updated Figure 30-1 on page 54. The positive Mux has two "Input" while the negative Mux has four "Input" |

## 39.4 8387E – 11/2013

| | |
|---|---|
| 1. | Updated Flash size column in "Ordering Information" on page 2 for:<br>ATxmega128A4U-AU, ATxmega128A4U-AUR, ATxmega128A4U-MH and ATxmega128A4U-MHR |

## 39.5 8387D – 02/2013

| | |
|---|---|
| 1. | Updated typos in "Ordering Information" on page 2. |
| 2. | Updated PE2 and PE3 pins in "Pinout/Block Diagram" on page 4 to indicate that these can be used as TOSC pins. |
| 3. | Renamed pin 19 from VDD to VCC in Figure 2-1 on page 4. |
| 4. | Updated page size for ATxmega128A4U in Table 7-3 on page 17. |
| 5. | Added column for TWI using external driver interface in Table 32-3 on page 59. |
| 6. | Updated ATxmega16A4U leakage current in Table 36-7 on page 77. |
| 7. | Added application erase time for ATxmega16A4U in Table 36-21 on page 84. |
| 8. | Updated limits for VIH and VIL:<br>ATxmega16A4U: Table 36-7 on page 77<br>ATxmega32A4U: Table 36-39 on page 98<br>ATxmega64A4U: Table 36-71 on page 120<br>ATxmega128A4U:Table 36-103 on page 142 |
| 9. | Updated DAC clock and timing characteristics:<br>ATxmega16A4U: Table 36-13 on page 81<br>ATxmega32A4U: Table 36-45 on page 101<br>ATxmega64A4U: Table 36-77 on page 123<br>ATxmega128A4U: Table 36-109 on page 145. |
| 10. | Updated ATxmega16A4U " External clock characteristics" on page 86. |
| 11. | Added ESR parameter to the External 16MHz crystal oscillator and XOSC characteristics:<br>ATxmega16A4U: Table 36-29 on page 87<br>ATxmega32A4U: Table 36-61 on page 108<br>ATxmega64A4U: Table 36-93 on page 130<br>ATxmega128A4U: Table 36-125 on page 152. |
| 12. | Updated ATxmega32A4U leakage current in Table 36-39 on page 98. |
| 13. | Added application erase time for ATxmega32A4U in Table 36-53 on page 105. |
| 14. | Updated ATxmega32A4U " External clock characteristics" on page 107. |
| 15. | Updated ATxmega32A4U current consumption in electrical characteristics section, see "Current consumption" on page 117. |
| 16. | Updated electrical characteristics for "ATxmega64A4U" on page 115. |
| 17. | Updated typical characteristics for "ATxmega64A4U" on page 243. |
| 18. | Added application erase time for ATxmega128A4U in Table 36-117 on page 149. |
| 19. | Updated ATxmega128A4U " External clock characteristics" on page 151. |

## 39.6 8387C – 03/2012

| | |
|---|---|
| 1. | Updated "Ordering Information" on page 2. Added a new package PW. |
| 2. | Updated "Packaging information" on page 68. A new package PW added. |
| 3. | Updated the Table 36-4 on page 74 with new values for $I_{CC}$ active power consumption. |
| 4. | Updated all typical characteristics in " Active mode supply current" on page 159. |

| | |
|---|---|
| 5. | Updated all typical characteristics in “Power-down mode supply current” on page 166. |
| 6. | Added electrical characteristics for “ATxmega32A4U” on page 93. |
| 7. | Added electrical characteristics for “ATxmega64A4U” on page 115. |
| 8. | Added electrical characteristics for “ATxmega128A4U” on page 137. |
| 9. | Added typical characteristics for “ATxmega64A4U” on page 243 |
| 10. | Added typical characteristics for “ATxmega64A4U” on page 243. |
| 12. | Added typical characteristics for “ATxmega128A4U” on page 285. |
| 13. | Updated “Errata” on page 327. |
| 14. | Used Atmel new datasheet template that includes Atmel new addresses on the last page. |

## 39.7 8387B – 12/2011

| | |
|---|---|
| 1. | Updated Figure 2-1 on page 4: “Block Diagram and QFN/TQFP pinout” |
| 2. | Updated Figure 3-1 on page 7: “XMEGA A4U Block Diagram” |
| 3. | Updated “Overview” on page 13. |
| 4. | Updated “ADC – 12-bit Analog to Digital Converter” on page 49. |
| 5. | Updated Figure 28-1 on page 50: “ADC overview.” |
| 6. | Updated “Instruction Set Summary” on page 63. |
| 7. | Updated “Electrical Characteristics” on page 72. |
| 8. | Updated “Typical Characteristics” on page 159. |
| 9. | The order of several figures in the chapter “Typical Characteristics” has been changed |
| 10. | Several new figures have been added to and some figures have been removed from chapter “Typical Characteristics” |
| 11. | Several minor changes/corrections in text and figures have been performed |
| 12. | Table 32-2 on page 59 has been corrected |
| 13. | Table 32-4 on page 60 has been corrected |
| 14. | Table 36-29 on page 85 has been corrected |
| 15. | Table 36-30 on page 86 has been corrected |
| 16. | The heading ”I/O Pin Characteristics” on page 164 has been corrected (the text “and Reset” has been removed) |

## 39.8 8387A – 07/2011

| | |
|---|---|
| 1. | Initial revision. |

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