

***RoHS Recast Compliant***

# **ATA Disk Module**

***ADM5S 44P/270D Product Specifications***

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*Version 1.2*



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## Features:

- **Standard ATA/IDE Bus Interface**
  - ATA command set compatible
  - Compliant with ATA/ATAPI-8
  - ATA operating mode supports up to:
    - PIO Mode up to 4
    - Multiword DMA Mode up to 2
    - Ultra DMA Mode up to 6
- **Connector Type**
  - 44-pin female connector (2.00mm pitch)
- **Power Consumption\***
  - Supply voltage: 3.3V & 5V
  - Active mode: 265 mA
  - Idle mode: 5 mA
- **Performance\***
  - Sustained read: Up to 75 MB/sec
  - Sustained write: Up to 65 MB/sec
- **Capacity**
  - 128, 256, 512 MB
  - 1, 2, 4, 8, 16, 32, 64 GB
- **NAND Flash Type:** SLC
- **MTBF:** > 2,000,000 hours
- **Temperature Range**
  - Operation:
    - Standard: 0°C to 70°C
    - Extended: -40 to 85°C
  - Storage: -40°C to 100°C
- **Form Factor**
  - ATA Disk Module
  - Dimension: 45.0 x 28.0 x 6.85, unit: mm
- **Flash Management**
  - Advanced wear-leveling algorithms
  - Built-in hardware ECC
  - Flash block management
  - Power failure management
- **ATA Secure Erase**
- **S.M.A.R.T. Technology**
- **Shock & Vibration\*\***
  - Shock: 1,500 G
  - Vibration: 15 G
- **Master/Slave Switch** (optional)
- **RoHS Recast Compliant (2011/65/EU)**

\*Performance and power consumption addressed here are typical and may vary from flash configurations or platforms.

\*\*Non-operating

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## 1. General Description

Apacer's ATA Disk Module 5S (ADM5S) SSD delivers smooth performance and low power consumption. This device supports DMA mode up to UDMA 6 that offers advanced data transfer technology and internal memory efficiency, which effectively decreases the loading for the microprocessor. Compliant with ATA/ATAPI-8 standards, our ADM5S supports data transfer modes up to PIO 4, Multiword DMA 2, and Ultra DMA 6. Equipped with power Error Correction Coding (ECC) up to 72bit/1KB, the ADM5S can provide high data integrity. Aside from data efficiency, the ADM5S also comes with power management. The device can work at 3.3V or 5V power supply, with the output voltage automatically adjusted by the voltage regulator in the core. In addition, the built-in ECC engine can support multi-mode correction capability up to 72 bits and perform effective decoding throughput with high reliability.

ADM is a cost-effective solution with standard ATA compliance deployable at all major operating systems such as Microsoft's Windows series, Apple's Mac OS family, and Unix variants. Featuring technologies as wear leveling, S.M.A.R.T, power failure management, and ATA Secure Erase, Apacer's ADM is definitely the ideal and reliable system storage.

## 2. Functional Block

The ATA-Disk Module (ADM) includes the ATA controller and flash media, as well as the ATA standard interface. Figure 2-1 shows the functional block diagram.



Figure 2-1 Functional Block Diagram

## 3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 44-pin configuration. A “#” suffix indicates the active low signal. The pin type can be input, output or input/output.

**Table 3-1** Pin Assignments for the 44-Pin Configuration

| Pin No. | Signal Name                   | Pin Type | I/O Type* | Pin No. | Signal Name         | Pin Type | I/O Type |
|---------|-------------------------------|----------|-----------|---------|---------------------|----------|----------|
| 1       | RESET#                        | I        | I2U       | 2       | GND                 | -        | Ground   |
| 3       | D7                            | I/O      | I1Z, O2   | 4       | D8                  | I/O      | I1Z, O2  |
| 5       | D6                            | I/O      | I1Z, O2   | 6       | D9                  | I/O      | I1Z, O2  |
| 7       | D5                            | I/O      | I1Z, O2   | 8       | D10                 | I/O      | I1Z, O2  |
| 9       | D4                            | I/O      | I1Z, O2   | 10      | D11                 | I/O      | I1Z, O2  |
| 11      | D3                            | I/O      | I1Z, O2   | 12      | D12                 | I/O      | I1Z, O2  |
| 13      | D2                            | I/O      | I1Z, O2   | 14      | D13                 | I/O      | I1Z, O2  |
| 15      | D1                            | I/O      | I1Z, O2   | 16      | D14                 | I/O      | I1Z, O2  |
| 17      | D0                            | I/O      | I1Z, O2   | 18      | D15                 | I/O      | I1Z, O2  |
| 19      | GND                           | -        | Ground    | 20      | NC                  | -        | -        |
| 21      | DMARQ#                        | O        | O1        | 22      | GND                 | -        | Ground   |
| 23      | IOWR#<br>STOP                 | I        | I2Z       | 24      | GND                 | -        | Ground   |
| 25      | IORD#<br>HDMARDY#<br>HSTROBE# | I        | I2Z       | 26      | GND                 | -        | Ground   |
| 27      | IORDY<br>DDMARDY#<br>DSTROBE  | O        | O1        | 28      | NC/CSEL             | I        | I1U      |
| 29      | DMACK#                        | I        | I2U       | 30      | NC/WP# <sup>1</sup> | -/I      | -/I1U    |
| 31      | INTRQ                         | O        | O1        | 32      | IOCS16#             | O        | O2       |
| 33      | A1                            | I        | I1Z       | 34      | PDIAG#              | I/O      | I1U, O1  |
| 35      | A0                            | I        | I1Z       | 36      | A2                  | I        | I1Z      |
| 37      | CS1FX#                        | I        | I2Z       | 38      | CS3FX#              | I        | I2Z      |
| 39      | DASP#                         | I/O      | I1U, O6   | 40      | GND                 | -        | Ground   |
| 41      | VDD                           | -        | Power     | 42      | VDD                 | -        | Power    |
| 43      | GND                           | -        | Ground    | 44      | NC                  | -        | -        |

\*Pin 30 is selectable as NC or WP# through a zero ohm resistor jumper. Default is NC. Note that pin 30 is a GND pin on standard ATA interface. This pin could be redesigned for host to control the write protect function on ADM.

## 4. Product Specifications

### 4.1 Capacity

Capacity specifications of the ATA-Disk Module (ADM) product family are available as shown in Table 4-1.

**Table 4-1** Capacity Specifications (unformatted)

| Capacity | Total bytes    | Cylinders | Heads | Sectors | Max LBA     |
|----------|----------------|-----------|-------|---------|-------------|
| 128 MB   | 128,057,344    | 977       | 8     | 32      | 250,112     |
| 256 MB   | 256,901,120    | 980       | 16    | 32      | 501,760     |
| 512 MB   | 512,483,328    | 993       | 16    | 63      | 1,000,944   |
| 1 GB     | 1,011,032,064  | 1959      | 16    | 63      | 1,974,672   |
| 2 GB     | 2,011,226,112  | 3897      | 16    | 63      | 3,928,176   |
| 4 GB     | 4,011,614,208  | 7773      | 16    | 63      | 7,835,184   |
| 8 GB     | 8,012,390,400  | 15525     | 16    | 63      | 15,649,200  |
| 16 GB    | 16,013,942,784 | 16383     | 16    | 63      | 31,277,232  |
| 32 GB    | 32,017,047,552 | 16383     | 16    | 63      | 62,533,296  |
| 64 GB    | 64,023,257,088 | 16383     | 16    | 63      | 125,045,424 |

\*Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies.

\*\*Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

### 4.2 Performance

Performance of the ATA-Disk Module is listed in Table 4-2.

**Table 4-2** Performance Specifications

| Capacity \ Performance | 128 MB | 256 MB | 512 MB | 1 GB | 2 GB | 4 GB | 8 GB | 16 GB | 32 GB | 64 GB |
|------------------------|--------|--------|--------|------|------|------|------|-------|-------|-------|
| Sustained read (MB/s)  | 24     | 24     | 31     | 31   | 35   | 65   | 70   | 75    | 75    | 75    |
| Sustained write (MB/s) | 11     | 11     | 20     | 20   | 28   | 50   | 60   | 65    | 65    | 65    |

\*Results may differ from various flash configurations and platforms.

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### 4.3 Environmental Specifications

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Environmental specifications of the ATA-Disk Module (ADM) follow the MIL-STD-810F standard.

**Table 4-3** Environmental Specifications

| Environment               |           | Specifications                                        |
|---------------------------|-----------|-------------------------------------------------------|
| Temperature               | Operation | 0°C to 70°C (Standard); -40°C to 85°C (Extended)      |
|                           | Storage   | -40°C to 100°C                                        |
| Vibration (Non-Operating) |           | Sine wave: 10~2000Hz, 15G (X, Y, Z axes)              |
| Shock (Non-Operating)     |           | Half sine wave, 1,500 G, 11 ms (X, Y, Z ; All 6 axes) |

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## 5. Flash Management

### 5.1 Advanced Wear-Leveling algorithms

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Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Wear leveling is an important mechanism that level out the wearing of blocks so that the wearing-down of blocks can be almost evenly distributed. This will increase the lifespan of SSDs. Commonly used wear leveling types are Static and Dynamic.

### 5.2 Built-in Hardware ECC

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The properties of NAND flash memory make it ideal for applications that require high integrity while operating in challenging environments. The integrity of data to NAND flash memory is generally maintained through ECC algorithms. This ATA-Flash Drive is programmed with a hardware ECC engine which correct up to 72 bits per 1KB.

### 5.3 Flash Block Management

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Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

### 5.4 Power Failure Management

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Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

### 5.5 Mean Time Between Failures (MTBF)

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Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in the drive. The prediction result for the drive is more than 2,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.



## 6. Software Interface

### 6.1 Command Set

This section defines the software requirements and the format of the commands the host sends to the ATA-Disk Module (ADM). Commands are issued to the ADM by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies.

**Table 6-1** Command Set (1 of 2)

| Command                     | Code       |
|-----------------------------|------------|
| Check-Power-Mode            | E5H or 98H |
| Execute-Drive-Diagnostic    | 90H        |
| Erase Sector(s)             | C0H        |
| Flush-Cache                 | E7H        |
| Format Track                | 50H        |
| Identify-Drive              | ECH        |
| Idle                        | E3H or 97H |
| Idle-Immediate              | E1H or 95H |
| Initialize-Drive-Parameters | 91H        |
| NOP                         | 00H        |
| Read-Buffer                 | E4H        |
| Read-DMA                    | C8H or C9H |
| Read-Multiple               | C4H        |
| Read-Sector(s)              | 20H or 21H |
| Read-Verify-Sector(s)       | 40H or 41H |
| Recalibrate                 | 1XH        |
| Request-Sense               | 03H        |
| Security-Disable-Password   | F6H        |
| Security-Erase-Prepare      | F3H        |
| Security-Erase-Unit         | F4H        |
| Security-Freeze-Lock        | F5H        |
| Security-Set-Password       | F1H        |
| Security-Unlock             | F2H        |
| Seek                        | 7XH        |
| Set-Features                | EFH        |

**Table 6-1** Command Set (2 of 2)

| <b>Command</b>               | <b>Code</b> |
|------------------------------|-------------|
| SMART                        | B0H         |
| Set-Multiple-Mode            | C6H         |
| Set-Sleep-Mode               | E6H or 99H  |
| Standby                      | E2H or 96H  |
| Standby-Immediate            | E0H or 94H  |
| Translate-Sector             | 87H         |
| Write-Buffer                 | E8H         |
| Write-DMA                    | CAH or CBH  |
| Write-Multiple               | C5H         |
| Write-Multiple-Without-Erase | CDH         |
| Write-Sector(s)              | 30H or 31H  |
| Write-Sector-Without-Erase   | 38H         |
| Write-Verify                 | 3CH         |

## **6.2 S.M.A.R.T.**

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and attributes parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

## **6.3. ATA Secure Erase**

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

## 7. Electrical Specifications

**Table 7-1** Operating Range

|                            |                              |
|----------------------------|------------------------------|
| <b>Ambient Temperature</b> | 0°C to 70°C<br>-40°C to 85°C |
| <b>Operating voltage</b>   | 3.135-3.465V<br>4.75-5.25V   |

**Table 7-2** Power Consumption

| <b>Capacity</b><br><b>Modes</b> | <b>128 MB</b> | <b>256 MB</b> | <b>512 MB</b> | <b>1 GB</b> | <b>2 GB</b> | <b>4 GB</b> | <b>8 GB</b> | <b>16 GB</b> | <b>32 GB</b> | <b>64 GB</b> |
|---------------------------------|---------------|---------------|---------------|-------------|-------------|-------------|-------------|--------------|--------------|--------------|
| <b>Active (mA)</b>              | 110           | 110           | 125           | 125         | 130         | 190         | 220         | 240          | 245          | 265          |
| <b>Idle (mA)</b>                | 5             | 5             | 5             | 5           | 5           | 5           | 5           | 5            | 5            | 5            |

\*Results were tested at 5.0V power supply and may differ from various flash configurations and platforms.

## 8. Mechanical Specifications



## 9. Product Ordering Information

### 9.1 Product Code Designations



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## 9.2 Valid Combinations

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### 9.2.1 Standard Temperature

| Capacity | P/N (3.3V)        | P/N (5V)          |
|----------|-------------------|-------------------|
| 128MB    | AP-FM0128D3003S-T | AP-FM0128D3005S-T |
| 256MB    | AP-FM0256D3003S-T | AP-FM0256D3005S-T |
| 512MB    | AP-FM0512D3003S-T | AP-FM0512D3005S-T |
| 1GB      | AP-FM001GD3003S-T | AP-FM001GD3005S-T |
| 2GB      | AP-FM002GD3003S-T | AP-FM002GD3005S-T |
| 4GB      | AP-FM004GD3003S-T | AP-FM004GD3005S-T |
| 8GB      | AP-FM008GD3003S-T | AP-FM008GD3005S-T |
| 16GB     | AP-FM016GD3003S-T | AP-FM016GD3005S-T |
| 32GB     | AP-FM032GD3003S-T | AP-FM032GD3005S-T |
| 64GB     | AP-FM064GD3003S-T | AP-FM064GD3005S-T |

### 9.2.2 Extended Temperature

| Capacity | P/N (3.3V)         | P/N (5V)           |
|----------|--------------------|--------------------|
| 128MB    | AP-FM0128D3003S-TW | AP-FM0128D3005S-TW |
| 256MB    | AP-FM0256D3003S-TW | AP-FM0256D3005S-TW |
| 512MB    | AP-FM0512D3003S-TW | AP-FM0512D3005S-TW |
| 1GB      | AP-FM001GD3003S-TW | AP-FM001GD3005S-TW |
| 2GB      | AP-FM002GD3003S-TW | AP-FM002GD3005S-TW |
| 4GB      | AP-FM004GD3003S-TW | AP-FM004GD3005S-TW |
| 8GB      | AP-FM008GD3003S-TW | AP-FM008GD3005S-TW |
| 16GB     | AP-FM016GD3003S-TW | AP-FM016GD3005S-TW |
| 32GB     | AP-FM032GD3003S-TW | AP-FM032GD3005S-TW |
| 64GB     | AP-FM064GD3003S-TW | AP-FM064GD3005S-TW |

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## Revision History

| Revision | Date       | Description                   | Remark |
|----------|------------|-------------------------------|--------|
| 1.0      | 12/09/2014 | Official release              |        |
| 1.1      | 1/19/2015  | Capacity reorganized.         |        |
| 1.2      | 3/30/2016  | Added 128MB and 256MB support |        |

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## Global Presence

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